Ordering number : ENA0858

LC87F76C8A

CMOS IC
FROM 128K byte, RAM 4K byte on-chip
8-bit 1-chip Microcontroller

ON Semiconductor®
http://onsemi.com

Overview

The LC87F76C8A is an 8-bit microcomputer that, centered around a CPU running at a minimum bus cycle time of 83.3ns, integrates on a single chip a number of hardware features such as 128K-byte flash ROM (onboard programmable), 4K-byte RAM, an on-chip debugger, an LCD controller/driver, a sophisticated 16-bit timer/counter (may be divided into 8-bit timers), a 16-bit timer (may be divided into 8-bit timers or 8-bit PWMs), four 8-bit timers with a prescaler, a base timer serving as a time-of-day clock, a day and time counter, a synchronous SIO interface (with automatic block transmission/reception capabilities), an asynchronous/synchronous SIO interface, a UART interface (full duplex), a 8-bit 12-channel AD converter, two 12-bit PWM channels, a high-speed clock counter, a system clock frequency divider, a small signal detector, an infrared remote controller receiver function, and a 22-source 10-vector interrupt feature.

Features

■Flash ROM
- Capable of on-board-programming with a wide range of souce voltages: 3.0 to 5.5V.
- Block-erasable in 2-byte units
- 131072 × 8 bits (LC87F76C8A)

■RAM
- 4096 × 9 bits (LC87F76C8A)

■Minimum Bus Cycle Time
- 83.3ns (12MHz) V_{DD}=3.0 to 5.5V
- 125ns (8MHz) V_{DD}=2.5 to 5.5V
- 250ns (4MHz) V_{DD}=2.2 to 5.5V

Note: The bus cycle time here refers to the ROM read speed.

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■Minimum Instruction Cycle Time (tCYC)
- 250ns (12MHz) V_{DD}=3.0 to 5.5V
- 375ns (8MHz) V_{DD}=2.5 to 5.5V
- 750ns (4MHz) V_{DD}=2.2 to 5.5V

■Ports
- Normal withstand voltage I/O ports
  Ports whose I/O direction can be designated in 1-bit units 23 (P1n, P30 to P31, P70 to P73, P8n, XT2)
  Ports whose I/O direction can be designated in 4-bit units 8 (P0n)
- Normal withstand voltage input port 1 (XT1)
- LCD ports
  Segment output 32 (S00 to S31)
  Common output 4 (COM0 to COM3)
  Bias terminals for LCD driver 3 (V1 to V3)

Other functions
  Input/output ports 32 (PAn, PBn, PCn, PDn,)
  Input ports 7 (PLn)
- Dedicated oscillator ports 2 (CF1, CF2)
- Reset pins 1 ($\overline{RES}$)
- Power pins 6 ($V_{SS}1$ to $V_{SS}3$, $V_{DD}1$ to $V_{DD}3$)

■LCD Controller
1) Seven display modes are available (static, 1/2, 1/3, 1/4 duty × 1/2, 1/3 bias)
2) Segment output and common output can be switched to general-purpose input/output ports

■Small Signal Detection (MIC signals etc)
1) Counts pulses with the level which is greater than a preset value
2) 2-bit counter

■Timers
- Timer 0: 16-bit timer/counter with two capture registers.
  Mode 0: 8-bit timer with an 8-bit programmable prescaler (with 8-bit capture registers) × 2 channels
  Mode 1: 8-bit timer with an 8-bit programmable prescaler (with 8-bit capture registers)
  + 8-bit counter (with two 8-bit capture registers)
  Mode 2: 16-bit timer with an 8-bit programmable prescaler (with 16-bit capture registers)
  Mode 3: 16-bit counter (with 16-bit capture registers)
- Timer 1: 16-bit timer that supports PWM/toggle outputs
  Mode 0: 8-bit timer with an 8-bit prescaler (with toggle outputs)
  + 8-bit timer with an 8-bit prescaler (with toggle outputs)
  Mode 1: 8-bit PWM with an 8-bit prescaler × 2 channels
  Mode 2: 16-bit timer/counter with an 8-bit prescaler (with toggle outputs)
  (toggle outputs also possible from the lower-order 8 bits)
  Mode 3: 16-bit timer with an 8-bit prescaler (with toggle outputs)
  (The lower-order 8 bits can be used as PWM.)
- Timer 4: 8-bit timer with a 6-bit prescaler
- Timer 5: 8-bit timer with a 6-bit prescaler
- Timer 6: 8-bit timer with a 6-bit prescaler (with toggle output)
- Timer 7: 8-bit timer with a 6-bit prescaler (with toggle output)
- Base timer
  1) The clock is selectable from the subclock (32.768kHz crystal oscillation), system clock, and timer 0 prescaler output.
  2) Interrupts programmable in 5 different time schemes
- Day and time counter
  1) Used with a base timer, the day and time counter can be used as a 65000 day + minute + second counter.

■High-speed Clock Counter
1) Can count clocks with a maximum clock rate of 20MHz (at a main clock of 10MHz).
2) Can generate output real-time.

■SIO
- SIO0: 8-bit synchronous serial interface
  1) LSB first/MSB first mode selectable
  2) Built-in 8-bit baudrate generator (maximum transfer clock cycle = 4/3 tCYC)
  3) Automatic continuous data transmission (1 to 256 bits specifiable in 1-bit units, suspension and resumption of data transmission possible in 1-byte units)
- SIO1: 8-bit asynchronous/synchronous serial interface
  Mode 0: Synchronous 8-bit serial I/O (2- or 3-wire configuration, 2 to 512 tCYC transfer clocks)
  Mode 1: Asynchronous serial I/O (half-duplex, 8-data bits, 1-stop bit, 8 to 2048 tCYC baudrates)
  Mode 2: Bus mode 1 (start bit, 8-data bits, 2 to 512 tCYC transfer clocks)
  Mode 3: Bus mode 2 (start detect, 8-data bits, stop detect)

■UART
- Full duplex
- 7/8/9 bit data bits selectable
- 1 stop bit (2-bit in continuous data transmission)
- Built-in baudrate generator

* When using UART, set P0LDDR (PODDR: Bit0) to “0”

■AD Converter: 12 bits × 12 channels

■PWM: Multi frequency 12-bit PWM × 2 channels

■Infrared Remote Control Receiver Circuit
1) Noise reduction function
   (Time constant of noise reduction filter: approx. 120μs, when selecting a 32.768kHz crystal oscillator as a reference clock.)
2) X’tal HOLD mode cancellation function

■Watchdog Timer
- External RC watchdog timer
- Interrupt and reset signals selectable

■Clock Output Function
1) Can output selected oscillation clock 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, or 1/64 as system clock.
2) Can output the source oscillation clock for the sub clock.

■Interrupts

- 22 sources, 10 vector addresses
  1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
  2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/remote control receiver
4	0001BH	H or L	INT3/base timer
5	00023H	H or L	T0H
6	0002BH	H or L	T1L/T1H
7	00033H	H or L	SIO0/UART1 receive
8	0003BH	H or L	SIO1/UART1 transmit
9	00043H	H or L	ADC/MIC/T6/T7/PWM4, PWM5
10	0004BH	H or L	Port 0/T4/T5

  - Priority levels X > H > L
  - Of interrupts of the same level, the one with the smallest vector address takes precedence.

- IFLG (List of interrupt source flag function)
  1) Shows a list of interrupt source flags that caused a branching to a particular vector address

■Subroutine Stack Levels: 2048 levels maximum (The stack is allocated in RAM.)

■High-speed Multiplication/Division Instructions

- 16 bits × 8 bits (5 tCYC execution time)
- 24 bits × 16 bits (12 tCYC execution time)
- 16 bits ÷ 8 bits (8 tCYC execution time)
- 24 bits ÷ 16 bits (12 tCYC execution time)

■Oscillation Circuits

- RC oscillation circuit (internal): For system clock
- CF oscillation circuit: For system clock, with internal Rf and external Rd
- Crystal oscillation circuit: For low-speed system clock, with internal Rf and external Rd
- Multifrequency RC oscillation circuit (internal): For system clock
  1) Adjustable in ±4% (typ) increments from the selected center frequency.
  2) Measures the frequency of the source oscillation clock using the input signal from XT1 as the reference.

■System Clock Divider Function

- Can run on low current.
- The minimum instruction cycle selectable from 300ns, 600ns, 1.2µs, 2.4µs, 4.8µs, 9.6µs, 19.2µs, 38.4µs, and 76.8µs (at a main clock rate of 10MHz).

■System Clock Divider Function

- Can run on low current.
- The minimum instruction cycle selectable from 300ns, 600ns, 1.2µs, 2.4µs, 4.8µs, 9.6µs, 19.2µs, 38.4µs, and 76.8µs (at a main clock rate of 10MHz).

■System Clock Multiplier Function

- Allows the 2 or 3 times the clock frequency to be selected when the crystal oscillation output is used as the system clock.

■Standby Function

- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
  (Some parts of the serial transfer function stops operation.)
  1) Oscillation is not stopped automatically.
  2) Canceled by a system reset or occurrence of an interrupt
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
  1) The CF, RC, X'tal, and multifrequency RC oscillators automatically stop operation.
  2) There are three ways of resetting the HOLD mode.
     (1) Setting the reset pin to the low level
     (2) Setting at least one of the INT0, INT1, and INT2, pins to the specified level
     (3) Having an interrupt source established at port 0
- X'tal HOLD mode: Suspends instruction execution and the operation of the peripheral circuits except the base timer and infrared remote controller circuit.
  1) The CF, RC, and multifrequency RC oscillators automatically stop operation
  2) The state of crystal oscillation established when the X'tal HOLD mode is entered is retained.
  3) There are five ways of resetting the X'tal HOLD mode.
     (1) Setting the reset pin to the low level
     (2) Setting at least one of the INT0, INT1, and INT2 pins to the specified level
     (3) Having an interrupt source established at port 0
     (4) Having an interrupt source established in the base timer circuit
     (5) Having an interrupt source established in the infrared remote control receiver circuit

■On-chip Debugger

- Supports software debugging with the IC mounted on the target board.

■Package Form

- QIP80(14×14): Lead-free type
- TQFP80J(12×12): Lead-free type

■Development Tools

- On-chip debugger: TCB87-TypeB + LC87F76C8A

■Flash ROM Programming Board

Package	Programming Boards
QIP80(14×14)	W87F71256QF
TQFP80J(12×12)	W87F71256SQ

■Flash ROM Programmer

Maker	Model	Supported Version (Note)	Device
Flash Support Group, Inc (Single)	AF9708/AF9709/AF9709B (including models manufactured by Ando Electric Co., Ltd.)		LC87F76C8A
Flash Support Group, Inc (Gang)	AF9723 (main unit) (including models manufactured by Ando Electric Co., Ltd.)		LC87F76C8A
	AF9833 (unit) (including models manufactured by Ando Electric Co., Ltd.)		
SANYO	SKK(SANYO FWS)	Application Version: After 1.04 Chip Data Version: After 2.09	LC87F76C8A

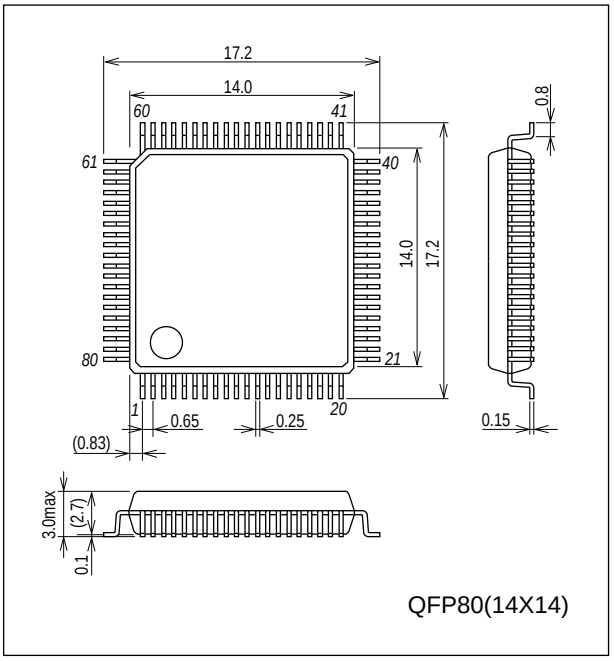
Note: Check for the latest version.

■Same Package and Pin Assignment as Mask ROM Version.

1) LC877600 series options can be specified by using flash ROM data. Thus the board used for mass production can be used for debugging and evaluation without modifications.
2) If the program for the mask ROM version is used, the size of the available ROM/RAM spaces is the same as that of the mask ROM version.

Package Dimensions

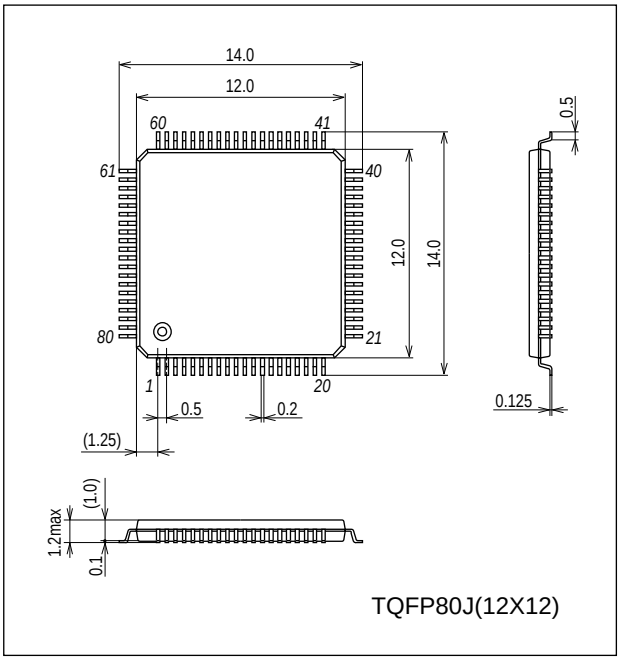
unit : mm (typ)
3255



QFP80(14X14)

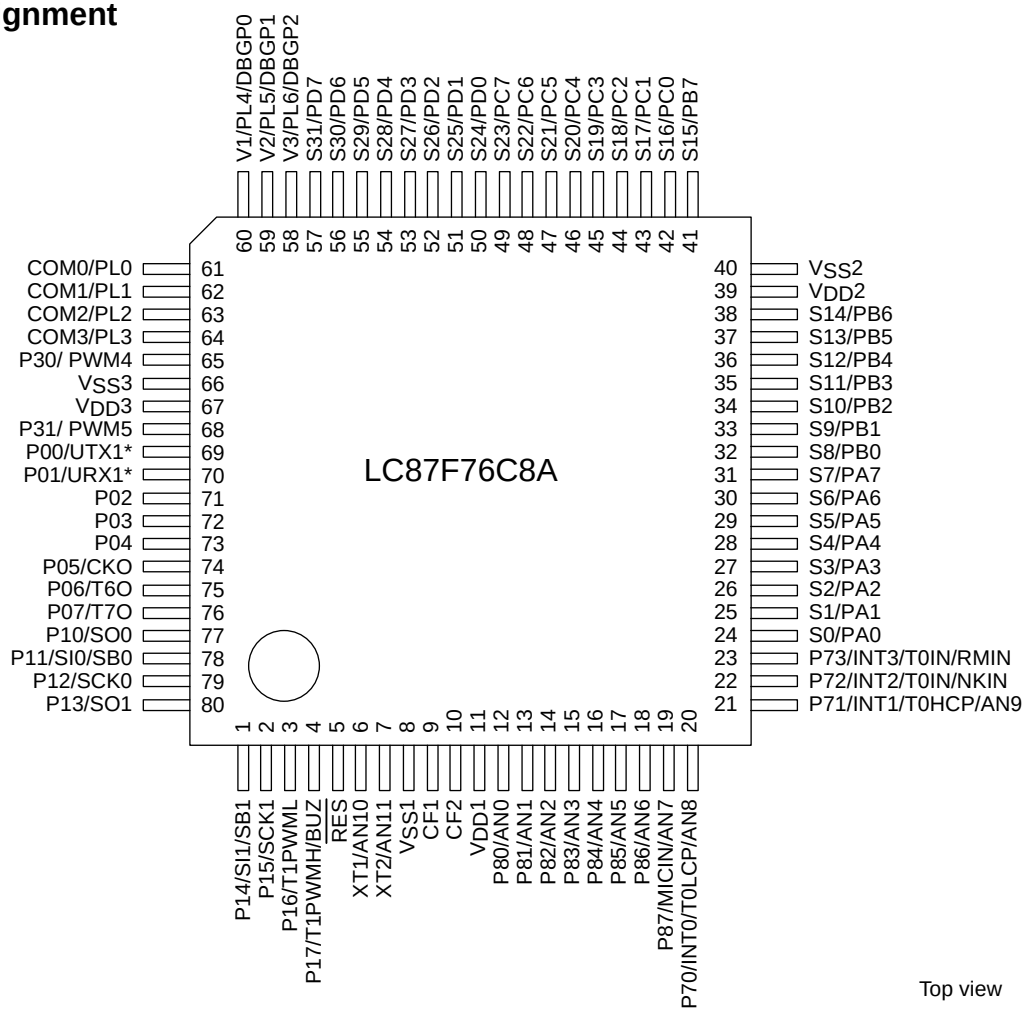
Package Dimensions

unit : mm (typ)
3290



TQFP80J(12X12)

Pin Assignment



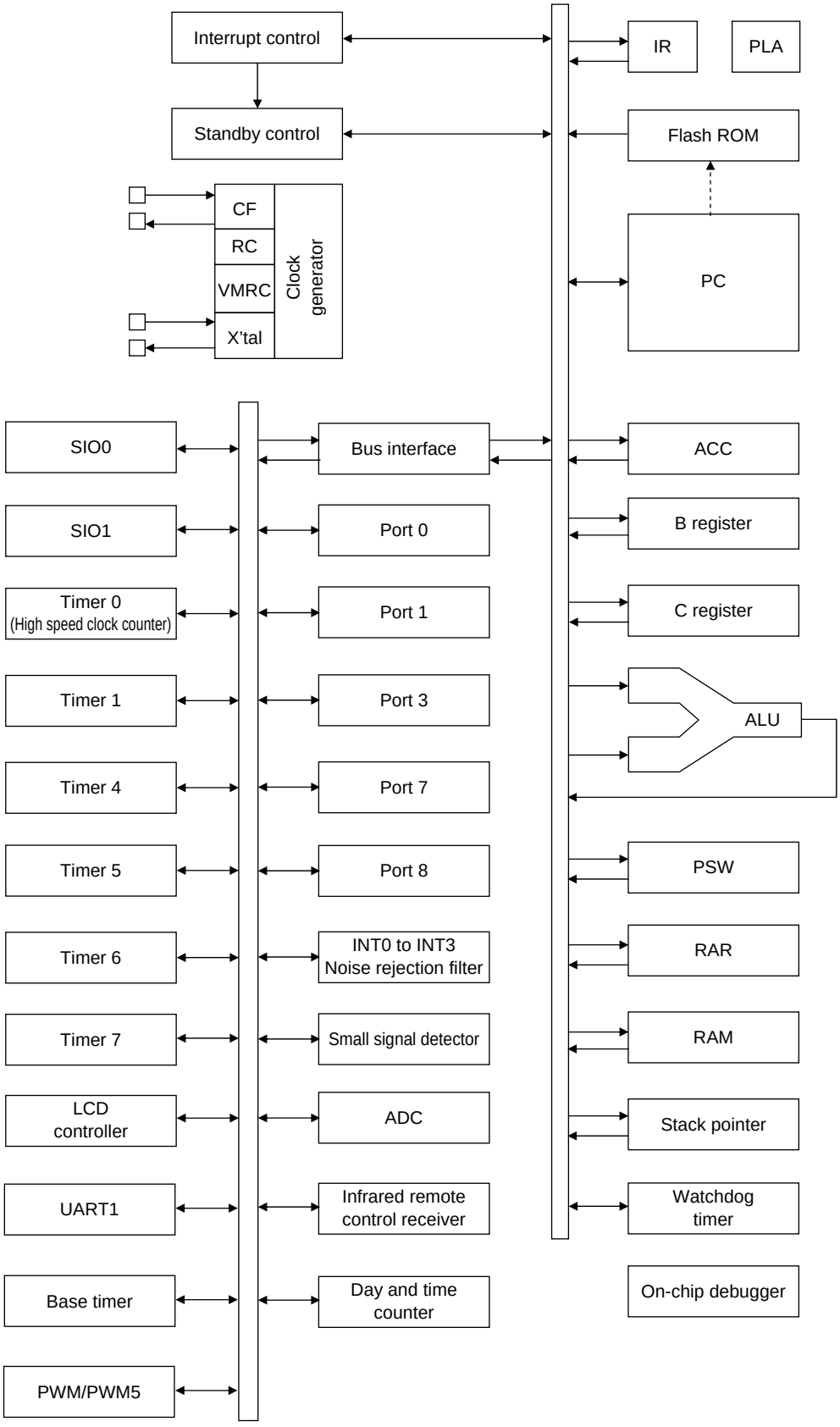
Top view

*When using UART, set P0LDDR (PODDR: Bit0) to “0”

SANYO: QFP80(14×14) “Lead-free Type”

SANYO: TQFP80J(12×12) “Lead-free Type”

System Block Diagram



Pin Description

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>$V_{SS}1$
$V_{SS}2$
$V_{SS}3$</td><td>-</td><td>- power supply pin</td><td>No</td></tr>
<tr><td>$V_{DD}1$
$V_{DD}2$
$V_{DD}3$</td><td>-</td><td>+ power supply pin</td><td>No</td></tr>
<tr><td>PORT0
P00 to P07</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 4-bit units
• Pull-up resistors can be turned on and off in 4-bit units.
• Input for HOLD release
• Input for port 0 interrupt
• Shared pins
P00: UART1 transmit *
P01: UART1 receive *
P05: Clock output (system clock/subclock selectable)
P06: Timer 6 toggle output
P07: Timer 7 toggle output
* When using UART, set P0LDDR (PODDR: Bit0) to “0”</td><td>Yes</td></tr>
<tr><td>PORT1
P10 to P17</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistors can be turned on and off in 1-bit units.
• Shared pins
P10: SIO0 data output
P11: SIO0 data input/bus I/O
P12: SIO0 clock I/O
P13: SIO1 data output
P14: SIO1 data input/bus I/O
P15: SIO1 clock I/O
P16: Timer 1 PWML output
P17: Timer 1PWMH output/beeper output</td><td>Yes</td></tr>
<tr><td>PORT3
P30 to P31</td><td>I/O</td><td>• 2-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistors can be turned on and off in 1-bit units.
• Shared pins
P30: PWM4 output
P31: PWM5 output</td><td>Yes</td></tr>
<tr><td>PORT7
P70 to P73</td><td>I/O</td><td>• 4-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistors can be turned on and off in 1-bit units.
• Shared pins
P70: INT0 input/HOLD release input/timer 0L capture input/watchdog timer output
P71: INT1 input/HOLD release input/timer 0H capture input
P72: INT2 input/HOLD release input/timer 0 event input/timer 0L capture input/ high speed clock counter input
P73: INT3 input (with noise filter)/timer 0 event input/timer 0H capture input/ infrared remote control receiver input
AD converter input ports: AN8 (P70), AN9 (P71)
• Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table>
</td><td>No</td></tr>
</table>

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Pin Name	I/O	Description	Option
PORT8 P80 to P87	I/O	• 8-bit I/O port • I/O specifiable in 1-bit units • Shared pins AD converter input ports: AN0 to AN7 Small signal detector input port: MICIN (P87)	No
S0/PA0 to S7/PA7	I/O	• Segment output for LCD • Can be used as general-purpose I/O port (PA)	No
S8/PB0 to S15/PB7	I/O	• Segment output for LCD • Can be used as general-purpose I/O port (PB)	No
S16/PC0 to S23/PC7	I/O	• Segment output for LCD • Can be used as general-purpose I/O port (PC)	No
S24/PD0 to S31/PD7	I/O	• Segment output for LCD • Can be used as general-purpose I/O port (PD)	No
COM0/PL0 to COM3/PL3	I/O	• Common output for LCD • Can be used as general-purpose input port (PL)	No
V1/PL4 to V3/PL6	I/O	• LCD drive bias power supply • Can be used as general-purpose input port (PL) • Shared pins On-chip debugger pins: DBGP0 (V1) to DBGP2 (V3)	No
$\overline{\text{RES}}$	Input	Reset pin	No
XT1	Input	• 32.768kHz crystal oscillator input pin • Shared pins General-purpose input port Must be connected to $V_{DD}1$ if not to be used. AD converter input port: AN10	No
XT2	I/O	• 32.768kHz crystal oscillator output pin • Shared pins General-purpose I/O port Must be set for oscillation and kept open if not to be used. AD converter input port: AN11	No
CF1	Input	Ceramic resonator input pin	No
CF2	Output	Ceramic resonator output pin	No

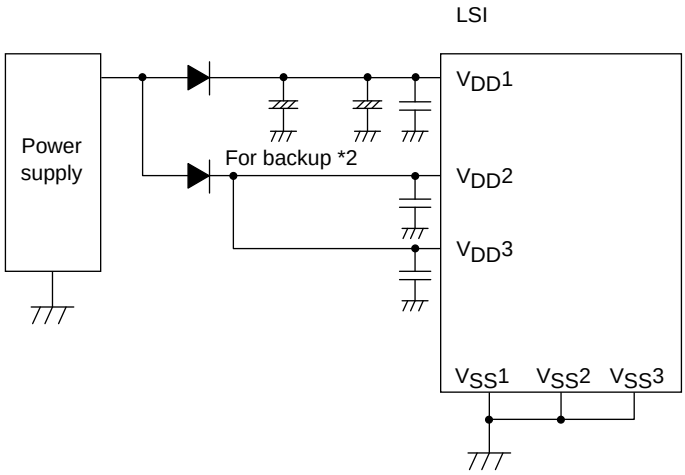
Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor.
Data can be read into any input port even if it is in the output mode.

Port Name	Option Selected in Units of	Option Type	Output Type	Pull-up Resistor
P00 to P07	each bit	1	CMOS	Programmable (Note)
		2	N-channel open drain	No
P10 to P17	each bit	1	CMOS	Programmable
		2	N-channel open drain	Programmable
P30 to P31	each bit	1	CMOS	Programmable
		2	N-channel open drain	Programmable
P70	-	No	N-channel open drain	Programmable
P71 to P73	-	No	CMOS	Programmable
P80 to P87	-	No	N-channel open drain	No
S0/PA0 to S31/PD7	-	No	CMOS	Programmable
COM0/PL0 to COM3/PL3	-	No	Input only	No
V1/PL4 to V3/PL6	-	No	Input only	No
XT1	-	No	Input only	No
XT2	-	No	Output for 32.768kHz crystal oscillator (Nch-open drain when in general-purpose output mode)	No

Note: Programmable pull-up resistors for port 0 are controlled in 4 bit units (P00 to 03, P04 to 07).

*1 Connect the IC as shown below to minimize the noise input to the $V_{DD}1$ pin.
Be sure to electrically short the $V_{SS}1$, $V_{SS}2$, and $V_{SS}3$ pins.



*2 The internal memory is sustained by $V_{DD}1$. If none of $V_{DD}2$ and $V_{DD}3$ are backed up, the high level output at the ports are unstable in the HOLD backup mode, allowing through current to flow into the input buffer and thus shortening the backup time.
Make sure that the port outputs are held at the low level in the HOLD backup mode.

Absolute Maximum Ratings at Ta = 25°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter		Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Maximum supply voltage		V_{DD} max	$V_{DD}1$,$V_{DD}2$, $V_{DD}3$	$V_{DD}1=V_{DD}2=V_{DD}3$		-0.3		+6.5	V
Supply voltage for LCD		VLCD	V1/PL4, V2/PL5, V3/PL6	$V_{DD}1=V_{DD}2=V_{DD}3$		-0.3		V_{DD}	
Input voltage		V_I(1)	• Port L • XT1, CF1, $\overline{RES}$			-0.3		V_{DD}+0.3	
Input/output voltage		V_{IO}(1)	• Ports 0, 1, 3, 7, 8 • Ports A, B, C, D • XT2			-0.3		V_{DD}+0.3	
High level output current	Peak output current	IOPH(1)	Ports 0, 1	• CMOS output selected • Per applicable pin		-10			mA
		IOPH(2)	Port 3	• CMOS output selected • Per applicable pin		-20			
		IOPH(3)	Ports 71 to 73	Per applicable pin		-5			
		IOPH(4)	Ports A, B, C, D	Per applicable pin		-5			
	Average output current (Note 1-1)	IOMH(1)	Ports 0, 1	• CMOS output selected • Per applicable pin		-7.5			
		IOMH(2)	Port 3	• CMOS output selected • Per applicable pin		-15			
		IOMH(3)	Ports 71 to 73	Per applicable pin		-3			
		IOMH(4)	Ports A, B, C, D	Per applicable pin		-3			
	Total output current	ΣIOAH(1)	Ports 0, 1, 31	Total of currents at all applicable pins		-25			
		ΣIOAH(2)	Port 30	Total of currents at all applicable pins		-15			
		ΣIOAH(3)	Ports 0, 1, 3	Total of currents at all applicable pins		-40			
		ΣIOAH(4)	Ports 71 to 73	Total of currents at all applicable pins		-5			
		ΣIOAH(5)	Ports A, B	Total of currents at all applicable pins		-25			
		ΣIOAH(6)	Ports C, D	Total of currents at all applicable pins		-25			
		ΣIOAH(7)	Ports A, B, C, D	Total of currents at all applicable pins		-45			
Low level output current	Peak output current	IOPL(1)	Ports 0, 1	Per applicable pin				20	
		IOPL(2)	Port 3	Per applicable pin				30	
		IOPL(3)	• Ports 7, 8 • XT2	Per applicable pin				10	
		IOPL(4)	Ports A, B, C, D	Per applicable pin				10	
	Average output current (Note 1-1)	IOML(1)	Ports 0, 1	Per applicable pin				15	
		IOML(2)	Port 3	Per applicable pin				20	
		IOML(3)	• Ports 7, 8 • XT2	Per applicable pin				7.5	
		IOML(4)	Ports A, B, C, D	Per applicable pin				7.5	

Note 1-1: Average output current refers to the average of output currents measured for a period of 100ms.

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Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Continued from preceding page.

Parameter		Symbol	Pin/Remarks	Conditions	Specification				
					V_{DD}[V]	min	typ	max	unit
Low level output current	Total output current	ΣIOAL(1)	Ports 0, 1, 31	Total of currents at all applicable pins				45	mA
		ΣIOAL(2)	Port 30	Total of currents at all applicable pins				45	
		ΣIOAL(3)	Ports 0, 1, 3	Total of currents at all applicable pins				80	
		ΣIOAL(4)	• Ports 7, 8 • XT2	Total of currents at all applicable pins				20	
		ΣIOAL(5)	Ports A, B	Total of currents at all applicable pins				45	
		ΣIOAL(6)	Ports C, D	Total of currents at all applicable pins				45	
		ΣIOAL(7)	Ports A, B, C, D	Total of currents at all applicable pins				80	
Maximum power dissipation		Pd max	QFP80(14×14)	Ta=-20 to+70°C				290	mW
			TQFP80J(12×12)						
Operating ambient temperature		Topr				-20		+85	°C
Storage ambient temperature		Tstg				-55		+125	

Note 1-1: Average output current refers to the average of output currents measured for a period of 100 ms.

Allowable Operating Range at Ta = -20°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Operating supply voltage (Note 2-1)	$V_{DD}(1)$	$V_{DD}1=V_{DD}2=V_{DD}3$	0-237μs≤tCYC≤200μs		3.0		5.5	V
	$V_{DD}(2)$		0-356μs≤tCYC≤200μs		2.5		5.5	
	$V_{DD}(3)$		0-712μs≤tCYC≤200μs		2.2		5.5	
Memory sustaining supply voltage	VHD	$V_{DD}1$	RAM and register contents sustained in HOLD mode		2.0		5.5	
High level input voltage	$V_{IH}(1)$	• Ports 0, 3, 8 • Ports A, B, C, D • Port L	Output disabled	2.2 to 5.5	$0.3V_{DD}$ +0.7		V_{DD}	
	$V_{IH}(2)$	• Port 1 • Ports 71 to 73 • Port 70 port input/ interrupt side	• Output disabled • When INT1VTSL=0 (P71only)	2.2 to 5.5	$0.3V_{DD}$ +0.7		V_{DD}	
	$V_{IH}(3)$	Port 71 interrupt side	• Output disabled • When INT1VTSL=1	2.2 to 5.5	$0.85V_{DD}$		V_{DD}	
	$V_{IH}(4)$	Port 87 small signal input side	Output disabled	2.2 to 5.5	$0.75V_{DD}$		V_{DD}	
	$V_{IH}(5)$	Port 70 watchdog timer side	Output disabled	2.2 to 5.5	$0.9V_{DD}$		V_{DD}	
	$V_{IH}(6)$	XT1, XT2, CF1, $\overline{RES}$		2.2 to 5.5	$0.75V_{DD}$		V_{DD}	

Note 2-1: V_{DD} must be held greater than or equal to 3.0V in the flash ROM onboard programming mode.

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Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Low level input voltage	V_{IL}(1)	• Ports 0, 3, 8 • Ports A, B, C, D • Port L	Output disabled	4.0 to 5.5	V_{SS}		$0.15V_{DD}$ +0.4	V
				2.2 to 4.0	V_{SS}		$0.2V_{DD}$	
	VIL(2)	• Port 1 • Ports 71 to 73 • Port 70 port input/ interrupt side	• Output disabled • When INT1VTSL=0 (P71 only)	4.0 to 5.5	V_{SS}		$0.1V_{DD}$ +0.4	
				2.2 to 4.0	V_{SS}		$0.2V_{DD}$	
	V_{IL}(3)	Port 71 interrupt side	• Output disabled • When INT1VTSL=1	2.2 to 5.5	V_{SS}		$0.45V_{DD}$	
	V_{IL}(4)	Port 87 small signal input side	Output disabled	2.2 to 5.5	V_{SS}		$0.25V_{DD}$	
	V_{IL}(5)	Port 70 watchdog timer side	Output disabled	2.2 to 5.5	V_{SS}		$0.8V_{DD}$ -1.0	
	V_{IL}(6)	XT1, XT2, CF1, $\overline{RES}$		2.2 to 5.5	V_{SS}		$0.25V_{DD}$	
Instruction cycle time (Note 2-2)	tCYC			3.0 to 5.5	0.237		200	µs
				2.5 to 5.5	0.356		200	
				2.2 to 5.5	0.712		200	
External system clock frequency	FEXCF(1)	CF1	• CF2 pin open • System clock frequency division ratio=1/1 • External system clock DUTY50±5%	3.0 to 5.5	0.1		12	MHz
				2.5 to 5.5	0.1		8	
				2.2 to 5.5	0.1		4	
			• CF2 pin open • System clock frequency division ratio=1/2	3.0 to 5.5	0.2		24.4	
				2.5 to 5.5	0.2		16	
				2.2 to 5.5	0.2		8	
Oscillation frequency range (Note 2-3)	FmCF(1)	CF1, CF2	• 12MHz ceramic oscillation • See figure 1.	3.0 to 5.5		12		
	FmCF(2)	CF1, CF2	• 8MHz ceramic oscillation • See figure 1.	2.5 to 5.5		8		
	FmCF(3)	CF1, CF2	• 4MHz ceramic oscillation • See figure 1.	2.2 to 5.5		4		
	FmRC		Internal RC oscillation	2.2 to 5.5	0.3	1.0	2.0	
	FmVMRC(1)		• Multifrequency RC source oscillation • VMRAJ2 to 0=4, VMFAJ2 to 0=0, When VMSL4M=0	2.2 to 5.5		10		
	FmVMRC(2)		• Multifrequency RC source oscillation • VMRAJ2 to 0=4, VMFAJ2 to 0=0, When VMSL4M=1	2.2 to 5.5		4		
	FsX'tal	XT1, XT2	• 32.768kHz crystal oscillation • See figure 2.	2.2 to 5.5		32.768		kHz
Multifrequency RC oscillation usable range	OpVMRC(1)		When VMSL4M=0	2.2 to 5.5	8	10	12	MHz
	OpVMRC(2)		When VMSL4M=1	2.2 to 5.5	3.5	4	4.5	
Multifrequency RC oscillation adjustment range	VmADJ(1)		VMRAJn 1STEP (Wide range)	2.2 to 5.5	8	24	64	%
	VmADJ(2)		VMFAJn 1STEP (Narrow range)	2.2 to 5.5	1	4	8	

Note 2-2: Relationship between tCYC and oscillation frequency is 3/FmCF at a division ratio of 1/1 and 6/FmCF at a division ratio of 1/2.

Note 2-3: See Tables 1 and 2 for the oscillation constants.

Electrical Characteristics at Ta = -20°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
High level input current	$I_{IH}(1)$	• Ports 0, 1, 3, 7, 8 • Ports A, B, C, D • Port L	• Output disabled • Pull-up resistor off • $V_{IN}=V_{DD}$ (including output Tr's off leakage current)	2.2 to 5.5			1	μA
	$I_{IH}(2)$	$\overline{RES}$	$V_{IN}=V_{DD}$	2.2 to 5.5			1	
	$I_{IH}(3)$	XT1, XT2	• When configured as input ports • $V_{IN}=V_{DD}$	2.2 to 5.5			1	
	$I_{IH}(4)$	CF1	$V_{IN}=V_{DD}$	2.2 to 5.5			15	
	$I_{IH}(5)$	Port 87 small signal input side	V_{IN}=VBIS+0.5V (VBIS denotes bias voltage)	4.5 to 5.5	4.2	8.5	15	
				2.2 to 4.5	1.5	5.5	10	
Low level input current	$I_{IL}(1)$	• Ports 0, 1, 3, 7, 8 • Ports A, B, C, D • Port L	• Output disabled • Pull-up resistor off • $V_{IN}=V_{SS}$ (including output Tr's off leakage current)	2.2 to 5.5	-1			
	$I_{IL}(2)$	$\overline{RES}$	$V_{IN}=V_{SS}$	2.2 to 5.5	-1			
	$I_{IL}(3)$	XT1, XT2	• When configured as input ports • $V_{IN}=V_{SS}$	2.2 to 5.5	-1			
	IIL(4)	CF1	$V_{IN}=V_{SS}$	2.2 to 5.5	-15			
	$I_{IL}(5)$	Port 87 small signal input side	V_{IN}=VBIS-0.5V (VBIS denotes bias voltage)	4.5 to 5.5	-15	-8.5	-4.2	
				2.2 to 4.5	-10	-5.5	-1.5	
High level output voltage	$V_{OH}(1)$	CMOS output ports 0, 1	I_{OH}=-1mA	4.5 to 5.5	V_{DD}-1			V
	$V_{OH}(2)$		I_{OH}=-0.4mA	3.0 to 5.5	V_{DD}-0.4			
	$V_{OH}(3)$		I_{OH}=-0.2mA	2.2 to 5.5	V_{DD}-0.4			
	$V_{OH}(4)$	CMOS output ports 30, 31	I_{OH}=-10mA	4.5 to 5.5	V_{DD}-1.5			
	$V_{OH}(5)$		I_{OH}=-1.6mA	3.0 to 5.5	V_{DD}-0.4			
	$V_{OH}(6)$		I_{OH}=-1mA	2.2 to 5-5	V_{DD}-0.4			
	$V_{OH}(7)$	Ports 71 to 73	I_{OH}=-0.4mA	3.0 to 5.5	V_{DD}-0.4			
	$V_{OH}(8)$		I_{OH}=-0.2mA	2.2 to 5.5	V_{DD}-0.4			
	$V_{OH}(9)$	Ports A, B, C, D	I_{OH}=-1mA	4.5 to 5.5	V_{DD}-1			
	$V_{OH}(10)$		I_{OH}=-0.4mA	3.0 to 5.5	V_{DD}-0.4			
	$V_{OH}(11)$		I_{OH}=-0.2mA	2.2 to 5.5	V_{DD}-0.4			
Low level output voltage	$V_{OL}(1)$	Ports 0, 1 • Port 3 (PWM4, 5 function output mode)	I_{OL}=10mA	4.5 to 5.5			1.5	
	$V_{OL}(2)$		I_{OL}=1.6mA	3.0 to 5.5			0.4	
	$V_{OL}(3)$		I_{OL}=1mA	2.2 to 5.5			0.4	
	$V_{OL}(4)$	Port 3 (Port function output mode)	I_{OL}=30mA	4.5 to 5.5			1.5	
	$V_{OL}(5)$		I_{OL}=5mA	3.0 to 5.5			0.4	
	$V_{OL}(6)$		I_{OL}=2.5mA	2.2 to 5.5			0.4	
	$V_{OL}(7)$	• Ports 7, 8 • XT2	I_{OL}=1.6mA	3.0 to 5.5			0.4	
	$V_{OL}(8)$		I_{OL}=1mA	2.2 to 5.5			0.4	
	$V_{OL}(9)$	Ports A, B, C, D	I_{OH}=1.6mA	3.0 to 5.5			0.4	
	$V_{OL}(10)$		I_{OL}=1mA	2.2 to 5.5			0.4	
LCD output voltage deviation	VODLS	S0 to S31	• I_O=0mA • VLCD, 2/3VLCD 1/3VLCD level output • See Fig. 8.	2.2 to 5.5	0		±0.2	
	VODLC	COM0 to COM3	• I_O=0mA • VLCD, 2/3VLCD 1/2VLCD, 1/3VLCD level output • See Fig. 8.	2.2 to 5.5	0		±0.2	
LCD bias resistor	RLCD(1)	Resistance per one bias resister	See Fig. 8.	2.2 to 5.5		60		kΩ
	RLCD(2)	• Resistance per one bias resister • 1/2 resistance mode	See Fig. 8.	2.2 to 5.5		30		

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Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Pull-up MOS Tr. resistance	Rpu(1)	• Ports 0, 1, 3, 7 • Ports A, B, C, D	V_{OH}=0-9V_{DD}	4.5 to 5.5	15	35	80	kΩ
	Rpu(2)			2.2 to 4.5	18	50	150	
Hysteresis voltage	VHYS(1)	• Ports 1, 7 • $\overline{RES}$		2.2 to 5.5		0.1V_{DD}		V
	VHYS(2)	Port 87 small signal input side		2.2 to 5.5		0.1V_{DD}		
Pin capacitance	CP	All pins	• V_{IN}=V_{SS} for pins other than that under test • f=1MHz • Ta=25°C	2.2 to 5.5		10		pF
Input sensitivity	Vsen	Port 87 small signal input side		2.2 to 5.5	0.12V_{DD}			Vp-p

Serial I/O Characteristics at Ta = -20°C to +85°C, $V_{SS}1$ = $V_{SS}2$ = $V_{SS}3$ = 0V

1. SIO0 Serial I/O Characteristics (Note 4-1-1)

Parameter			Symbol	Pin/Remarks	Conditions	Specification				
						V_{DD}[V]	min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(1)	SCK0(P12)	See Fig. 6.	2.2 to 5.5	2			tCYC
		Low level pulse width	tSCKL(1)				1			
		High level pulse width	tSCKH(1)				1			
			tSCKHA(1)		• Continuous data transmission/reception mode • See Fig. 6. • (Note 4-1-2)		4			
	Output clock	Frequency	tSCK(2)	SCK0(P12)	• CMOS output selected • See Fig. 6.	2.2 to 5.5	4/3			
		Low level pulse width	tSCKL(2)				1/2			tSCK
		High level pulse width	tSCKH(2)				1/2			
			tSCKHA(2)		• Continuous data transmission/reception mode • CMOS output selected • See Fig. 6.		tSCKH(2) +2tCYC		tSCKH(2) +(10/3) tCYC	tCYC
Serial input	Data setup time		tsDI(1)	SB0(P11), SI0(P11)	• Must be specified with respect to rising edge of SIOCLK • See Fig. 6.	2.2 to 5.5	0.03			µs
	Data hold time		thDI(1)				0.03			
Serial output	Input clock	Output delay time	tdDO(1)	SO0(P10), SB0(P11)	• Continuous data transmission/reception mode • (Note 4-1-3)	2.2 to 5.5			(1/3)tCYC +0.05	
			tdDO(2)		• Synchronous 8-bit mode • (Note 4-1-3)				1tCYC +0.05	
	Output clock		tdDO(3)		(Note 4-1-3)				(1/3)tCYC +0.05	

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: To use serial-clock-input in continuous transmission/reception mode, a time from SI0RUN being set when serial clock is "H" to the first falling edge of the serial clock must be longer than tSCKHA.

Note 4-1-3: Must be specified with respect to falling edge of SIOCLK. Must be specified as the time to the beginning of output state change in open drain output mode. See Fig. 6.

2. SIO1 Serial I/O Characteristics (Note 4-2-1)

Parameter			Symbol	Pin/Remarks	Conditions		Specification			
						V_{DD}[V]	min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(3)	SCK1(P15)	See Fig.6.	2.2 to 5.5	2			tCYC
		Low level pulse width	tSCKL(3)				1			
		High level pulse width	tSCKH(3)				1			
	Output clock	Frequency	tSCK(4)	SCK1(P15)	• CMOS output selected • See Fig. 6.	2.2 to 5.5	2			tSCK
		Low level pulse width	tSCKL(4)				1/2			
		High level pulse width	tSCKH(4)				1/2			
Serial input	Data setup time		tsDI(2)	SB1(P14), SI1(P14)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 6.	2.2 to 5.5	0.03			µs
	Data hold time		thDI(2)				0.03			
Serial output	Output delay time		tdDO(4)	SO1(P13), SB1(P14)	• Must be specified with respect to falling edge of SIOCLK. • Must be specified as the time to the beginning of output state change in open drain output mode. • See Fig. 6.	2.2 to 5.5			(1/3)tCYC +0.05	

Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

Pulse Input Conditions at Ta = -20°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
High/low level pulse width	tPIH(1) tPIL(1)	INT0(P70), INT1(P71), INT2(P72)	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.2 to 5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3(P73) when noise filter time constant is 1/1	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.2 to 5.5	2			
	tPIH(3) tPIL(3)	INT3(P73) when noise filter time constant is 1/32	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.2 to 5.5	64			
	tPIH(4) tPIL(4)	INT3(P73) when noise filter time constant is 1/128	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.2 to 5.5	256			
	tPIH(5) tPIL(5)	MICIN(P87)	The pulses can be counted by the small signal sensor/counter.	2.2 to 5.5	1			
	tPIH(6) tPIL(6)	RMIN(P73)	The pulses can be recognized as signals by the infrared remote control receiver circuit.	2.2 to 5.5	3			RMCK (Note5-1)
	tPIL(7)	$\overline{RES}$	Resetting is enabled.	2.2 to 5.5	2000			µs

Note 5-1: RMCK denotes the frequency of the base clock (1tCYC to 128tCYC/subclock source oscillation frequency) for the infrared remote control receiver circuit

AD Converter Characteristics at $V_{SS}1 = V_{SS}2 = 0V$

<12bits AD Converter Mode at Ta =-30 to +70°C>

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Resolution	N	AN0(P80) to AN7(P87), AN8(P70), AN9(P71), AN10(XT1), AN11(XT2)		3.0 to 5.5		12		bit
Absolute accuracy	ET		(Note 6-1)	3.0 to 5.5			±16	LSB
Conversion time	tCAD		See conversion time calculation formulas. (Note 6-2)	4.0 to 5.5	32		100	µs
				3.0 to 5.5	40		100	
Analog input voltage range	VAIN				V_{SS}		V_{DD}	V
Analog port input current	IAINH		VAIN=V_{DD}				1	µA
	IAINL		VAIN=V_{SS}	5	-1			

<8bits AD Converter Mode at Ta =-30 to +70°C>

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Resolution	N	AN0(P80) to AN7(P87), AN8(P70), AN9(P71), AN10(XT1) AN11(XT2)		3.0 to 5.5		8		bit
Absolute accuracy	ET		(Note 6-1)	3.0 to 5.5			1.5	LSB
Conversion time	tCAD		See "Conversion time calculation method." (Note 6-2)	4.0 to 5.5	20		90	µs
				3.0 to 5.5	40		90	
			See "Conversion time calculation method." (Note 6-2) Ta=-10 to 50°C	3.0 to 5.5	V_{SS}		V_{DD}	
Analog input voltage range	VAIN			3.0 to 5.5			1	V
Analog port input current	IAINH		VAIN=V_{DD}	3.0 to 5.5	-1			µA
	IAINL		VAIN=V_{SS}	3.0 to 5.5	-1			

<Conversion time calculation method>

12bits AD Converter Mode: tCAD (conversion time) = ((52/(division ratio)) + 2) × (1/3)×tCYC
8bits AD Converter Mode: tCAD (conversion time) = ((32/(division ratio)) + 2) × (1/3)×tCYC

<Recommended Operating Conditions>

External oscillator FmCF[MHz]	Supply Voltage Range V_{DD}[V]	System Clock Division (SYSDIV)	Cycle Time tCYC [ns]	AD Frequency Division Ratio (ADDIV)	Conversion Time (tCAD)[µs]	
					12-bit AD	8-bit AD
12	4.0 to 5.5	1/1	250	1/8	34.8	21.5
	3.0 to 5.5	1/1	250	1/16	69.5	42.8

Note 6-1: The quantization error (±1/2LSB) is excluded from the absolute accuracy value. The absolute accuracy refers to the accuracy that is measured while there is no change in the I/O state of the pins adjacent to the analog input channel.

Note 6-2: The conversion time refers to the interval from the time the instruction for starting the converter is issued till the time the complete digital- conversion-value corresponding to the analog input value is loaded in the required register.

Consumption Current Characteristics at Ta = -20°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Normal mode consumption current (Note 7-1)	IDDOP(1)	$V_{DD}1 = V_{DD}2 = V_{DD}3$	• FmCF=12MHz ceramic oscillation mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 12MHz side • Internal RC oscillation stopped • Multifrequency RC oscillation stopped • 1/1 frequency division ratio	4.5 to 5.5		8.2	18.0	mA
	IDDOP(2)			3.0 to 3.6		4.8	10.6	
	IDDOP(3)		• FmCF=8MHz ceramic oscillation mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 8MHz side • Internal RC oscillation stopped • Multifrequency RC oscillation stopped • 1/1 frequency division ratio	4.5 to 5.5		6.4	13.9	
	IDDOP(4)			3.0 to 3.6		3.8	8.8	
	IDDOP(5)			2.5 to 3.0		3.0	6.7	
	IDDOP(6)		• FmCF=4MHz ceramic oscillation mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 4MHz side • Internal RC oscillation stopped • Multifrequency RC oscillation stopped • 1/2 frequency division ratio	4.5 to 5.5		3.9	8.5	
	IDDOP(7)			3.0 to 3.6		2.5	5.2	
	IDDOP(8)			2.2 to 3.0		2.1	4.3	
	IDDOP(9)		• FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillation mode • System clock set to internal RC oscillation • Multifrequency RC oscillation stopped • 1/2 frequency division ratio	4.5 to 5.5		0.7	1.6	
	IDDOP(10)			3.0 to 3.6		0.4	0.9	
	IDDOP(11)			2.2 to 3.0		0.3	0.7	
	IDDOP(12)		• FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillation mode • Internal RC oscillation stopped • System clock set to 10MHz multifrequency RC oscillation • 1/1 frequency division ratio	4.5 to 5.5		7.6	16.7	
	IDDOP(13)			3.0 to 3.6		4.3	9.5	
	IDDOP(14)		• FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillation mode • Internal RC oscillation stopped • System clock set to 4MHz multifrequency RC oscillation • 1/1 frequency division ratio	4.5 to 5.5		4.1	8.9	
	IDDOP(15)			3.0 to 3.6		2.3	5.0	
	IDDOP(16)			2.2 to 3.0		2.0	4.1	
	IDDOP(17)		• FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz side • Internal RC oscillation stopped • Multifrequency RC oscillation stopped • 1/2 frequency division ratio	4.5 to 5.5		41.8	171.4	µA
	IDDOP(18)			3.0 to 3.6		17.7	84.3	
	IDDOP(19)			2.2 to 3.0		13	67.2	

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

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Parameter	Symbol	Pin/ Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
HALT mode consumption current (Note 7-1)	IDDHALT(1)	$V_{DD}1$ =$V_{DD}2$ =$V_{DD}3$	HALT mode • FmCF=12MHz ceramic oscillation • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 12MHz side. • Internal RC oscillation stopped • Multifrequency RC oscillation stopped • 1/1 frequency division ratio	4.5 to 5.5		3.7	8.2	mA
	IDDHALT(2)			3.0 to 3.6		1.9	4.3	
	IDDHALT(3)		HALT mode • FmCF=8MHz ceramic oscillation mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 8MHz side • Internal RC oscillation stopped • Multifrequency RC oscillation stopped • 1/1 frequency division ratio	4.5 to 5.5		6.4	13.9	
	IDDHALT(4)			3.0 to 3.6		3.8	8.8	
	IDDHALT(5)			2.5 to 3.0		3.0	6.7	
	IDDHALT(6)		HALT mode • FmCF=4MHz ceramic oscillation mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 4MHz side • Internal RC oscillation stopped • Multifrequency RC oscillation stopped • 1/2 frequency division ratio	4.5 to 5.5		3.9	8.5	
	IDDHALT(7)			3.0 to 3.6		2.5	5.2	
	IDDHALT(8)			2.2 to 3.0		2.1	4.3	
	IDDHALT(9)		HALT mode • FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillation mode • System clock set to internal RC oscillation • Multifrequency RC oscillation stopped • 1/2 frequency division ratio	4.5 to 5.5		0.4	0.9	
	IDDHALT(10)			3.0 to 3.6		0.18	0.4	
	IDDHALT(11)			2.2 to 3.0		0.13	0.3	
	IDDHALT(12)		HALT mode • FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillation mode • Internal RC oscillation stopped • System clock set to 10MHz multifrequency RC oscillation • 1/1 frequency division ratio	4.5 to 5.5		3.4	7.3	
	IDDHALT(13)			3.0 to 3.6		1.7	3.7	
	IDDHALT(14)		HALT mode • FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillation mode • Internal RC oscillation stopped • System clock set to 4MHz multifrequency RC oscillation • 1/1 frequency division ratio	4.5 to 5.5		1.7	3.9	
	IDDHALT(15)			3.0 to 3.6		0.8	1.8	
	IDDHALT(16)			2.2 to 3.0		0.6	1.4	
	IDDHALT(17)		HALT mode • FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz side • Internal RC oscillation stopped • Multifrequency RC oscillation stopped • 1/2 frequency division ratio	4.5 to 5.5		25.7	141.9	µA
	IDDHALT(18)			3.0 to 3.6		8.3	66.6	
	IDDHALT(19)			2.2 to 3.0		5.2	52.3	
HOLD mode consumption current	IDDHOLD(1)	$V_{DD}1$	HOLD mode • CF1=V_{DD} or open (external clock mode)	4.5 to 5.5		0.14	28.0	
	IDDHOLD(2)			3.0 to 3.6		0.03	19.0	
	IDDHOLD(3)			2.2 to 3.0		0.03	16.0	
Clock HOLD mode consumption current	IDDHOLD(4)	$V_{DD}1$	Clock HOLD mode • CF1=V_{DD} or open (external clock mode) • FmX'tal=32.768kHz crystal oscillation mode	4.5 to 5.5		21.9	80	
	IDDHOLD(5)			3.0 to 3.6		6.3	37	
	IDDHOLD(6)			2.2 to 3.0		3.6	30	

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

F-ROM Programming Characteristics at Ta = +10°C to +55°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

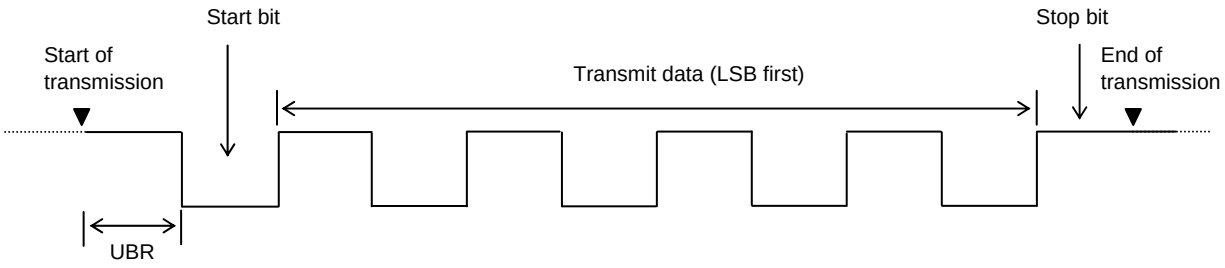
Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Onboard programming current	IDDFW(1)	$V_{DD}1$	• 128-byte programming • Erasing current included	3.0 to 5.5				mA
Programming time	tFW(1)		• 128-byte programming • Erasing current included • Time for setting up 128-byte data is excluded.	3.0 to 5.5				ms

UART (Full Duplex) Operating Conditions at Ta = -20 to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

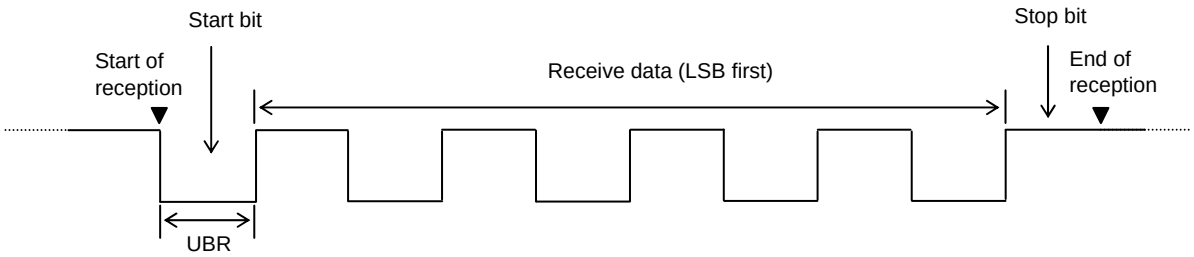
Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Transfer rate	UBR	UTX(P00), URX(P01)		2.2 to 5.5	16/3		8192/3	tCYC

Data length: 7/8/9 bits (LSB first)
Stop bits: 1 bit (2-bit in continuous data transmission mode)
Parity bits: None

Example of 8-bit Data Transmission Mode Processing (Transmit Data=55H)



Example of 8-bit Data Reception Mode Processing (Receive Data=55H)



*When using UART, set P0LDDR (PODDR: Bit0) to “0”

Characteristics of a Sample Main System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a SANYO-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Oscillator

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rf1 [Ω]	Rd1 [Ω]		typ [ms]	max [ms]	
12MHz	MURATA	CSTCE12M0G52-R0	(10)	(10)	Open	2.2k	2.8 to 5.5			Built-in C1, C2
8MHz	MURATA	CSTCE8M00G52-R0	(10)	(10)	Open	1.0k	2.5 to 5.5			Built-in C1, C2
		CSTLS8M00G52-R0	(15)	(15)	Open	1.0k				
4MHz	MURATA	CSTCR4M00F53-R0	(15)	(15)	Open	2.2k	2.1 to 5.5			Built-in C1, C2
		CSTLS4M0053-B0	(15)	(15)	Open	2.2k				

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after V_{DD} goes above the operating voltage lower limit (see Figure 4).

Characteristics of a Sample Subsystem Clock Oscillator Circuit

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a SANYO-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit with a Crystal Oscillator

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C3 [pF]	C4 [pF]	Rf2 [Ω]	Rd2 [Ω]		typ [s]	max [s]	
32.768kHz										

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillation circuit is executed and to the time interval that is required for the oscillation to get stabilized after the HOLD mode is reset (see Figure 4).

Caution: The components that are involved in oscillation should be placed as close to the IC and to one another as possible because they are vulnerable to the influences of the circuit pattern.

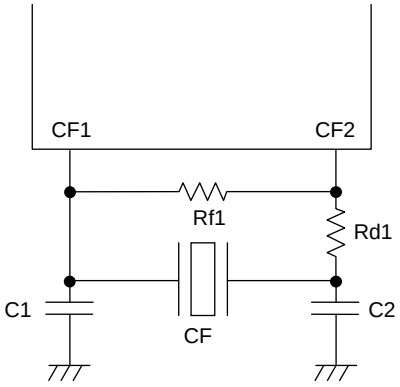


Figure 1 CF Oscillator Circuit

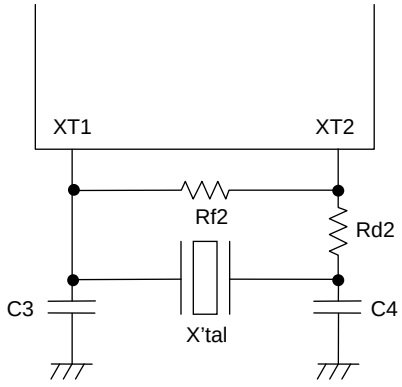


Figure 2 XT Oscillator Circuit

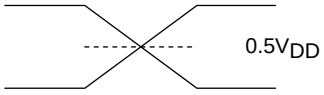
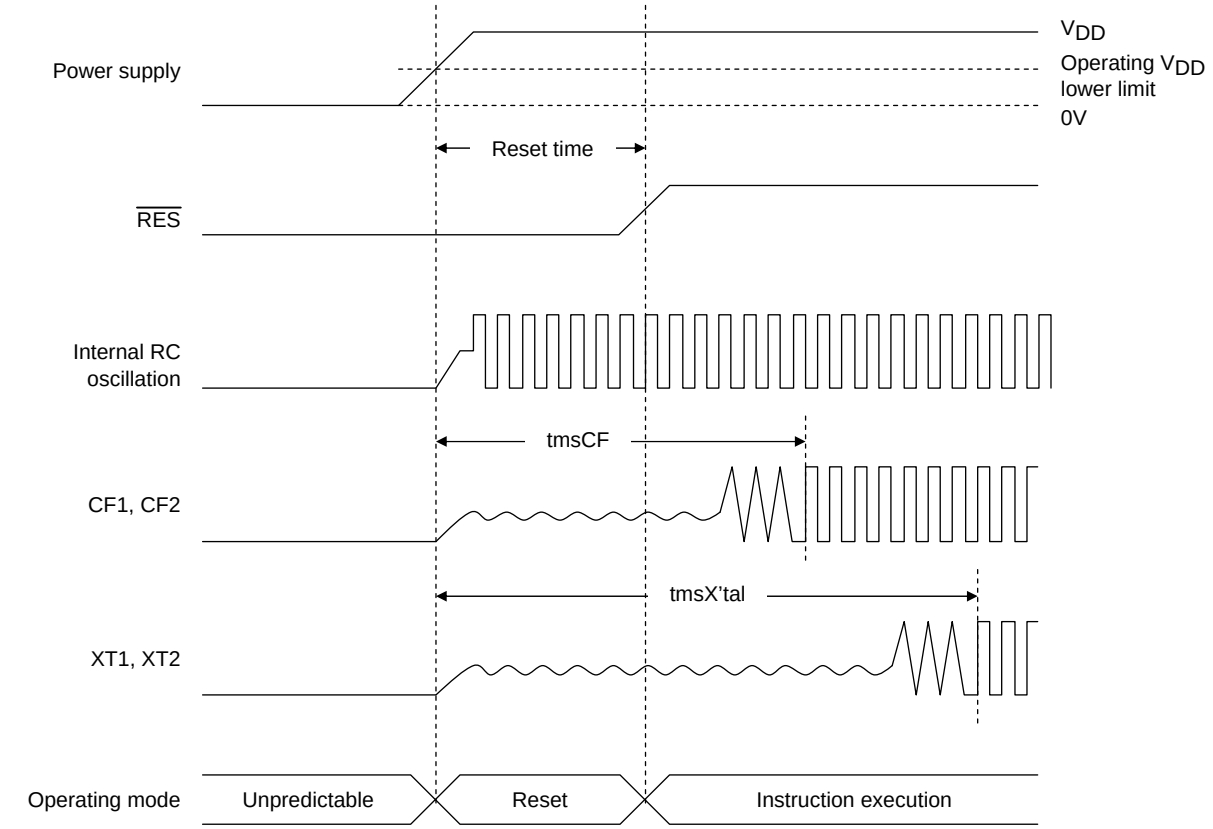
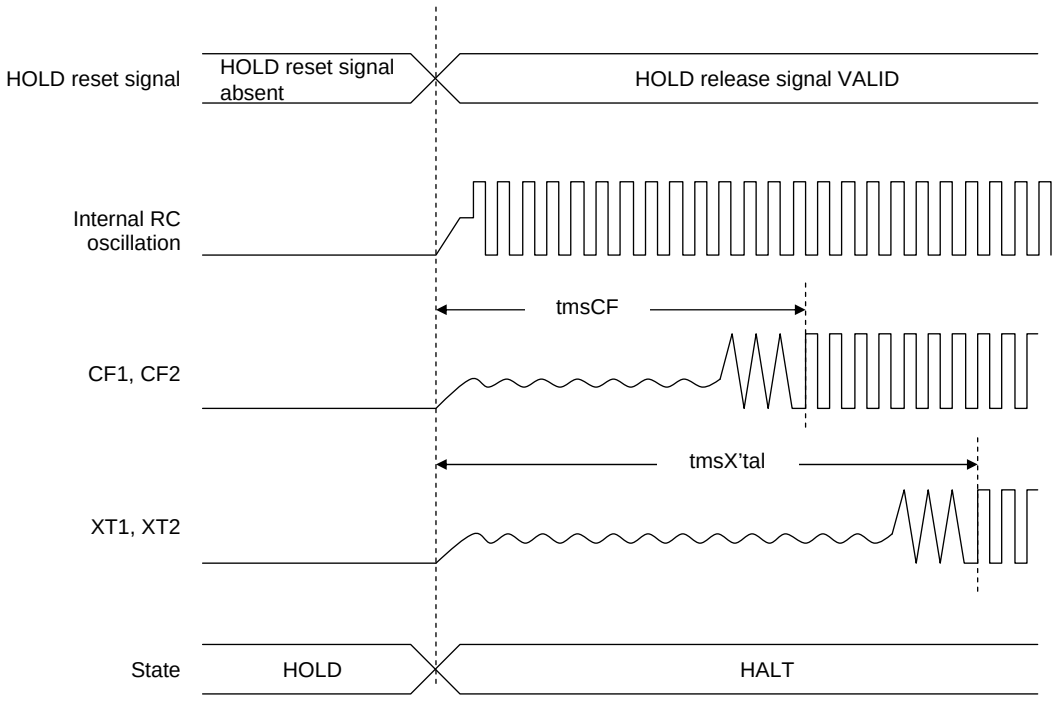


Figure 3 AC Timing Measurement Point

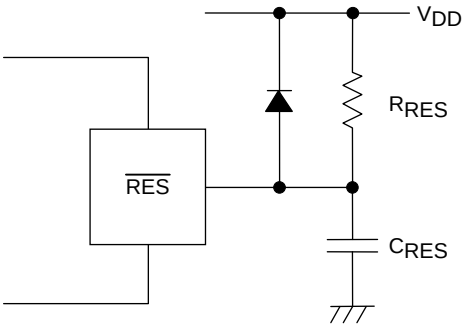


Reset Time and Oscillation Stabilization Time



HOLD Reset Signal and Oscillation Stabilization Time

Figure 4 Oscillation Stabilization Times



Note:
Determine the value of C_{RES} and R_{RES} so that the reset signal is present for a period of 200µs after the supply voltage goes beyond the lower limit of the IC's operating voltage.

Figure 5 Reset Circuit

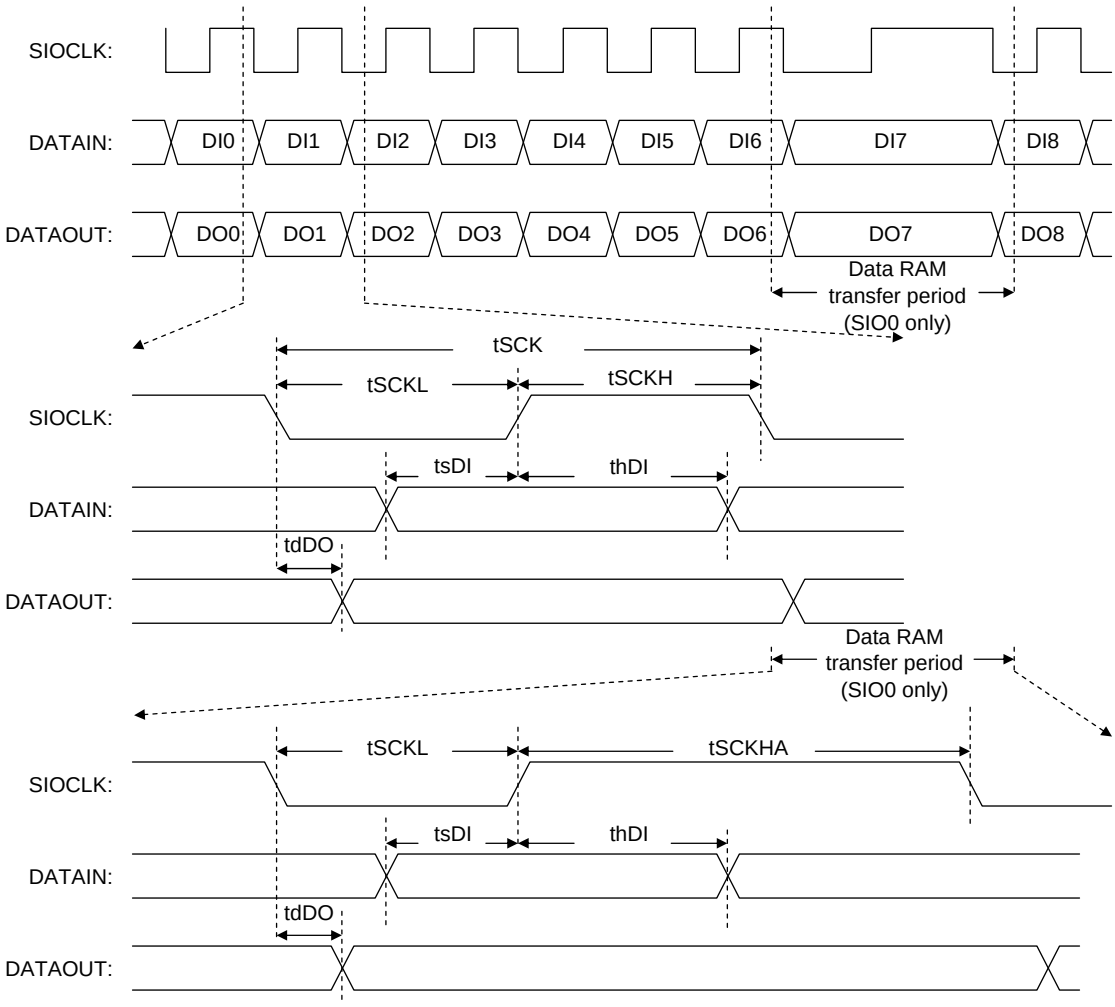


Figure 6 Serial I/O Waveforms

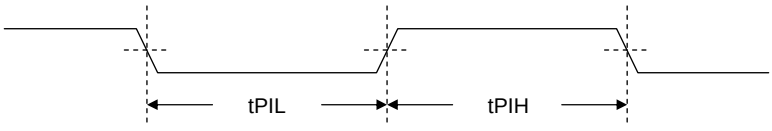


Figure 7 Pulse Input Timing Signal Waveform

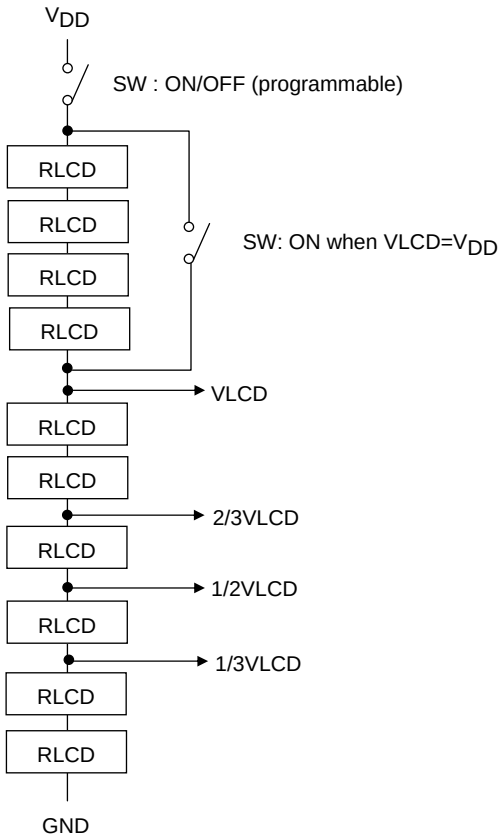


Figure 8 LCD Bias Resistors

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