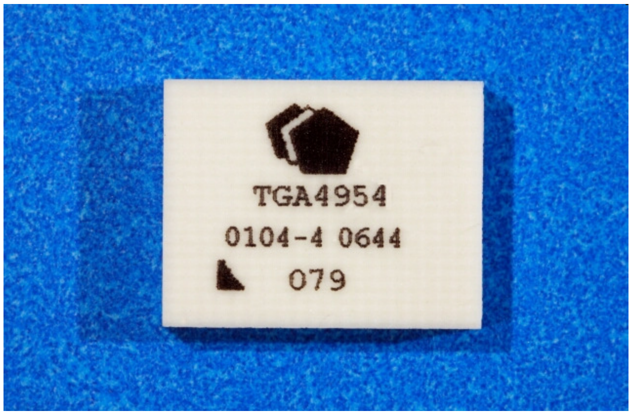
9.9 - 12.5 Gb/s Optical Modulator Driver TGA4954-SL



Key Features and Performance

- Wide Drive Range (3V to 10V)
- Single-Ended Input/Output
- Low Power Dissipation (1.1W @ 6Vo)
- Low Rail Ripple
- 25psec Edge Rates (20/80%)
- Hot-pluggable
- Package Dimensions:
  11.4 x 8.9 x 2.0 mm
  (0.450 x 0.350 x 0.080 inches)

Product Description

The TriQuint TGA4954-SL is part of a series of surface mount modulator drivers suitable for a variety of driver applications and is compatible with Metro MSA standards.

The TGA4954-SL consists of two high performance wideband amplifiers combined with off chip circuitry assembled in a surface mount package. A single TGA4954-SL placed between the MUX and Optical Modulator provides OEMs with a board level modulator driver surface mount solution.

The TGA4954-SL provides Metro and Long Haul designers with system critical features such as: low power dissipation (1.1W at Vo = 6V), low rail ripple, high voltage drive capability at 5V bias (6 V amplitude adjustable to 3 V), low output jitter, and low input drive sensitivity (250mV at Vo = 6V).

The TGA4954-SL requires external DC blocks, a low frequency choke, and control circuitry.

Evaluation boards available upon request.

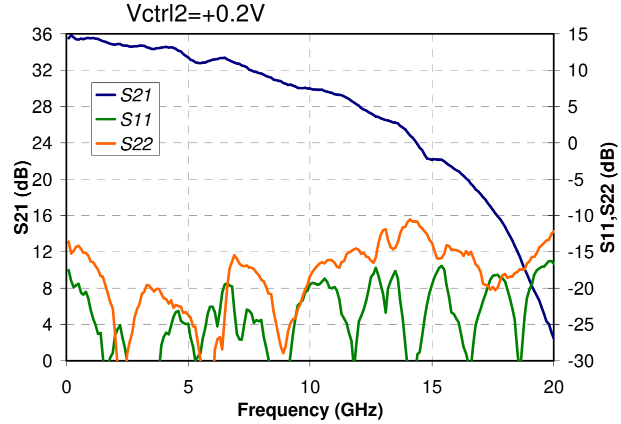
Lead Free finish & RoHS compliant.

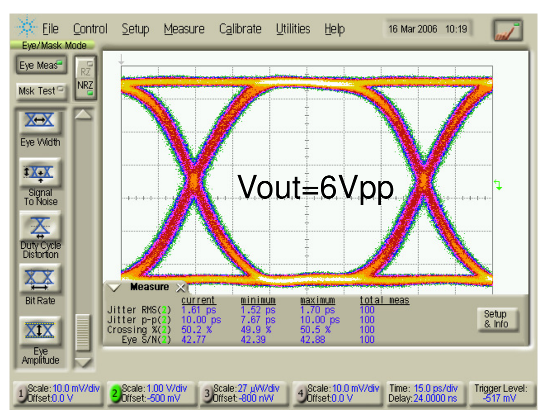
Primary Applications

- Mach-Zehnder Modulator Driver

Measured Data

Vdd=5V; Id1=65mA; Id2T=115mA; Vctrl1=-0.2V; Vctrl2=+0.2V





TriQuint Semiconductor: www. triquint.com (972)994-8465 Fax (972)994-8504 info-networks@tqs.com

TABLE I
MAXIMUM RATINGS

Symbol	Parameter	Value	Notes
V_{D1} V_{D2T}	Drain Voltage	8 V	1/ 2/
V_{G1} V_{G2}	Gate Voltage Range	-3V to 0V	1/
V_{CTRL1} V_{CTRL2}	Control Voltage Range	-3V to V_D	1/
I_{D1} I_{D2T}	Drain Supply Current (Quiescent)	200 mA 350 mA	1/ 2/
$\| I_{G1} \|$ $\| I_{G2} \|$	Gate Supply Current	15 mA	1/
$\| I_{CTRL1} \|$ $\| I_{CTRL2} \|$	Control Supply Current	15 mA	1/
P_{IN}	Input Continuous Wave Power	23 dBm	1/ 2/
V_{IN}	12.5Gb/s PRBS Input Voltage	4 V_{PP}	1/ 2/
P_D	Power Dissipation	4 W	1/ 2/ 3/
T_{CH}	Operating Channel Temperature	150 ^{0}C	4/
T_M	Mounting Temperature (10-20 Seconds)	260 ^{0}C	
T_{STG}	Storage Temperature	-65 to 150 ^{0}C	

1/ These ratings represent the maximum operable values for this device

2/ Combinations of supply voltage, supply current, input power, and output power shall not exceed P_D at a package base temperature of 80°C

3/ When operated at this bias condition with a baseplate temperature of 80°C, the MTTF is reduced

4/ Junction operating temperature will directly affect the device median time to failure (MTTF). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.

TABLE II
THERMAL INFORMATION

Parameter	Test Conditions	T_{CH} (°C)	$R_{\Theta JC}$ (°C/W)	MTTF (hrs)
$R_{\Theta JC}$ Thermal Resistance (Channel to Backside of Package)	V_{DD} = 5V I_{DD} = 215mA P_{DISS} = 1.08W T_{BASE} = 70°C	92	20.4	>1E6

Note: Thermal transfer is conducted through the bottom of the TGA4954-SL package into the motherboard. The motherboard must be designed to assure adequate thermal transfer to the base plate.

TABLE III
RF CHARACTERIZATION TABLE
(T_A = 25°C, Nominal)

Parameter	Test Conditions	Min	Typ	Max	Units	Notes
Small Signal Bandwidth			8		GHz	
Saturated Power Bandwidth			12		GHz	
Small Signal Gain	0.1, 2, 4 GHz 6 GHz 10 GHz 14 GHz 16 GHz	28 26 24 17 12	34 33 30 25 21		dB	1/
Input Return Loss	0.1, 2, 4, 6, 10, 14, 16 GHz	10	15		dB	1/
Output Return Loss	0.1, 2, 4, 6, 10, 14, 16 GHz	10	15		dB	1/
Noise Figure	3 GHz		2.5		dB	
Small Signal AGC Range	Midband		28		dB	
Saturated Output Power	2, 4, 6, 8 & 10 GHz	24	26.5		dBm	4/ 5/

TABLE III (Continued)
RF CHARACTERIZATION TABLE
(T_A = 25°C, Nominal)

Parameter	Test Conditions	Min	Typ	Max	Units	Notes
Eye Amplitude	V_{D2} = 8.0V V_{D2} = 6.5V V_{D2} = 5.5V V_{D2} = 4.5V V_{D2} = 4.0V	9.0 7.0 6.0 5.5 5.0			V_{PP}	2/
Additive Jitter (RMS)	V_{IN} = 500mV_{PP} V_{IN} = 800mV_{PP}		1.2 1.4	3.0 3.0	psec	3/
Q-Factor	V_{IN} = 500mV_{PP} V_{IN} = 800mV_{PP}	25 25	42 42		V/V	
Delta Eye Amplitude	800mV_{PP}	-0.50	0.0	0.50	V_{PP}	
Delta Crossing Percentage	500–800 mV $_{in\ p-p}$	-8		8	%	

Table III Notes:

1/ Typical Package RF Bias Conditions: Vdd = 5V, adjust V_{G1} to achieve I_{D1} = 65mA then adjust V_{G2} to achieve I_{D2T} = 115mA – 155 mA (Idd = 180 – 220 mA), V_{CTRL1} = -0.2V & V_{CTRL2} = +0.2 V

2/ V_{IN} = 250mV, Data Rate = 10.7Gb/s, V_{D1} = V_{D2T} or greater, V_{CTRL2} and V_{G2} are adjusted for maximum output. Typical final Idd under drive ~ 220 mA.

3/ Computed using RSS Method where $J_{RMS\_DUT} = \sqrt{(J_{RMS\_TOTAL}^2 - J_{RMS\_SOURCE}^2)}$

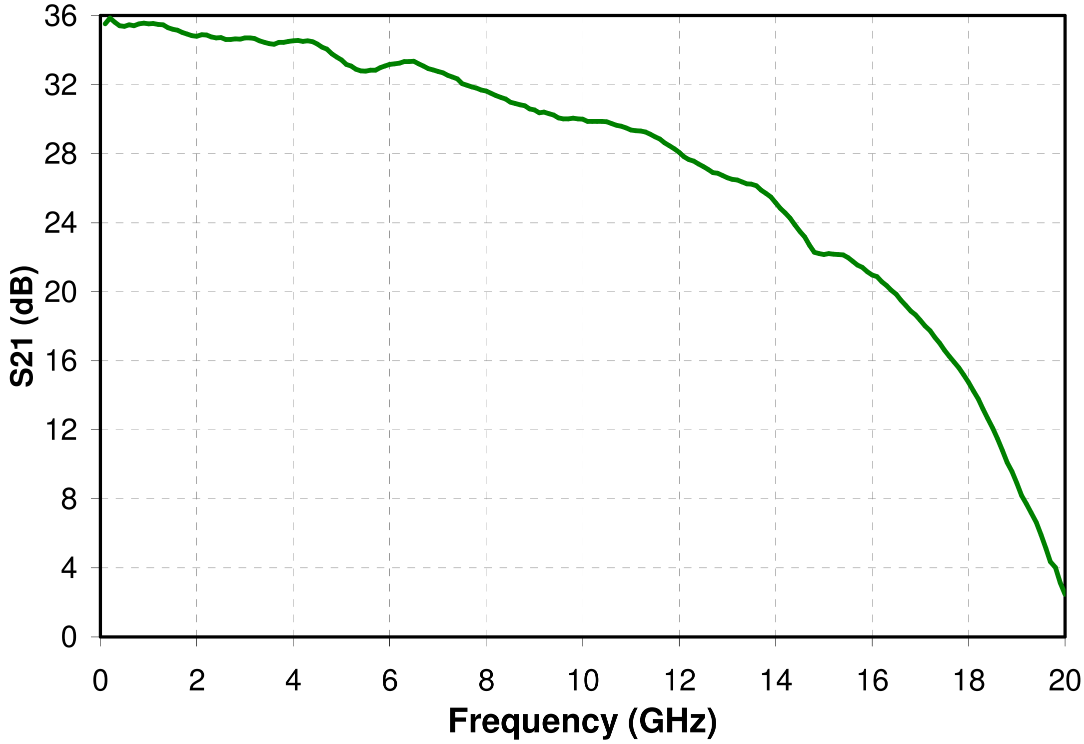
4/ Verified at die level on-wafer probe

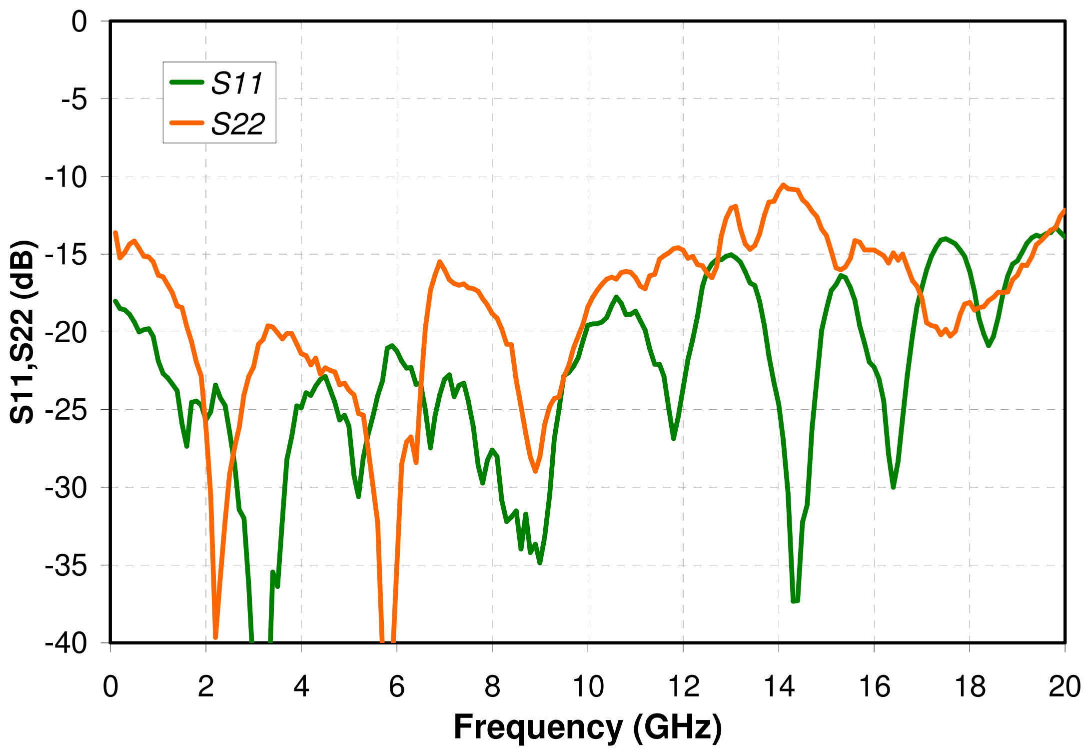
5/ Power Bias Die Probe: V_{TEE} = 8V, adjust V_G to achieve Idd = 175mA ±5%, V_{CTRL} = +1.5V

Note: At the die level, drain bias is applied through the RF output port using a bias tee, voltage is at the DC input to the bias tee

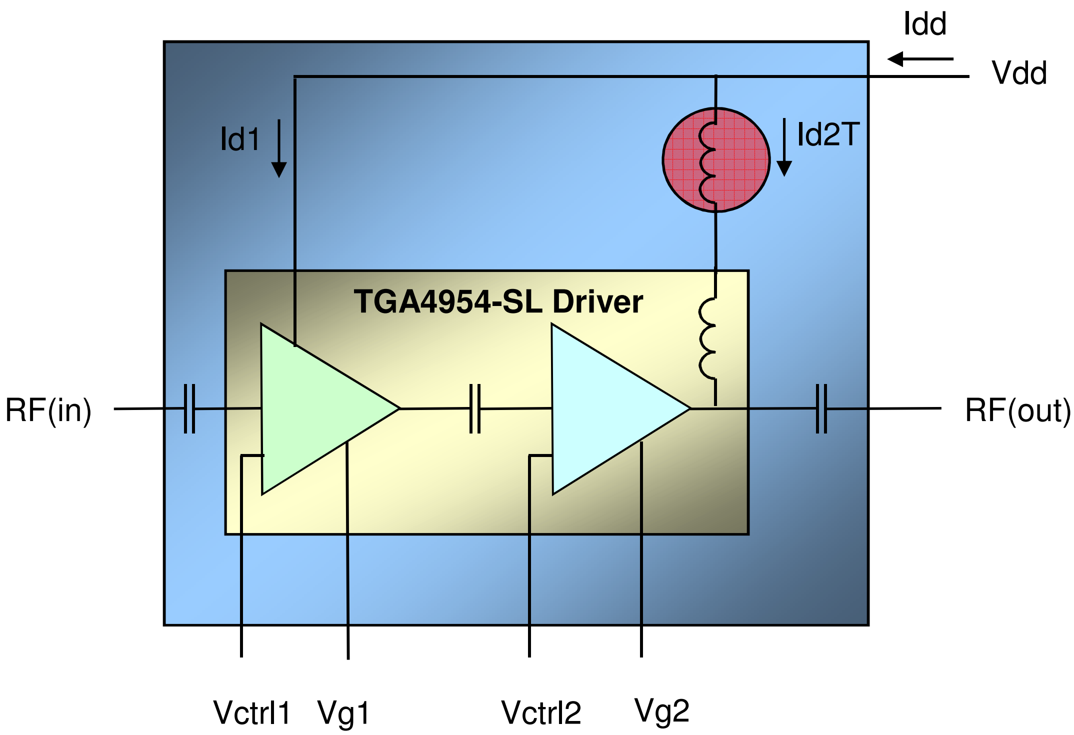
Measured Data

Vdd=5V; Id1=65mA; Id2=115mA; Vctrl1=-0.2V; Vctrl2=+0.2V





TGA4954-SL Typical Performance Data is measured in a Test Fixture

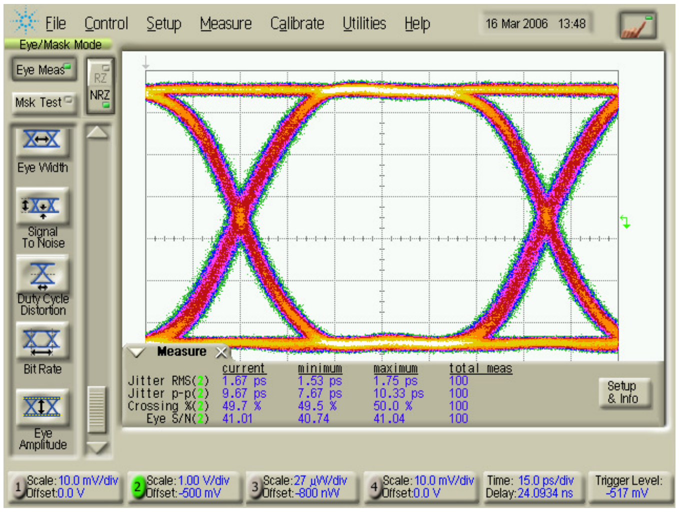


Test Fixture Block Diagram

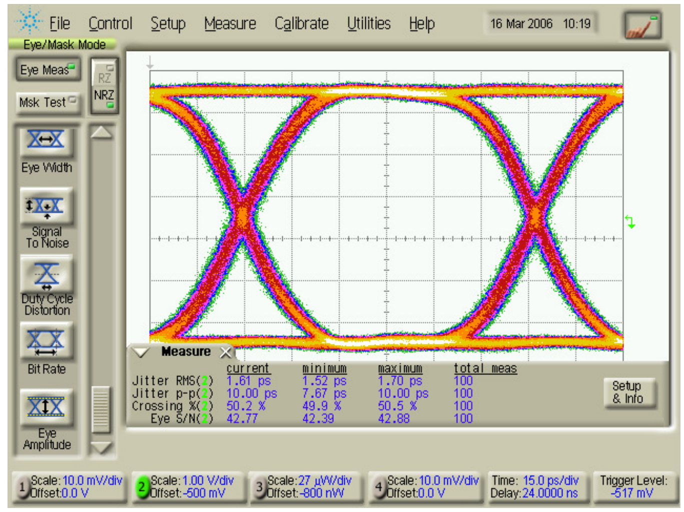
Measured Data

Vdd=5V; Id1=65mA; Vctrl1=-0.2V; Vin=500mVpp; Vo=6Vpp
Vg2 & Vctrl2 are varied to achieve 6Vo & 50% crossing

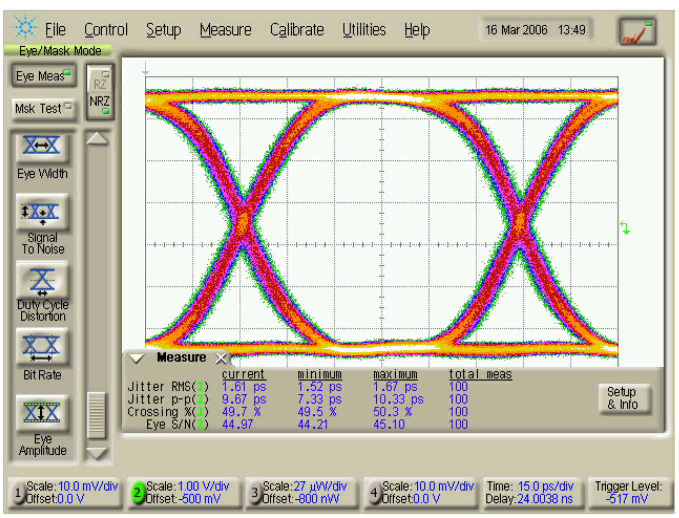
9.953Gbps



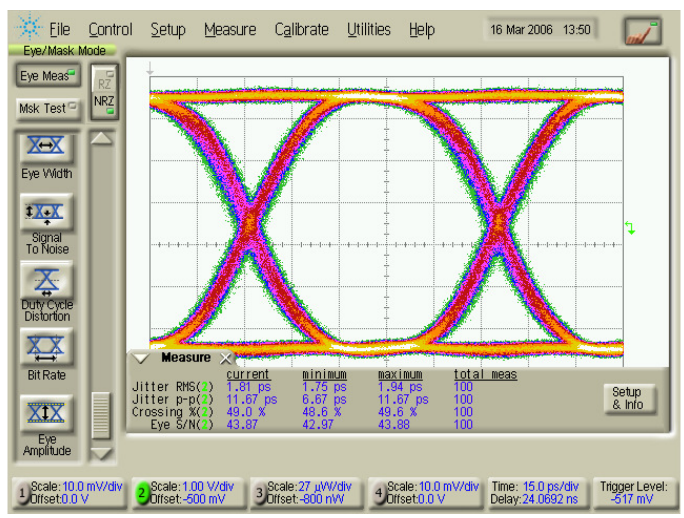
10.7Gbps



11.3Gbps



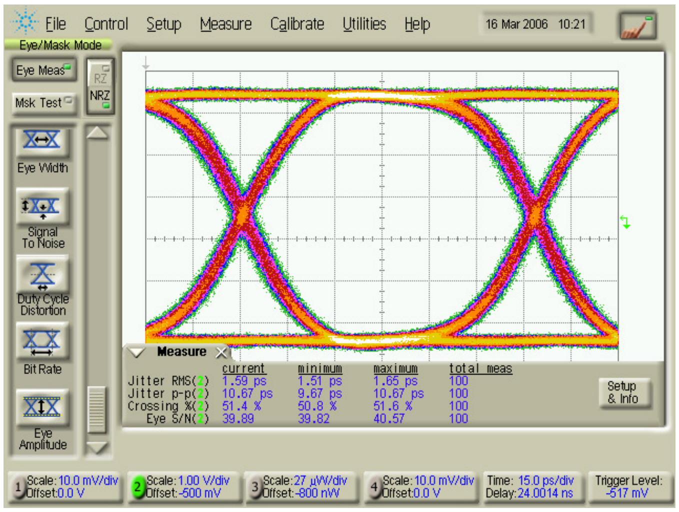
12.5Gbps



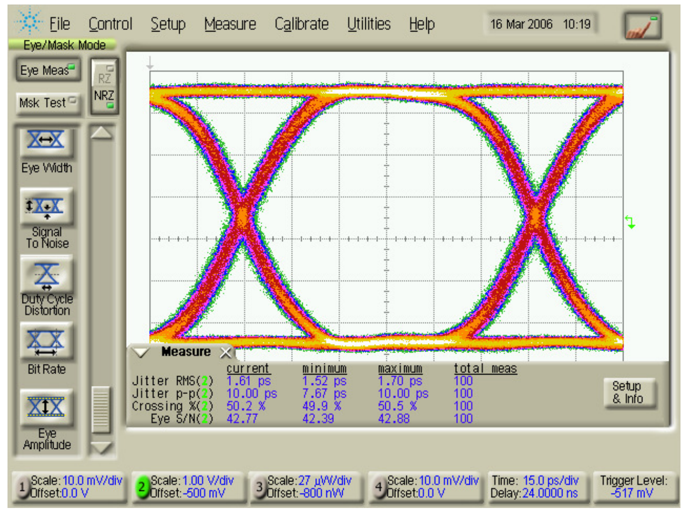
Measured Data

Vdd=5V; Id1=65mA; Vctrl1=-0.2V; Vo=6Vpp; 10.7Gbps
Vg2 & Vctrl2 are varied to achieve 6Vo & 50% crossing

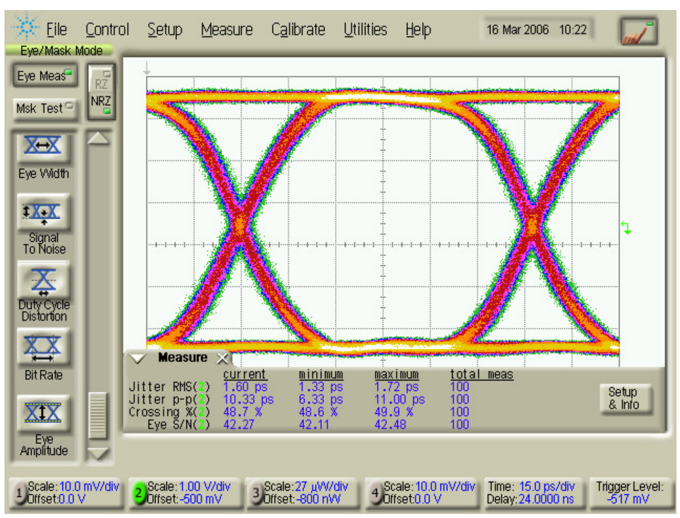
Vin=250mVpp



Vin=500mVpp



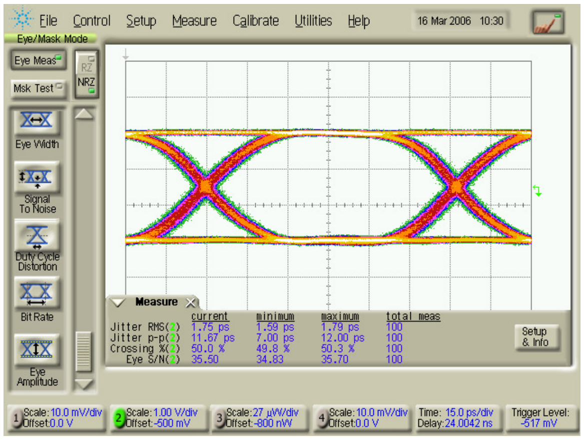
Vin=800mVpp



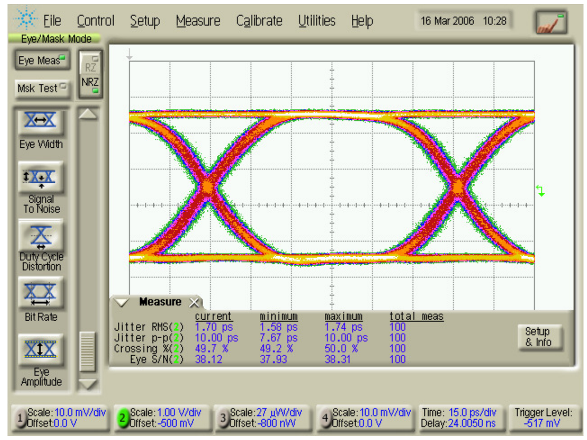
Measured Data

Vdd=5V; Id1=65mA; Vctrl1=-0.2V; Vin=500mVpp; 10.7Gbps
Vg2 & Vctrl2 are varied to achieve 6Vo & 50% crossing

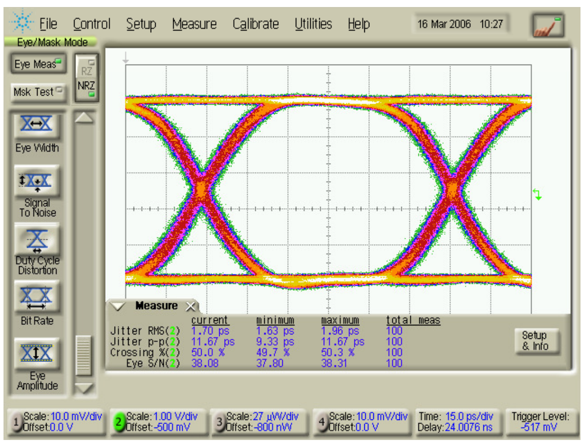
3Vo



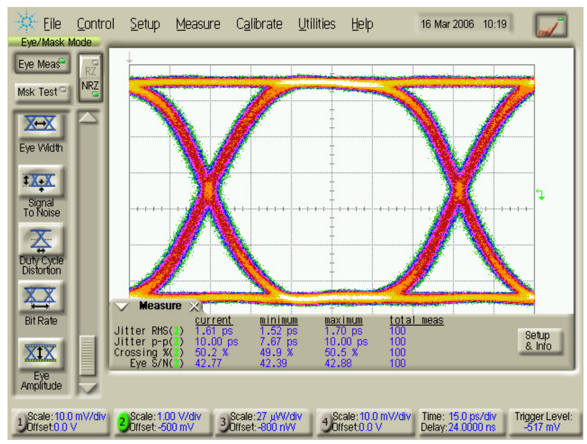
4Vo



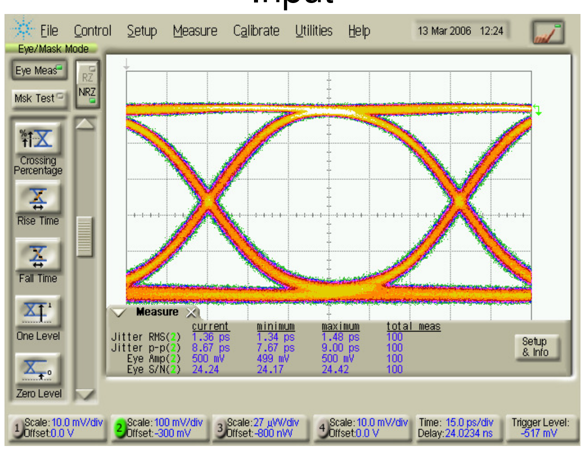
5Vo



6Vo



Input



Production - Initial Alignment - Bias Procedure

Vdd=5V, Vo=6Vamp, CPC=50%

(Hot-Pluggable)

Bias Network Initial Conditions -

Vg1=-1.5V
Vg2=-1.5V
Vctrl1=-0.2V
Vctrl2=+.1V
Vdd=5V

Bias ON

1. Disable the output of MUX
2. Apply Vg1, Vg2, Vctrl1 and Vctrl2 in any sequence.
3. Apply Vdd.
4. Make Vg1 more positive until **Idd=65mA**.
   - This is Id1 (current into the first stage)
   - Typical value for **Vg1 is -0.65V**
5. Make Vg2 more positive until Idd=180 – 220 mA.
   - This sets Id2T to 115 – 155 mA.
   - Typical value for Vg2 is -0.55V
6. Enable the output of the MUX.
   - Set Vin=500mV
7. Output Swing Adjust: Adjust Vctrl2 slightly positive to increase output swing or adjust Vctrl2 slightly negative to decrease the output swing.
   - Typical value for **Vctrl2 is +0.22V** for Vo=6V.
8. Crossover Adjust: Adjust Vg2 slightly positive to push the crossover down or adjust Vg2 slightly negative to push the crossover up.
   - Typical value for **Vg2 is -0.57V** to center crossover with Vo=6V.

Bias OFF

1. Remove Vdd.
2. Remove Vg1, Vg2, Vctrl1 and Vctrl2 in any sequence.

General Comments for Production Operation of TGA4954-SL:

1. Due to natural variations in gate voltages observed with GaAs FET amplifiers used internally to the TGA4954-SL, optimal eye performance is obtained when the gate voltages (Vg1 and Vg2) are set to control desired drain currents (Id1 and Id2T)
2. Vc2 feedback circuit recommended for output amplitude correction.

Production - Post Alignment - Bias Procedure
Vdd=5V, Vo=6Vamp, CPC=50%
(Hot-Pluggable)

Bias Network Initial Conditions -
Vg1= As found during initial alignment
Vg2=-As found during initial alignment
Vctrl1=-0.2V
Vctrl2=As found during initial alignment
Vdd=5V

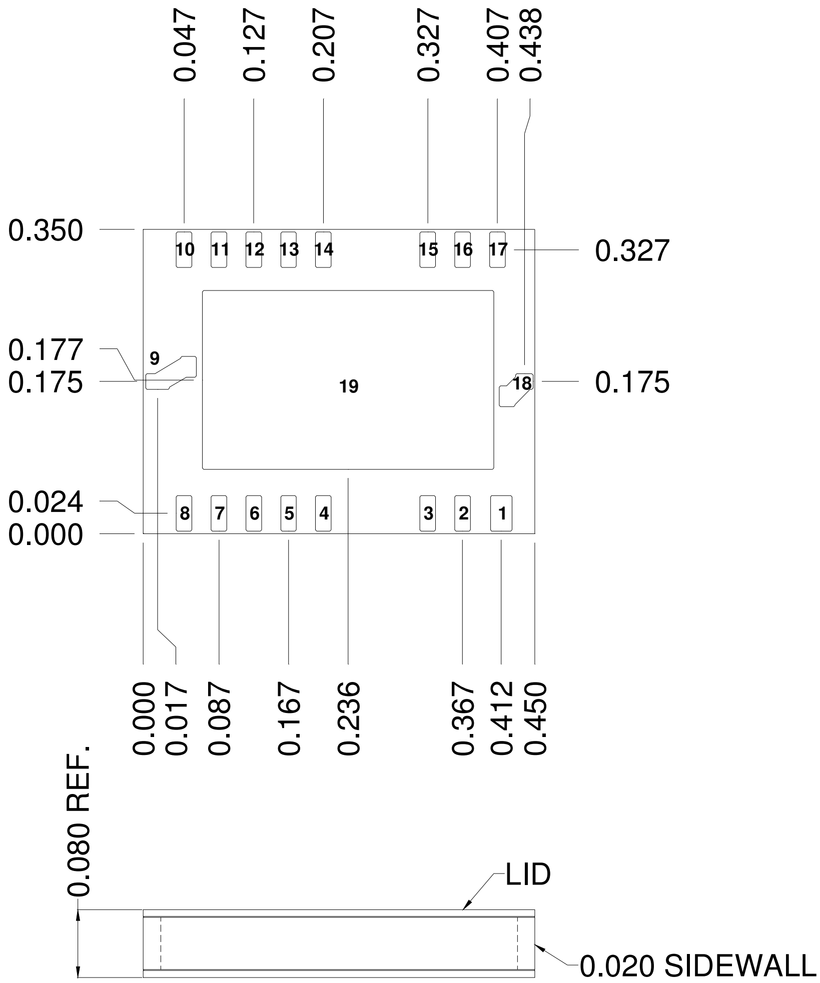
Bias ON
1. Mux output can be either Enabled or Disabled
2. Apply Vg1, Vg2, Vctrl1 and Vctrl2 in any sequence.
3. Apply Vdd.
4. Enable the output of the MUX
5. Output Swing Adjust: Adjust Vctrl2 slightly positive to increase output swing or adjust Vctrl2 slightly negative to decrease the output swing.
6. Crossover Adjust: Adjust Vg2 slightly positive to push the crossover down or adjust Vg2 slightly negative to push the crossover up.

Bias OFF
1. Remove Vdd.
2. Remove Vg1, Vg2, Vctrl1 and Vctrl2 in any sequence.

General Comments for Production Operation of TGA4954-SL:

1. Due to natural variations in gate voltages observed with GaAs FET amplifiers used internally to the TGA4954-SL, optimal eye performance is obtained when the gate voltages (Vg1 and Vg2) are set to control desired drain currents (Id1 and Id2T)
2. Vc2 feedback circuit recommended for output amplitude correction.

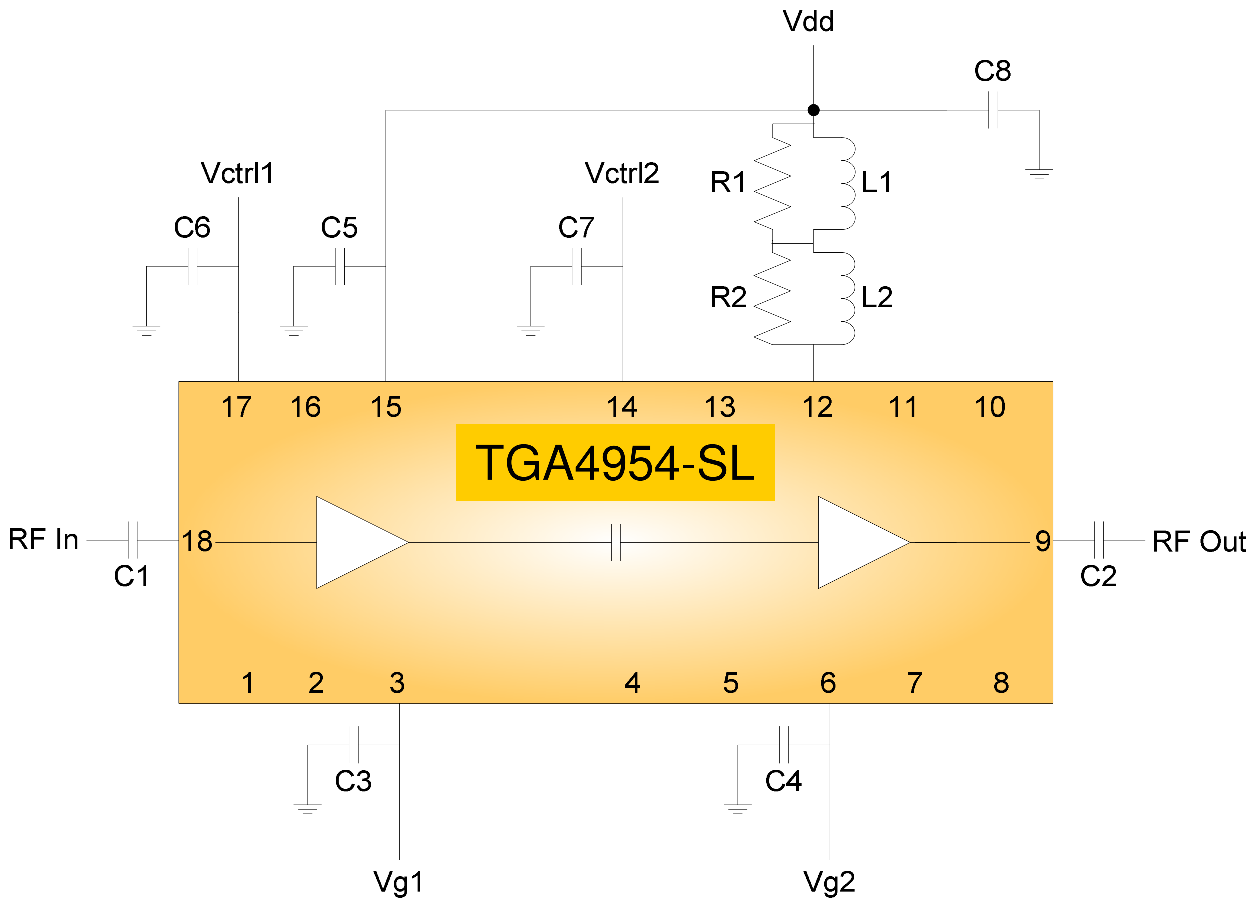
Mechanical Drawing



Bond Pad #1	N/C	0.025 x 0.041	Bond Pad #10	N/C	0.018 x 0.041
Bond Pad #2	N/C	0.018 x 0.041	Bond Pad #11	N/C	0.018 x 0.041
Bond Pad #3	Vg1	0.018 x 0.041	Bond Pad #12	Vd2T	0.018 x 0.041
Bond Pad #4	N/C	0.018 x 0.041	Bond Pad #13	N/C	0.018 x 0.041
Bond Pad #5	N/C	0.018 x 0.041	Bond Pad #14	Vctrl2	0.018 x 0.041
Bond Pad #6	Vg2	0.018 x 0.041	Bond Pad #15	Vd1	0.018 x 0.041
Bond Pad #7	N/C	0.018 x 0.041	Bond Pad #16	N/C	0.018 x 0.041
Bond Pad #8	N/C	0.018 x 0.041	Bond Pad #17	Vctrl1	0.018 x 0.041
Bond Pad #9	RF Out	0.027 x 0.018	Bond Pad #18	RF In	0.020 x 0.018
			Bond Pad #19	GND	0.335 x 0.206

Note for Pin 13: Pin 13 can be soldered to the PCB but MUST be left electrically open.

Application Circuit



Recommended Components:

DESIGNATOR	DESCRIPTION	MANUFACTURER	PART NUMBER
C1, C2	DC Block, Broadband	Presidio	BB0502X7R104M16VNT9820
C3, C4, C5	10uF Capacitor MLC Ceramic	AVX	0802YC106KAT
C6, C7	0.01 uFCapacitor MLC Ceramic	AVX	0603YC103KAT
C8	10 uF Capacitor Tantalum	AVX	TAJA106K016R
L1	220 uH Inductor	Panasonic or Belfuse	ELLCTV221M S581-4000-14
L2	330 nH Inductor	Panasonic	ELJ-FAR33MF2
R1, R2	274 Ω Resistor	Panasonic	ERJ-2RKF2740X

Notes:

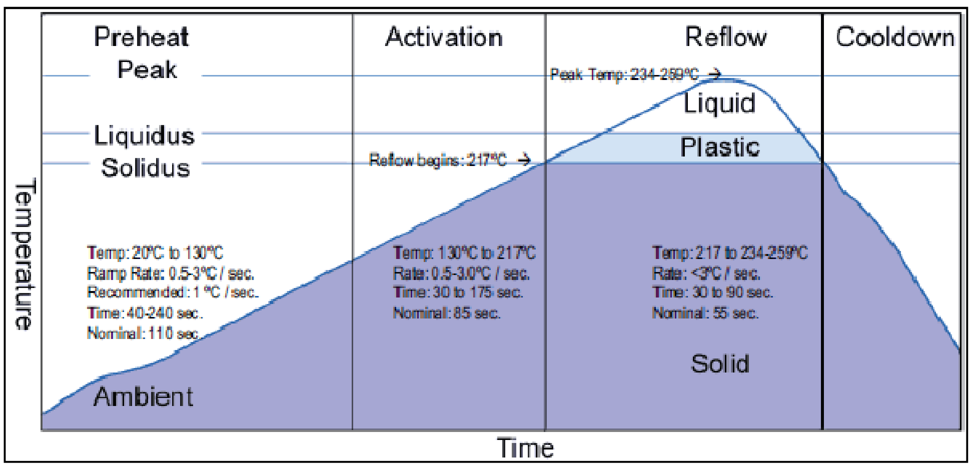
1. C3 and C4 extend low frequency performance thru 30 KHz. For applications requiring low frequency performance thru 100 kHz, C3 and C4 may be omitted

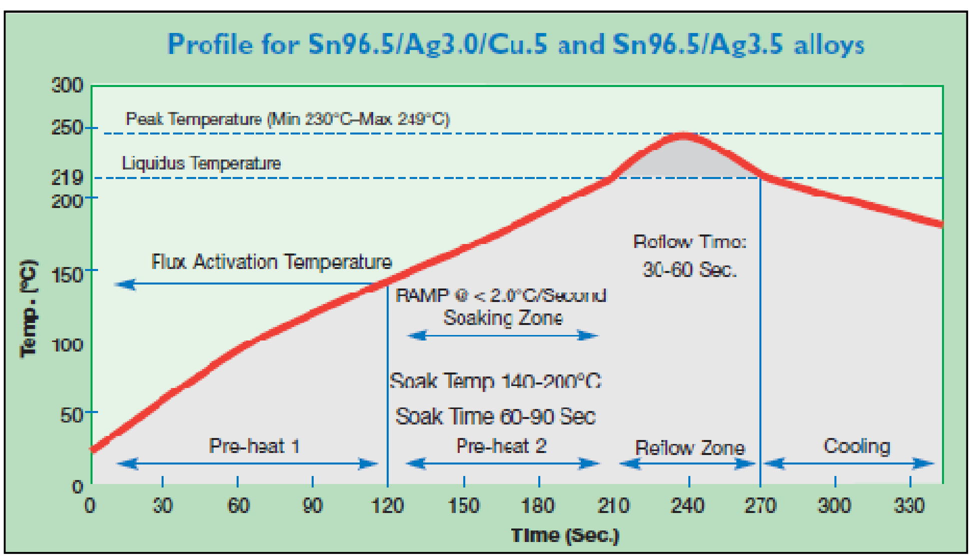
2. C6 and C7 are power supply decoupling capacitors and may be omitted when driven directly with an op-amp. Impedance looking into VCTRL1 and VCTRL2 is 10kΩ real

Assembly Notes

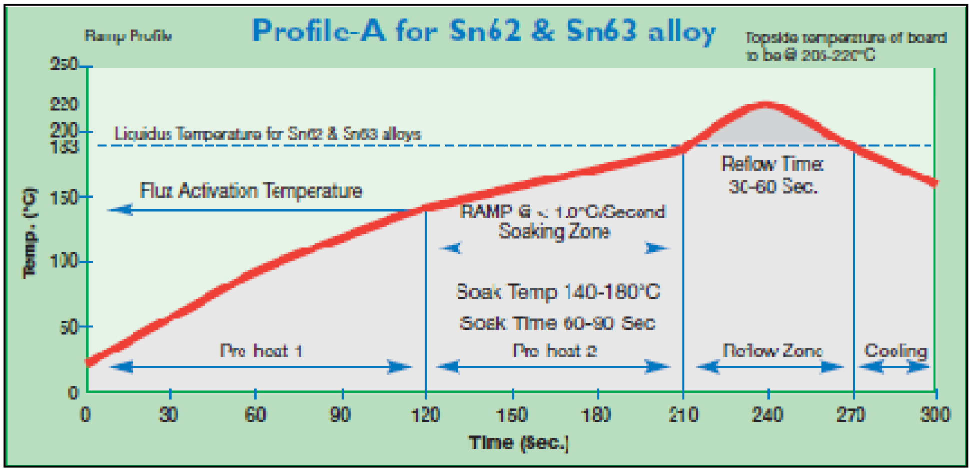
- Proper ESD precautions must be followed while handling parts.
- Parts must be in dry condition prior to soldering. See shipping label instructions.
- TGA4954-SL may be processed using conventional SMT processes.
- Both, lead-free and leaded solders may be used while maintaining following limits:
  - Maximum temperature .... 260°C
  - Total time above 220°C ...... 60 seconds
  - Maximum ramp rate .... 3°C/second
  - Time within 5 °C of Peak Temperature ....10 – 20 sec max
- Typical solder reflow profiles are shown in figures below.
- Hand soldering is not recommended. Solder paste may be applied using a stencil printer or dot placement. The volume of solder paste depends on PCB and component layout and should be well controlled to ensure consistent mechanical and electrical performance.
- TGA4954-SL may be removed from circuit board and re-soldered once. After removal, solder pads must leveled and cleaned. Prior to re-soldering, the part must be dried in accordance with shipping label instructions.

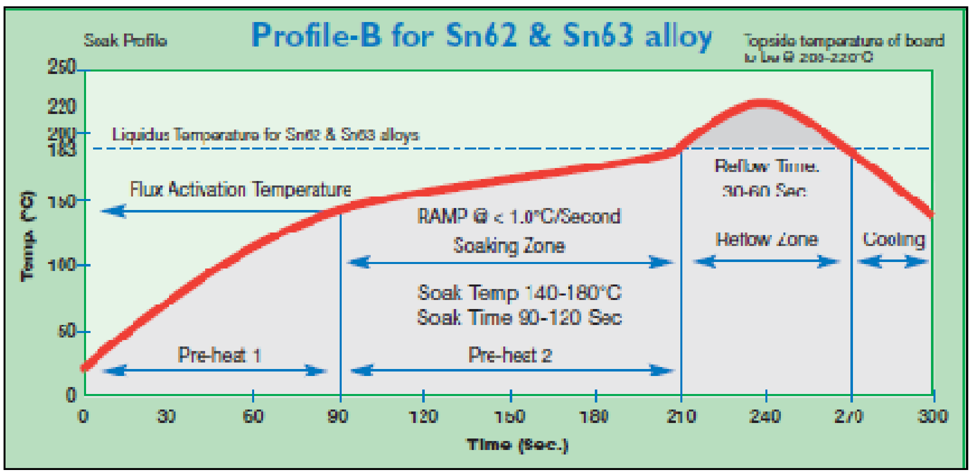
Solder reflow profiles for lead-free solders





Solder reflow profiles for Sn63/Pb37 and Sn62/Pb36/Ag2 solders





Environmental Ratings

Moisture Sensitivity Rating	ESD Rating
MSL3	1B

Ordering Information

Part	Package Style
TGA4954-SL	Land Grid Array, Surface Mount (RoHS)

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.