32-Channel LCD Driver with Separate Backplane Output

Ordering Information

Device	Package Options		
	44 Lead Quad Plastic Gullwing	44 J-Lead Quad Plastic Chip Carrier	Die in waffle pack
HV66	HV66PG	HV66PJ	HV66X

Features

- Processed with HVCMOS® technology
- 32 push-pull CMOS output up to 60V
- Low power level shifting
- Source/sink current minimum 1mA
- Shift register speed 5MHz
- Latched data outputs
- Bidirectional shift register (DIR)
- Backplane output

General Description

The HV66 is a low-voltage serial to high-voltage parallel converter with push-pull outputs. This device has been designed for use as a driver circuit for LCD displays. It can also be used in any application requiring multiple output high-voltage current sourcing and sinking capabilities. The inputs are fully CMOS compatible.

The device consists of a 32-bit shift register, 32 latches, and control logic to perform blanking and polarity control of the outputs. HV_{OUT1} is connected to the first stage of the shift register. Data is shifted through the shift register on the logic rising transition of the clock. A DIR pin causes data shifting clockwise when grounded and counterclockwise when connected to V_{DD} . A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register. Operation of the shift register is not affected by the LE (latch enable), BL (blank) or the POL (polarity) inputs. Transfer of data from the shift register to the latch occurs when the LE (latch enable) input is high. The data in the latch is stored after LE transitions from high to low.

Absolute Maximum Ratings[1]

Supply voltage, V_{DD}[2]	-0.5V to +7.0V
Output voltage, V_{PP}[2]	-0.5V to +70V
Logic input levels[2]	-0.5V to V_{DD} + 0.5V
Ground current[3]	1.5A
Continuous total power dissipation[4]	1200mW
Operating temperature range	-40°C to +85°C
Storage temperature range	-65°C to +125°C
Lead temperature 1.6mm (1/16 inch) from case for 10 seconds	260°C

Notes:

1. Device will survive (but operation may not be specified or guaranteed) at these extremes.
2. All voltages are referenced to V_{SS}.
3. Duty cycle is limited by the total power dissipated in the package.
4. For operation above 25°C ambient derate linearly to 85°C at 20mW/°C.

09/30/02

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Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics (V_{DD} = 5V, V_{PP} = 60V, V_{SS} = GND)

Symbol	Parameter		Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current			15	mA	$V_{DD} = V_{DD}$ max f_{CLK} = 5MHz
I_{PPQ}	High voltage supply current			0.5	mA	Outputs high
				0.5	mA	Outputs low
I_{DDQ}	Quiescent V_{DD} supply current			0.5	mA	All $V_{IN} = V_{SS}$ or V_{DD}
V_{OH}	High-level output	Q	50		V	I_O= -5mA, V_{PP} = 60V
		Data out	4.6		V	I_O= -100μA
V_{OL}	Low-level output	Q		8	V	I_O= 5mA, V_{PP} = 60V
		Data out		0.4	V	I_O= 100μA
I_{IH}	High-level logic input current			1	μA	$V_{IH} = V_{DD}$
I_{IL}	Low-level logic input current			-1	μA	V_{IL} = 0V
V_{OLBP}	Low-level output voltage, backplane			3	V	I_O = 10mA
V_{OHBP}	High-level output voltage, backplane		29		V	I_O = -10mA

AC Characteristics (V_{DD} = 5V, V_{PP} = 60V, T_C = 25°C), logic input rises/fall time = 10ns.

Symbol	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency		5	MHz	
t_W	Clock width high or low	100		ns	
t_{SU}	Data set-up time before clock rises	25		ns	
t_H	Data hold time after clock rises	50		ns	
t_{ON}, t_{OFF}	Time from latch enable or POL to HV_{OUT}		500	ns	C_L = 20pF
t_{ON}, t_{OFF}	Time from POL to BP output		500	ns	C_L = 20pF
t_{DHL}	Delay time clock to data high to low		200	ns	C_L = 10pF
t_{DLH}	Delay time clock to data low to high		200	ns	C_L = 10pF
t_{DLE}	Delay time clock to LE low to high	50		ns	
t_{WLE}	Width of LE pulse	100		ns	
t_{SLE}	LE set-up time before clock rises	50		ns	
t_{BR}, t_{BF}	BP_{OUT} rise/fall time	10	1000	μs	C_L = 350nF
$\lvert t_{BR} - t_{BF} \rvert$	BP_{OUT} rise and fall difference		100	μs	C_L = 350nF

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{DD}	Logic supply voltage	4.5	5.5	V
V_{PP}	Output voltage*	0	60	V
V_{IH}	High-level input voltage	2.4	V_{DD}	V
V_{IL}	Low-level input voltage	0	0.8	V
f_{CLK}	Clock frequency	0	5	MHz
T_A	Operating free-air temperature	-40	+85	°C
I_{OD}	Allowable current through output diodes		200	mA

Notes:

*Output will not switch below 12V.

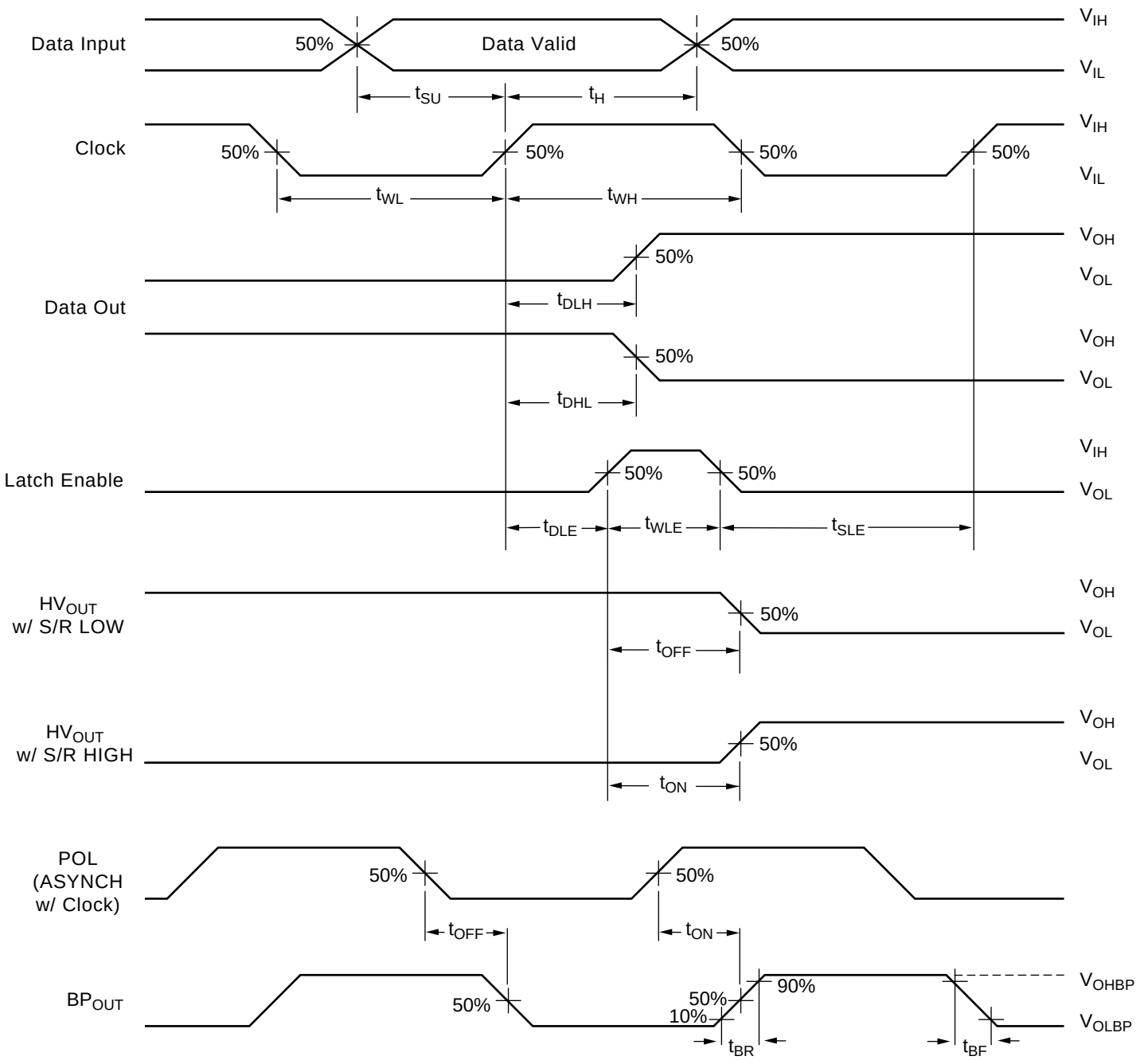
Power-up sequence should be the following:

1. Connect ground.
2. Apply V_{DD}.
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply V_{PP}.

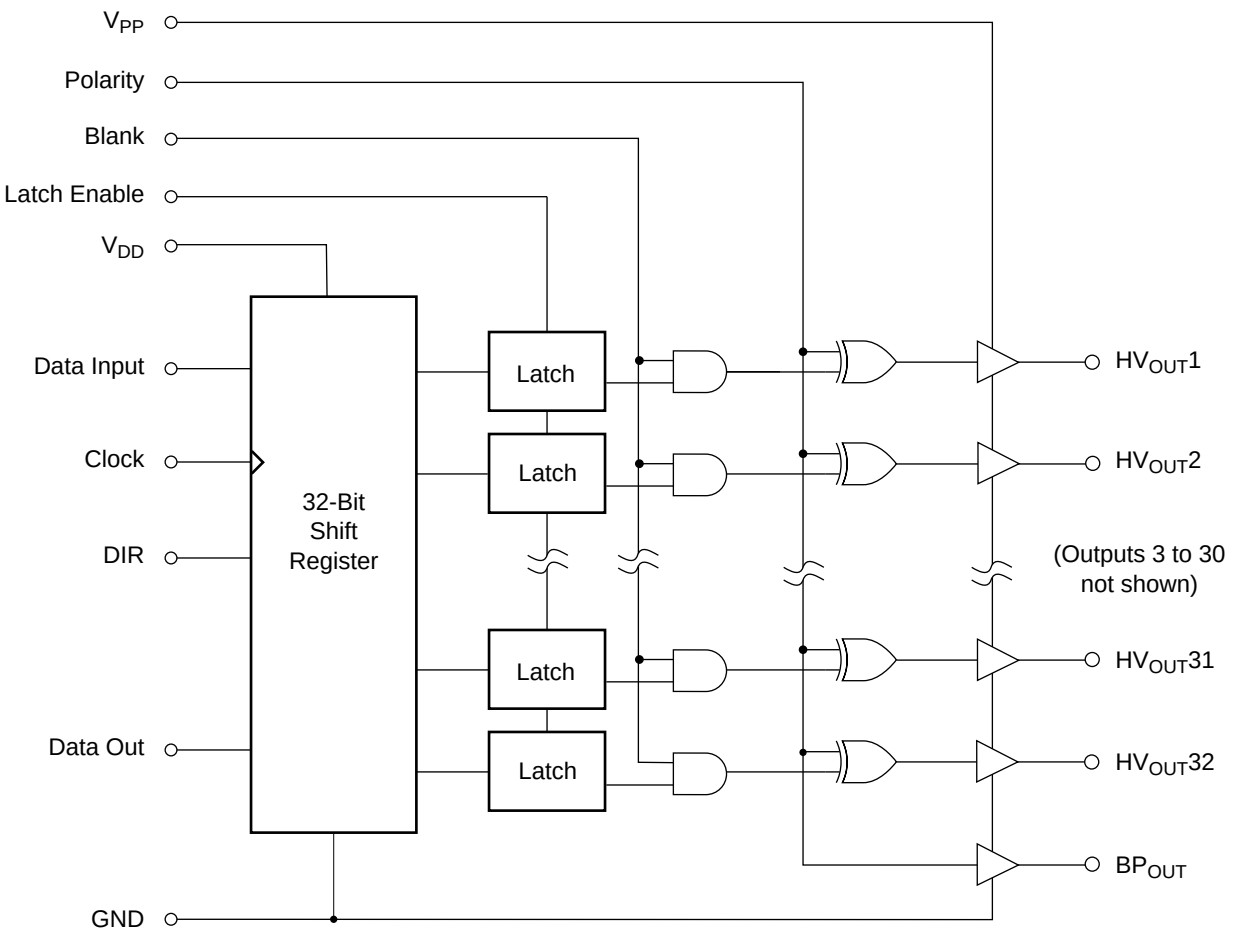
Power-down sequence should be the reverse of the above.

The V_{PP} should not drop below V_{DD} during operation.

Switching Waveforms



Functional Block Diagram



Function Table

Function	Inputs						Outputs					
	Data	CLK	LE	BL	POL	DIR	Shift Reg 1	Shift Reg 2…32	HV Outputs 1	HV Outputs 2…32	Data Out 2…32	BP_{OUT} *
Load S/R	H or L	↑	L	H	H	X	H or L	*…*	$\overline{*}$	$\overline{*…*}$	*	H
Load latches	X	H or L	L	H	H	X	*	*…*	$\overline{*}$	$\overline{*…*}$	*	H
	X	H or L	L	H	L	X	*	*…*	*	*…*	*	L
Transparent Mode	L	↑	H	H	H	X	L	*…*	H	*…*	*	H
	H	↑	H	H	H	X	H	*…*	L	*…*	*	H
	L	↑	H	H	L	X	L	*…*	L	*…*	*	L
	H	↑	H	H	L	X	H	*…*	H	*…*	*	L
R/L Shift	X	↑	X	H	X	H	Qn → Qn+1		*	*…*	Q32	
	X	↑	X	H	X	L	Qn → Qn-1		*	*…*	Q1	
Blank	X	X	X	L	L	X	*	*…*	L	L…L	*	L
Control	X	X	X	L	H	X	*	*…*	H	H…H	*	H

Notes:
H = high level, L = low level, X = irrelevant, ↑ = low-to-high transition.
* = dependent on previous stage's state before the last CLK or last LE high.

Pin Configuration

HV66
44 Pin Plastic Gullwing (QFP) Package

Pin	Function	Pin	Function
1	HV_{OUT}22/11	23	Data Out
2	HV_{OUT}21/12	24	GND
3	HV_{OUT}20/13	25	N/C
4	HV_{OUT}19/14	26	BL
5	HV_{OUT}18/15	27	POL
6	HV_{OUT}17/16	28	LE
7	HV_{OUT}16/17	29	V_{DD}
8	HV_{OUT}15/18	30	Clock
9	HV_{OUT}14/19	31	DIR
10	HV_{OUT}13/20	32	Data In
11	HV_{OUT}12/21	33	V_{PP}
12	HV_{OUT}11/22	34	BP Out
13	HV_{OUT}10/23	35	HV_{OUT}32/1
14	HV_{OUT}9/24	36	HV_{OUT}31/2
15	HV_{OUT}8/25	37	HV_{OUT}30/3
16	HV_{OUT}7/26	38	HV_{OUT}29/4
17	HV_{OUT}6/27	39	HV_{OUT}28/5
18	HV_{OUT}5/28	40	HV_{OUT}27/6
19	HV_{OUT}4/29	41	HV_{OUT}26/7
20	HV_{OUT}3/30	42	HV_{OUT}25/8
21	HV_{OUT}2/31	43	HV_{OUT}24/9
22	HV_{OUT}1/32	44	HV_{OUT}23/10

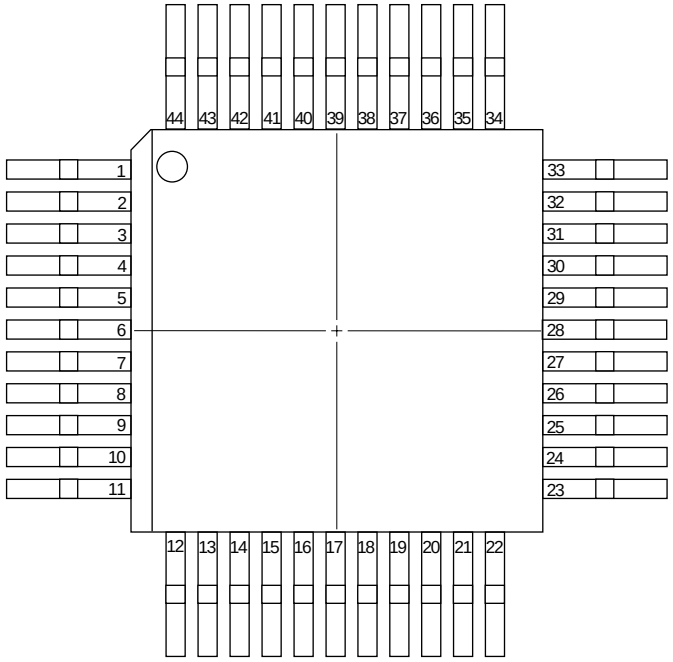
Note:

Pin designation for DIR = L/H

Example: for DIR = L, Pin 1 is HV_{OUT} 22

for DIR = H, Pin 1 is HV_{OUT} 11

Package Outline



top view
44-pin PQFP Package

Pin Configuration

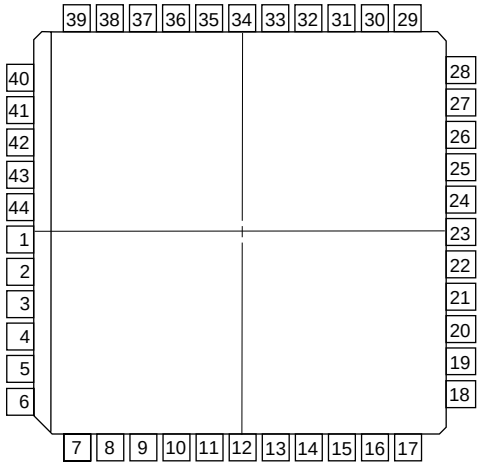
HV66
44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HV_{OUT} 17/16	23	LE
2	HV_{OUT} 16/17	24	V_{DD}
3	HV_{OUT} 15/18	25	Clock
4	HV_{OUT} 14/19	26	DIR
5	HV_{OUT} 13/20	27	Data In
6	HV_{OUT} 12/21	28	V_{PP}
7	HV_{OUT} 11/22	29	BP Out
8	HV_{OUT} 10/23	30	HV_{OUT} 32/1
9	HV_{OUT} 9/24	31	HV_{OUT} 31/2
10	HV_{OUT} 8/25	32	HV_{OUT} 30/3
11	HV_{OUT} 7/26	33	HV_{OUT} 29/4
12	HV_{OUT} 6/27	34	HV_{OUT} 28/5
13	HV_{OUT} 5/28	35	HV_{OUT} 27/6
14	HV_{OUT} 4/29	36	HV_{OUT} 26/7
15	HV_{OUT} 3/30	37	HV_{OUT} 25/8
16	HV_{OUT} 2/31	38	HV_{OUT} 24/9
17	HV_{OUT} 1/32	39	HV_{OUT} 23/10
18	Data Out	40	HV_{OUT} 22/11
19	GND	41	HV_{OUT} 21/12
20	N/C	42	HV_{OUT} 20/13
21	BL	43	HV_{OUT} 19/14
22	POL	44	HV_{OUT} 18/15

Note:

1. Pin designation for DIR = L/H
   Example: for DIR = L, Pin 1 = HV_{OUT} 17
   for DIR = H, Pin 1 = HV_{OUT} 16

Package Outline



top view
44-pin PLCC

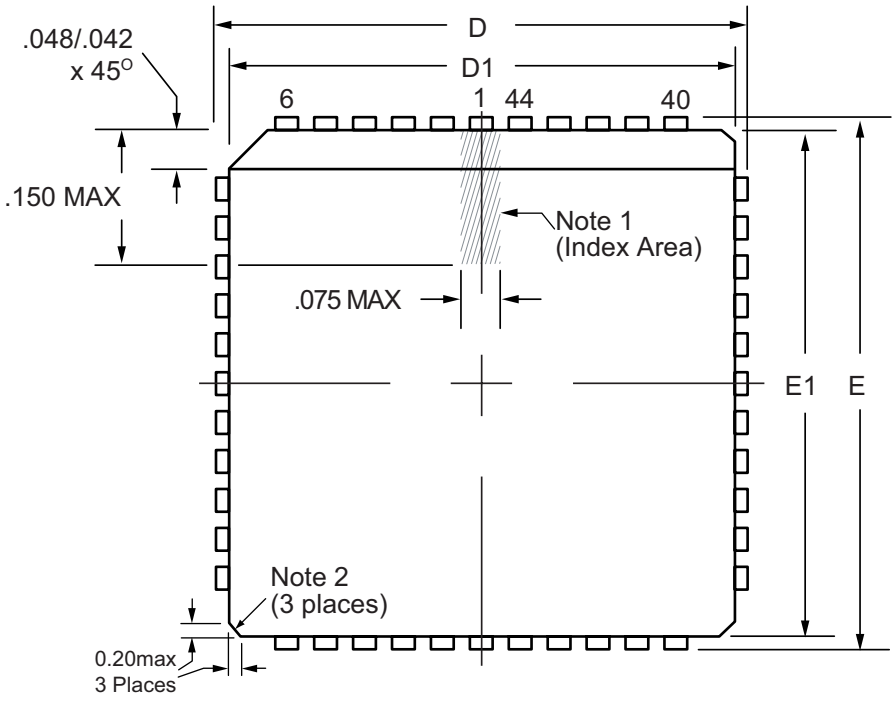
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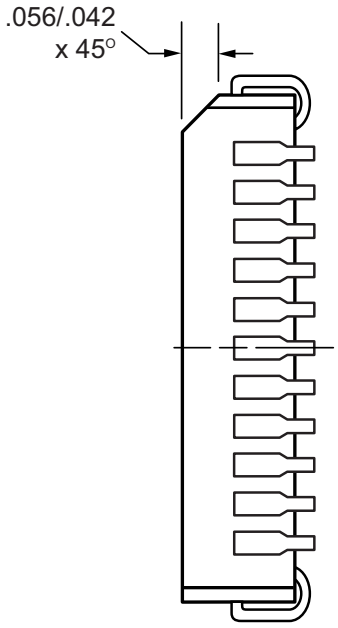
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44-Lead PLCC Package Outline (PJ)

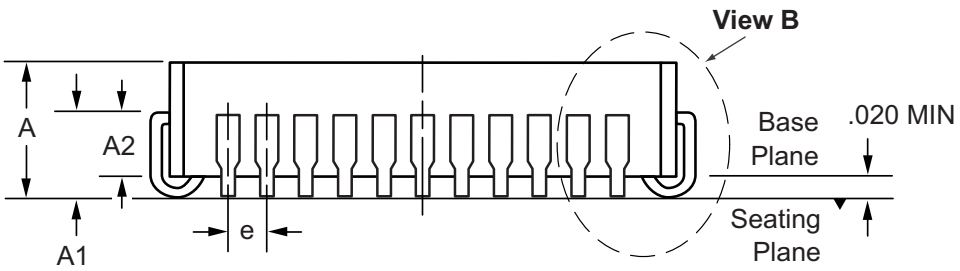
.653x.653in body, .180in height (max.), .050in pitch



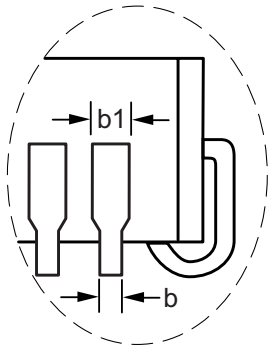
Top View



Side View



Side View



View B

Note:

1. A Pin 1 identifier must be located in the index area indicated.The Pin 1 identifier may be either a mold, or an embedded metal or marked feature.

2. Exact shape of this feature is optional.

Symbol		A	A1	A2	b	b1	D	D1	E	E1	e
Dimension (inches)	MIN	.165	.090	.062	.013	.026	.685	.650	.685	.650	.050 BSC
	NOM	.172	.105	-	-	-	.690	.653	.690	.653	
	MAX	.180	.120	.083	.021	.036	.695	.656	.695	.656	

JEDEC Registration MS-018, Variation AC, Issue A, June, 1993.

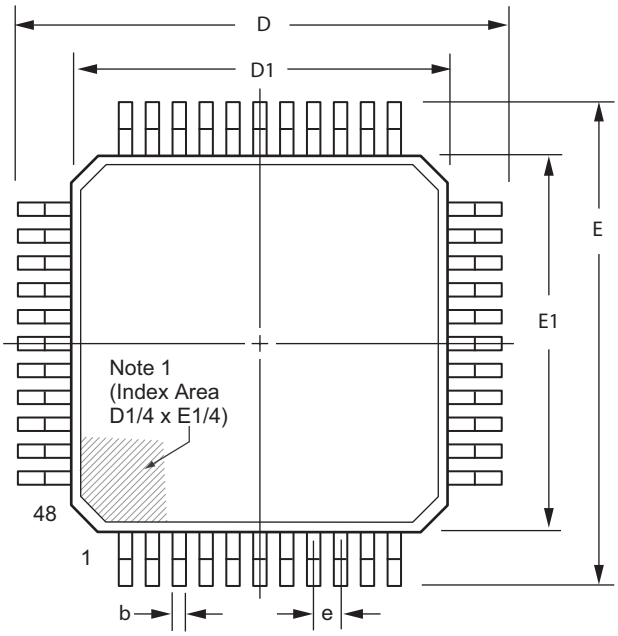
Drawings are not to scale.

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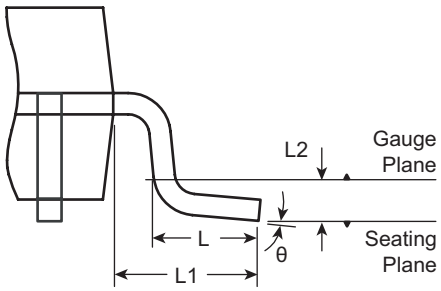
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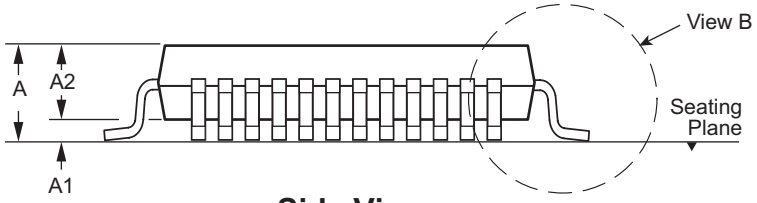
44-Lead PQFP Package Outline (PG)



Top View



View B



Side View

Note 1:
A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier may be either a mold, or an embedded metal or marked feature.

Symbol		A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	θ	θ1
Dimension (mm)	MIN	-	0.25	1.95	0.30	13.65	9.80	13.65	9.80	0.80 BSC	0.73	1.95 REF	0.25 BSC	3.5°	5°
	NOM	-	-	2.00	-	13.90	10.00	13.90	10.00		0.88			-	-
	MAX	2.45	-	2.10	0.45	14.15	10.20	14.15	10.20		1.03			7°	16°

JEDEC Registration M0-112, Variation AA-2, Issue B, Sep.1995.

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