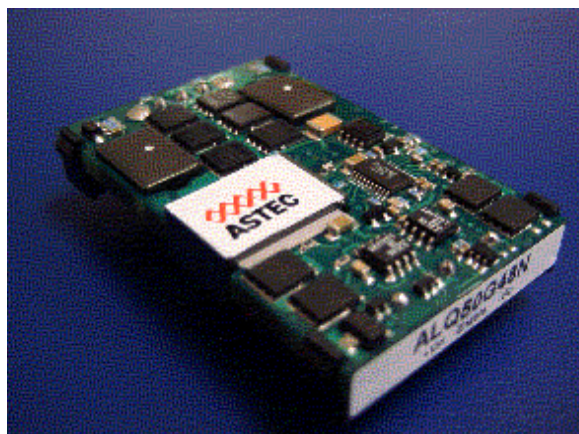


50 Amps

ALQ50

High Efficiency Quarter Brick



Total Power: 132W
Input Voltages: 48V
No. of Outputs: Single

Electrical Specs

Input

Input Range 36 to 75 VDC
Input Surge 100V /100ms
Efficiency 3.3V @ 91% (typical)

Output

Line / Load Regulation < 0.3% Vo (typical)
Output Current up to 50A max
(3.3V at 40A max)
Noise/Ripple¹ 40mV_{PK-PK} (typical)
Remote sense Up to 10% of Vo
Transient Response 100mV (typ) deviation
50% to 75% Load change
250μs (typ) recovery
Overvoltage Protection 130% typ for Vo < 3.3V
125% typ for 3.3V
Over Current Protection 120% Iout typ (autorecovery)
Over Temperature Protection 115C average PCB temperature
(autorecovery)
Switching Frequency 480kHz
540kHz (2.5V output)
Isolation Voltage 1500Vdc

Control

Voltage Voltage Trim ±10% V_{O,NOM}
Enable Postive or Negative Logic options

Special Features

- Industry standard Quarter Brick package 1.48" x 2.30" x 0.38"
- Openframe low profile construction
- High capacitive load start-up
- Regulation to zero load
- Fixed frequency switching for EMI predictability
- Industry Standard Features: Input UVLO with hysteresis, Enable, OCP, OCP, OTP, Output Voltage Trim, Differential Remote Sense
- Meets Basic Insulation

Environmental

Operating Ambient Temperature: -40°C to +85°C
Storage Temperature: -40°C to +125°C
MTBF: > 1 million hours

Safety

UL, cUL 60950
TUV EN60950

AMERICAS

5810 Van Allen Way
Carlsbad, CA 92008
Telephone: 760-930-4600
Facsimile: 760-930-0698

EUROPE

Astec House, Waterfront Business Park
Merry Hill, Dudley
West Midlands, DY5 1LX, UK
Telephone: 44 (1384) 842-211
Facsimile: 44 (1384) 843-355

ASIA

Units 2111-2116, Level 21
Tower1, Metroplaza
223, Hing Fong Road
Fwai Fong, New Territories
Hong Kong
Telephone: 852-2437-9662
Facsimile: 852-2402-4426



Ordering Information

Input Voltage	Output Voltage	Output Current	Efficiency ²	Model Number
36V to 75V	3.3V	40A	91% Typ	ALQ40F48 (N)
36V to 75V	2.5V	50A	90% Typ	ALQ50G48(N)
36V to 75V	1.8V	50A	89% Typ	ALQ50Y48 (N)
36V to 75V	1.2V	50A	86% Typ	ALQ50K48 (N)

OPTIONS:

(N) : "N" = designates Negative Logic Enable (default is Positive Enable with no suffix "N" required)

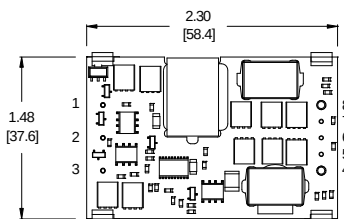
Pin Assignments

Single Output

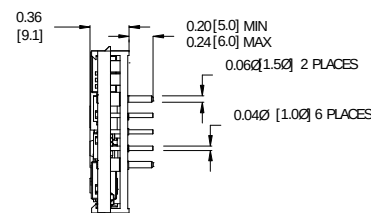
1. +Vin
2. Enable (On/Off)
3. -Vin
4. -Vout
5. -Sense
6. Trim
7. +Sense
8. +Vout

Notes:

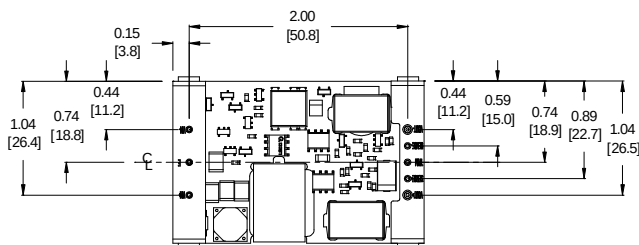
1. 20 MHz bandwidth. External 10 uF tant. capacitor in parallel with 1 uF ceramic capacitor placed across the output and secondary return ground.
2. Efficiency measurements are typical values taken at full load, nominal line and $T_A = 25^\circ\text{C}$.
3. All specifications are typical at nominal line, full load and $T_A = 25^\circ\text{C}$ unless otherwise noted.
4. All specifications subject to change without notice.
5. Mechanical drawings are for reference only. Dimensions are in inches [millimeters]. Pin placement tolerance ± 0.005 [0.127]. Mechanical Tolerance ± 0.02 [0.5]. $\varnothing = 0.060$ " for Pins 4&8, the rest are $\varnothing = 0.40$ ".
6. Technical Reference Notes should be consulted for detailed information when available.
7. Warranty 1yr.



PIN SIDE DOWN



SIDE VIEW



PIN SIDE UP

Astec reserves the right to make changes to the information contained herein without notice and assumes no liability as a result of its use and application. (REV 07: OCTOBER 19, 2004)

ALQ50

Astec Industry Standard