

Power Management ICs for Li-Ion Powered Systems

FEATURES

- **1.6A, 1.0A or 0.8A, 97% Efficient Step-Down Converter for System Voltage (VDCDC1)**
  - **3.3V or 2.80V or Adjustable**
- **1.6A, 1.0A or 0.8A, up to 95% Efficient Step-Down Converter for Memory Voltage (VDCDC2)**
  - **1.8V or 2.5V or Adjustable**
- **0.8A, 90% Efficient Step-Down Converter for Processor Core (VDCDC3)**
- **Two Selectable Voltages for VDCDC3**
  - **TPS650240:**
    - **DEFDCDC3= LOW: V_O = 1.0V**
    - **DEFDCDC3= HIGH: V_O = 1.3V**
  - **TPS650241:**
    - **DEFDCDC3= LOW: V_O = 0.9V**
    - **DEFDCDC3= HIGH: V_O= 1.375V**
  - **TPS650242:**
    - **DEFDCDC3= LOW: V_O = 1.0V**
    - **DEFDCDC3= HIGH: V_O = 1.5V**
  - **TPS650243:**
    - **DEFDCDC3= LOW: V_O = 1.0V**
    - **DEFDCDC3= HIGH: V_O = 1.2V**
  - **TPS650244:**
    - **DEFDCDC3= LOW: V_O = 1.55V**
    - **DEFDCDC3= HIGH: V_O = 1.6V**
  - **TPS650245:**
    - **DEFDCDC3= LOW: V_O = 0.9V**
    - **DEFDCDC3= HIGH: V_O = 1.1V**
- **30mA LDO for Vdd_alive**
- **2 × 200mA General Purpose LDOs (LDO1 and LDO2)**
- **Dynamic Voltage Management for Processor Core**
- **LDO1 and LDO2 Voltage Externally Adjustable**
- **Separate Enable Pins for Inductive Converters**
- **2.25MHz Switching Frequency**
- **85μA Quiescent Current**
- **Thermal Shutdown Protection**

APPLICATIONS

- **PDA**
- **Cellular/Smart Phone**
- **GPS**
- **Digital Still Camera**
- **Split Supply DSP and μP Solutions:, Samsung ARM-Based Processors, etc.**

DESCRIPTION

The TPS65024x are integrated Power Management ICs for applications powered by one Li-Ion or Li-Polymer cell, which require multiple power rails. The TPS65024x provide three highly efficient, step-down converters targeted at providing the core voltage, peripheral, I/O and memory rails in a processor based system. All three step-down converters enter a low power mode at light load for maximum efficiency across the widest possible range of load currents. The converters can be forced into fixed frequency PWM mode by pulling the MODE pin high. The TPS65024x also integrate two general purpose 200mA LDO voltage regulators, which are enabled with an external input pin. Each LDO operates with an input voltage range between 1.5V and 6.5V allowing them to be supplied from one of the step-down converters or directly from the battery. The output voltage of the LDOs can be set with an external resistor divider for maximum flexibility. Additionally there is a 30mA LDO typically used to provide power in a processor based system to a voltage rail that is always on. TPS65024x provide voltage scaling on DCDC3 using the DEFDCDC3 pin. This pin either needs to be connected to a logic HIGH or logic LOW level to set the output voltage of DCDC3. TPS65024x come in a small 5mm x 5mm 32 pin QFN package (RHB).



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_A	VOLTAGE AT DCDC3	OUTPUT CURRENT ON DCDC1 / DCDC2 / DCDC3	VOLTAGE AT VDD_ALIVE	PACKAGE	PART NUMBER(2)
–40°C to 85°C	1.0V / 1.3V	1.0A / 0.8A / 0.8A	1.2V	32 Pin QFN (RHB)	TPS650240RHB
	0.9V / 1.375V	1.6A / 1.0A / 0.8A	1.2V		TPS650241RHB
	1.0V / 1.5V	1.0A / 0.8A / 0.8A	1.2V		TPS650242RHB
	1.0V / 1.2V	1.6A / 1.0A / 0.8A	1.2V		TPS650243RHB
	1.55V / 1.6V	0.8A / 1.6A / 0.8A	1.2V		TPS650244RHB
	0.9V / 1.1V	1.0A / 0.8A / 0.8A	1.1V		TPS650245RHB

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) The RHB package is available in tape and reel. Add R suffix (TPS650240RHBR) to order quantities of 3000 parts per reel. Add T suffix (TPS650240RHBT) to order quantities of 250 parts per reel.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE	UNIT
	Input voltage range on all pins except A/PGND pins with respect to AGND	–0.3 to 7	V
	Current at VINDCDC1, L1, PGND1, VINDCDC2, L2, PGND2, VINDCDC3, L3, PGND3	2000	mA
	Peak current at all other pins	1000	mA
	Continuous total power dissipation	See Dissipation Rating Table	
T_A	Operating free-air temperature	–40 to 85	°C
T_J	Maximum junction temperature	125	°C
T_{st}	Storage temperature	–65 to 150	°C
	Lead temperature 1,6 mm (1/16-inch) from case for 10 seconds	260	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS

PACKAGE(1)	$R_{\theta JA}$	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
RHB	35K/W	2.85W	28mW/K	1.57W	1.14W

(1) The thermal resistance junction to ambient of the RHB package is measured on a high K board. The thermal resistance junction to power pad is 1.5k/W.

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RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
$V_{INDCDC1}$, $V_{INDCDC2}$, $V_{INDCDC3}$, V_{CC}	Input voltage range step-down converters	2.5		6.0	V
V_{DCDC1}	Output voltage range for VDCDC1 step-down converter(1)	0.6		$V_{INDCDC1}$	V
V_{DCDC2}	Output voltage range for mem step-down converter(1)	0.6		$V_{INDCDC2}$	V
V_{DCDC3}	Output voltage range for core step-down converter	0.9		1.5	V
V_{INLDO1}, V_{INLDO2}	Input voltage range for LDOs	1.5		6.5	V
V_{LDO1-2}	Output voltage range for LDOs	1.0		$V_{INLDO1-2}$	V
$I_{OUTDCDC1}$	Output current at L1			1600	mA
L1	Inductor at L1(2)	1.5	2.2		µH
$C_{INDCDC1}$	Input capacitor at $V_{INDCDC1}$(2)	10			µF
$C_{OUTDCDC1}$	Output capacitor at V_{DCDC1}(2)	10	22		µF
$I_{OUTDCDC2}$	Output current at L2			1600	mA
L2	Inductor at L2(2)	1.5	2.2		µH
$C_{INDCDC2}$	Input capacitor at $V_{INDCDC2}$ (2)	10			µF
$C_{OUTDCDC2}$	Output capacitor at V_{DCDC2} (2)	10	22		µF
$I_{OUTDCDC3}$	Output current at L3			800	mA
L3	Inductor at L3(2)	1.5	2.2		µH
$C_{INDCDC3}$	Input capacitor at $V_{INDCDC3}$(2)	10			µF
$C_{OUTDCDC3}$	Output capacitor at V_{DCDC3} (2)	10	22		µF
C_{VCC}	Input capacitor at VCC(2)	1			µF
C_{in1-2}	Input capacitor at VINLDO(2)	1			µF
C_{OUT1-2}	Output capacitor at VLDO1, VLDO2(2)	2.2			µF
$I_{LDO1,2}$	Output current at VLDO1, VLDO2			200	mA
C_{VRTC}	Output capacitor at Vdd_alive(2)	2.2			µF
I_{Vdd_alive}	Output current at Vdd_alive			30	mA
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C
R_{CC}	Resistor from VINDCDC3,VINDCDC2, VINDCDC1 to Vcc used for filtering(3)		1	10	Ω

(1) When using an external resistor divider at DEFDCDC2, DEFDCDC1.
(2) See applications section for more information, for Vout > 2.85V choose 3.3µH inductor.
(3) Up to 2.5mA can flow into Vcc when all 3 converters are running in PWM, this resistor will cause the UVLO threshold to be shifted accordingly.

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ELECTRICAL CHARACTERISTICS

VINDCDC1 = VINDCDC2 = VINDCDC3 = VCC = VINLDO = 3.6V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

COMTROL SIGNALS: EN_DCDC1, EN_DCDC2, EN_DCDC3, EN_LDO, MODE, EN_VDD_ALIVE							
PARAMETER		**TEST CONDITIONS**		**MIN**	**TYP**	**MAX**	**UNIT**
V_{IH}	High level input voltage			1.45		VCC	V
V_{IL}	Low level input voltage			0		0.4	V
I_H	Input bias current				0.01	0.1	µA
SUPPLY PINS: VCC, VINDCDC1, VINDCDC2, VINDCDC3							
$I_{(qPFM)}$	Operating quiescent current	PFM All 3 DCDC converters enabled, zero load and no switching, LDOs enabled	Vcc = 3.6V		135	170	uA
		PFM All 3 DCDC converters enabled, zero load and no switching, LDO1, LDO2 = OFF, Vdd_alive = ON			75	100	
		PFM DCDC1 and DCDC2 converters enabled, zero load and no switching, LDO1, LDO2 = OFF, Vdd_alive = ON			55	80	
		PFM DCDC1 converter enabled, zero load and no switching, LDO1, LDO2 = OFF, Vdd_alive = ON			40	60	
$I_{VCC(PWM)}$	Current into Vcc; PWM	All 3 DCDC converters enabled & running in PWM, LDOs off	Vcc = 3.6V		2		mA
		PWM DCDC1 and DCDC2 converters enabled and running in PWM, LDOs off			1.5	2.5	
		PWM DCDC1 converter enabled and running in PWM, LDOs off			0.85	2.0	
I_q	Quiescent current	All converters disabled, LDO1, LDO2 = OFF, Vdd_alive = OFF	Vcc = 3.6V		16		µA
		All converters disabled, LDO1, LDO2 = OFF, Vdd_alive = ON			26		

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ELECTRICAL CHARACTERISTICS

VINDCDC1 = VINDCDC2 = VINDCDC3 = VCC = VINLDO = 3.6V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDCDC1 STEP-DOWN CONVERTER							
$V_{VINDCDC1}$	Input voltage range			2.5		6.0	V
I_O	Maximum output current for TPS650240, TPS650242 and TPS650245		V_O = 3.3V	1000			mA
I_O	Maximum output current for TPS650241 and TPS650243		V_O = 3.3V	1600			mA
I_O	Maximum output current for TPS650244		V_O = 3.3V	800			mA
I_{SD}	Shutdown supply current in VINDCDC1		EN_DCDC1 = GND		0.1	1	µA
$R_{DS(ON)}$	P-channel MOSFET on-resistance		VINDCDC1 = VGS = 3.6V		125	261	mΩ
I_{LP}	P-channel leakage current		VINDCDC1 = 6.0V			2	µA
$R_{DS(ON)}$	N-channel MOSFET on-resistance		VINDCDC1 = VGS = 3.6V		130	260	mΩ
I_{LN}	N-channel leakage current		V_{DS} = 6.0V		7	10	µA
I_{LIMF}	Forward current limit (P- and N-channel) for TPS650244		2.5V < V_{INMAIN} < 6.0V	0.98	1.10	1.21	A
I_{LIMF}	Forward current limit (P- and N-channel) for TPS650240, TPS650242 and TPS650245		2.5V < V_{INMAIN} < 6.0V	1.15	1.30	1.39	A
I_{LIMF}	Forward current limit (P- and N-channel) for TPS650241 and TPS650243		2.5V < V_{INMAIN} < 6.0V	1.75	1.97	2.15	A
f_S	Oscillator frequency			1.95	2.25	2.55	MHz
VDCDC1	Fixed output voltage MODE=0 (PWM/PFM)	2.80V	VINDCDC1 = 3.3V to 6.0V; 0 mA ≤ I_O ≤ 1.6A	–2%		2%	
		3.3V		–2%		2%	
	Fixed output voltage MODE=1 (PWM)	2.80V	VINDCDC1 = 3.7V to 6.0V; 0 mA ≤ I_O ≤ 1.6A	–1%		1%	
		3.3V		–1%		1%	
	Adjustable output voltage with resistor divider at DEFDCDC1 MODE = 0 (PWM/PFM)		VINDCDC1 = VDCDC1 +0.4V (min 2.5V) to 6.0V; 0mA ≤ I_O ≤ 1.6A	–2%		2%	
	Adjustable output voltage with resistor divider at DEFDCDC1; MODE = 1 (PWM)		VINDCDC1 = VDCDC1 +0.4V (min 2.5V) to 6.0V; 0mA ≤ I_O ≤ 1.6A	–1%		1%	
	Line regulation		VINDCDC1 = VDCDC1 + 0.3V (min. 2.5 V) to 6.0V; I_O = 10mA		0.0		%/V
	Load regulation		I_O = 10mA to 1.6A		0.25		%/A
T_{SS}	Soft start ramp time		VDCDC1 ramping from 5% to 95% of target value		750		µs
R(L1)	Internal resistance from L1 to GND				1		MΩ

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ELECTRICAL CHARACTERISTICS

VINDCDC1 = VINDCDC2 = VINDCDC3 = VCC = VINLDO = 3.6V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDCDC2 STEP-DOWN CONVERTER							
$V_{VINDCDC2}$	Input voltage range			2.5		6.0	V
I_O	Maximum output current for TPS650240, TPS650242 and TPS650245		V_O = 2.5V	800			mA
I_O	Maximum output current for TPS650241 and TPS650243		V_O = 2.5V	1000			mA
I_O	Maximum output current for TPS650244		V_O = 2.5V	1600			mA
I_{SD}	Shutdown supply current in VINDCDC2		EN_DCDC2 = GND		0.1	1	µA
$R_{DS(ON)}$	P-channel MOSFET on-resistance		VINDCDC2 = V_{GS} = 3.6V		140	300	mΩ
I_{LP}	P-channel leakage current		VINDCDC2 = 6.0V			2	µA
$R_{DS(ON)}$	N-channel MOSFET on-resistance		VINDCDC2 = VGS = 3.6V		150	297	mΩ
I_{LN}	N-channel leakage current		V_{DS} = 6.0V		7	10	µA
I_{LIMF}	Forward current limit (P- and N-channel) for TPS650240, TPS650242 and TPS650245		2.5V < VINDCDC2 < 6.0V	1.05	1.16	1.29	A
I_{LIMF}	Forward current limit (P- and N-channel) for TPS650241 and TPS650243		2.5V < VINDCDC2 < 6.0V	1.22	1.35	1.50	A
I_{LIMF}	Forward current limit (P- and N-channel) for TPS650244		2.5V < VINDCDC2 < 6.0V	1.75	1.97	2.15	A
f_S	Oscillator frequency			1.95	2.25	2.55	MHz
VDCDC2	Fixed output voltage MODE = 0 (PWM/PFM)	1.8V	VINDCDC2 = 2.5V to 6.0V; 0 mA ≤ I_O ≤ 1.6A	–2%		2%	
		2.5V	VINDCDC2 = 3.0V to 6.0V; 0 mA ≤ I_O ≤ 1.6A	–2%		2%	
	Fixed output voltage MODE = 1 (PWM)	1.8V	VINDCDC2 = 2.5V to 6.0V; 0 mA ≤ I_O ≤ 1.6A	–2%		2%	
		2.5V	VINDCDC2 = 3.0V to 6.0V; 0 mA ≤ I_O ≤ 1.6A	–1%		1%	
	Adjustable output voltage with resistor divider at DEFDCDC2 MODE = 0 (PWM)		VINDCDC2 = VDCDC2 + 0.5V (min 2.5V) to 6.0V; 0mA ≤ I_O ≤ 1.6A	–2%		2%	
	Adjustable output voltage with resistor divider at DEFDCDC2; MODE = 1 (PWM)		VINDCDC2 = VDCDC2 + 0.5V (min 2.5V) to 6.0V; 0mA ≤ I_O ≤ 1.6A	–1%		1%	
	Line regulation		VINDCDC2 = VDCDC2 + 0.3 V (min. 2.5 V) to 6.0V; I_O = 10mA		0.0		%/V
	Load regulation		I_O = 10mA to 1.6A		0.25		%/A
T_{SS}	Soft start ramp time		VDCDC2 ramping from 5% to 95% of target value		750		µs
R(L2)	Internal resistance from L2 to GND				1		MΩ

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ELECTRICAL CHARACTERISTICS

VINDCDC1 = VINDCDC2 = VINDCDC3 = VCC = VINLDO = 3.6V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDCDC3 STEP-DOWN CONVERTER							
$V_{VINDCDC3}$	Input voltage range			2.5		6.0	V
I_O	Maximum output current		V_O = 1.6V	800			mA
I_{SD}	Shutdown supply current in VINDCDC3		EN_DCDC3 = GND		0.1	1	µA
$R_{DS(ON)}$	P-channel MOSFET on-resistance		$V_{INDCDC3}$ = V_{GS} = 3.6V		310	698	mΩ
I_{LP}	P-channel leakage current		VINDCDC3 = 6.0V		0.1	2	µA
$R_{DS(ON)}$	N-channel MOSFET on-resistance		$V_{INDCDC3}$ = V_{GS} = 3.6V		220	503	mΩ
I_{LN}	N-channel leakage current		V_{DS} = 6.0V		7	10	µA
I_{LIMF}	Forward current limit (P- and N-channel)		2.5V < $V_{INDCDC3}$ < 6.0V	1.00	1.20	1.40	A
f_S	Oscillator frequency			1.95	2.25	2.55	MHz
VDCDC3	Fixed output voltage MODE = 0 (PWM/PFM)	V_O = 0.9V to 1.6V	VINDCDC3 = 2.5V to 6.0V; 0mA ≤ I_O ≤ 800mA	–2%		2%	
	Fixed output voltage MODE = 1 (PWM)			–1%		1%	
	Line regulation		VINDCDC3 = VDCDC3 + 0.3V (min. 2.5 V) to 6.0V; I_O = 10mA		0.0		%/V
	Load regulation		I_O = 10mA to 600mA		0.25		%/A
T_{SS}	Soft start ramp time		VDCDC3 ramping from 5% to 95% of target value		750		µs
R(L3)	Internal resistance from L3 to GND				1		MΩ

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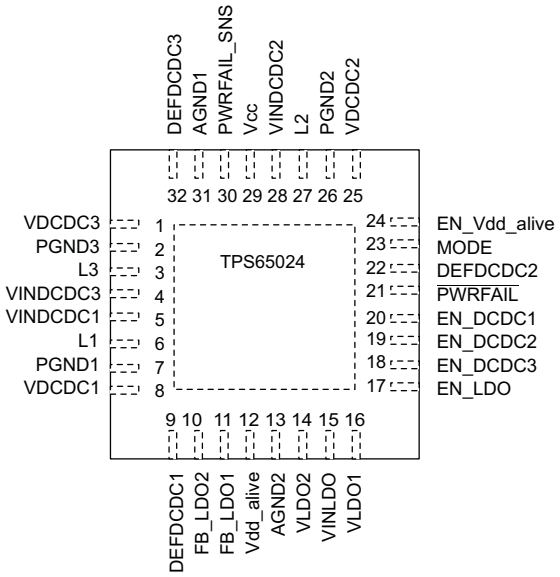
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VLDO1 and VLDO2 Low Dropout Regulators						
I(q)	Operating quiescent current	Current per LDO into VINLDO		16	30	µA
I(SD)	Shutdown current	Total current into VINLDO, VLDO = 0V		0.6	2	µA
V_{INLDO}	Input voltage range for LDO1, LDO2		1.5		6.5	V
V_{LDO1}	LDO1 output voltage range		1.0		VinLDO	V
V_{LDO2}	LDO2 output voltage range		1.0		VinLDO	V
VFB	LDO1 and LDO2 feedback voltage	See (1)		1.0		V
I_O	Maximum output current for LDO1, LDO2	Vin = 1.8V, Vo = 1.3V	200			mA
I_O	Maximum output current for LDO1, LDO2	Vin = 1.5V; Vo = 1.3V		120		mA
I_{SC}	LDO1 & LDO2 short circuit current limit	V_{LDO1} = GND, V_{LDO2} = GND			400	mA
	Minimum voltage drop at LDO1, LDO2	I_O = 50mA, VINLDO = 1.8V			120	mV
	Minimum voltage drop at LDO1, LDO2	I_O = 50mA, VINLDO = 1.5V		65	150	mV
	Minimum voltage drop at LDO1, LDO2	I_O = 200mA, VINLDO = 1.8V			300	mV
	Output voltage ccuracy for LDO1, LDO2	I_O = 10mA	–2%		1%	
	Line regulation for LDO1, LDO2	$V_{INLDO1,2}$ = $V_{LDO1,2}$ + 0.5V (min. 2.5V) to 6.5V, I_O = 10mA	–1%		1%	
	Load regulation for LDO1, LDO2	I_O = 0mA to 200mA	–1%		1%	
	Regulation time for LDO1, LDO2	Load change from 10% to 90%		10		µs
Vdd_alive Low Dropout Regulator						
Vdd_alive	Vdd_alive LDO output voltage, TPS650240 to TPS650244	I_O = 0mA		1.2		V
Vdd_alive	Vdd_alive LDO output voltage, TPS650245	I_O = 0mA		1.1		V
IO	Output current for Vdd_alive				30	mA
ISC	Vdd_alive short circuit current limit	Vdd_alive = GND			100	mA
	Output voltage accuracy for Vdd_alive	I_O = 0mA	–1%		1 %	
	Line regulation for Vdd_alive	V_{CC} = Vdd_alive + 0.5 V to 6.5 V, I_O = 0mA	–1%		1 %	
	Regulation time for Vdd_alive	Load change from 10% to 90%		10		µs
AnaLogic Signals DEFDCDC1, DEFDCDC2, DEFDCDC3						
V_{IH}	High level input voltage		1.3		VCC	V
V_{IL}	Low level input voltage		0		0.1	V
I_H	Input bias current			0.001	0.05	µA
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown	Increasing junction temperature		160		°C
	Thermal shudown hysteresis	Decreasing junction temperature		20		°C
INTERNAL UNDER VOLTAGE LOCK OUT						
UVLO	Internal UVLO	VCC falling	–3%	2.35	3%	V
V_{UVLO_HYST}	internalUVLO comparator hysteresis			120		mV
VOLTAGE DETECTOR COMPARATOR						
PWRFAIL_SNS	Comparator threshold	Falling threshold	–2%	1.0	2%	V
	Hysteresis		40	50	60	mV
	Propagation delay	25mV overdrive			10	µs
V_{OL}	Power fail output low voltage	I_{OL} = 5 mA			0.3	V

(1) If the feedback voltage is forced higher than above 1.2V, a leakage current into the feedback pin may occur.

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DEVICE INFORMATION

PIN ASSIGNMENTS



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
SWITCHING REGULATOR SECTION			
AGND1	31		Analog ground connection. All analog ground pins are connected internally on the chip.
AGND2	13		Analog ground connection. All analog ground pins are connected internally on the chip.
PowerPad	–		Connect the power pad to analog ground.
VINDCDC1	5	I	Input voltage for VDCDC1 step-down converter. This must be connected to the same voltage supply as VINDCDC2, VINDCDC3 and VCC.
L1	6		Switch pin of VDCDC1 converter. The VDCDC1 inductor is connected here.
VDCDC1	8	I	VDCDC1 feedback voltage sense input, connect directly to VDCDC1
PGND1	7		Power ground for VDCDC1 converter
VINDCDC2	28	I	Input voltage for VDCDC2 step-down converter. This must be connected to the same voltage supply as VINDCDC1, VINDCDC3 and VCC.
L2	27		Switch pin of VDCDC2 converter. The VDCDC2 inductor is connected here.
VDCDC2	25	I	VDCDC2 feedback voltage sense input, connect directly to VDCDC2
PGND2	26		Power ground for VDCDC2 converter
VINDCDC3	4	I	Input voltage for VDCDC3 step-down converter. This must be connected to the same voltage supply as VINDCDC1, VINDCDC2 and VCC.
L3	3		Switch pin of VDCDC3 converter. The VDCDC3 inductor is connected here.
VDCDC3	1	I	VDCDC3 feedback voltage sense input, connect directly to VDCDC3
PGND3	2		Power ground for VDCDC3 converter
Vcc	29	I	Power supply for digital and analog circuitry of DCDC1, DCDC2 and DCDC3 DC-DC converters. This must be connected to the same voltage supply as VINDCDC3, VINDCDC1 and VINDCDC2.
DEFDCDC1	9	I	Input signal indicating default VDCDC1 voltage, 0 = 2.80V, 1 = 3.3V This pin can also be connected to a resistor divider between VDCDC1 and GND. In this case the output voltage of the DCDC1 converter can be set in a range from 0.6V to VINDCDC1
DEFDCDC2	22	I	Input signal indicating default VDCDC2 voltage, 0=1.8V, 1=2.5V This pin can also be connected to a resistor divider between VDCDC2 and GND. In this case the output voltage of the DCDC2 converter can be set in a range from 0.6V to VINDCDC2.

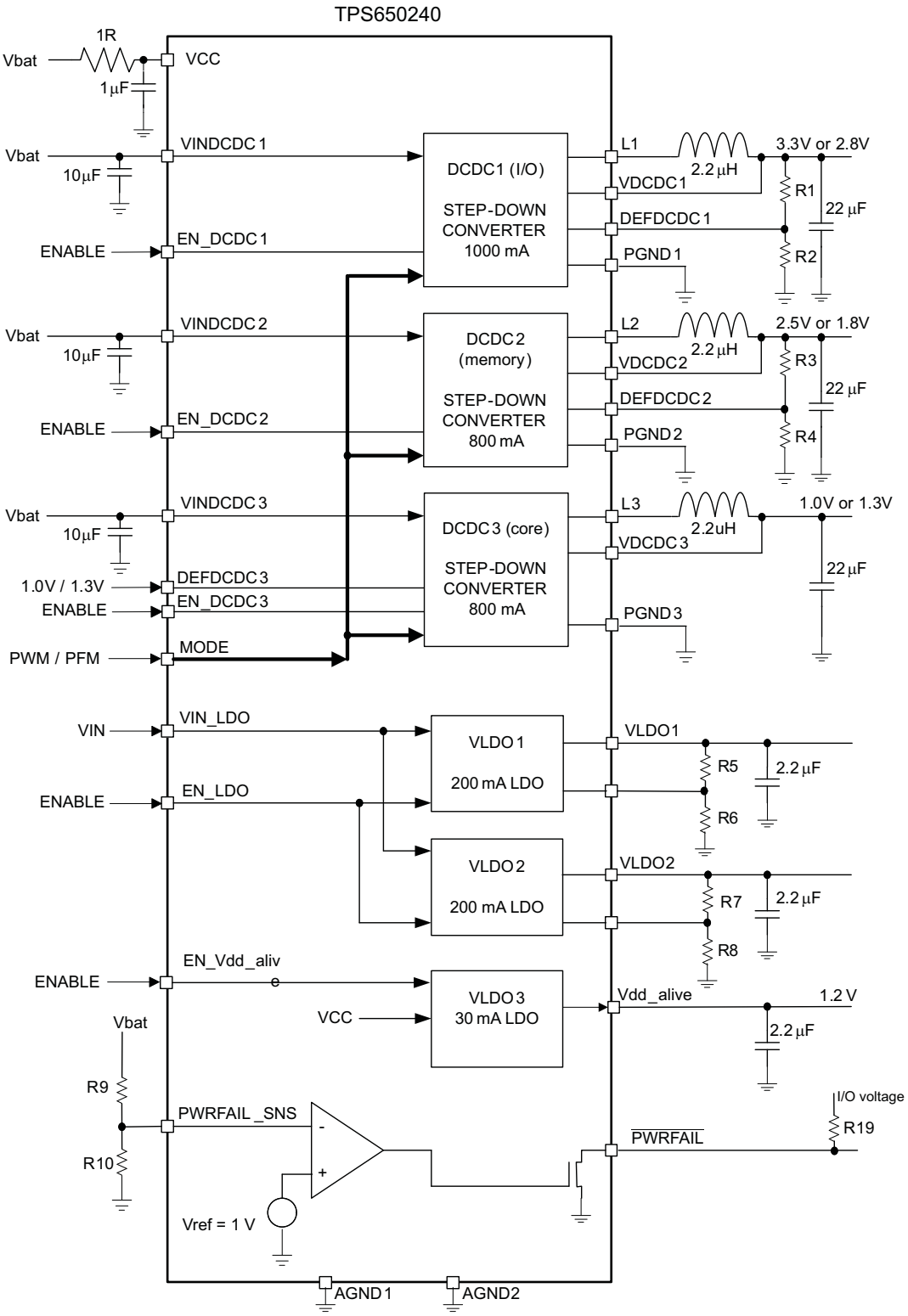
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TERMINAL FUNCTIONS (continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
DEFDCDC3	32	I	Input signal indicating VDCDC3 voltage. TPS650240: 0 = 1.0V, 1 = 1.3V TPS650241: 0 = 0.9V, 1 = 1.375V TPS650242: 0 = 1.0V, 1 = 1.5V TPS650243: 0 = 1.0V, 1 = 1.2V TPS650244: 0 = 1.55V, 1 = 1.6V TPS650245: 0 = 0.9V, 1 = 1.1V
EN_DCDC1	20	I	VDCDC1 enable pin. A logic high enables the regulator, a logic low disables the regulator.
EN_DCDC2	19	I	VDCDC2 enable pin. A logic high enables the regulator, a logic low disables the regulator.
EN_DCDC3	18	I	VDCDC3 enable pin. A logic high enables the regulator, a logic low disables the regulator.
LDO REGULATOR SECTION			
VINLDO	15	I	Input voltage for LDO1 and LDO2
VLDO1	16	O	Output voltage of LDO1
VLDO2	14	O	Output voltage of LDO2
EN_LDO	17	I	Enable input for LDO1 and LDO2. Logic high enables the LDOs, logic low disables the LDOs
EN_Vdd_alive	24	I	Enable input for Vdd_alive LDO. Logic high enables the LDO, logic low disables the LDO
Vdd_alive	12	O	Output voltage for Vdd_alive
FB_LDO1	11	I	Feedback pin for LDO1
FB_LDO2	10	I	Feedback pin for LDO2
CONTROL AND I2C SECTION			
MODE	23	I	Select between Power Safe Mode and forced PWM Mode for DCDC1, DCDC2 and DCDC3. In Power Safe Mode PFM is used at light loads, PWM for higher loads. If PIN is set to high level, forced PWM Mode is selected. If Pin has low level, then Device operates in Power Safe Mode.
$\overline{\text{PWRFAIL}}$	21	O	Open drain output. Active low when PWRFAIL comparator indicates low VBAT condition.
PWRFAIL_SNS	30	I	Input for the comparator driving the /PWRFAIL output

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FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

Parameter Measurement Information

Graphs were taken using the EVM with the following inductor/output capacitor combinations:

CONVERTER	INDUCTOR	OUTPUT CAPACITOR	OUTPUT CAPACITOR VALUE
DCDC1	VLCF4020-3R3	C2012X5R0J226M	22µF
DCDC2	VLCF4020-2R2	C2012X5R0J226M	22µF
DCDC3	LPS3010-222	C2012X5R0J226M	22µF

Table of Graphs

			FIGURE
η	Efficiency VDCDC1	vs Load current PWM/PFM; V_O = 3.3V	Figure 1
η	Efficiency VDCDC1	vs Load current PWM; V_O = 3.3V	Figure 2
η	Efficiency VDCDC2	vs Load current PWM/PFM; V_O = 1.8V	Figure 3
η	Efficiency VDCDC2	vs Load current PWM; V_O = 1.8V	Figure 4
η	Efficiency VDCDC3	vs Load current PWM/PFM; V_O = 1.3V	Figure 5
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	Line transient response VDCDC1		Figure 7
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	Output voltage ripple DCDC2; PFM mode		Figure 13
	Output voltage ripple DCDC2; PWM mode		Figure 14
	Load regulation for Vdd_alive		Figure 15
	Start-up VDCDC1 to VDCDC3		Figure 16
	Start-up LDO1 and LDO2		Figure 17

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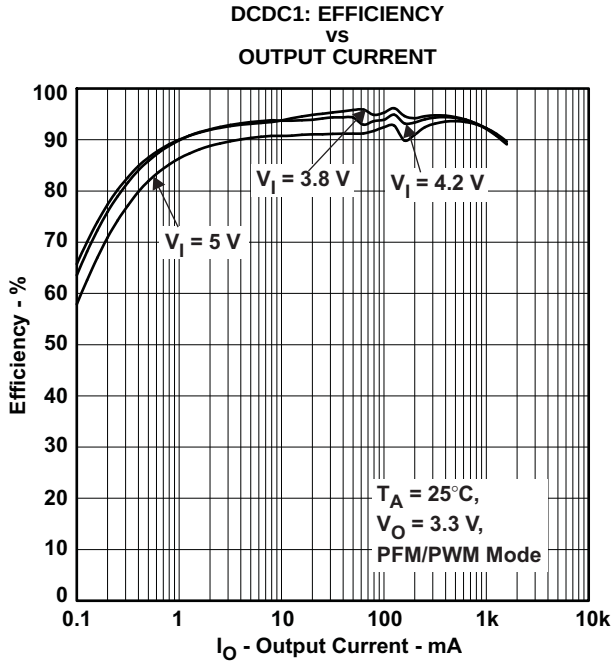


Figure 1.

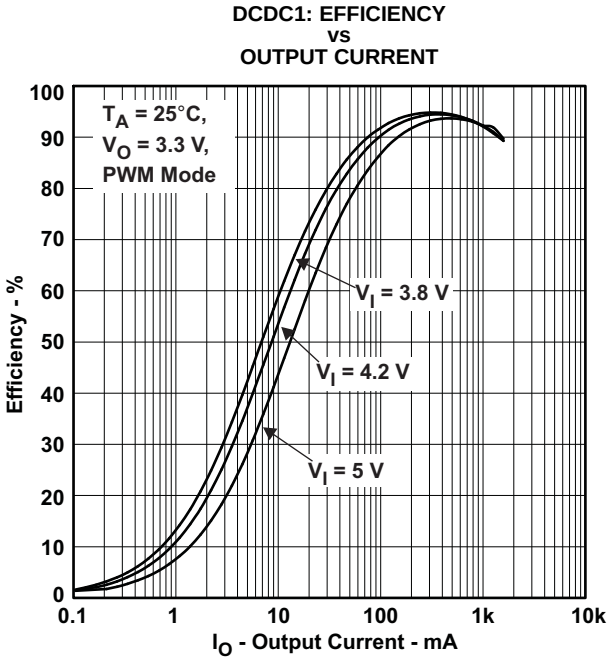


Figure 2.

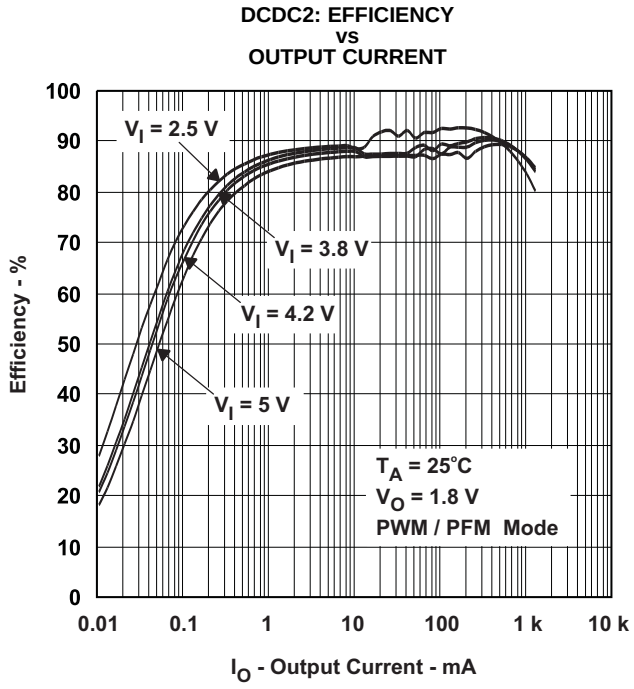


Figure 3.

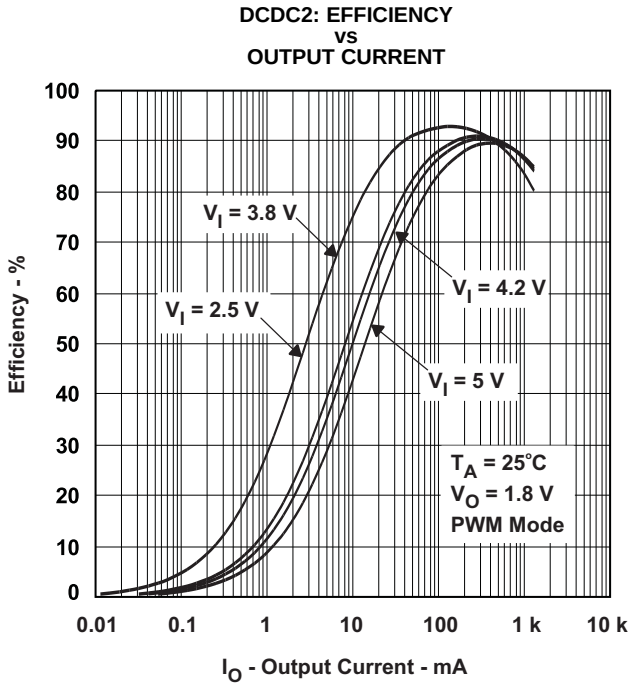


Figure 4.

DCDC3: EFFICIENCY vs OUTPUT CURRENT

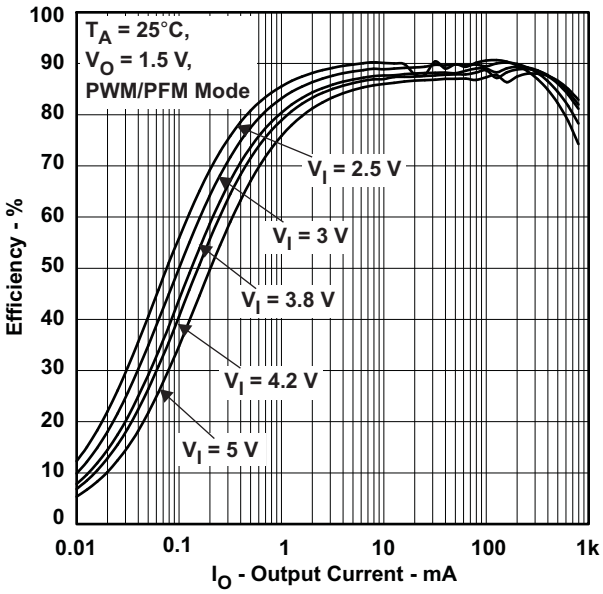


Figure 5.

DCDC3: EFFICIENCY vs OUTPUT CURRENT

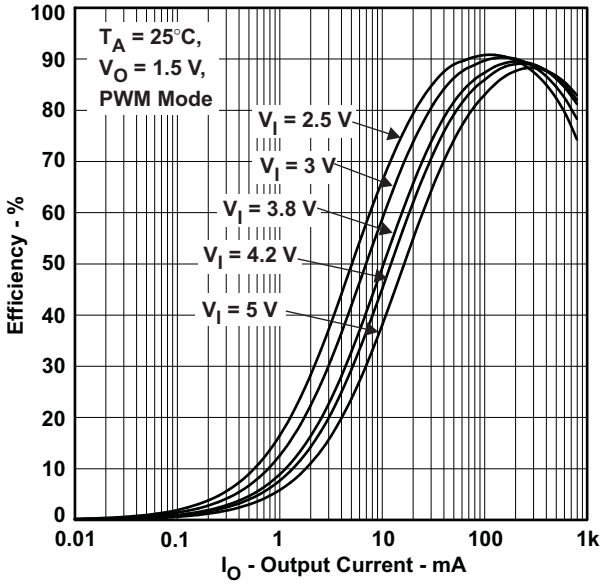


Figure 6.

VDCDC1 LINE TRANSIENT RESPONSE

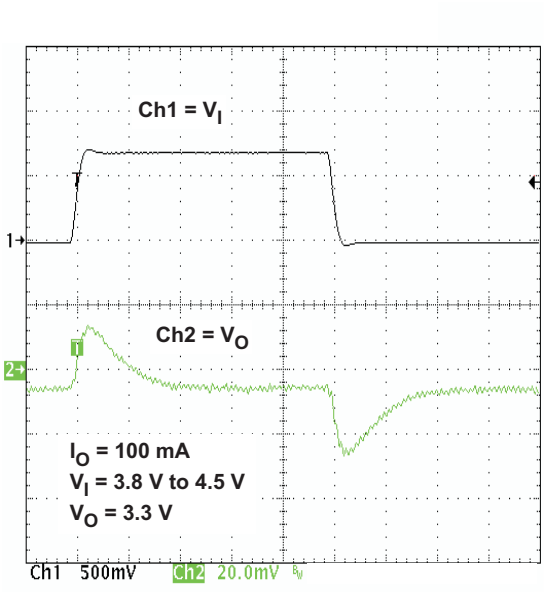


Figure 7.

VDCDC2 LINE TRANSIENT RESPONSE

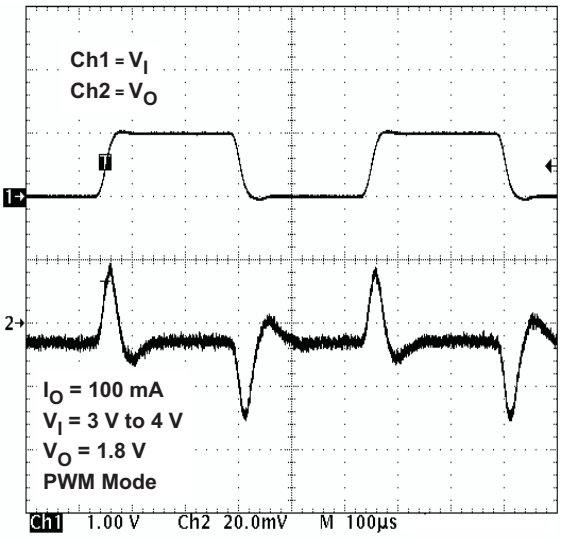


Figure 8.

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VDCDC3 LINE TRANSIENT RESPONSE

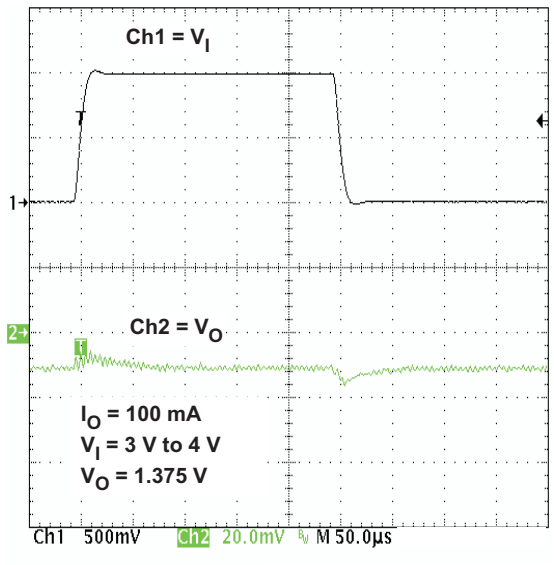


Figure 9.

VDCDC1 LOAD TRANSIENT RESPONSE

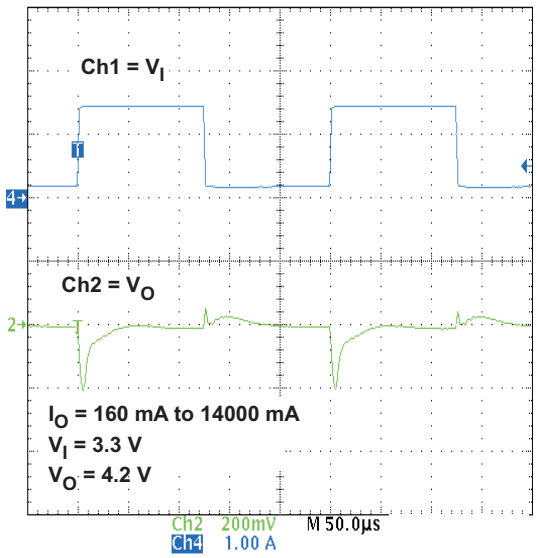


Figure 10.

VDCDC2 LOAD TRANSIENT RESPONSE

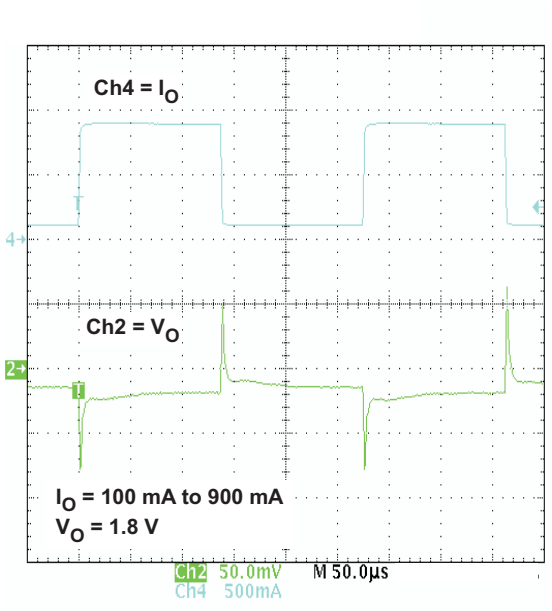


Figure 11.

VDCDC3 LOAD TRANSIENT RESPONSE

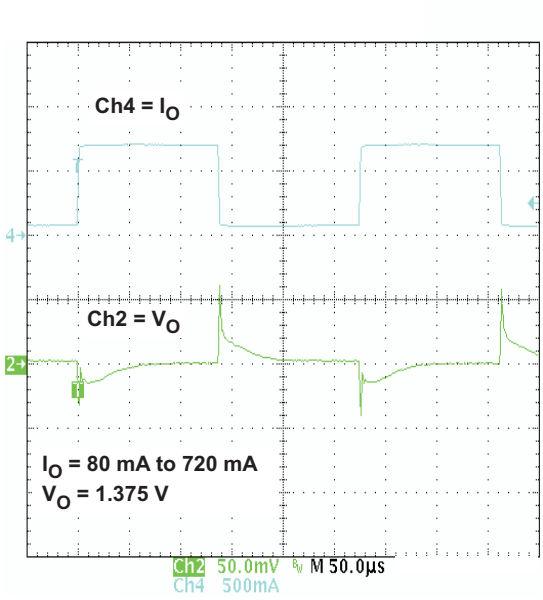


Figure 12.

VDCDC2 OUTPUT VOLTAGE RIPPLE

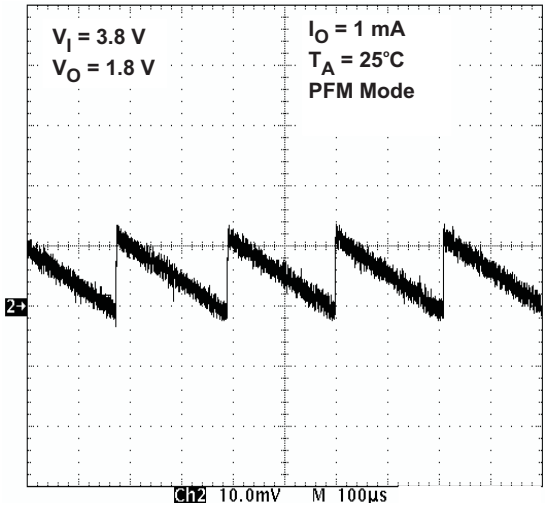


Figure 13.

VDCDC2 OUTPUT VOLTAGE RIPPLE

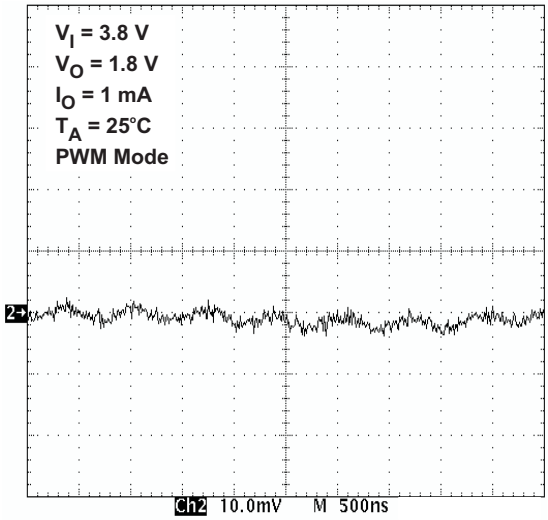


Figure 14.

VDD_ALIVE OUTPUT VOLTAGE vs OUTPUT CURRENT

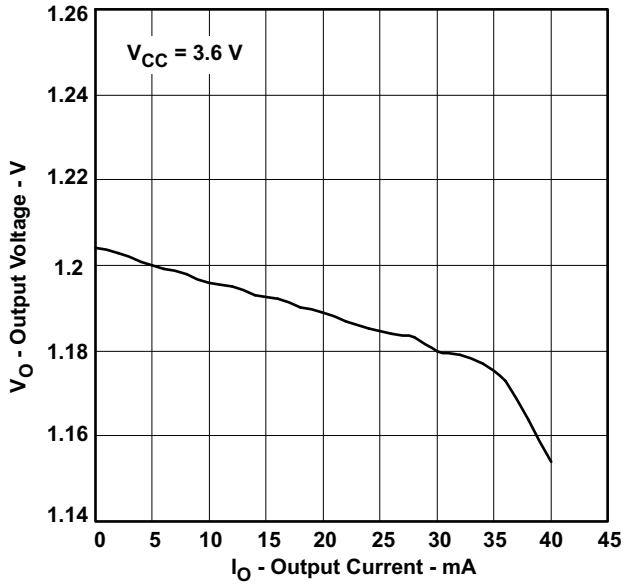


Figure 15.

STARTUP VDCDC1, VDCDC2, VDCDC3

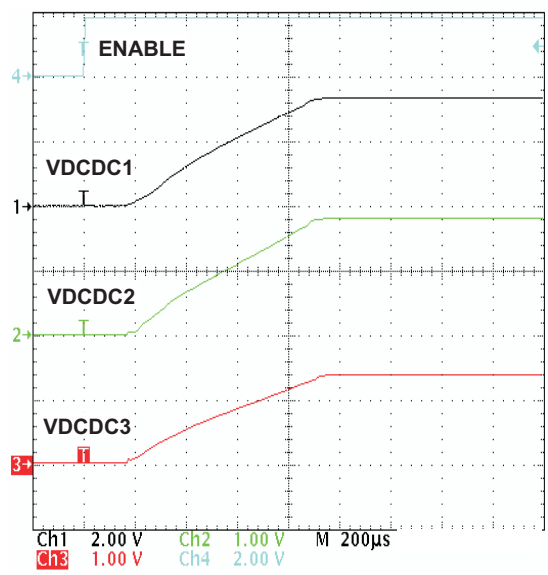


Figure 16.

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STARTUP LDO1 AND LDO2

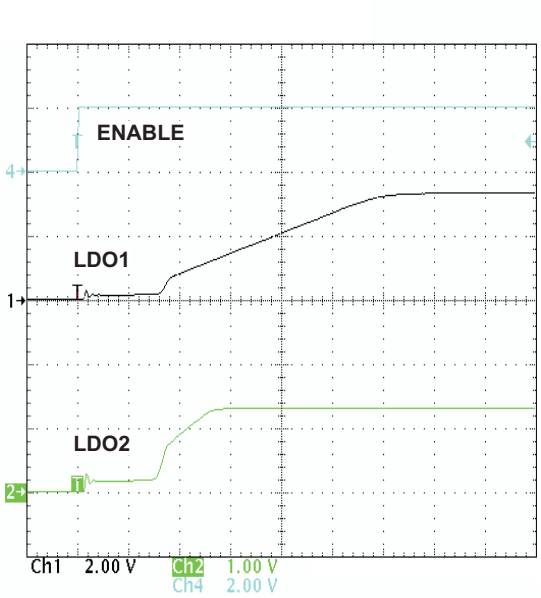


Figure 17.

DETAILED DESCRIPTION

STEP-DOWN CONVERTERS, VDCDC1, VDCDC2 AND VDCDC3

The TPS65024x incorporate three synchronous step-down converters operating typically at 2.25MHz fixed frequency PWM (Pulse Width Modulation) at moderate to heavy load currents. At light load currents the converters automatically enter Power Save Mode and operate with PFM (Pulse Frequency Modulation). VDCDC1 delivers up to 1.6A, VDCDC2 is capable of delivering up to 1.0A of output current while the VDCDC3 converter is capable of delivering up to 800mA.

The converter output voltages can be programmed via the DEFDCDC1, DEFDCDC2 and DEFDCDC3 pins. The pins can either be connected to GND, VCC or to a resistor divider between the output voltage and GND. The VDCDC1 converter defaults to 2.80V or 3.3V depending on the DEFDCDC1 configuration pin, if DEFDCDC1 is tied to ground the default is 2.80V, if it is tied to VCC the default is 3.3V. When the DEFDCDC1 pin is connected to a resistor divider, the output voltage can be set in the range of 0.6V to VINDCDC1 V. Reference the section on Output Voltage Selection for details on setting the output voltage range.

The VDCDC2 converter defaults to 1.8V or 2.5V depending on the DEFDCDC2 configuration pin, if DEFDCDC2 is tied to ground the default is 1.8V, if it is tied to VCC the default is 2.5V. When the DEFDCDC2 pin is connected to a resistor divider, the output voltage can be set in the range of 0.6V to VINDCDC2 V.

The VDCDC3 converter defaults to 1.0V or 1.3V for the TPS650240 depending on the DEFDCDC3 configuration pin, if DEFDCDC3 is tied to ground the default is 1.0V, if it is tied to VCC the default is 1.3V. The DEFDCDC3 pin cannot be connected to a resistor divider. In opposition to DEFDCDC1 and DEFDCDC2, the DEFDCDC3 pin can be used to change the core voltage during operation by changing its logic level from HIGH to LOW or vice versa. TPS650241 to TPS650245 allow different voltages for the VDCDC3 converter. Reference Table 4 for the TPS650240, TPS650241, TPS650242, TPS650243, TPS650244 and TPS650245 default voltage options.

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During PWM operation the converters use a unique fast response voltage mode controller scheme with input voltage feed-forward to achieve good line and load regulation allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the P-channel MOSFET switch is turned on and the inductor current ramps up until the comparator trips and the control logic turns off the switch. The current limit comparator also turns off the switch in case the current limit of the P-channel switch is exceeded. After the adaptive dead time used to prevent shoot through current, the N-channel MOSFET rectifier is turned on and the inductor current ramps down. The next cycle is initiated by the clock signal again turning off the N-channel rectifier and turning on the P-channel switch.

The three DC/DC converters operate synchronized to each other, with the VDCDC1 converter as the master. A 180° phase shift between the VDCDC1 switch turn on and the VDCDC2 and a further 90° shift to the VDCDC3 switch turn on decreases the input RMS current and smaller input capacitors can be used. This is optimized for a typical application where the VDCDC1 converter regulates a Li-Ion battery voltage of 3.7V to 3.3V, the VDCDC2 converter from 3.7V to 2.5V and the VDCDC3 converter from 3.7V to 1.5V.

POWER SAVE MODE OPERATION

As the load current decreases, the converters enter Power Save Mode operation. During Power Save Mode the converters operate in a burst mode (PFM mode) with a frequency between 1.125MHz and 2.25MHz for one burst cycle. However, the frequency between different burst cycles depends on the actual load current and is typically far less than the switching frequency, with a minimum quiescent current to maintain high efficiency.

In order to optimize the converter efficiency at light load the average current is monitored and if in PWM mode the inductor current remains below a certain threshold, then Power Save Mode is entered. The typical threshold to enter Power Save Mode can be calculated as follows:

$$I_{PFMDCDC1enter} = \frac{VINDCDC\ 1}{24\ \Omega}$$

$$I_{PFMDCDC2enter} = \frac{VINDCDC\ 2}{26\ \Omega}$$

$$I_{PFMDCDC3leave} = \frac{VINDCDC\ 3}{39\ \Omega} \quad (1)$$

During Power Save Mode the output voltage is monitored with a comparator and by maximum skip burst width. As the output voltage falls below the threshold, set to the nominal V_O, the P-channel switch turns on and the converter effectively delivers a constant current as defined below.

$$I_{PFMDCDC1leave} = \frac{VINDCDC\ 1}{18\ \Omega}$$

$$I_{PFMDCDC2leave} = \frac{VINDCDC\ 2}{20\ \Omega}$$

$$I_{PFMDCDC3enter} = \frac{VINDCDC\ 3}{29\ \Omega} \quad (2)$$

If the load is below the delivered current then the output voltage rises until the same threshold is crossed in the other direction. All switching activity ceases, reducing the quiescent current to a minimum until the output voltage has again dropped below the threshold. The power save mode is exited, and the converter returns to PWM mode if either of the following conditions are met:

1. The output voltage drops 2% below the nominal V_O due to increased load current
2. The PFM burst time exceeds 16 × 1/fs (7.1µs typical)

These control methods reduce the quiescent current to typically 14µA per converter and the switching activity to a minimum thus achieving the highest converter efficiency. Setting the comparator thresholds at the nominal output voltage at light load current results in a very low output voltage ripple. The ripple depends on the comparator delay and the size of the output capacitor; increasing capacitor values makes the output ripple tend to zero. Power Save Mode can be disabled by pulling the MODE pin high. This forces all DC/DC converters into fixed frequency PWM mode.

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SOFT START

Each of the three converters has an internal soft start circuit that limits the inrush current during start-up. The soft start is realized by using a very low current to initially charge the internal compensation capacitor. The soft start time is typically 750µs if the output voltage ramps from 5% to 95% of the final target value. If the output is already pre-charged to some voltage when the converter is enabled, then this time is reduced proportionally. There is a short delay of typically 170µs between the converter being enabled and switching activity actually starting. This is to allow the converter to bias itself properly, to recognize if the output is pre-charged, and if so, to prevent discharging of the output while the internal soft start ramp catches up with the output voltage.

100% DUTY CYCLE LOW DROPOUT OPERATION

The TPS65024x converters offer a low input to output voltage difference while still maintaining operation with the use of the 100% duty cycle mode. In this mode the P-channel switch is constantly turned on. This is particularly useful in battery-powered applications to achieve the longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage required to maintain DC regulation depends on the load current and output voltage and can be calculated as:

$$Vin_{min} = Vout_{min} + Iout_{max} \times \left(RDSon_{max} + R_L\right) \quad (3)$$

With:

$Iout_{max}$ = Maximum load current (note: ripple current in the inductor is zero under these conditions)

$RDSon_{max}$ = Maximum P-channel switch RDSon

R_L = DC resistance of the inductor

$Vout_{min}$ = Nominal output voltage minus 2% tolerance limit

LOW DROPOUT VOLTAGE REGULATORS

The low dropout voltage regulators are designed to operate well with low value ceramic input and output capacitors. They operate with input voltages down to 1.5V. The LDOs offer a maximum dropout voltage of 300mV at the rated output current. Each LDO sports a current limit feature. Both LDOs are enabled by the EN_LDO pin. The LDOs also have reverse conduction prevention. This allows the possibility to connect external regulators in parallel in systems with a backup battery. The TPS65024x step-down and LDO voltage regulators automatically power down when the Vcc voltage drops below the UVLO threshold or when the junction temperature rises above 160°C.

UNDERVOLTAGE LOCKOUT

The undervoltage lockout circuit for the five regulators on the TPS65024x prevents the device from malfunctioning at low input voltages and from excessive discharge of the battery. It disables the converters and LDOs. The UVLO circuit monitors the Vcc pin; the threshold is set internally to 2.35V with 5% (120mV) hysteresis. Note that when any of the DC/DC converters are running there is an input current at the Vcc pin, which can be up to 3mA when all three converters are running in PWM mode. This current needs to be taken into consideration if an external RC filter is used at the Vcc pin to remove switching noise from the TPS65024x internal analog circuitry supply. See the Vcc-Filter section for details on the external RC filter.

POWER-UP SEQUENCING

The TPS65024x power-up sequencing is designed to be entirely flexible and customer driven; this is achieved simply by providing separate enable pins for each switch-mode converter and a common enable signal for LDO1 and LDO2. The relevant control pins are described in Table 1.

Table 1. Control Pins for DCDC Converters

PIN NAME	INPUT/ OUTPUT	FUNCTION
DEFDCDC3	I	Defines the default voltage of the VDCDC3 switching converter. See table 4 for details.
DEFDCDC2	I	Defines the default voltage of the VDCDC2 switching converter. DEFDCDC2 = 0 defaults VDCDC2 to 1.8V, DEFDCDC2 = VCC defaults VDCDC2 to 2.5V.
DEFDCDC1	I	Defines the default voltage of the VDCDC1 switching converter. DEFDCDC1 = 0 defaults VDCDC1 to 2.80V, DEFDCDC1 = VCC defaults VDCDC1 to 3.3V.

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Table 1. Control Pins for DCDC Converters (continued)

PIN NAME	INPUT/ OUTPUT	FUNCTION
EN_DCDC3	I	Set EN_DCDC3 = 0 to disable or EN_DCDC3 = 1 to enable the VDCDC3 converter
EN_DCDC2	I	Set EN_DCDC2 = 0 to disable or EN_DCDC2 = 1 to enable the VDCDC2 converter
EN_DCDC1	I	Set EN_DCDC1 = 0 to disable or EN_DCDC1 = 1 to enable the VDCDC1 converter

$\overline{\text{PWRFAIL}}$

The $\overline{\text{PWRFAIL}}$ signal is generated by a voltage detector at the PWRFAIL_SNS input. The input signal is compared to a 1V threshold (falling edge) with 5% (50mV) hysteresis. $\overline{\text{PWRFAIL}}$ is an open drain output which is actively low when the input voltage at PWRFAIL_SNS is below the threshold.

DESIGN PROCEDURE

Inductor Selection for the dcdc Converters

The three converters operate with 2.2uH output inductors. Larger or smaller inductor values can be used to optimize performance of the device for specific conditions. The selected inductor has to be rated for its dc resistance and saturation current. The dc resistance of the inductor influences directly the efficiency of the converter. Therefore, an inductor with the lowest dc resistance should be selected for the highest efficiency.

For a fast transient response, a 2.2µH inductor in combination with a 22µF output capacitor is recommended. For an output voltage above 2.8V, an inductor value of 3.3µH minimum is required. Lower values result in an increased output voltage ripple in PFM mode. The minimum inductor value is 1.5µH, but an output capacitor of 22µF minimum is needed in this case.

Equation 4 calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 4. This is recommended because during heavy load transient the inductor current rises above the calculated value.

$$\Delta I_L = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \qquad I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2} \tag{4}$$

With:

f = Switching frequency (2.25 MHz typical)

L = Inductor value

ΔI_L = Peak-to-peak inductor ripple current

I_{Lmax} = Maximum inductor current

The highest inductor current occurs at maximum Vin.

Open core inductors have a soft saturation characteristic and they can usually handle higher inductor currents versus a comparable shielded inductor.

A more conservative approach is to select the inductor current rating just for the maximum switch current of the corresponding converter. Consideration must be given to the difference in the core material from inductor to inductor which has an impact on efficiency especially at high switching frequencies. See Table 2 and the typical applications for possible inductors.

Table 2. Tested Inductors

DEVICE	INDUCTOR VALUE	TYPE	COMPONENT SUPPLIER
	3.3µH	LPS3015-332 (output current up to 1A)	Coilcraft
	2.2µH	LPS3015-222 (output current up to 1A)	Coilcraft
	3.3µH	VLCF4020T-3R3N1R5	TDK
	2.2µH	VLCF4020T-2R2N1R7	TDK

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Table 2. Tested Inductors (continued)

DEVICE	INDUCTOR VALUE	TYPE	COMPONENT SUPPLIER
DCDC3 converter	2.2µH	LPS3010-222	Coilcraft
	2.2µH	LPS3015-222	Coilcraft
	2.2µH	VLCF4020-2R2	TDK

Output Capacitor Selection

The advanced Fast Response voltage mode control scheme of the inductive converters implemented in the TPS65024x allows the use of small ceramic capacitors with a typical value of 10uF for each converter, without having large output voltage under and overshoots during heavy load transients. Ceramic capacitors having low ESR values have the lowest output voltage ripple and are recommended. Refer to Table 3 for recommended components.

If ceramic output capacitors are used, the capacitor RMS ripple current rating will always meet the application requirements. For completeness, the RMS ripple current is calculated as:

$$I_{RMSCout} = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (5)$$

At nominal load current the inductive converters operate in PWM mode and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta Vout = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \times \left(\frac{1}{8 \times Cout \times f} + ESR \right) \quad (6)$$

Where the highest output voltage ripple occurs at the highest input voltage, Vin.

At light load currents the converters operate in Power Save Mode and output voltage ripple is dependent on the output capacitor value. The output voltage ripple is set by the internal comparator delay and the external capacitor. Typical output voltage ripple is less than 1% of the nominal output voltage.

Input Capacitor Selection

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing interference with other circuits caused by high input voltage spikes. Each dcdc converter requires a 10uF ceramic input capacitor on its input pin VINDCDCx. The input capacitor can be increased without any limit for better input voltage filtering. The Vcc pin should be separated from the input for the DC/DC converters. A filter resistor of up to 10Ω and a 1µF capacitor should be used for decoupling the Vcc pin from switching noise. Note that the filter resistor may affect the UVLO threshold since up to 3mA can flow via this resistor into the Vcc pin when all converters are running in PWM mode.

Table 3. Possible Capacitors

CAPACITOR VALUE	CASE SIZE	COMPONENT SUPPLIER		COMMENTS
22µF	1206	TDK	C3216X5R0J226M	Ceramic
22µF	1206	Taiyo Yuden	JMK316BJ226ML	Ceramic
22µF	0805	TDK	C2012X5R0J226MT	Ceramic
22µF	0805	Taiyo Yuden	JMK212BJ226MG	Ceramic
10µF	0805	Taiyo Yuden	JMK212BJ106M	Ceramic
10µF	0805	TDK	C2012X5R0J106M	Ceramic

Output Voltage Selection

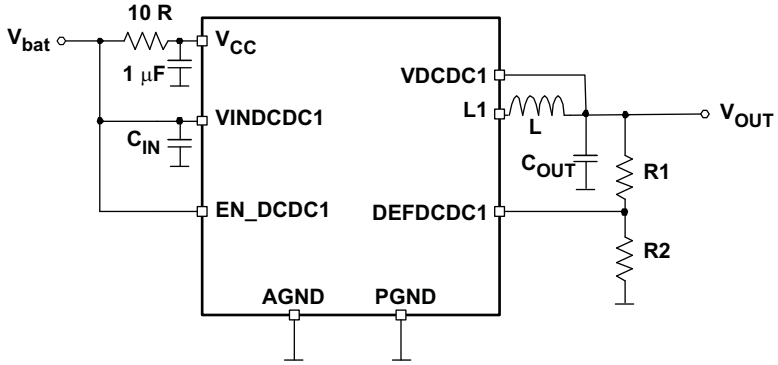
The DEFDCDC1, DEFDCDC2, and DEFDCDC3 pins are used to set the output voltage for each step-down converter. See Table 4 for the default voltages if the pins are pulled to GND or to Vcc.

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Table 4. Voltage Options

PIN		LEVEL	DEFAULT OUTPUT VOLTAGE
DEFDCDC1	All versions	VCC	3.3V
		GND	2.80V
DEFDCDC2	All versions	VCC	2.5V
		GND	1.8V
DEFDCDC3	TPS650240	VCC	1.3V
		GND	1.0V
	TPS650241	VCC	1.375V
		GND	0.9V
	TPS650242	VCC	1.5V
		GND	1.0V
	TPS650243	VCC	1.2V
		GND	1.0V
	TPS650244	VCC	1.6V
		GND	1.55V
	TPS650245	VCC	1.1V
		GND	0.9V

If a different voltage is needed, an external resistor divider can be added to the DEFDCDC1 or DEFDCDC2 pin as shown below:



When a resistor divider is connected to DEFDCDC1 or DEFDCDC2, the output voltage can be set from 0.6V up to the input voltage V_{bat}. The total resistance (R1+R2) of the voltage divider should be kept in the 1MΩ range in order to maintain a high efficiency at light load. $V_{DEFDCDCx}$ = 0.6V

$$V_{OUT} = V_{DEFDCDCx} \times \frac{R1 + R2}{R2}$$

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{DEFDCDCx}} \right) - R2$$

Voltage Change on VDCDC3

The output voltage of VDCDC3 can be changed during operation from e.g. 1.0V to 1.3V (TPS650240) and back. While the output voltage at VDCDC1 and VDCDC2 is fixed after the device exits undervoltage lockout (UVLO), the status of the DEFDCDC3 pin is sensed during operation and the voltage is changed as soon as the logic level on this pin changes from low to high or vice versa. Therefore it is not possible to connect a resistor divider to DEFDCDC3 and set a voltage different from the predefined voltages.

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Vdd_alive Output

The Vdd_alive LDO is typically connected to the Vdd_alive input of the Samsung application processor. It provides an output voltage of 1.2V at 30mA. For the TPS650245, the output voltage is 1.1V. It is recommended to add a capacitor of 2.2µF minimum to the Vdd_alive pin. The LDO can be disabled by pulling the EN_Vdd_alive pin to GND.

LDO1 and LDO2

The LDOs in the TPS65024x are general purpose LDOs which are stable using ceramics capacitors. The minimum output capacitor required is 2.2µF. The LDOs output voltage can be changed to different voltages between 1.0V and Vin using an external resistor divider. Therefore they can also be used as general purpose LDOs in the application. The supply voltage for the LDOs needs to be connected to the VINLDO pin, giving the flexibility to connect the lowest voltage available in the system and therefore providing the highest efficiency.

The total resistance (R5+R6) of the voltage divider should be kept in the 1MΩ range in order to maintain high efficiency at light load. V_{FBLDOx}= 1.0V.

$$V_{OUT} = V_{FBLDOx} \times \frac{R5 + R6}{R6}$$

$$R5 = R6 \times \left(\frac{V_{OUT}}{V_{FBLDOx}} \right) - R6$$

Vcc-Filter

An RC filter connected at the Vcc input is used to keep noise from the internal supply for the bandgap and other analog circuitry. A typical value of 1Ω and 1µF is used to filter the switching spikes, generated by the DC/DC converters. A larger resistor than 10Ω should not be used because the current into Vcc of up to 2.5mA causes a voltage drop at the resistor causing the undervoltage lockout circuitry connected at Vcc internally to switch off too early.

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APPLICATION INFORMATION

TYPICAL CONFIGURATION FOR THE TITAN 2 PROCESSOR

The core voltage is generated using DCDC2 with the output voltage set to 1.2V using a resistor divider at DEFDCDC2 as only DCDC2 can support an output current of up to 1.6A. DCDC3 is used for the memory voltage of 1.8V. As DCDC3 does not support an external resistor divider, the output voltage is programmed to 1.6V by setting DEFDCDC3 = HIGH. In addition, there is a resistor at the input of the internal voltage divider at pin VDCDC3 which adds another 200mV. The internal resistance at VDCDC3 when programmed to 1.6V is 480kΩ, so the external resistance needed to increase the output voltage from 1.6V to 1.8V is 60kΩ (62kΩ). The typical configuration for the Titan 2 processor is shown in Figure 18.

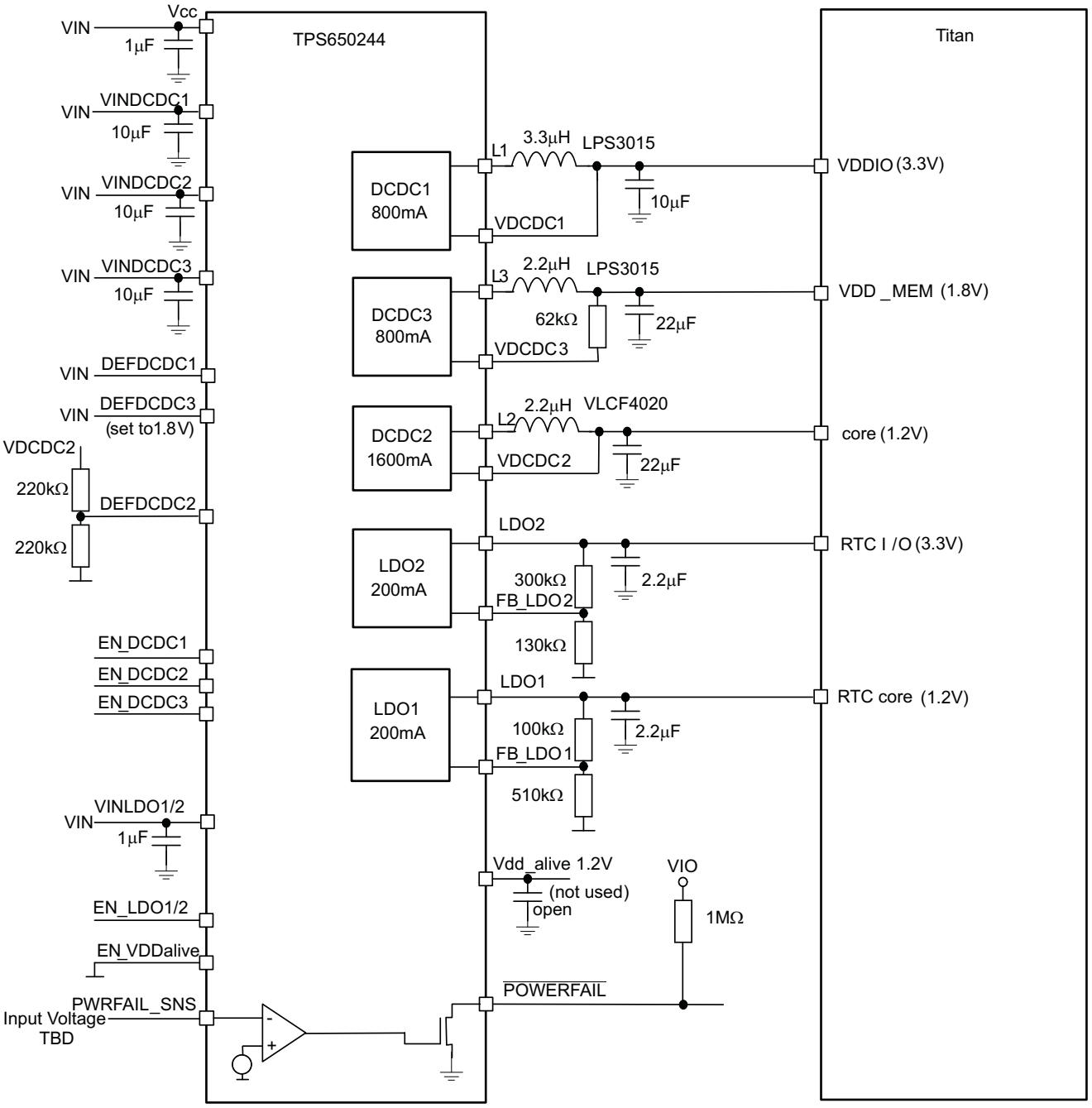


Figure 18. Titan Processor Configuration

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TYPICAL CONFIGURATION FOR THE SAMSUNG PROCESSOR S3C6400-533MHz

The typical configuration for the Samsung processor S3C6400-533MHz is shown in Figure 19.

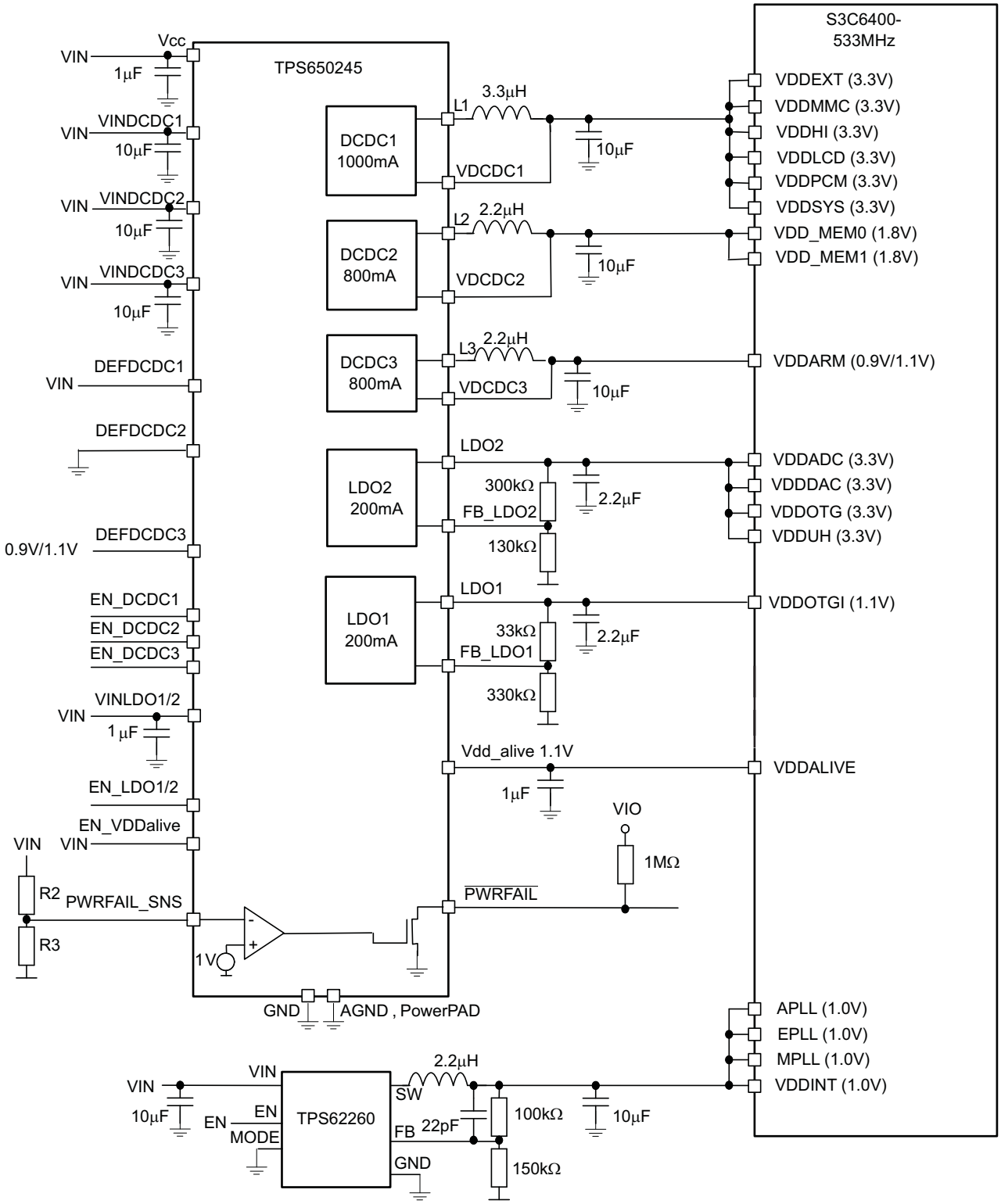


Figure 19. Samsung Processor Configuration

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS650240RHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS650240RHBRG4	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS650240RHBT	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS650240RHBTG4	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS650241RHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS650241RHBRG4	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS650241RHBT	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS650241RHBTG4	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS650242RHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS650242RHBRG4	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS650242RHBT	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS650242RHBTG4	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS650243RHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS650243RHBRG4	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS650243RHBT	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS650243RHBTG4	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS650244RHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS650244RHBRG4	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS650244RHBT	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS650244RHBTG4	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS650245RHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS650245RHBRG4	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS650245RHBT	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS650245RHBTG4	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

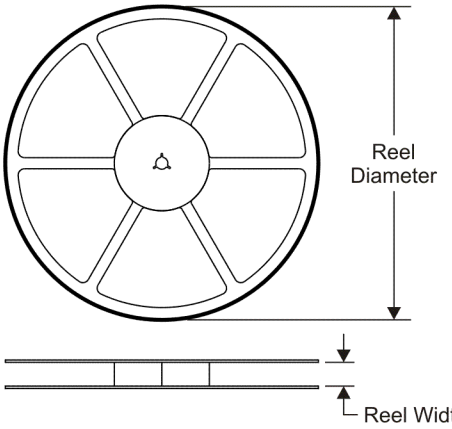
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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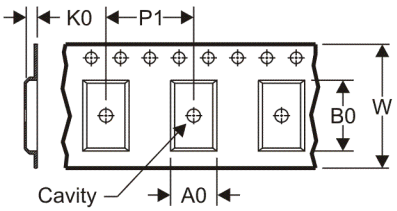
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

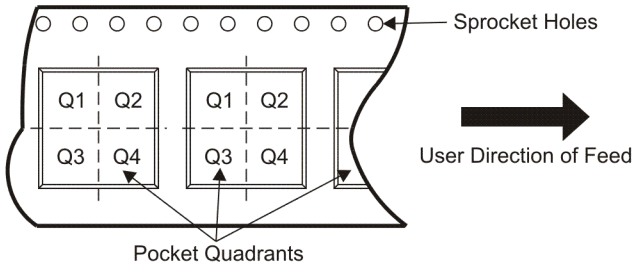


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

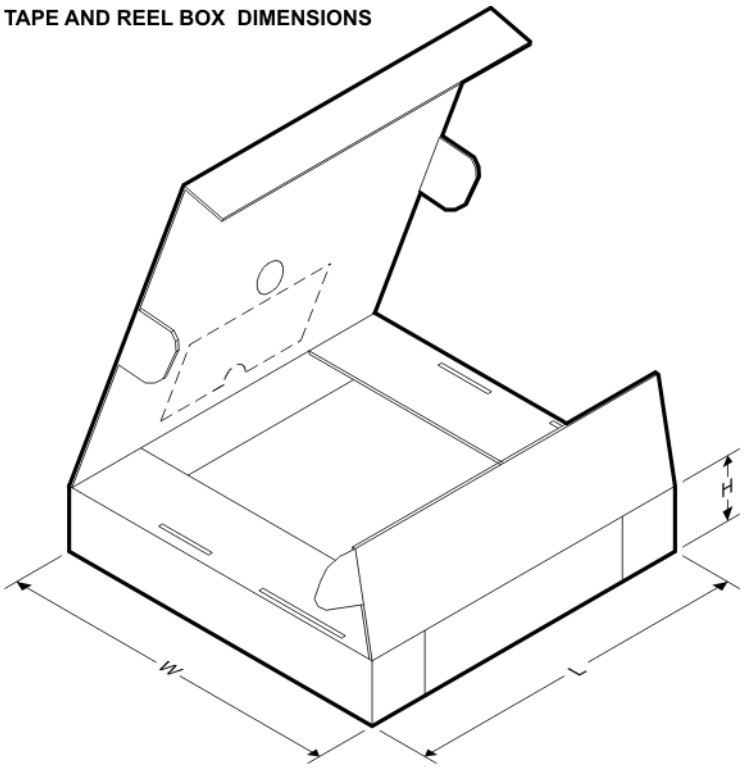
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS650240RHBR	QFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TPS650240RHBT	QFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TPS650241RHBR	QFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TPS650241RHBT	QFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TPS650242RHBR	QFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TPS650242RHBT	QFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TPS650243RHBR	QFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TPS650243RHBT	QFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TPS650244RHBR	QFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TPS650244RHBT	QFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TPS650245RHBR	QFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TPS650245RHBT	QFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

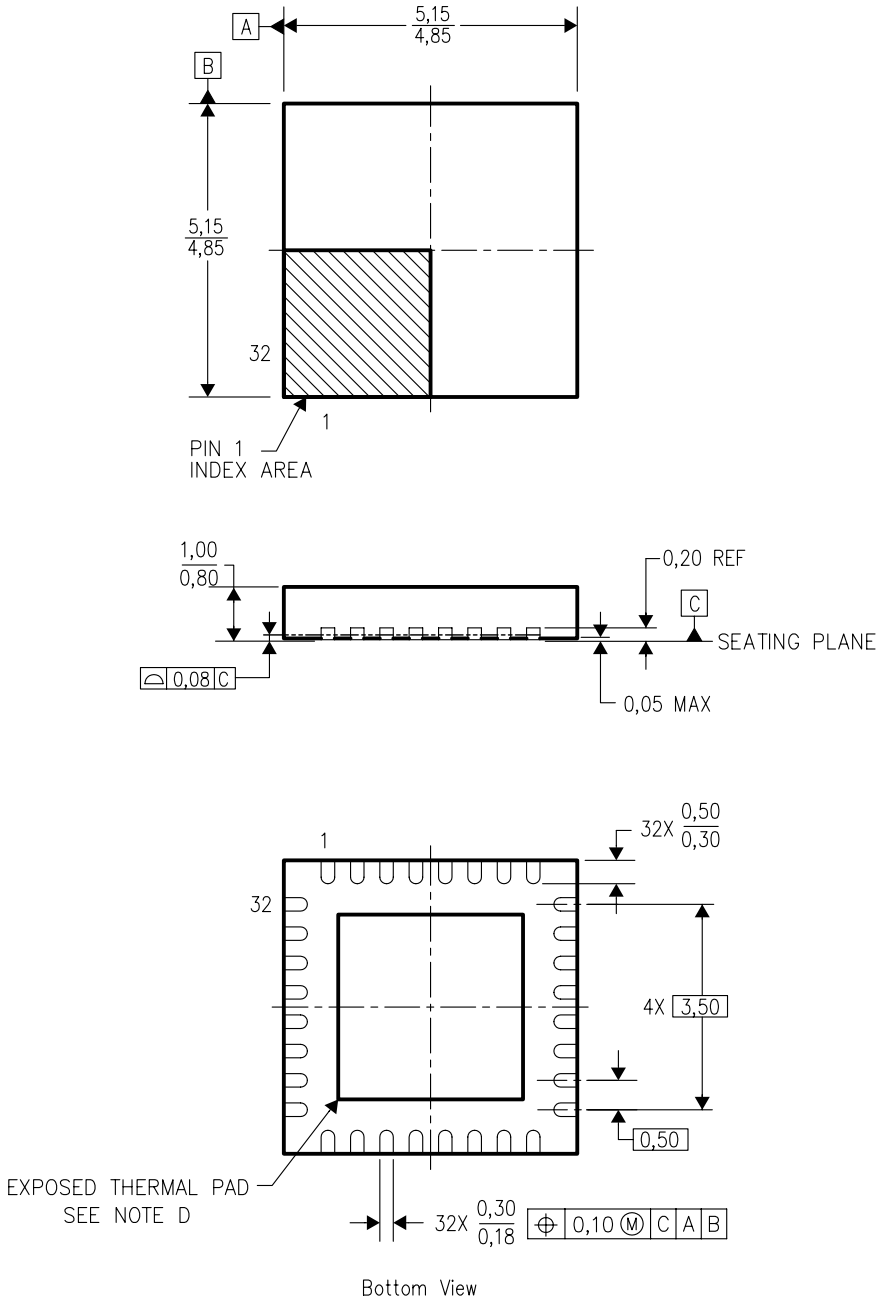
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS650240RHBR	QFN	RHB	32	3000	346.0	346.0	29.0
TPS650240RHBT	QFN	RHB	32	250	190.5	212.7	31.8
TPS650241RHBR	QFN	RHB	32	3000	346.0	346.0	29.0
TPS650241RHBT	QFN	RHB	32	250	190.5	212.7	31.8
TPS650242RHBR	QFN	RHB	32	3000	346.0	346.0	29.0
TPS650242RHBT	QFN	RHB	32	250	190.5	212.7	31.8
TPS650243RHBR	QFN	RHB	32	3000	346.0	346.0	29.0
TPS650243RHBT	QFN	RHB	32	250	190.5	212.7	31.8
TPS650244RHBR	QFN	RHB	32	3000	346.0	346.0	29.0
TPS650244RHBT	QFN	RHB	32	250	190.5	212.7	31.8
TPS650245RHBR	QFN	RHB	32	3000	346.0	346.0	29.0
TPS650245RHBT	QFN	RHB	32	250	190.5	212.7	31.8

RHB (S–PQFP–N32) PLASTIC QUAD FLATPACK



4204326/C xx/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D The Package thermal pad must be soldered to the board for thermal and mechanical performance. See product data sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

THERMAL PAD MECHANICAL DATA

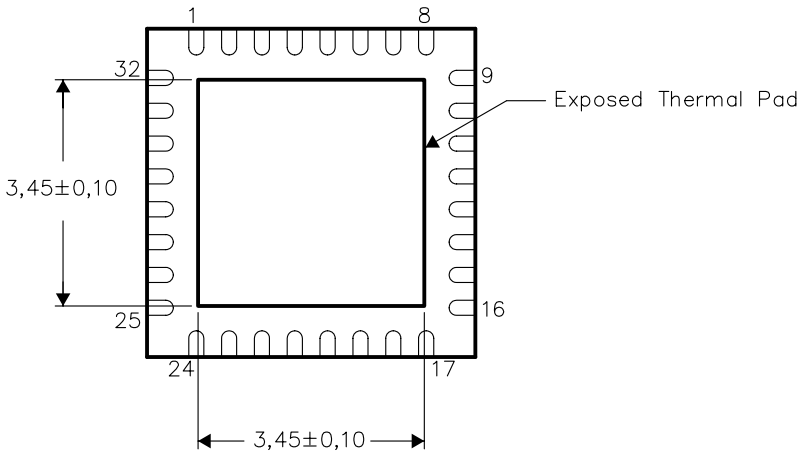
RHB (S–PQFP–N32)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

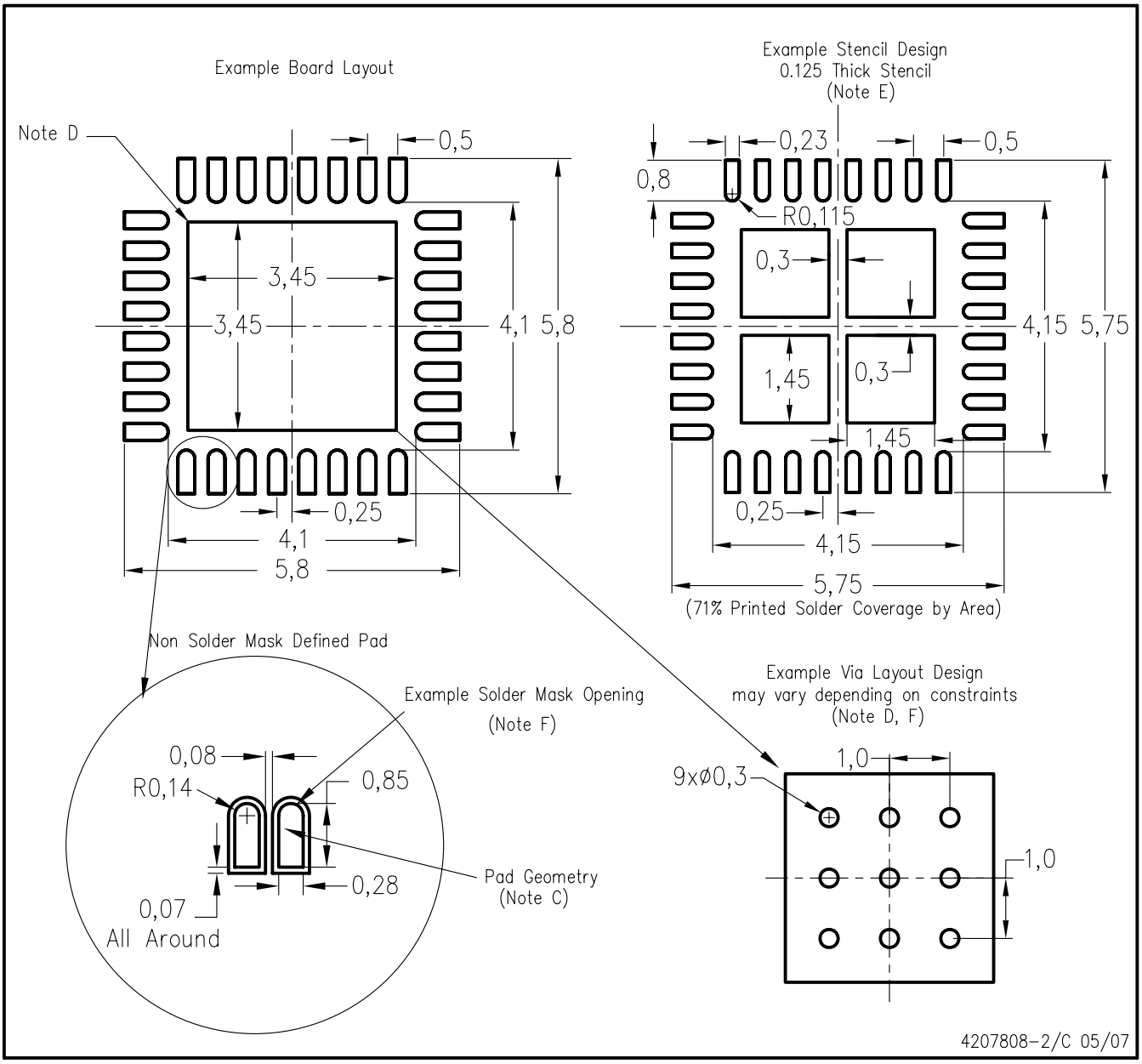


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RHB (S–PQFP–N32)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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