Freescale Semiconductor
Data Sheet: Technical Data

Document Number: DSP56720
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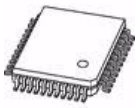
DSP56720 / DSP56721



DSP56720
144-Pin LQFP
20 mm x 20 mm
0.5 mm pitch

DSP56721
80-Pin LQFP
14 mm x 14 mm
0.65 mm pitch

144-Pin LQFP
20 mm x 20 mm
0.5 mm pitch

Symphony™ DSP56720 / DSP56721 Multi-Core Audio Processors

The Symphony DSP56720/DSP56721 Multi-Core Audio Processors are part of the DSP5672x family of programmable CMOS DSPs, designed using multiple DSP56300 24-bit cores.

The DSP56720/DSP56721 devices are intended for automotive, consumer, and professional audio applications that require high performance for audio processing. In addition, the DSP56720 is ideally suited for applications that need the capability to expand memory off-chip or to interface to external parallel peripherals. Potential applications include A/V receivers, HD-DVD and Blu-Ray players, car audio/amplifiers, and professional recording equipment.

The DSP56720/DSP56721 devices excel at audio processing for automotive and consumer audio applications requiring high MIPs. Higher MIPs and memory requirements are driven by the new high-definition audio standards (Dolby Digital+, Dolby TrueHD, DTS-HD, for example) and the desire to process multiple audio streams.

In addition, DSP56720/DSP56721 devices are optimal for the professional audio market requiring audio recording, signal processing, and digital audio synthesis.

The DSP56720/DSP56721 processors provide a wealth of on-chip audio processing functions, via a plug and play software architecture system that supports audio decoding algorithms, various equalization algorithms, compression, signal generator, tone control, fade/balance, level meter/spectrum analyzer, among others. The DSP56720/DSP56721 devices also support various matrix decoders and sound field processing algorithms.

With two DSP56300 cores, a single DSP56720 or DSP56721 device can replace dual-DSP designs, saving costs while meeting high MIPs requirements. Legacy peripherals from the previous DSP5636x/7x families are included, as well as a variety of new modules. Included among the new modules are an Asynchronous Sample Rate Converter (ASRC), Inter-Core Communication (ICC), an External Memory Controller (EMC) to support SDRAM, and a Sony/Philips Digital Interface (S/PDIF).

Ordering Information

Device	Device Marking or Operating Temperature Range	LQFP Package
DSP56720	DSPA56720AG	20 mm x 20 mm
	DSPB56720AG	20 mm x 20 mm
DSP56720	DSPA56721AG	20 mm x 20 mm
	DSPB56721AG	20 mm x 20 mm
	DSPA56721AF	14 mm x 14 mm
	DSPB56721AF	14 mm x 14 mm

The DSP56720/DSP56721 offer 200 million instructions per second (MIPs) per core using an internal 200 MHz clock.

The DSP56720/DSP56721 are high density CMOS devices with 3.3 V inputs and outputs.

The DSP56720 device is slightly different than the DSP56721 device—the DSP56720 includes an external memory interface while the DSP56721 device does not. The DSP56720 block diagram is shown in Figure 1; the DSP56721 block diagram is shown in Figure 2.

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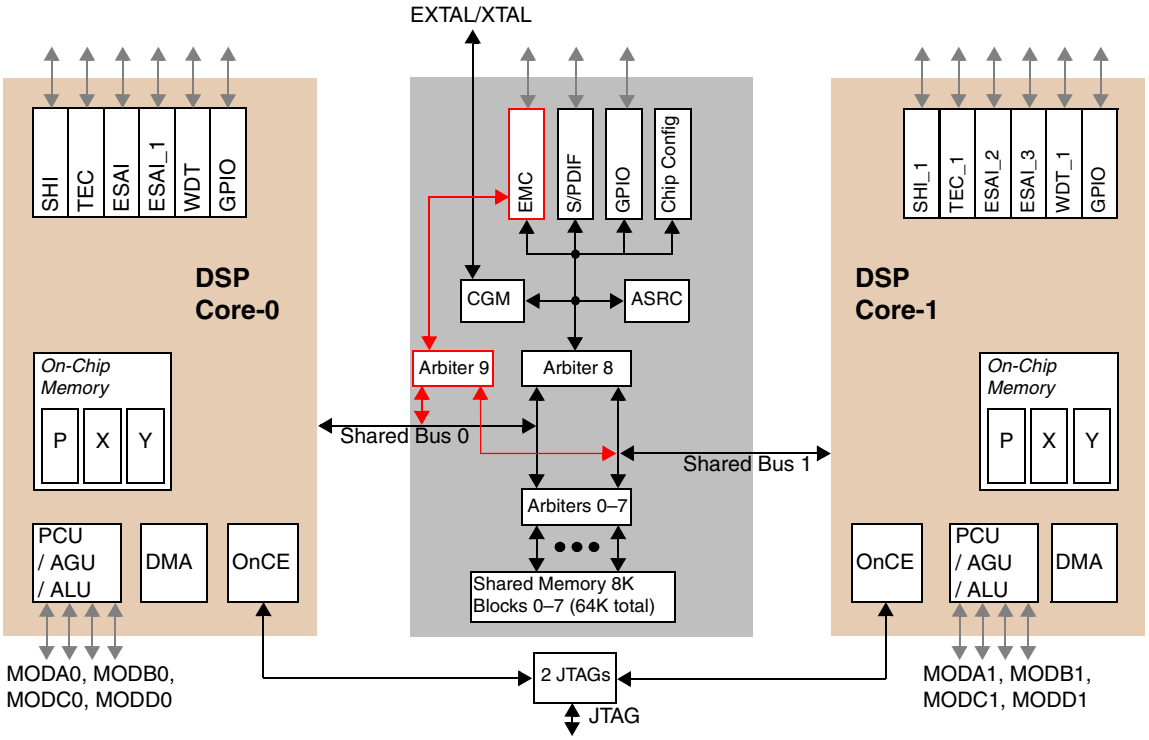


Figure 1. DSP56720 Block Diagram

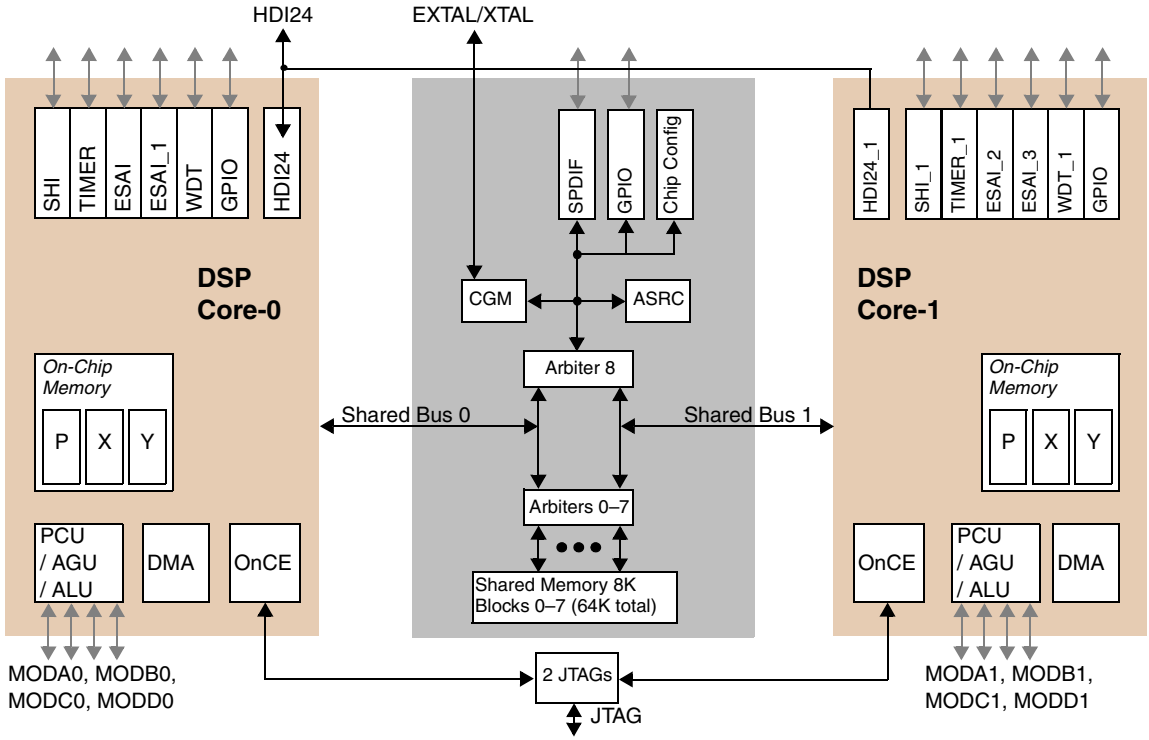


Figure 2. DSP56721 Block Diagram

1 Pin Assignments

DSP56720 devices are available in one package type; DSP56721 devices are available in two package types. For the pin assignments of a specific device in a specific package, please see sections 1.2–1.1.

Table 1. Pin Assignments by Package

Device	Package	See
DSP56720	144-pin plastic LQFP	Figure 3 on page 5
DSP56721	80-pin plastic LQFP	Figure 4 on page 6
	144-pin plastic LQFP	Figure 5 on page 7

For more detailed information about signals, refer to the *DSP56720/DSP56721 Reference Manual* (DSP56720RM).

1.1 Pinout for DSP56720 144-Pin Plastic LQFP Package

For the pinout of the DSP56720 144-pin plastic LQFP package, see Figure 3.

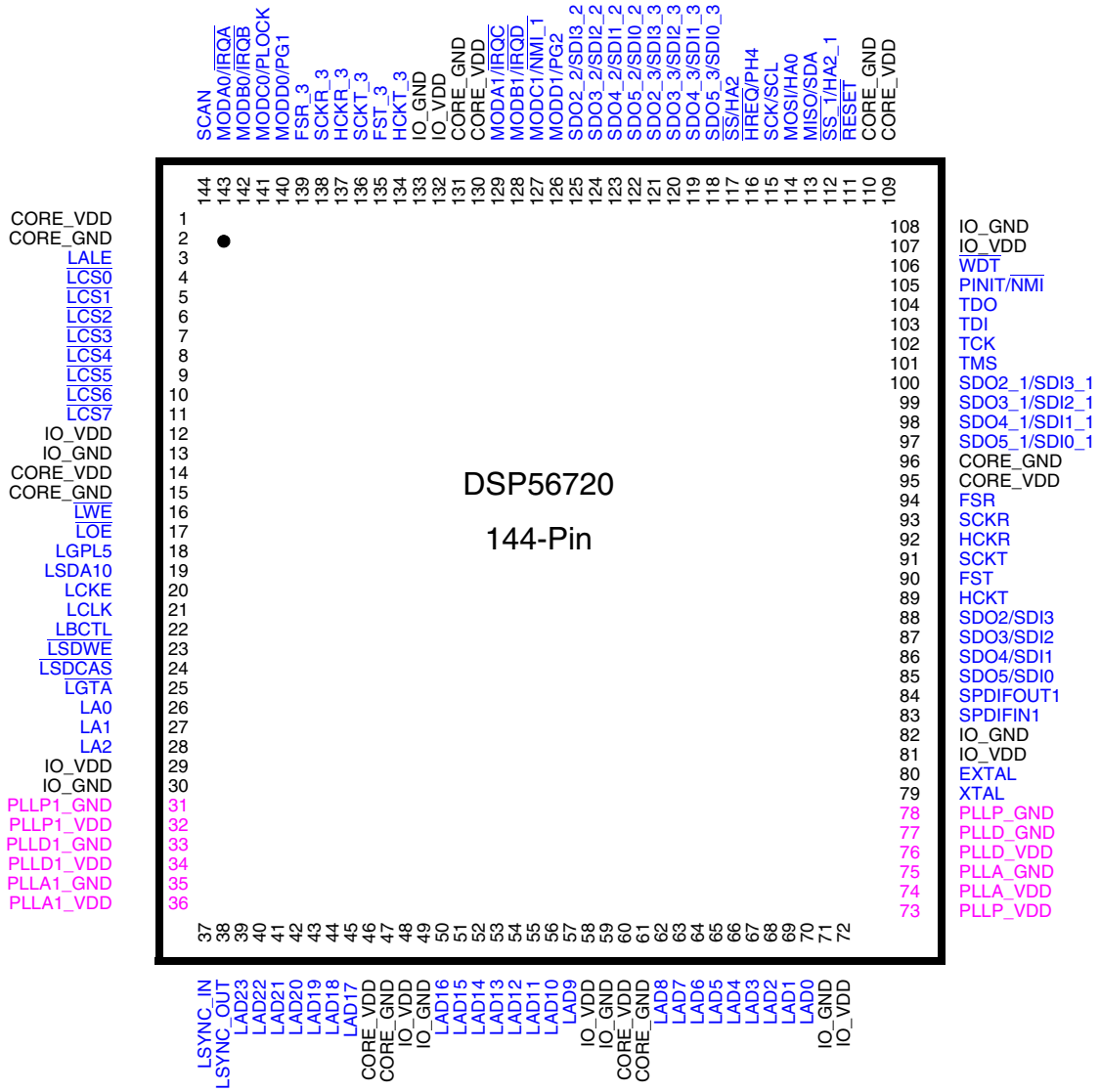


Figure 3. DSP56720 144-Pin Package Pinout

1.2 Pinout for DSP56721 80-Pin Plastic LQFP Package

For the pinout of the DSP56721 80-pin plastic LQFP package, see Figure 4.

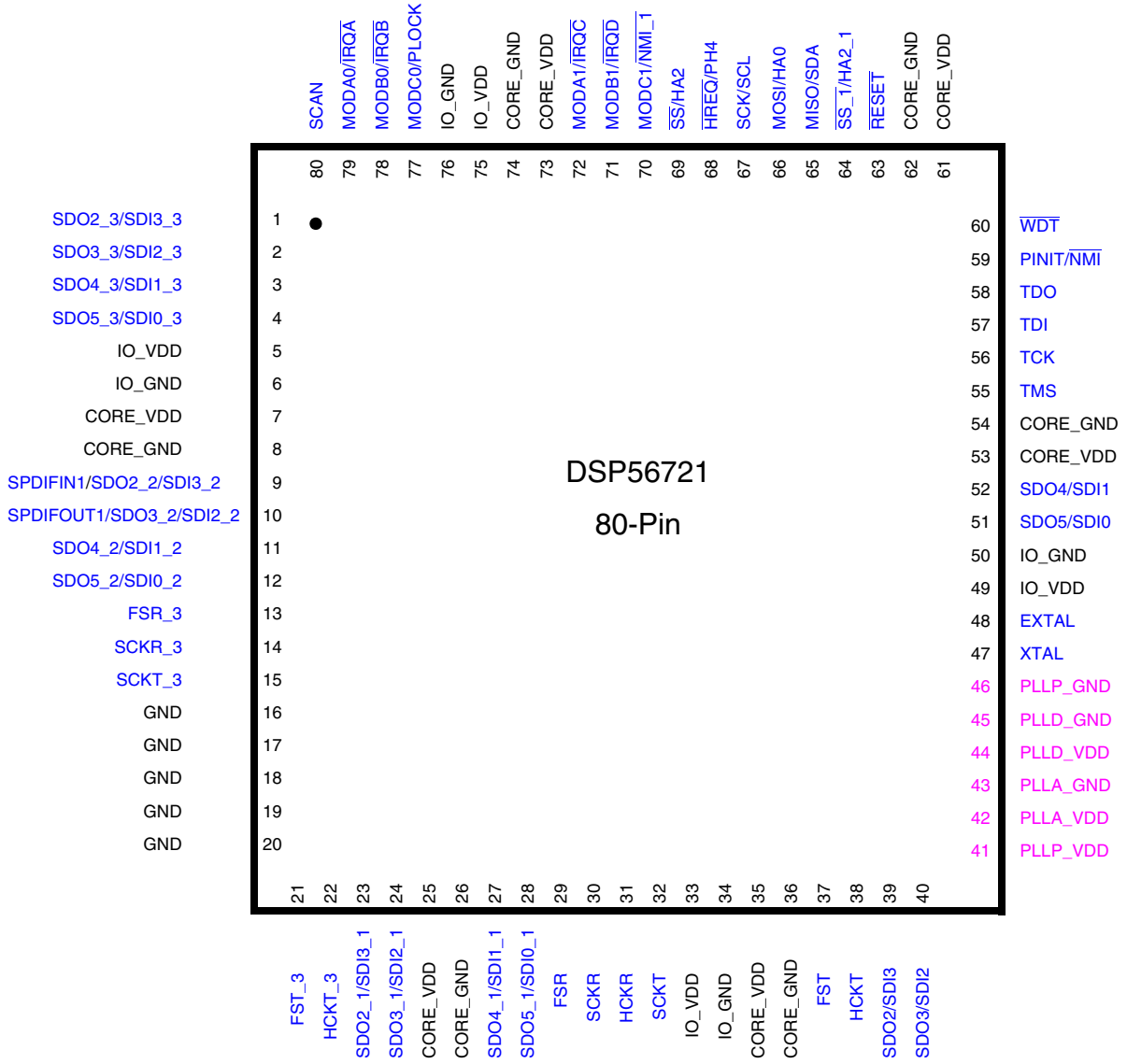


Figure 4. DSP56721 80-Pin Package

1.3 Pinout for DSP56721 144-Pin Plastic LQFP Package

For the pinout of the DSP56721 144-pin plastic LQFP package, see Figure 5.

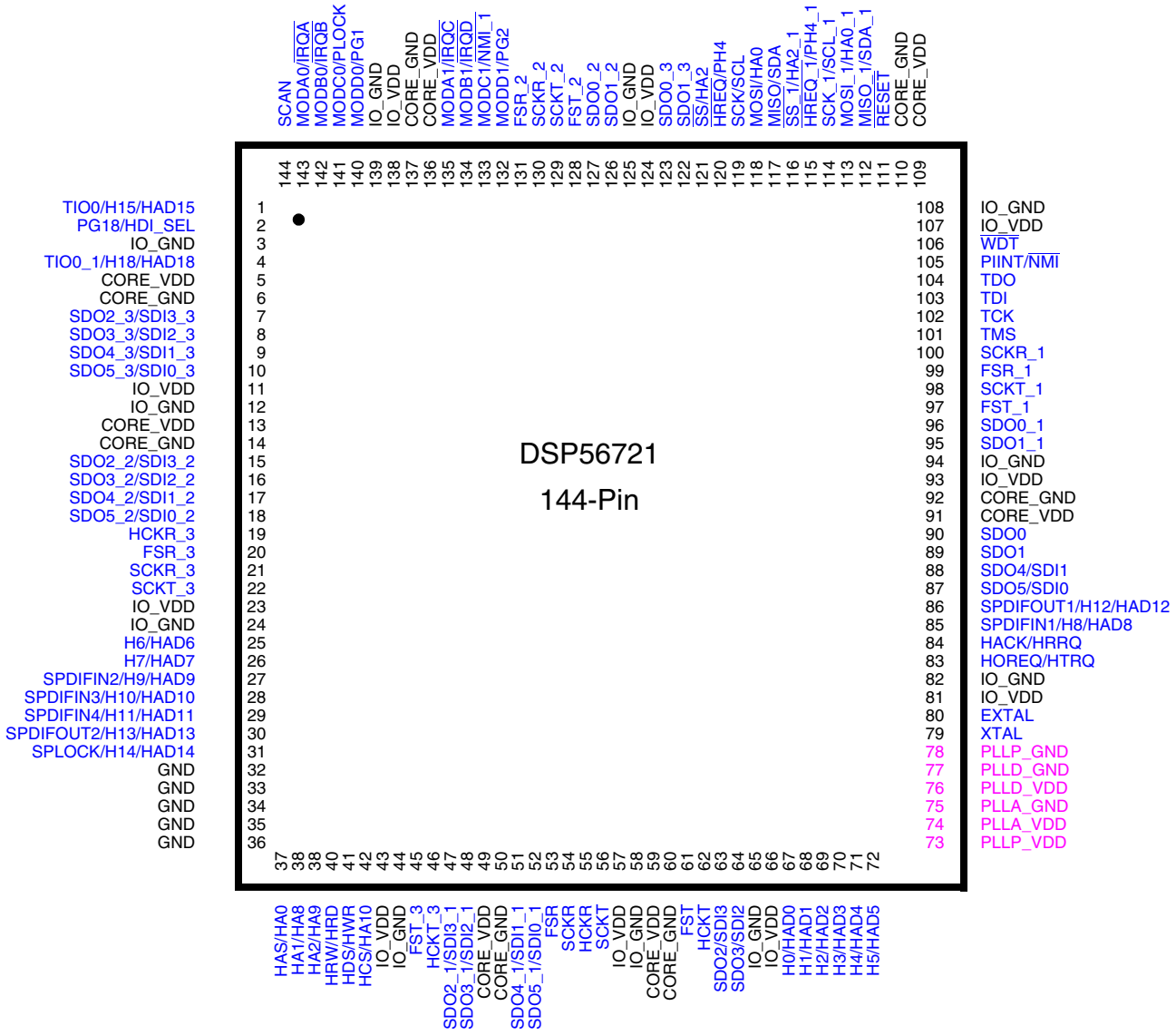


Figure 5. DSP56721 144-Pin Package Pinout

1.4 Pin Multiplexing

Many pins are multiplexed. For more about pin multiplexing, refer to the *DSP56720/DSP56721 Reference Manual* (DSP56720RM).

2 Electrical Characteristics

For electrical characteristics, see Table 2.

Table 2. Electrical Characteristics

For	See
Section 2.1, “Chip-Level Conditions”	on page 8
Section 2.2, “Module-Level Specifications”	on page 17

2.1 Chip-Level Conditions

For a summary of chip-level conditions in this section, see Table 3.

Table 3. Chip-Level Conditions

For	See
Section 2.1.1, “Maximum Ratings”	on page 8
Section 2.1.2, “Thermal Characteristics”	on page 10
Section 2.1.3, “Power Requirements”	on page 10
Section 2.1.4, “DC Electrical Characteristics”	on page 11
Section 2.1.5, “AC Electrical Characteristics”	on page 12
Section 2.1.6, “Internal Clocks”	on page 12
Section 2.1.7, “External Clock Operation”	on page 13
Section 2.1.8, “Reset, Stop, Mode Select, and Interrupt Timing”	on page 14

2.1.1 Maximum Ratings

For maximum ratings, see Table 4.

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields. However, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability of operation is enhanced if unused inputs are pulled to an appropriate logic voltage level (for example, either GND or V_{DD}). The suggested value for a pull-up or pull-down resistor is 4.7 kΩ.

NOTE

In the calculation of timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a “maximum” value for a specification will never occur in the same device that has a “minimum” value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 4. Maximum Ratings

Rating[1]	Symbol	Value[1, 2]	Unit
Supply Voltage	V_{CORE_VDD}, V_{PLLD_VDD}	-0.3 to + 1.26	V
	V_{PLLP_VDD}, V_{IO_VDD}, V_{PLLA_VDD},	-0.3 to + 4.0	V
Maximum CORE_VDD power supply ramp time[4]	Tr	10	ms
Input Voltage per pin excluding VDD and GND	V_{IN}	GND -0.3 to 5.5V	V
Current drain per pin excluding V_{DD} and GND (Except for pads listed below)	I	12	mA
LSYNC_OUT	I_{lsync_out}	16	mA
LCLK	I_{lclk}	16	mA
LALE	I_{ale}	16	mA
TDO	I_{JTAG}	24	mA
Operating temperature range[3]	T_J	-40 to +125	°C
Storage temperature	T_{STG}	-65 to +150	°C
ESD protected voltage (Human Body Model)	–	2000	V
ESD protected voltage (Charged Device) • All pins • Corner pins	–	 500 750	V

Notes:
1. GND = 0 V, T_J = -40°C to 125°C, CL = 50pF
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the maximum rating may affect device reliability or cause permanent damage to the device.
3. Operating temperature qualified for consumer applications. $T_J = T_A + q_{JA}$ x Power. Variables used were Core Current = 900mA, I/O Current = 200mA, Core Voltage = 1.1 V, I/O Voltage = 3.6 V, T_A = 105°C.
4. If the power supply ramp to full supply time is longer than 10 ms, the POR circuitry will not operate correctly, causing erroneous operation.

2.1.2 Thermal Characteristics

For thermal characteristics, see Table 5.

Table 5. Thermal Characteristics

Characteristic	Board Type	Symbol	LQFP Values	Unit
Natural Convection, Junction-to-ambient thermal resistance[1,2]	Single layer board (1s)	$R_{\theta JA}$ or θ_{JA}	57 for 80 QFP 49 for 144 QFP	°C/W
	Four layer board (2s2p)		44 for 80 QFP 40 for 144 QFP	°C/W
Junction-to-case thermal resistance[3]	–	$R_{\theta JC}$ or θ_{JC}	10 for 80 QFP 9 for 144 QFP	°C/W

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

2.1.3 Power Requirements

To prevent high current conditions due to possible improper sequencing of the power supplies, use an external Schottky diode as shown in Figure 6, connected between the DSP56720/DSP56721 IO_VDD and Core_VDD power pins.

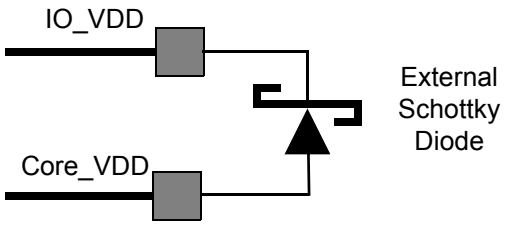


Figure 6. Prevent High Current Conditions by Using External Schottky Diode

If an external Schottky diode is not used (to prevent a high current condition at power-up), then IO_VDD must be applied ahead of Core_VDD, as shown in Figure 7.

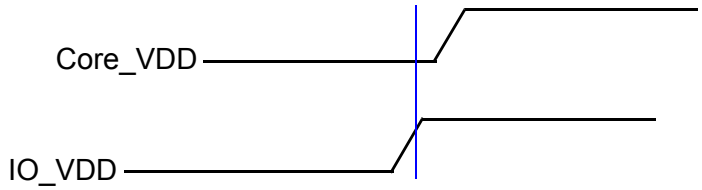


Figure 7. Prevent High Current Conditions by Applying IO_VDD Before Core_VDD

For correct operation of the internal power-on reset logic, the Core_VDD ramp rate (Tr) to full supply must be less than 10 ms, as shown in Figure 8.

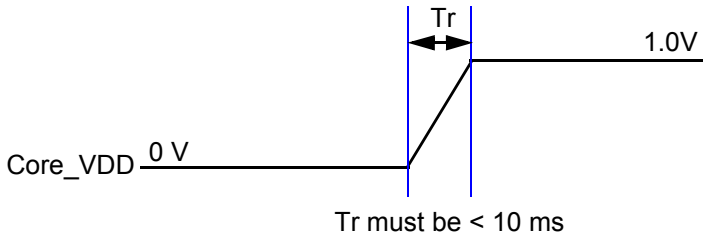


Figure 8. Ensure Correct Operation of Power-On Reset with Fast Ramp of Core_VDD

2.1.4 DC Electrical Characteristics

For DC electrical characteristics, see Table 6.

Table 6. DC Electrical Characteristics

Characteristics	Symbol	Min	Typ	Max	Unit
Supply voltages • Core (Core_VDD) • PLL (PLLD_VDD, PLLD1_VDD)	V_{DD}	0.9	1.0	1.1	V
Supply voltages • I/O (IO_VDD) • PLL (PLLP_VDD, PLLP1_VDD) • PLL (PLLA_VDD, PLLA1_VDD)	V_{DDIO}	3.14	3.3	3.46	V
Input high voltage	V_{IH}	2.0	–	V_{IO_VDD+2V}	V
Note: To avoid a high current condition and possible system damage, all 3.3 volt supplies must rise before the 1.0 volt supplies rise.					
Input low voltage	V_{IL}	-0.3	–	0.8	V
Input leakage current	I_{IN}	–	–	± 84	μA
Clock pin Input Capacitance (EXTAL)	C_{IN}		18		pF
High impedance (off-state) input current (@ 3.3 V or 0 V)	I_{TSI}	-10	–	10	μA
Output high voltage I_{OH} = -12 mA LSYNC_OUT, LALE, LCLK Pins I_{OH} = -16 mA, TDO Pin I_{OH} = -24 mA	V_{OH}	2.4	–	–	V
Output low voltage I_{OL} = 12 mA LSYNC_OUT, LALE, LCLK Pins I_{OL} = 16 mA, TDO Pins I_{OL} = 24 mA	V_{OL}	–	–	0.4	V

Table 6. DC Electrical Characteristics (Continued)

Characteristics	Symbol	Min	Typ	Max	Unit
Internal supply current[1] (core only) at internal clock of 200 MHz					
• In Normal mode	I_{CCI}	–	190	780	mA
• In Wait mode	I_{CCW}	–	90	680	mA
• In Stop mode[2]	I_{CCS}	–	50	640	mA
Input capacitance	C_{IN}	–	–	10	pF

Notes:
1. The Current Consumption section provides a formula to compute the estimated current requirements in Normal mode. In order to obtain these results, all inputs must be terminated (i.e., not allowed to float). Measurements are based on synthetic intensive DSP benchmarks. The power consumption numbers in this specification are 90% of the measured results of this benchmark. This reflects typical DSP applications. Typical internal supply current is measured with V_{CORE_VDD} = 1.0V, V_{DD_IO} = 3.3V at T_J = 25°C. Maximum internal supply current is measured with V_{CORE_VDD} = 1.10V, $V_{IO\_VDD)}$ = 3.6V at T_J = 125°C.
2. In order to obtain these results, all inputs, which are not disconnected at Stop mode, must be terminated (i.e., not allowed to float).

2.1.5 AC Electrical Characteristics

The timing waveforms shown in the AC electrical characteristics section are tested with a V_{IL} maximum of 0.8 V and a V_{IH} minimum of 2.0 V for all pins. AC timing specifications, which are referenced to a device input signal, are measured in production with respect to the 50% point of the respective input signal's transition. DSP56720/DSP56721 output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 0.4 V and 2.4 V, respectively.

2.1.6 Internal Clocks

Internal clock characteristics are listed in Table 7.

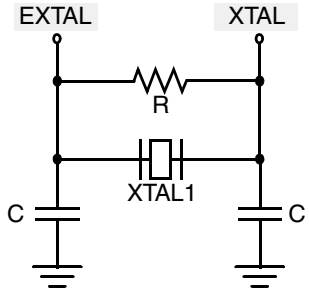
Table 7. Internal Clocks

No.	Characteristics	Symbol	Min	Typ	Max	Unit	Condition
1	Comparison Frequency	Fref	2	–	8	MHz	Fref = Fin/NR
2	Input Clock Frequency	Fin	Max = 200 MHz				
3	PLL VCO Frequency	Fvco	200	–	400	MHz	Fvco = (Fin * NF)/NR
4	Output Clock Frequency[1] • with PLL enabled • with PLL disabled	Fout	 25 –	–	 200 200	MHz	 Fout= Fvco/NO Fout = Fin
5	Duty Cycle	–	40	50	60	%	Fvco= 200 MHz – 400 MHz

Notes:
Fin = External frequency, NF = Multiplication Factor, NR = Predivision Factor, NO = Output Divider

2.1.7 External Clock Operation

The DSP56720/DSP56721 system clock is derived from the on-chip oscillator or is externally supplied. To use the on-chip oscillator, connect a crystal and associated resistor/capacitor components to EXTAL and XTAL; see the example in Figure 9.



Suggested component values:

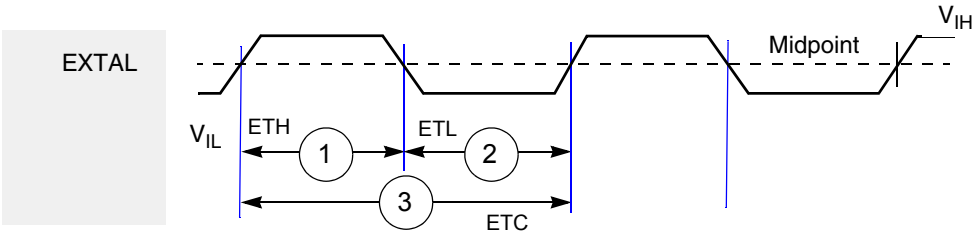
Fosc = 24.576 MHz
R = 1 M ±10%
C (EXTAL)= 18 pF
C (XTAL) = 18 pF

Calculations are for a 5 – 30 MHz crystal with the following parameters:

- Shunt capacitance (C_0) of 10 pF – 12 pF
- Series resistance 40 Ohm
- Drive level of 10 μW

Figure 9. Using the On-Chip Oscillator

If the DSP56720/DSP56721 system clock is an externally supplied square wave voltage source, it is connected to EXTAL (Figure 10). When the external square wave source is connected to EXTAL, the XTAL pin is not used.



Note: The midpoint is 0.5 (V_{IH} + V_{IL}).

Figure 10. External Clock Timing

Table 8. Clock Operation

No.	Characteristics	Symbol	Min	Max	Units
1	EXTAL input high [1] (40% to 60% duty cycle) • Crystal oscillator • Square wave input	Eth	 16.67 2.5	 100 inf	ns

Table 8. Clock Operation (Continued)

No.	Characteristics	Symbol	Min	Max	Units
2	EXTAL input low[1] (40% to 60% duty cycle) • Crystal oscillator • Square wave input	Etl	 16.67 2.5	 100 inf	ns
3	EXTAL cycle time • With PLL disabled • With PLL enabled	Etc	 5 33.3	 inf 500	ns
4	Instruction cycle time • With PLL disabled • With PLL enabled	Tc	 5.00 5.00	 inf 5120	ns

Notes:
1. Measured at 50% of the input transition.
2. The indicated duty cycle is for the specified maximum frequency for which a part is rated. The minimum clock high or low time required for correct operation, however, remains the same at lower operating frequencies; therefore, when a lower clock frequency is used, the signal symmetry may vary from the specified duty cycle as long as the minimum high time and low time requirements are met.
3. A valid clock signal must be applied to the EXTAL pin *within 3 ms* of the DSP56720/DSP56721 being powered up.

2.1.8 Reset, Stop, Mode Select, and Interrupt Timing

For reset, stop, mode select, and interrupt timing, see Table 9.

Table 9. Reset, Stop, Mode Select, and Interrupt Timing Parameters

No.	Characteristics	Expression	Min	Max	Unit
10	Delay from $\overline{\text{RESET}}$ assertion to all pins at reset value[3]	–	–	11	ns
11	Required $\overline{\text{RESET}}$ duration[4] • Power on, external clock generator, PLL disabled • Power on, external clock generator, PLL enabled	 $2 \times T_C$ $2 \times T_C$	 10 10	 – –	 ns ns
13	Syn reset deassert delay time • Minimum • Maximum (PLL enabled)	 $2 \times T_C$ $(2 \times T_C) + T_{LOCK}$	 10 200	 – –	 ns us
14	Mode select setup time	–	10.0	–	ns
15	Mode select hold time	–	10.0	–	ns
16	Minimum edge-triggered interrupt request assertion width	–	4	–	ns
17	Minimum edge-triggered interrupt request deassertion width	–	4	–	ns
18	Delay from interrupt trigger to interrupt code execution	$10 \times T_{C+4}$	54	–	ns

Table 9. Reset, Stop, Mode Select, and Interrupt Timing Parameters

No.	Characteristics	Expression	Min	Max	Unit
19	Duration of level sensitive $\overline{\text{IRQA}}$ assertion to ensure interrupt service (when exiting Stop)[1, 2, 3]				
	• PLL is active during Stop and Stop delay is enabled (OMR Bit 6 = 0)	$(128K \times T_{C)}$	655	–	µs
	• PLL is active during Stop and Stop delay is not enabled (OMR Bit 6 = 1)	$25 \times T_C$	125	–	ns
	• PLL is not active during Stop and Stop delay is enabled (OMR Bit 6 = 0)	$(128K \times T_C) + T_{LOCK}$	855	–	µs
	• PLL is not active during Stop and Stop delay is not enabled (OMR Bit 6 = 1)	$(25 \times T_C) + T_{LOCK}$	200	–	µs
20	• Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to general-purpose transfer output valid caused by first interrupt instruction execution[1]	$10 \times T_C + 3.8$	–	53.8	ns
21	Interrupt Requests Rate[1]				
	• ESAI, ESAI_1, ESAI_2, ESAI_3, SHI, SHI_1, Timer, Timer_1	$12 \times T_C$	–	60.0	ns
	• DMA	$8 \times T_C$	–	40.0	ns
	• $\overline{\text{IRQ}}$, $\overline{\text{NMI}}$ (edge trigger)	$8 \times T_C$	–	40.0	ns
	• $\overline{\text{IRQ}}$ (level trigger)	$12 \times T_C$	–	60.0	ns
22	DMA Requests Rate				
	• Data read from ESAI, ESAI_1, ESAI_2, ESAI_3, SHI, SHI_1	$6 \times T_C$	–	30.0	ns
	• Data write to ESAI, ESAI_1, ESAI_2, ESAI_3, SHI, SHI_1	$7 \times T_C$	–	35.0	ns
	• Timer, Timer_1	$2 \times T_C$	–	10.0	ns
	• $\overline{\text{IRQ}}$, $\overline{\text{NMI}}$ (edge trigger)	$3 \times T_C$	–	15.0	ns

Notes:

1. When using fast interrupts and when $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, and $\overline{\text{IRQD}}$ are defined as level-sensitive, timings 19 through 21 apply to prevent multiple interrupt service. To avoid these timing restrictions, the Edge-triggered mode is recommended when using fast interrupts. Long interrupts are recommended when using Level-sensitive mode.
2. For PLL disable, if using an external clock (PCTL Bit 13 = 1), no stabilization delay is required and recovery time will be defined by the OMR Bit 6 settings.
   For PLL enable, (if bit 12 of the PCTL register is 0), the PLL is shut down during Stop. Recovering from Stop requires the PLL to get locked. The PLL lock procedure duration, PLL Lock Cycles (PLC), may be in the range of 200 µs.
3. Periodically sampled and not 100% tested.
4. $\overline{\text{RESET}}$ duration is measured during the time in which $\overline{\text{RESET}}$ is asserted, V_{DD} is valid, and the EXTAL input is active and valid. When V_{DD} is valid, but the other "required $\overline{\text{RESET}}$ duration" conditions (as specified above) have not been yet met, the device circuitry will be in an uninitialized state that can result in significant power consumption and heat-up. Designs should minimize this state to the shortest possible duration.

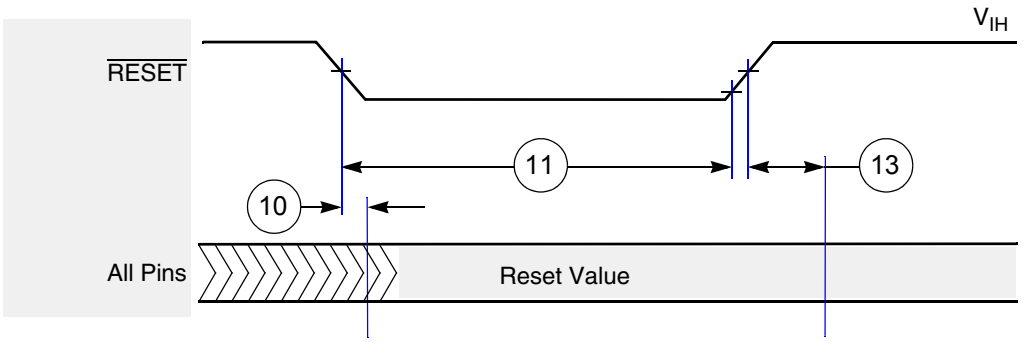
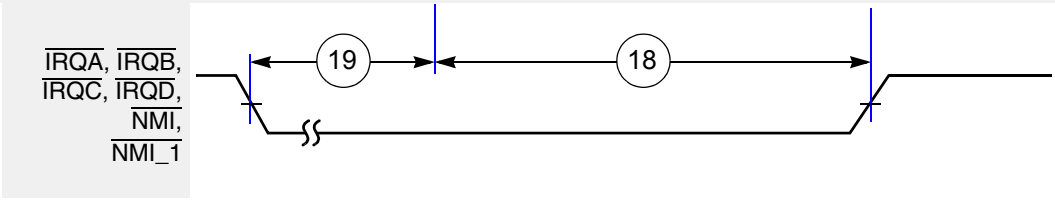


Figure 11. Reset Timing Diagram

a) First Interrupt Instruction Execution



b) General Purpose I/O

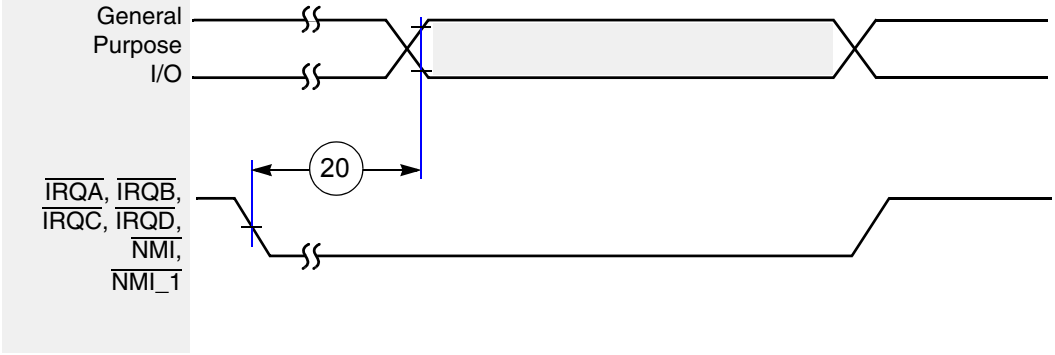


Figure 12. External Fast Interrupt Timing Diagram

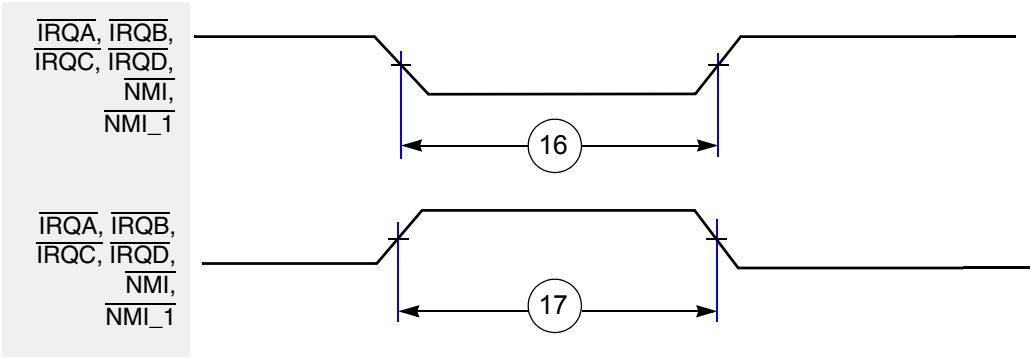


Figure 13. External Interrupt Timing Diagram (Negative Edge-Triggered)

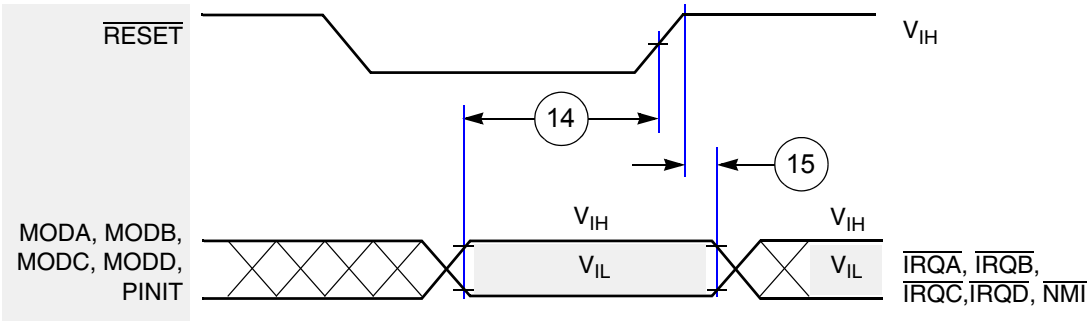


Figure 14. MODE Select Set-Up and Hold Timing Diagram

2.2 Module-Level Specifications

For a summary of the module-level specifications in this section, see Table 10.

Table 10. Module-Level Specifications

For	See
Section 2.2.1, “Serial Host Interface (SHI) SPI Protocol Timing”	on page 18
Section 2.2.2, “Serial Host Interface (SHI) I^2C Protocol Timing”	on page 24
Section 2.2.3, “Programming the SHI I^2C Serial Clock”	on page 26
Section 2.2.4, “Enhanced Serial Audio Interface (ESAI) Timing”	on page 27
Section 2.2.5, “Timer Timing”	on page 32
Section 2.2.6, “GPIO Timing”	on page 32
Section 2.2.7, “JTAG Timing”	on page 33
Section 2.2.8, “Watchdog Timer Timing”	on page 35
Section 2.2.9, “Host Data Interface (HDI24) Timing”	on page 35
Section 2.2.10, “S/PDIF Timing”	on page 42
Section 2.2.11, “EMC Timing (DSP56720 only)”	on page 43

2.2.1 Serial Host Interface (SHI) SPI Protocol Timing

See Table 11 for SHI SPI protocol timing parameters and Figure 15, Figure 16, Figure 17, and Figure 18 for timing diagrams.

Table 11. Serial Host Interface SPI Protocol Timing Parameters

No.	Characteristics[1,3,4]	Mode	Filter Mode	Expression	Min	Max	Unit
23	Minimum serial clock cycle = t_{SPICC}(min)	Master/Slave	Bypassed	10 x T_C + 9	59.0	–	ns
			Very Narrow	10 x T_C + 9	59.0	–	ns
			Narrow	10 x T_C + 133	183.0	–	ns
			Wide	10 x T_C + 333	373.0	–	ns
XX	Tolerable Spike width on data or clock in	–	Bypassed	–	–	0	ns
			Very Narrow	–	–	10	ns
			Narrow	–	–	50	ns
			Wide	–	–	100	ns
24	Serial clock high period	Master	Bypassed	0.5 x (t_{SPICC} -10)	33.0	–	ns
			Very Narrow	0.5 x (t_{SPICC} -10)	33.0	–	ns
			Narrow	0.5 x (t_{SPICC} -10)	86.0	–	ns
			Wide	0.5 x (t_{SPICC} -10)	121.5	–	ns
		Slave	Bypassed	2.5 x T_C + 12	22.5	–	ns
			Very Narrow	2.5 x T_C + 12	22.5	–	ns
			Narrow	2.5 x T_C + 102	114.5	–	ns
			Wide	2.5 x T_C + 189	201.5	–	ns
25	Serial clock low period	Master	Bypassed	0.5 x (t_{SPICC} -10)	33.0	–	ns
			Very Narrow	0.5 x (t_{SPICC} -10)	33.0	–	ns
			Narrow	0.5 x (t_{SPICC} -10)	86.0	–	ns
			Wide	0.5 x (t_{SPICC} -10)	121.5	–	ns
		Slave	Bypassed	2.5 x T_C + 12	22.5	–	ns
			Very Narrow	2.5 x T_C + 12	22.5	–	ns
			Narrow	2.5 x T_C + 102	114.5	–	ns
			Wide	2.5 x T_C + 189	201.5	–	ns
26	Serial clock rise/fall time	Master Slave	– –	– –	– –	– 5	ns ns

Table 11. Serial Host Interface SPI Protocol Timing Parameters (Continued)

No.	Characteristics[1,3,4]	Mode	Filter Mode	Expression	Min	Max	Unit
27	$\overline{SS}$ assertion to first SCK edge CPHA = 0	Slave	Bypassed	3.5 x TC+15	32.5	–	ns
			Very Narrow	3.5 x TC+5	22.5	–	ns
			Narrow	–	0	–	ns
			Wide	–	0	–	ns
	CPHA = 1	Slave	Bypassed	–	10	–	ns
			Very Narrow	–	0	–	ns
			Narrow	–	0	–	ns
			Wide	–	0	–	ns
28	Last SCK edge to $\overline{SS}$ not asserted	Slave	Bypassed	–	12	–	ns
			Very Narrow	–	22	–	ns
			Narrow	–	100	–	ns
			Wide	–	200	–	ns
29	Data input valid to SCK edge (data input set-up time)	Master /Slave	Bypassed	–	0	–	ns
			Very Narrow	–	0	–	ns
			Narrow	–	0	–	ns
			Wide	–	0	–	ns
30	SCK last sampling edge to data input not valid	Master /Slave	Bypassed	$2 \times T_C + 10$	10	–	ns
			Very Narrow	$2 \times T_C + 30$	40	–	ns
			Narrow	$2 \times T_C + 60$	70	–	ns
			Wide	–	100.0	–	ns
31	$\overline{SS}$ assertion to data out active	Slave	–	–	5	–	ns
32	$\overline{SS}$ deassertion to data high impedance[2]	Slave	–	–	–	9	ns
33	SCK edge to data out valid (data out delay time)	Master /Slave	Bypassed	–	–	46.2	ns
			Very Narrow	–	–	270	ns
			Narrow	–	–	376	ns
			Wide	–	–	521	ns
34	SCK edge to data out not valid (data out hold time)	Master /Slave	Bypassed	–	11.67	–	ns
			Very Narrow	–	15	–	ns
			Narrow	–	55	–	ns
			Wide	–	105	–	ns
35	$\overline{SS}$ assertion to data out valid (CPHA = 0)	Slave	–	–	–	14.0	ns

Table 11. Serial Host Interface SPI Protocol Timing Parameters (Continued)

No.	Characteristics[1,3,4]	Mode	Filter Mode	Expression	Min	Max	Unit
36	First SCK sampling edge to $\overline{\text{HREQ}}$ output deassertion	Slave	Bypassed	–	45	–	ns
			Very Narrow	–	55	–	ns
			Narrow	–	95	–	ns
			Wide	–	145	–	ns
37	Last SCK sampling edge to $\overline{\text{HREQ}}$ output not deasserted (CPHA = 1)	Slave	Bypassed	–	50.0	–	ns
			Very Narrow	–	60.0	–	ns
			Narrow	–	100.0	–	ns
			Wide	–	150.0	–	ns
38	$\overline{\text{SS}}$ deassertion to $\overline{\text{HREQ}}$ output not deasserted (CPHA = 0)	Slave	–	–	45.0	–	ns
39	$\overline{\text{SS}}$ deassertion pulse width (CPHA = 0)	Slave	–	$T_C + 6$	11.0	–	ns
40	$\overline{\text{HREQ}}$ in assertion to first SCK edge	Master	–	$0.5 \times T_{SPICC} + 3.0 \times T_C + 43$	96.0	–	ns
41	$\overline{\text{HREQ}}$ in deassertion to last SCK sampling edge ($\overline{\text{HREQ}}$ in set-up time) (CPHA = 1)	Master	–	–	0	–	ns
42	First SCK edge to $\overline{\text{HREQ}}$ in not asserted ($\overline{\text{HREQ}}$ in hold time)	Master	–	–	0	–	ns
43	$\overline{\text{HREQ}}$ assertion width	Master	–	$3.0 \times T_C$	15	–	ns

Notes:
1. V_{CORE_VDD} = 1.0± 0.10 V; T_J = -40°C to 125°C; C_L = 50 pF.
2. Periodically sampled, not 100% tested.
3. All times assume noise free inputs.
4. All times assume internal clock frequency of 200 MHz.
5. SHI_1 specs match those of SHI.

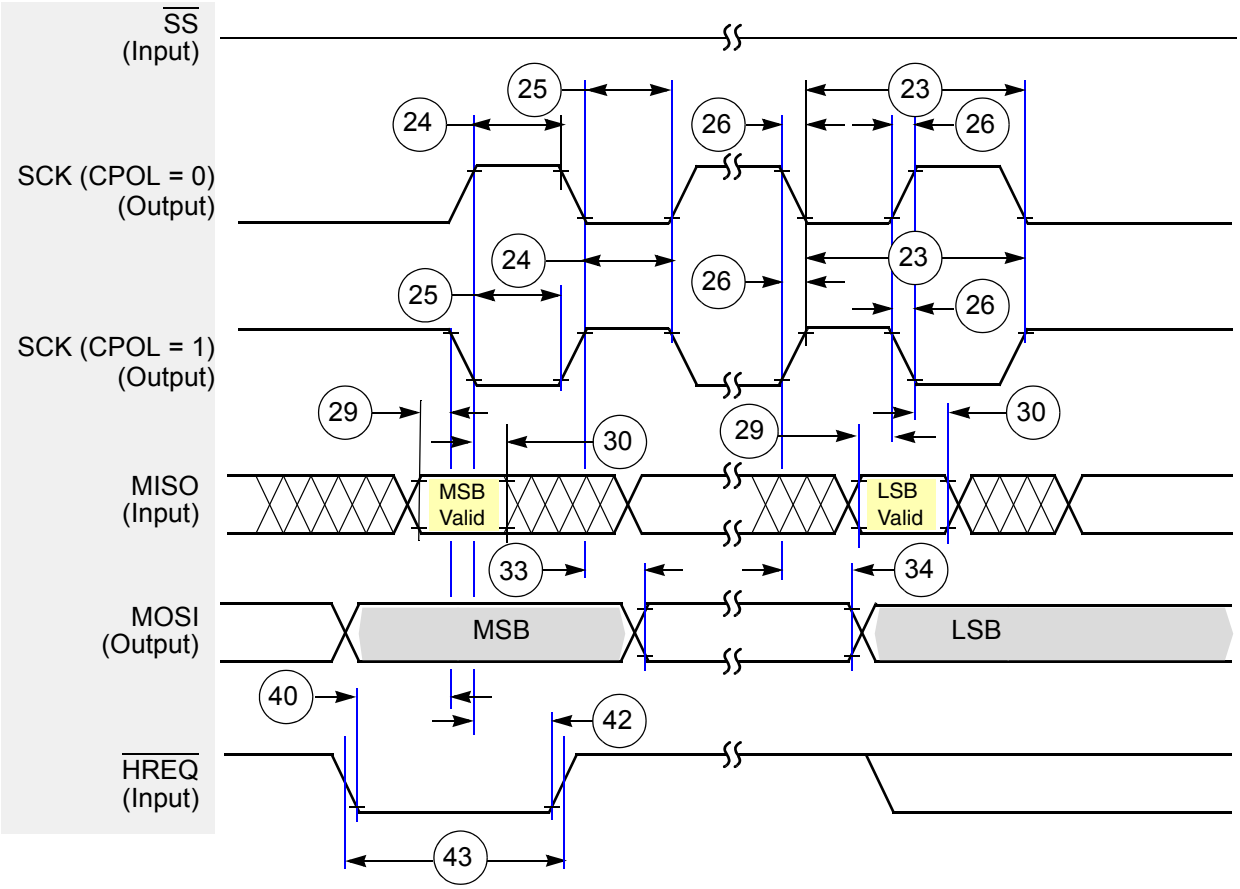


Figure 15. SPI Master Timing Diagram (CPHA = 0)

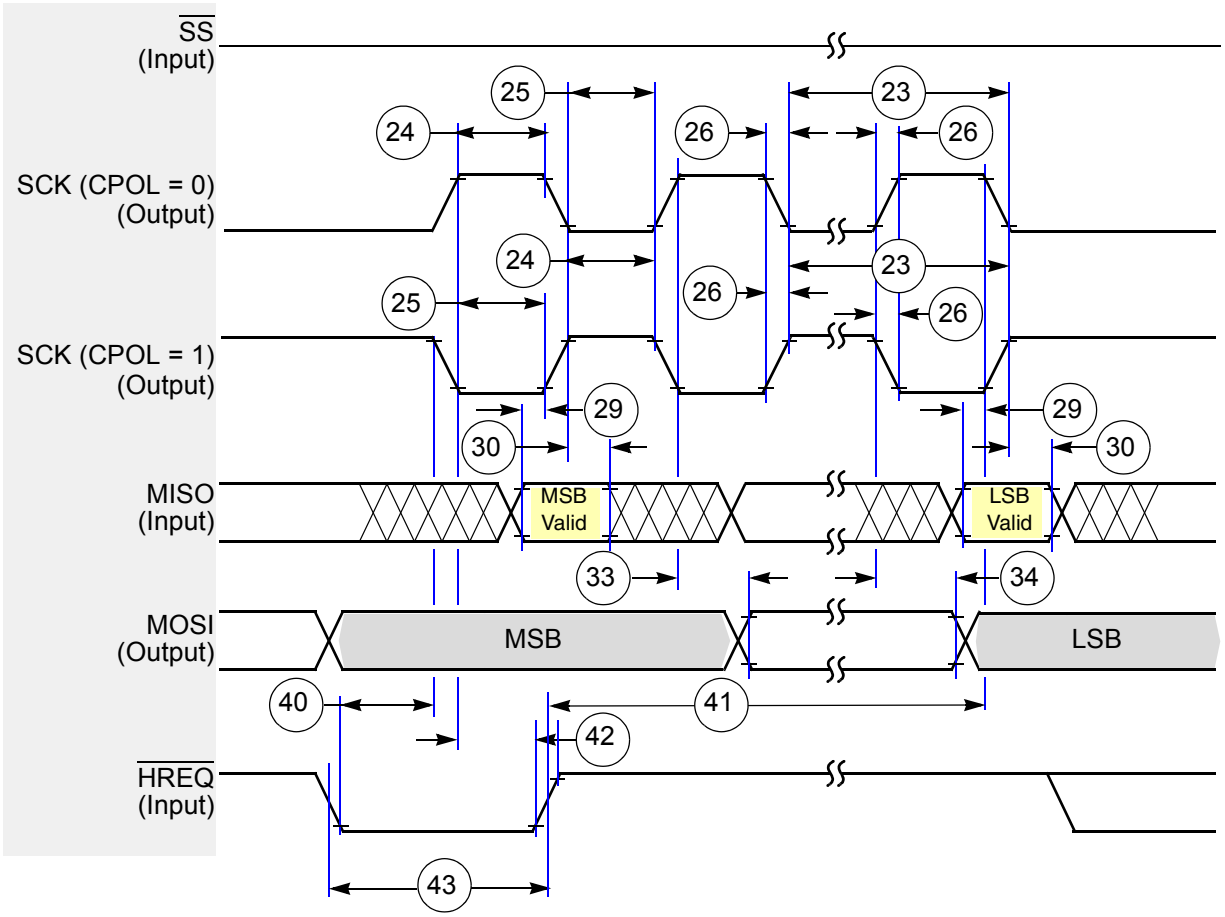


Figure 16. SPI Master Timing Diagram (CPHA = 1)

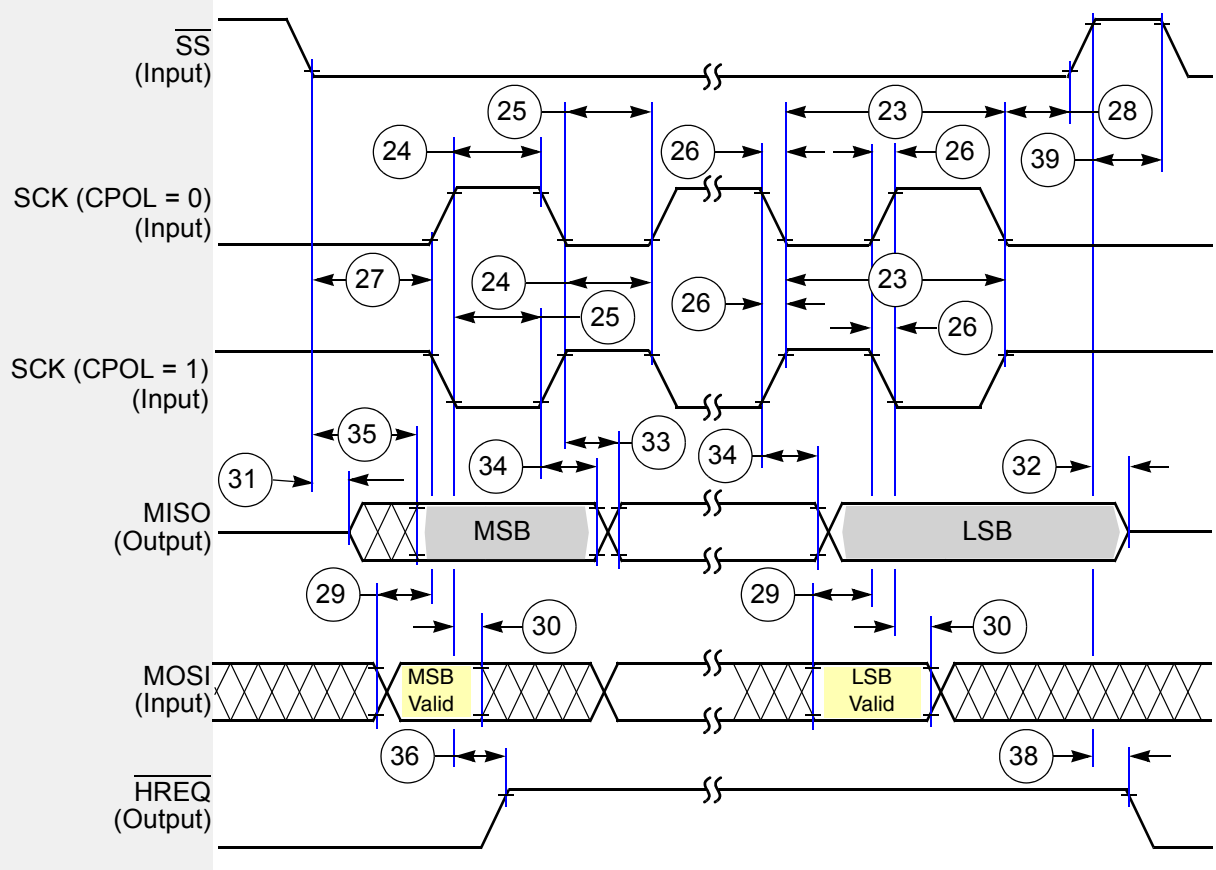


Figure 17. SPI Slave Timing Diagram (CPHA = 0)

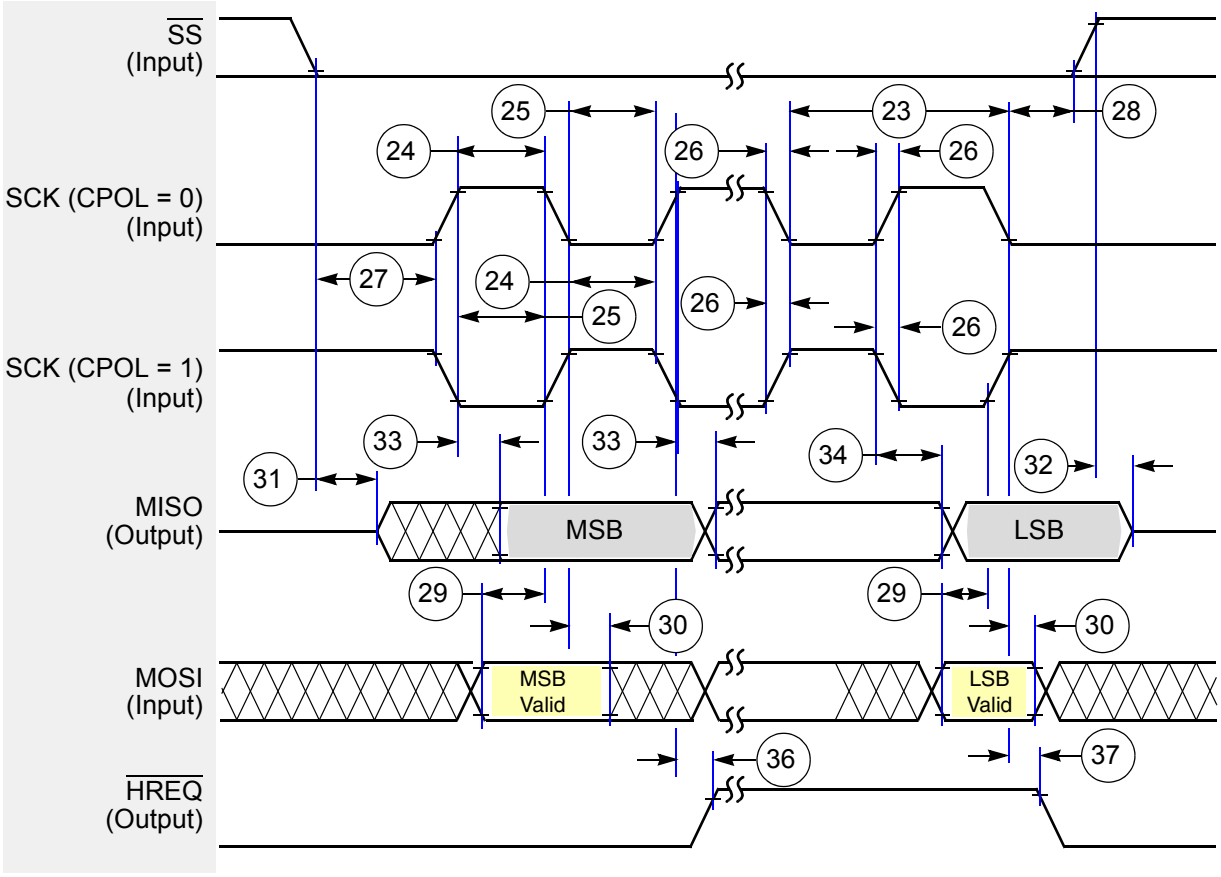


Figure 18. SPI Slave Timing Diagram (CPHA = 1)

2.2.2 Serial Host Interface (SHI) I²C Protocol Timing

See Table 12 for SHI I²C protocol timing parameters and Figure 19 for the timing diagram.

Table 12. SHI I²C Protocol Timing Parameters

Standard I²C							
No.	Characteristics[1,2,3,4,5]	Symbol/ Expression	Standard		Fast-Mode		Unit
			Min	Max	Min	Max	
	Tolerable Spike Width on SCL or SDA Filters Bypassed Very Narrow Filters enabled Narrow Filters enabled Wide Filters enabled.	–	 – – – –	 0 10 50 100	 – – – –	 0 10 50 100	 ns ns ns ns
44	SCL clock frequency	F_{SCL}	–	100	–	400	kHz
44	SCL clock cycle	T_{SCL}	10	–	2.5	–	µs
45	Bus free time	T_{BUF}	4.7	–	1.3	–	µs
46	Start condition set-up time	T_{SUSTA}	4.7	–	0.6	–	µs

Table 12. SHI I²C Protocol Timing Parameters (Continued)

Standard I²C							
No.	Characteristics[1,2,3,4,5]	Symbol/ Expression	Standard		Fast-Mode		Unit
			Min	Max	Min	Max	
47	Start condition hold time	$T_{HD;STA}$	4.0	–	0.6	–	µs
48	SCL low period	T_{LOW}	4.7	–	1.3	–	µs
49	SCL high period	T_{HIGH}	4.0	–	1.3	–	µs
50	SCL and SDA rise time	T_R	–	5.0	–	5.0	ns
51	SCL and SDA fall time	T_F	–	5.0	–	5.0	ns
52	Data set-up time	$T_{SU;DAT}$	250	–	100	–	ns
53	Data hold time	$T_{HD;DAT}$	0.0	–	0.0	0.9	µs
54	DSP clock frequency	F_{OSC}					
	• Filters bypassed		10.6	–	28.5	–	MHz
	• Very Narrow filters enabled		10.6	–	28.5	–	MHz
	• Narrow filters enabled		11.8	–	39.7	–	MHz
	• Wide filters enabled		13.1	–	61.0	–	MHz
55	SCL low to data out valid	$T_{VD;DAT}$	–	3.4	–	0.9	µs
56	Stop condition setup time	$T_{SU;STO}$	4.0	–	0.6	–	µs
57	$\overline{HREQ}$ in deassertion to last SCL edge ($\overline{HREQ}$ in set-up time)	$t_{SU;RQI}$	0.0	–	0.0	–	ns
58	First SCL sampling edge to $\overline{HREQ}$ output deassertion[2]	$T_{NG;RQO}$					
	• Filters bypassed	$4 \times T_C + 30$	–	50.0	–	50.0	ns
	• Very Narrow filters enabled	$4 \times T_C + 50$	–	70.0	–	70.0	ns
	• Narrow filters enabled	$4 \times T_C + 130$	–	250.0	–	150.0	ns
	• Wide filters enabled	$4 \times T_C + 230$	–	150.0	–	250.0	ns
59	Last SCL edge to $\overline{HREQ}$ output not deasserted[2]	$T_{AS;RQO}$					
	• Filters bypassed	$2 \times T_C + 30$	40	–	40	–	ns
	• Very Narrow filters enabled	$2 \times T_C + 40$	50	–	50	–	ns
	• Narrow filters enabled	$2 \times T_C + 80$	90	–	90	–	ns
	• Wide filters enabled	$2 \times T_C + 130$	140	–	140	–	ns
60	$\overline{HREQ}$ in assertion to first SCL edge	$T_{AS;RQI}$					
	• Filters bypassed		4327	–	927	–	ns
	• Very Narrow filters enabled		4317	–	917	–	ns
	• Narrow filters enabled		4282	–	877	–	ns
	• Wide filters enabled		4227	–	827	–	ns
61	First SCL edge to $\overline{HREQ}$ is not asserted ($\overline{HREQ}$ in hold time.)	$t_{HO;RQI}$	0.0	–	0.0	–	ns

Notes:
1. V_{CORE_VDD} = 1.00± 0.10 V; T_J = -40°C to 125°C; C_L = 50 pF.
2. Pull-up resistor: R_P(min) = 1.5K Ohms.
3. Capacitive load: C_b(max) = 50 pF.
4. All times assume noise free inputs.
5. All times assume internal clock frequency of 200 MHz.
6. SHI_1 specs match those of SHI.

2.2.3 Programming the SHI I²C Serial Clock

The programmed serial clock cycle, T_{I^2CCP}, is specified by the value of the HDM[7:0] and HRS bits of the HCKR (SHI clock control register).

The expression for T_{I^2CCP} is

$$T_{I^2CCP} = [T_C \times 2 \times (HDM[7:0] + 1) \times (7 \times (1 - HRS) + 1)] \quad \textit{Eqn. 1}$$

where

- HRS is the pre scaler rate select bit. When HRS is cleared, the fixed divide-by-eight pre scaler is operational. When HRS is set, the pre scaler is bypassed.
- HDM[7:0] are the divider modulus select bits. A divide ratio from 1 to 256 (HDM[7:0] = $00 to $FF) may be selected.

In I²C mode, the user may select a value for the programmed serial clock cycle from

$$6 \times T_C \quad \text{(if HDM[7:0] = \$02 and HRS = 1)} \quad \textit{Eqn. 2}$$

to

$$4096 \times T_C \quad \text{(if HDM[7:0] = \$FF and HRS = 0)} \quad \textit{Eqn. 3}$$

The programmed serial clock cycle (T_{I^2CCP}) should be chosen in order to achieve the desired SCL serial clock cycle (T_{SCL}), as shown in Equation 4.

$$T_{I^2CCP} + 3 \times T_C + 45ns + T_R \quad \text{(Nominal, SCL Serial Clock Cycle (TSCL) generated as master)} \quad \textit{Eqn. 4}$$

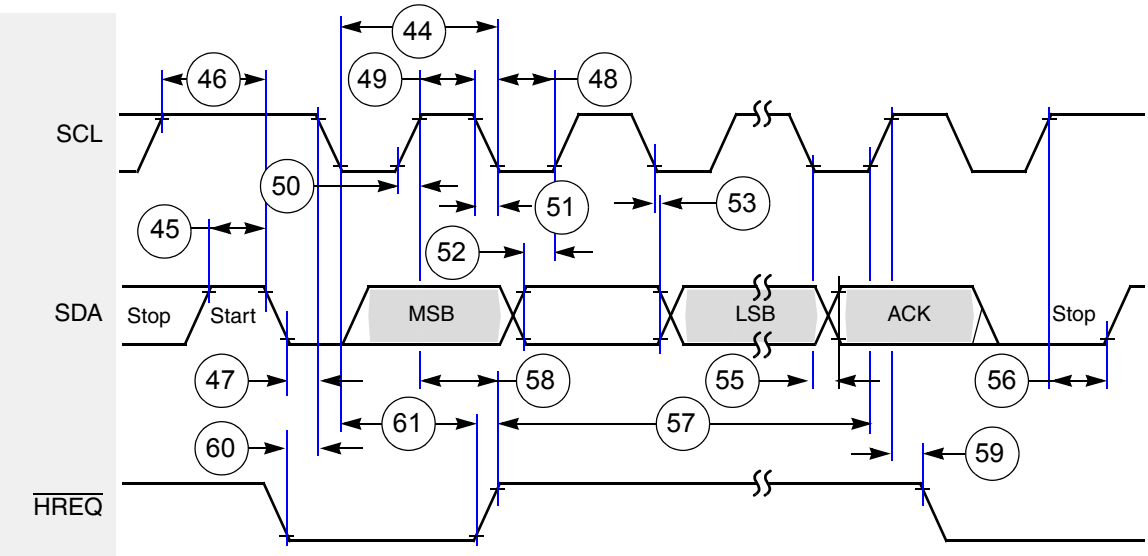


Figure 19. I²C Timing Diagram

2.2.4 Enhanced Serial Audio Interface (ESAI) Timing

See Table 13 For ESAI timing parameters and Figure 20, Figure 21, Figure 22, and Figure 23 for timing diagrams.

Table 13. Enhanced Serial Audio Interface Timing Parameters

No.	Characteristics[1, 3, 4]	Symbol	Expression[5]	Min	Max	Condition[2]	Unit
62	Clock cycle[5]	t_{SSICC}	$4 \times T_C$ $4 \times T_C$	20.0 20.0	– –	i ck i ck	ns
63	Clock high period • For internal clock • For external clock	–	 $2 \times T_C$ $2 \times T_C$	 10 10	 – –	 – –	ns
64	Clock low period • For internal clock • For external clock	–	 $2 \times T_C$ $2 \times T_C$	 10 10	 – –	 – –	ns
65	SCKR rising edge to FSR out (bl) high	–	–	– –	17.0 7.0	x ck i ck a	ns
66	SCKR rising edge to FSR out (bl) low	–	–	– –	17.0 7.0	x ck i ck a	ns
67	SCKR rising edge to FSR out (wr) high[6]	–	–	– –	19.0 9.0	x ck i ck a	ns
68	SCKR rising edge to FSR out (wr) low[6]	–	–	– –	19.0 9.0	x ck i ck a	ns
69	SCKR rising edge to FSR out (wl) high	–	–	– –	16.0 6.0	x ck i ck a	ns
70	SCKR rising edge to FSR out (wl) low	–	–	– –	17.0 7.0	x ck i ck a	ns
71	Data in setup time before SCKR (SCK in synchronous mode) falling edge	–	–	12.0 19.0	– –	x ck i ck	ns
72	Data in hold time after SCKR falling edge	–	–	3.5 9.0	– –	x ck i ck	ns
73	FSR input (bl, wr) high before SCKR falling edge [6]	–	–	2.0 12.0	– –	x ck i ck a	ns
74	FSR input (wl) high before SCKR falling edge	–	–	2.0 12.0	– –	x ck i ck a	ns
75	FSR input hold time after SCKR falling edge	–	–	2.5 8.5	– –	x ck i ck a	ns
76	Flags input setup before SCKR falling edge	–	–	0.0 19.0	– –	x ck i ck s	ns
77	Flags input hold time after SCKR falling edge	–	–	6.0 0.0	– –	x ck i ck s	ns
78	SCKT rising edge to FST out (bl) high	–	–	– –	18.0 8.0	x ck i ck	ns
79	SCKT rising edge to FST out (bl) low	–	–	– –	20.0 10.0	x ck i ck	ns

Table 13. Enhanced Serial Audio Interface Timing Parameters (Continued)

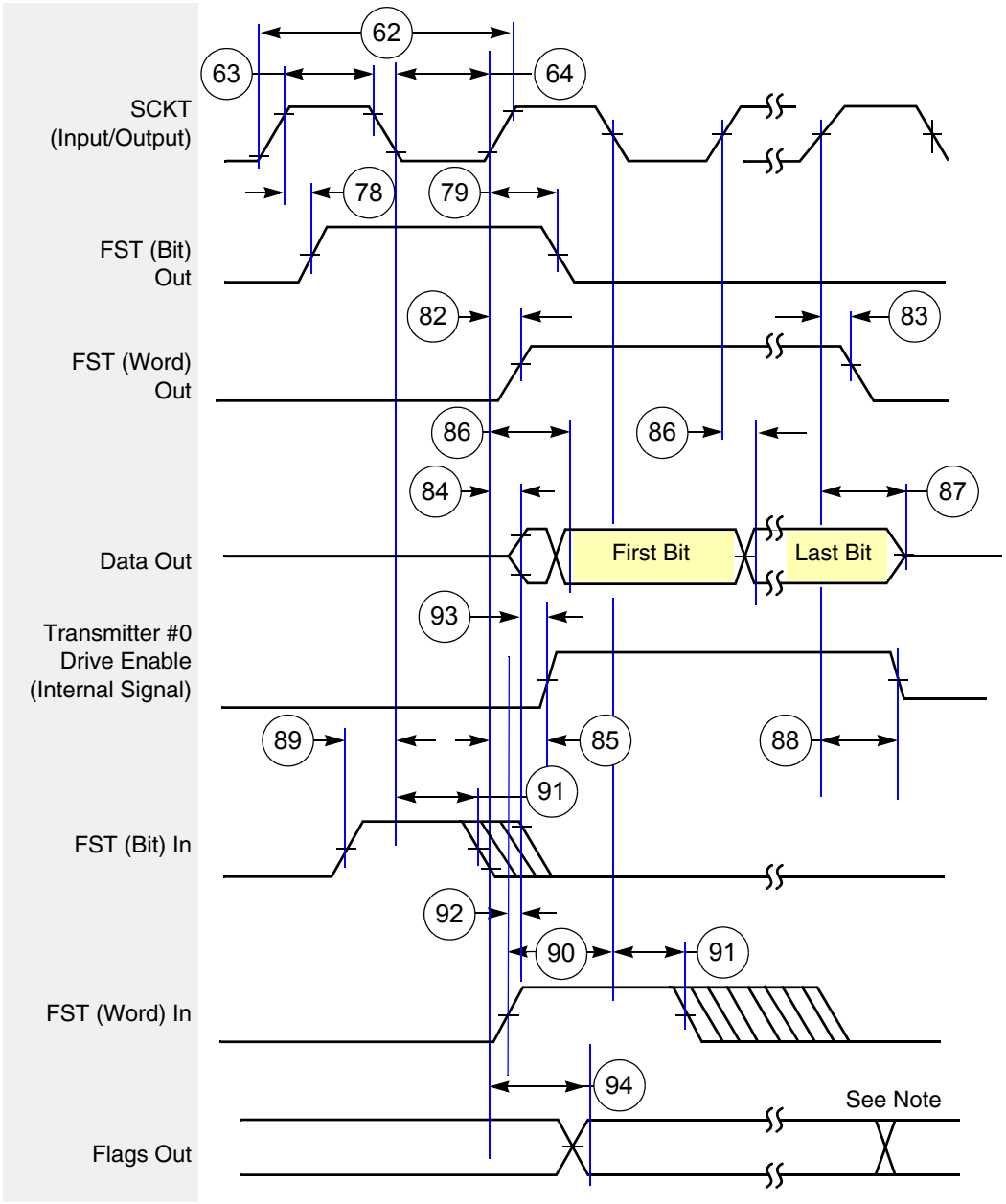
No.	Characteristics[1, 3, 4]	Symbol	Expression[5]	Min	Max	Condition[2]	Unit
80	SCKT rising edge to FST out (wr) high[6]	–	–	– –	20.0 10.0	x ck i ck	ns
81	SCKT rising edge to FST out (wr) low[6]	–	–	– –	22.0 12.0	x ck i ck	ns
82	SCKT rising edge to FST out (wl) high	–	–	– –	19.0 9.0	x ck i ck	ns
83	SCKT rising edge to FST out (wl) low	–	–	– –	20.0 10.0	x ck i ck	ns
84	SCKT rising edge to data out enable from high impedance	–	–	– –	22.0 17.0	x ck i ck	ns
85	SCKT rising edge to transmitter #0 drive enable assertion	–	–	– –	17.0 11.0	x ck i ck	ns
86	SCKT rising edge to data out valid	–	–	– –	18.0 13.0	x ck i ck	ns
87	SCKT rising edge to data out high impedance[7]	–	–	– –	21.0 16.0	x ck i ck	ns
88	SCKT rising edge to transmitter #0 drive enable deassertion[7]	–	–	– –	14.0 9.0	x ck i ck	ns
89	FST input (bl, wr) setup time before SCKT falling edge[6]	–	–	2.0 18.0	– –	x ck i ck	ns
90	FST input (wl) setup time before SCKT falling edge	–	–	2.0 18.0	– –	x ck i ck	ns
91	FST input hold time after SCKT falling edge	–	–	4.0 5.0	– –	x ck i ck	ns
92	FST input (wl) to data out enable from high impedance	–	–	–	21.0	–	ns
93	FST input (wl) to transmitter #0 drive enable assertion	–	–	–	14.0	–	ns
94	Flag output valid after SCKT rising edge	–	–	– –	14.0 9.0	x ck i ck	ns

Table 13. Enhanced Serial Audio Interface Timing Parameters (Continued)

No.	Characteristics[1, 3, 4]	Symbol	Expression[5]	Min	Max	Condition[2]	Unit
95	HCKR/HCKT clock cycle	–	2 x T_C	10	–	–	ns
96	HCKT input rising edge to SCKT output	–	–	–	18.0	–	ns
97	HCKR input rising edge to SCKR output	–	–	–	18.0	–	ns

Notes:

1. V_{CORE_VDD} = 1.00 ± 0.10 V; T_J = -40°C to 125°C; C_L = 50 pF.
2. i ck = internal clock
   x ck = external clock
   i ck a = internal clock, asynchronous mode
   (Asynchronous implies that SCKT and SCKR are two different clocks.)
   i ck s = internal clock, synchronous mode
   (Synchronous implies that SCKT and SCKR are the same clock.)
3. bl = bit length
   wl = word length
   wr = word length relative
4. SCKT(SCKT pin) = transmit clock
   SCKR(SCKR pin) = receive clock
   FST(FST pin) = transmit frame sync
   FSR(FSR pin) = receive frame sync
   HCKT(HCKT pin) = transmit high frequency clock
   HCKR(HCKR pin) = receive high frequency clock
5. For the internal clock, the external clock cycle is defined by Tc and the ESAI control register.
6. The word-relative frame sync signal waveform relative to the clock operates in the same manner as the bit-length frame sync signal waveform, but spreads from one serial clock before first bit clock (same as bit length frame sync signal), until the one before last bit clock of the first word in frame.
7. Periodically sampled and not 100% tested.
8. ESAI_1, ESAI_2, ESAI_3 specs match those of ESAI.



Note: In network mode, output flag transitions can occur at the start of each time slot within the frame. In normal mode, the output flag state is asserted for the entire frame period.

Figure 20. ESAI Transmitter Timing Diagram

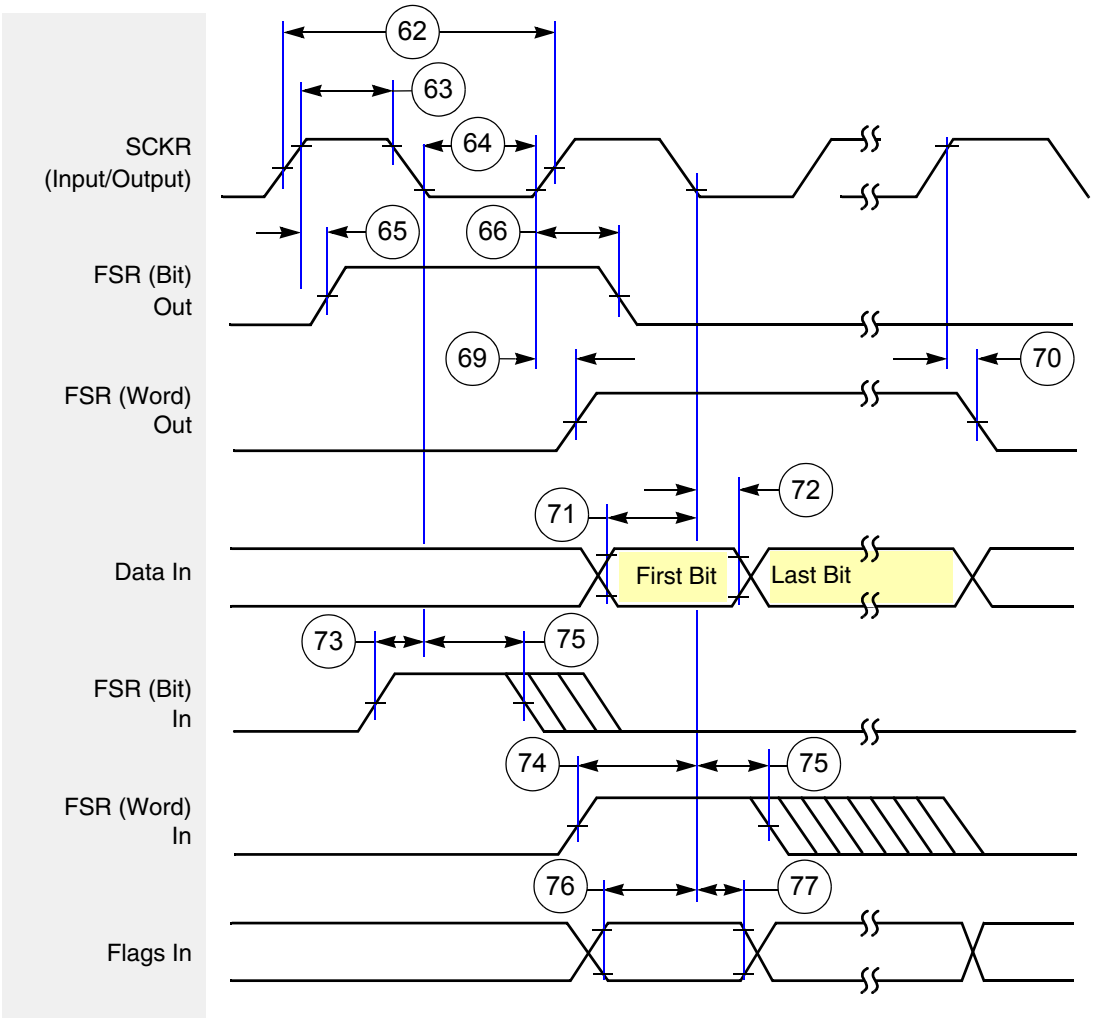


Figure 21. ESAI Receiver Timing Diagram

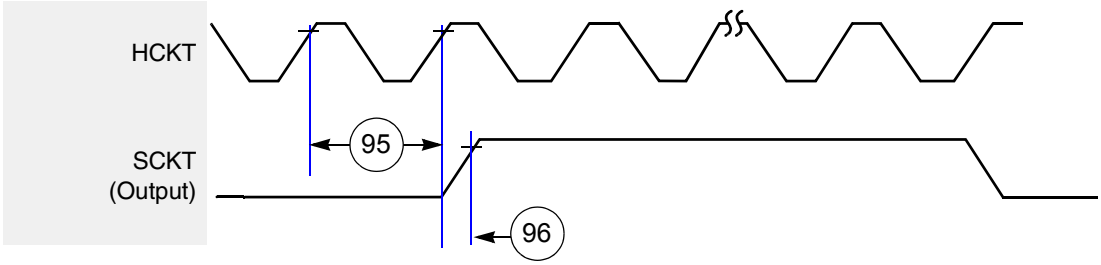


Figure 22. ESAI HCKT Timing Diagram

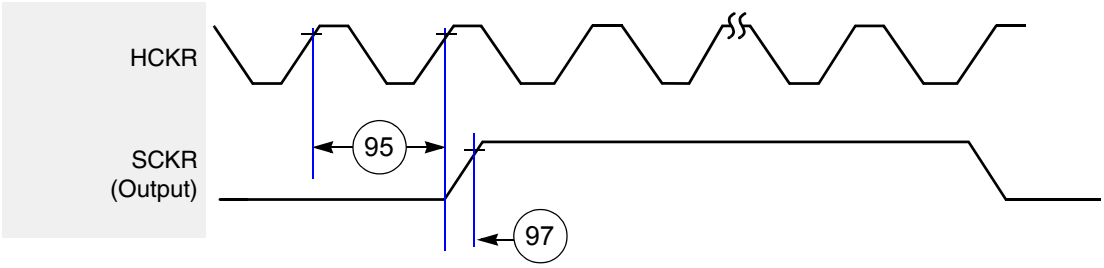


Figure 23. ESAI HCKR Timing

2.2.5 Timer Timing

See Table 14 for timer timing parameters and Figure 24 for the timing diagram.

Table 14. Timer Timing Parameters

No.	Characteristics	Expression			Unit
			Min	Max	
98	TIO Low	$2 \times T_C + 2.0$	12.0	–	ns
99	TIO High	$2 \times T_C + 2.0$	12.0	–	ns

Notes:
1. V_{CORE_VDD} = 1.00 V ± 0.10 V; T_J = -40°C to 125°C, C_L = 50 pF
2. TIMER_1 specs match those of TIMER

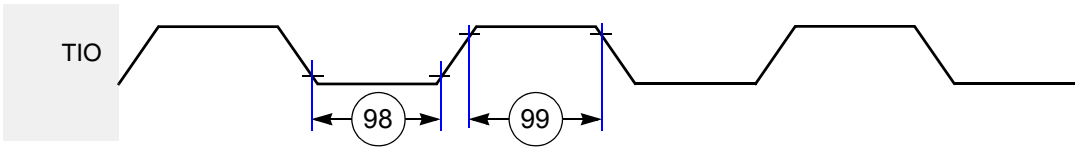


Figure 24. TIO Timer Event Input Restrictions Diagram

2.2.6 GPIO Timing

See Table 15 for general purpose input and output (GPIO) timing and Figure 25 for the timing diagram.

Table 15. GPIO Timing Parameters

No.	Characteristics[1]	Expression	Min	Max	Unit
100	Fsys edge to GPIO out valid (GPIO out delay time)[2]	–	–	7	ns
101	Fsys edge to GPIO out not valid (GPIO out hold time)[2]	–	–	7	ns
102	Fsys In valid to EXTAL edge (GPIO in set-up time)[2]	–	2	–	ns
103	Fsys edge to GPIO in not valid (GPIO in hold time)[2]	–	0	–	ns
104	Minimum GPIO pulse high width	2 x TC	10	–	ns

Table 15. GPIO Timing (Continued)Parameters

No.	Characteristics[1]	Expression	Min	Max	Unit
105	Minimum GPIO pulse low width	2 x TC	10	–	ns
106	GPIO out rise time	–	–	13.0	ns
107	GPIO out fall time	–	–	13.0	ns

Notes:
1. V_{CORE_VDD} = 1.0 V ± 0.10 V; T_J = -40°C to 125°C; C_L = 50 pF

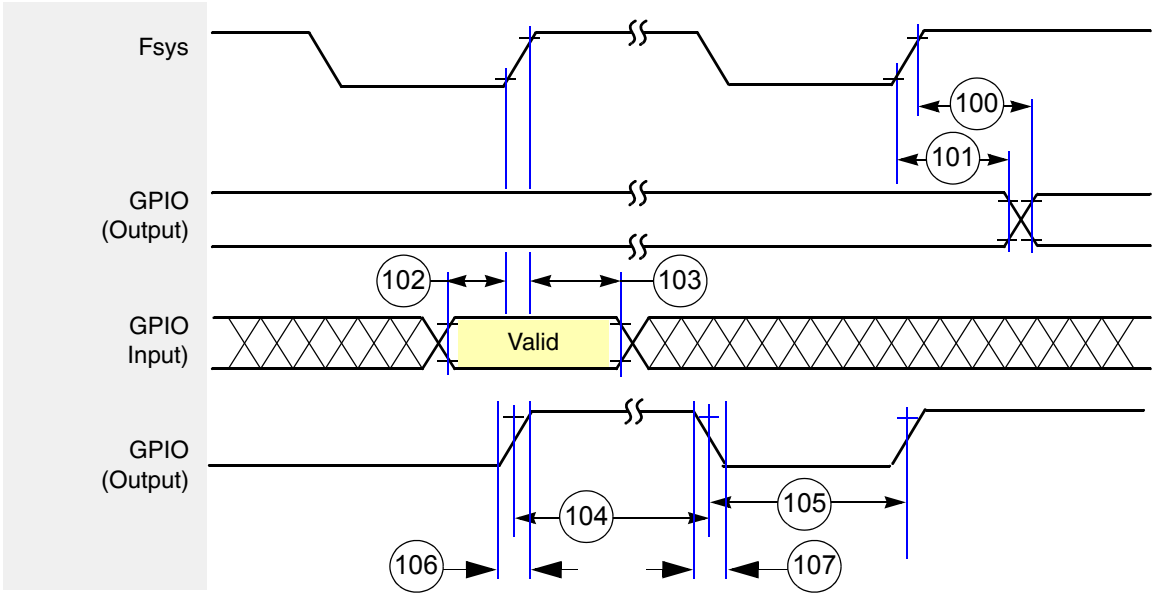


Figure 25. GPIO Timing Diagram

2.2.7 JTAG Timing

See Table 16 for joint test action group (JTAG) timing parameters, and Figure 26, Figure 27, and Figure 28 for timing diagrams.

Table 16. JTAG Timing Parameters

No.	Characteristics	All Frequencies		Unit
		Min	Max	
108	TCK frequency of operation (1/(T_C × 3); maximum 10 MHz)	–	10.0	MHz
109	TCK cycle time in Crystal mode	100.0	–	ns
110	TCK clock pulse width measured at 1.65 V	50.0	–	ns
111	TCK rise and fall times	–	3.0	ns
112	Boundary scan input data setup time	15.0	–	ns
113	Boundary scan input data hold time	24.0	–	ns
114	TCK low to output data valid	–	40.0	ns
115	TCK low to output high impedance	–	40.0	ns

Table 16. JTAG Timing Parameters (Continued)

No.	Characteristics	All Frequencies		Unit
		Min	Max	
116	TMS, TDI data setup time	5.0	–	ns
117	TMS, TDI data hold time	25.0	–	ns
118	TCK low to TDO data valid	–	44.0	ns
119	TCK low to TDO high impedance	–	44.0	ns

Notes:
1. V_{CORE_VDD} = 1.0 V ± 0.10 V; T_J = -40°C to 125°C , C_L = 50 pF
2. All timings apply to OnCE module data transfers because it uses the JTAG port as an interface.

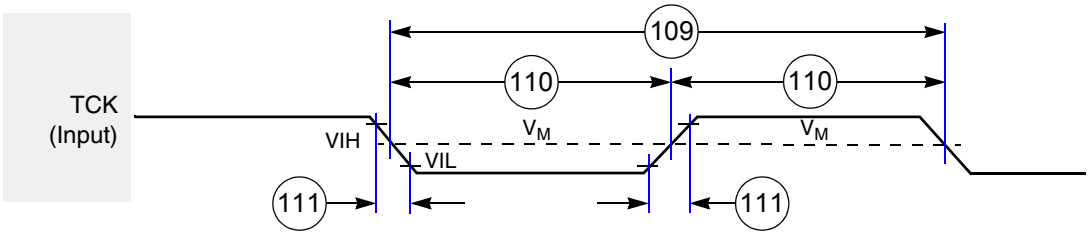


Figure 26. Test Clock Input Timing Diagram

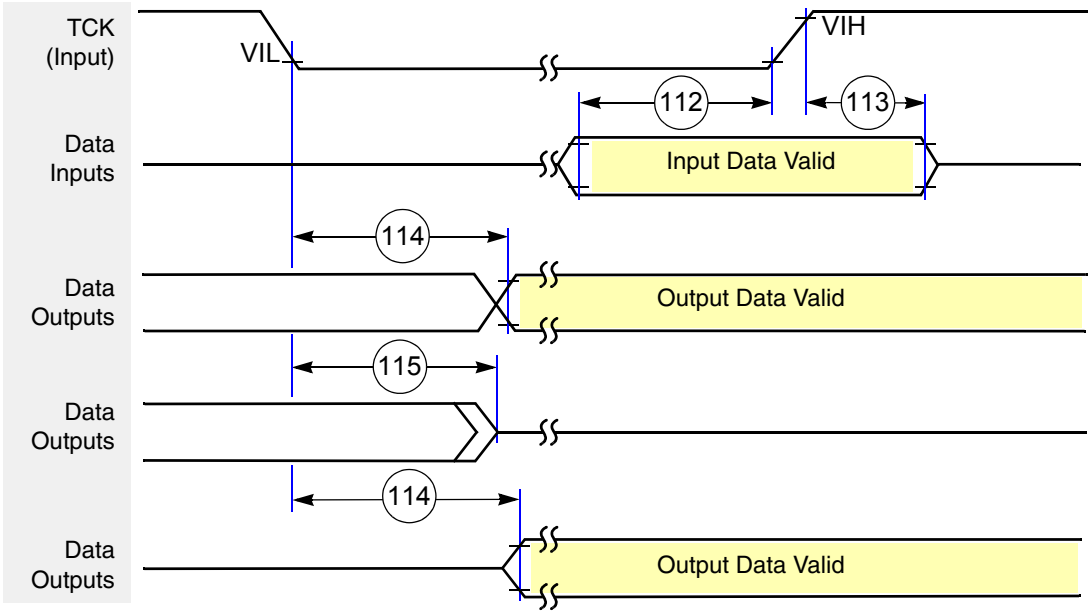


Figure 27. Debugger Port Timing Diagram

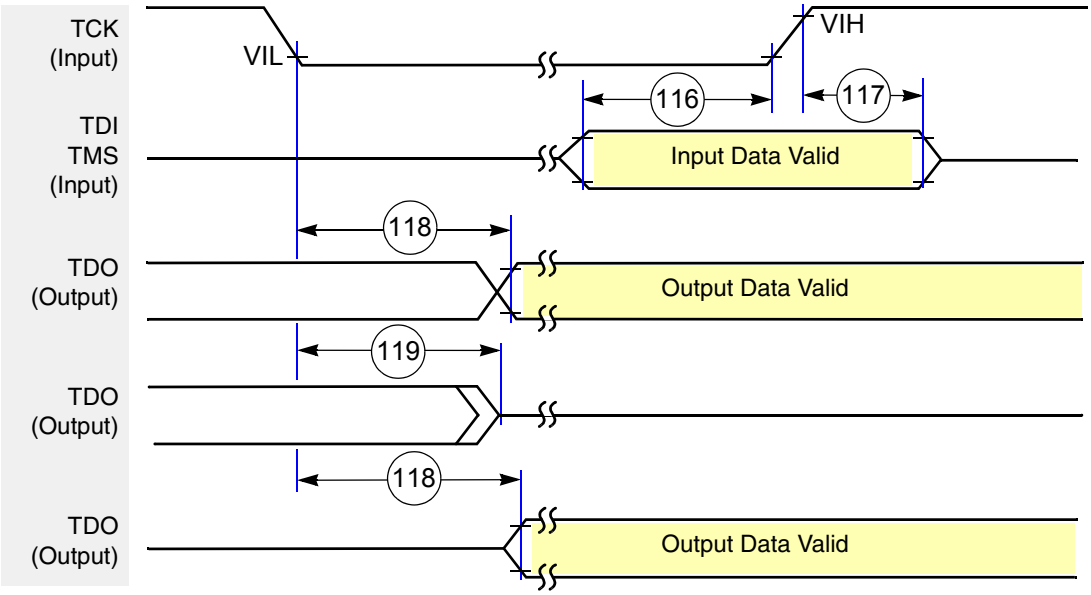


Figure 28. Test Access Port Timing Diagram

2.2.8 Watchdog Timer Timing

For watchdog timer timing, see Table 17.

Table 17. Watchdog Timer Timing Parameters

No.	Characteristics	Expression	Min	Max	Unit
120	Delay from time-out to fall of $\overline{\text{WDT}}$, $\overline{\text{WDT\_1}}$	$2 \times T_C$	10.0	–	ns
121	Delay from timer clear to rise of $\overline{\text{WDT}}$, $\overline{\text{WDT\_1}}$	2 × Tc	10.0	–	ns

2.2.9 Host Data Interface (HDI24) Timing

The HDI24 module is only on the DSP56721 device; the DSP56720 device does not have a HDI24 module. Also, only 16 bits of the HDI24 interface are pinned out on the DSP56721 device. See Table 18 for HDI24 timing and Figure 29, Figure 30, Figure 30, Figure 31, Figure 32, Figure 33, Figure 34, and Figure 35 for timing diagrams.

Table 18. HDI24 Timing Parameters

No.	Characteristics[2]	Expression	200 MHz		Unit
			Min	Max	
317	Read data strobe assertion width[3] $\overline{\text{HACK}}$ read assertion width	$T_C + 9.9$	14.9	–	ns
318	Read data strobe deassertion width[3] $\overline{\text{HACK}}$ read deassertion width	–	9.9	–	ns
319	Read data strobe deassertion width[3] after “Last Data Register” reads[4,5], or between two consecutive CVR, ICR, or ISR reads[6] $\overline{\text{HACK}}$ deassertion width after “Last Data Register” reads[4,5]	$2 \times T_C + 6.6$	16.6	–	ns

Table 18. HDI24 Timing Parameters (Continued)

No.	Characteristics[2]	Expression	200 MHz		Unit
			Min	Max	
320	Write data strobe assertion width[7] $\overline{HACK}$ write assertion width	–	13.2	–	ns
321	Write data strobe deassertion width[7] $\overline{HACK}$ write deassertion width • after ICR, CVR and "Last Data Register" writes[4]	$2 \times T_C + 6.6$	16.6	–	ns
	• after IVR writes, or • after TXH:TXM writes (with HBE=0), or • after TXL:TXM writes (with HBE=1)	–	16.5	–	
322	$\overline{HAS}$ assertion width	–	9.9	–	ns
323	$\overline{HAS}$ deassertion to data strobe assertion[8]	–	0.0	–	ns
324	Host data input setup time before write data strobe deassertion[7] Host data input setup time before $\overline{HACK}$ write deassertion	–	9.9	–	ns
325	Host data input hold time after write data strobe deassertion[7] Host data input hold time after $\overline{HACK}$ write deassertion	–	3.3	–	ns
326	Read data strobe assertion to output data active from high impedance[3] $\overline{HACK}$ read assertion to output data active from high impedance	–	3.3	–	ns
327	Read data strobe assertion to output data valid[3] $\overline{HACK}$ read assertion to output data valid	–	–	24.2	ns
328	Read data strobe deassertion to output data high impedance[3] $\overline{HACK}$ read deassertion to output data high impedance	–	–	9.9	ns
329	Output data hold time after read data strobe deassertion[3] Output data hold time after $\overline{HACK}$ read deassertion	–	3.3	–	ns
330	$\overline{HCS}$ assertion to read data strobe deassertion[3]	$T_C + 9.9$	14.9	–	ns
331	$\overline{HCS}$ assertion to write data strobe deassertion[7]	–	9.9	–	ns
332	$\overline{HCS}$ assertion to output data valid	–	–	19.1	ns
333	$\overline{HCS}$ hold time after data strobe deassertion[8]	–	0.0	–	ns
334	Address (AD7–AD0) setup time before $\overline{HAS}$ deassertion (HMUX=1)	–	4.7	–	ns
335	Address (AD7–AD0) hold time after $\overline{HAS}$ deassertion (HMUX=1)	–	3.3	–	ns
336	A10–A8 (HMUX=1), A2–A0 (HMUX=0), HR/$\overline{W}$ setup time before data strobe assertion[8] • Read	–	0	–	ns
	• Write	–	4.7	–	
337	A10–A8 (HMUX=1), A2–A0 (HMUX=0), HR/$\overline{W}$ hold time after data strobe deassertion[8]	–	3.3	–	ns
338	Delay from read data strobe deassertion to host request assertion for "Last Data Register" read[3, 4, 9]	T_C	5.0	–	ns

Table 18. HDI24 Timing Parameters (Continued)

No.	Characteristics[2]	Expression	200 MHz		Unit
			Min	Max	
339	Delay from write data strobe deassertion to host request assertion for “Last Data Register” write[4, 7, 9]	$2 \times T_C$	10.0	–	ns
340	Delay from data strobe assertion to host request deassertion for “Last Data Register” read or write (HROD = 0)[4, 8, 9]	–	–	19.1	ns
341	Delay from data strobe assertion to host request deassertion for “Last Data Register” read or write (HROD = 1, open drain Host Request)[4, 8, 9, 10]	–	–	300.0	ns
342	Delay from DMA $\overline{\text{HACK}}$ deassertion to HOREQ assertion				ns
	• For “Last Data Register” read[4]	$2 \times T_C + 19.1$	29.1	–	
	• For “Last Data Register” write[4]	$1 \times T_C + 19.1$	24.1	–	
	• For other cases	–	0.0	–	
343	Delay from DMA $\overline{\text{HACK}}$ assertion to HOREQ deassertion • HROD = 0[4]	–	–	20.2	ns
344	Delay from DMA $\overline{\text{HACK}}$ assertion to HOREQ deassertion for “Last Data Register” read or write • HROD = 1, open drain Host Request[4, 10]	–	–	300.0	ns

Notes:
1. In the timing diagrams that follow, the controls pins are drawn as active low. The pin polarity is programmable.
2. V_{CC} = 1.0 V ± 10%; T_J = –40°C to +125°C; C_L = 50 pF.
3. The read data strobe is HRD in the dual data strobe mode and HDS in the single data strobe mode.
4. The “last data register” is the register at address $7, which is the last location to be read or written in data transfers.
5. This timing is applicable only if a read from the “last data register” is followed by a read from the RXL, RXM, or RXH registers without first polling RXDF or HREQ bits, or waiting for the assertion of the HOREQ signal.
6. This timing is applicable only if two consecutive reads from one of these registers are executed.
7. The write data strobe is HWR in the dual data strobe mode and HDS in the single data strobe mode.
8. The data strobe is host read (HRD) or host write (HWR) in the dual data strobe mode and host data strobe (HDS) in the single data strobe mode.
9. The host request is HOREQ in the single host request mode and HRRQ and HTRQ in the double host request mode.
10. In this calculation, the host request signal is pulled up by a 4.7 kW resistor in the open-drain mode.
11. HDI24_1 specs match those of HDI24.

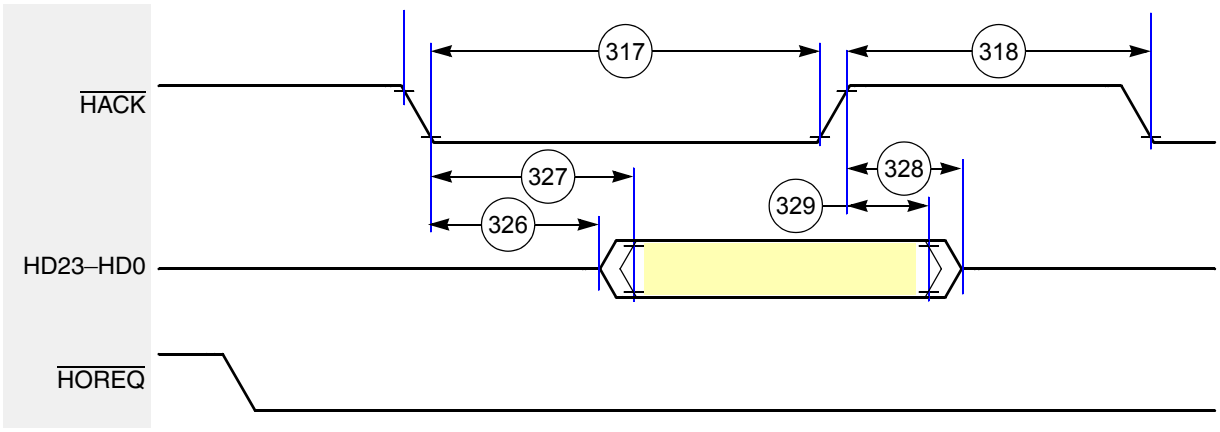


Figure 29. HDI24 Host Interrupt Vector Register (IVR) Read Timing Diagram

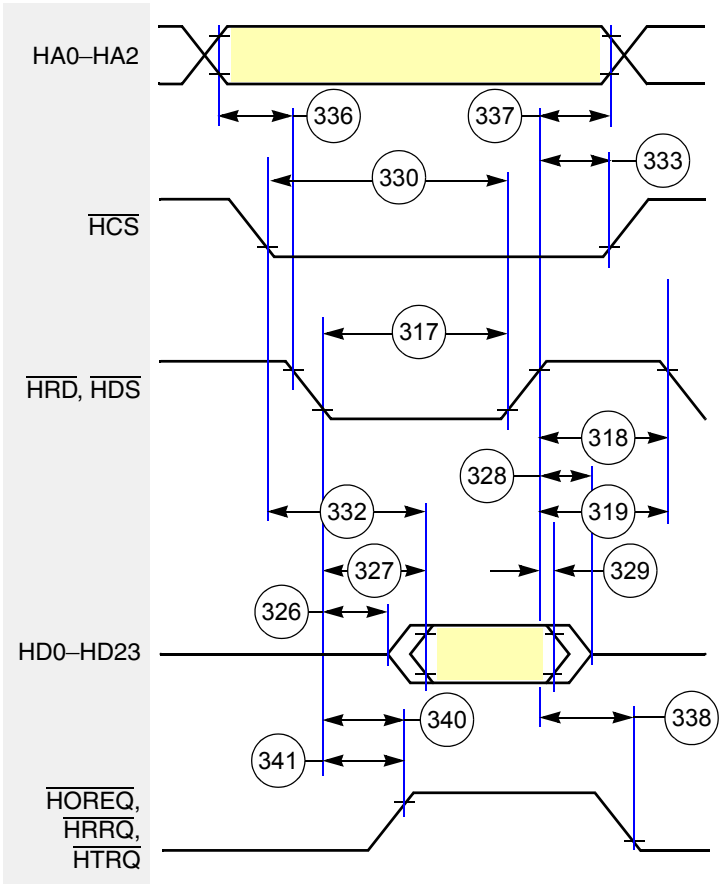


Figure 30. HDI24 Read Timing Diagram, Non-Multiplexed Bus

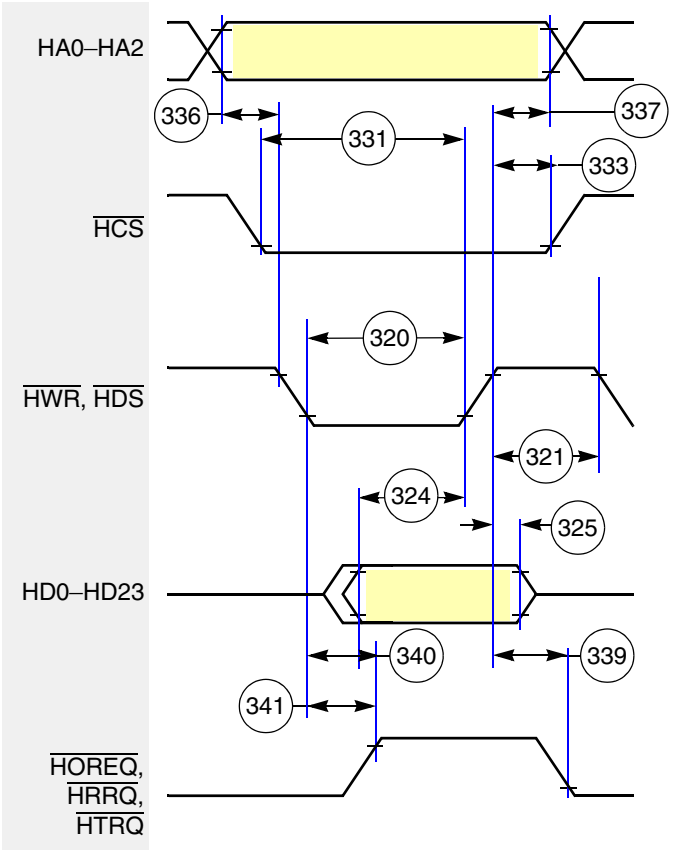


Figure 31. HDI24 Write Timing Diagram, Non-Multiplexed Bus

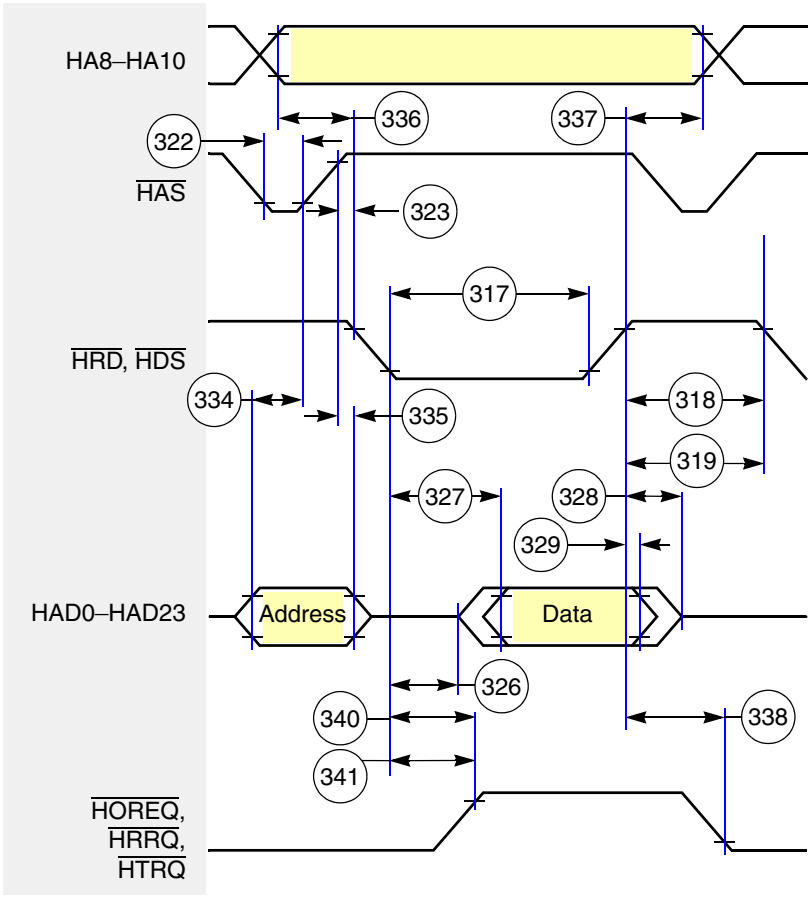


Figure 32. HDI24 Read Timing Diagram, Multiplexed Bus

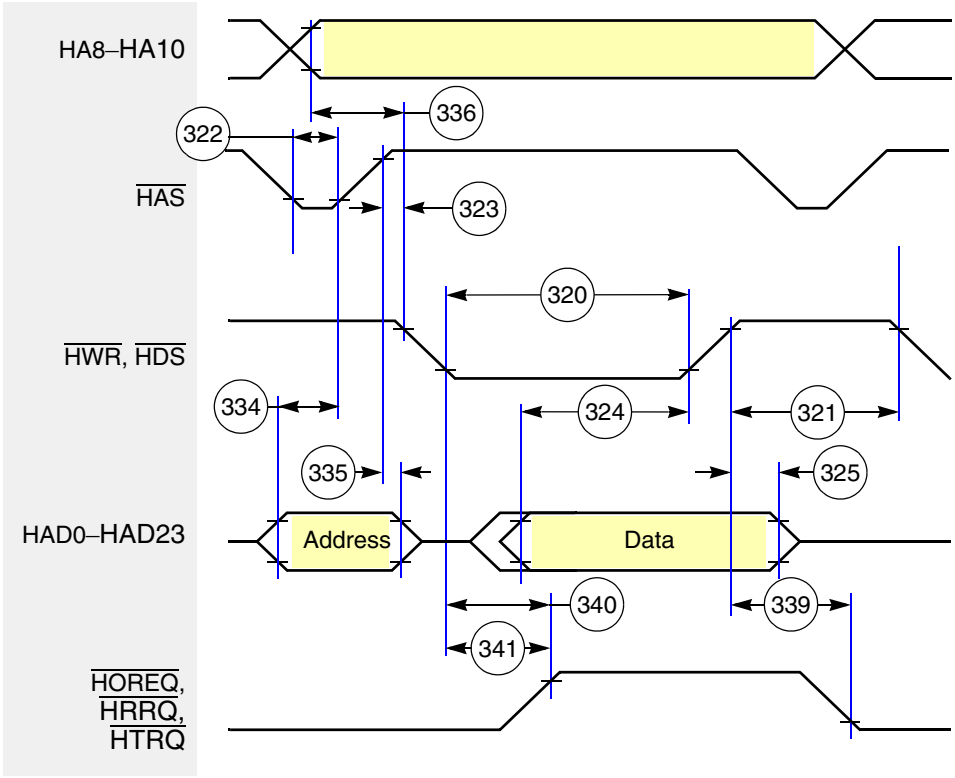


Figure 33. HDI24 Write Timing Diagram, Multiplexed Bus

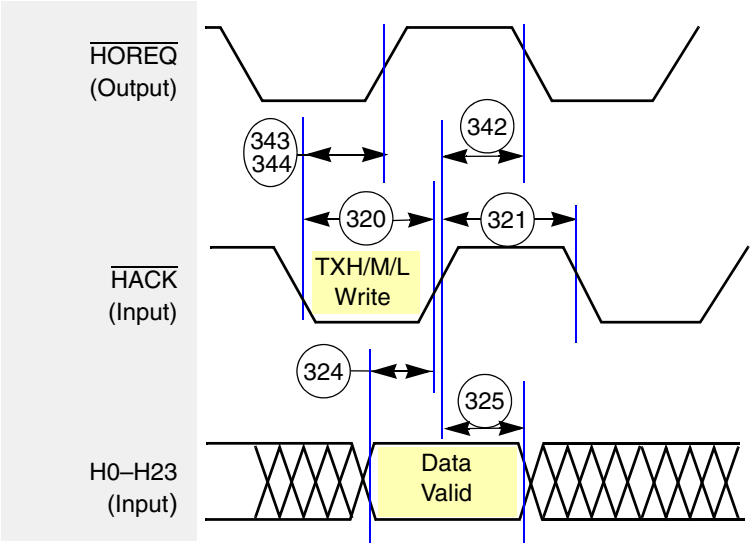


Figure 34. HDI24 Host DMA Write Timing Diagram

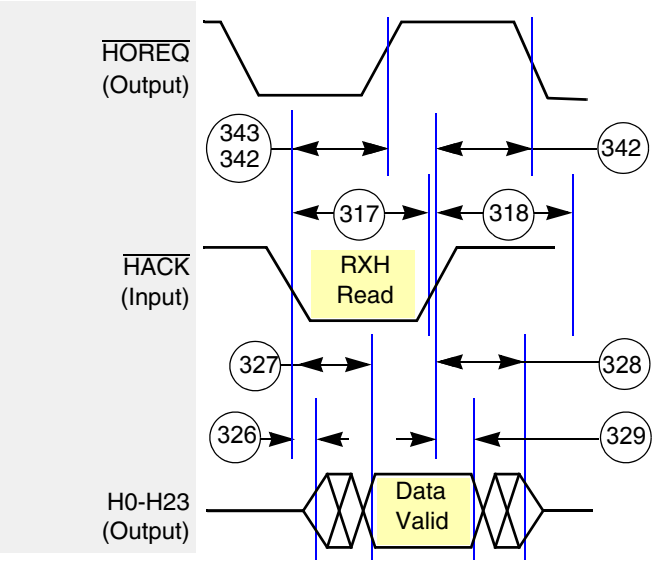


Figure 35. HDI24 Host DMA Read Timing Diagram

2.2.10 S/PDIF Timing

See Table 19 for Sony/Philips Digital Interconnect Format (S/PDIF) timing parameters and Figure 36 and Figure 37 for timing diagrams.

Table 19. S/PDIF Timing Parameters

Characteristics	Symbol	All Frequency		Unit
		Min	Max	
SPDIFIN1, SPDIFIN2, SPDIFIN3, SPDIFIN4 Skew: asynchronous inputs, no specs apply	–	–	0.7	ns
SPDIFOUT1,SPDIFOUT2 output (Load = 50 pf) • Skew • Transition Risng • Transition Falling	 – – –	 – – –	 1.5 24.2 31.3	ns
SPDIFOUT1, SPDIFOUT2 output (Load = 30 pf) • Skew • Transition Risng • Transition Falling	 – – –	 – – –	 1.5 13.6 18.0	ns
SRCK period	srckp	40.0	–	ns
SRCK high period	srckph	16.0	–	ns
SRCK low period	srckpl	16.0	–	ns
STCLK period	stclkp	40.0	–	ns
STCLK high period	stclkph	16.0	–	ns
STCLK low period	stclkpl	16.0	–	ns

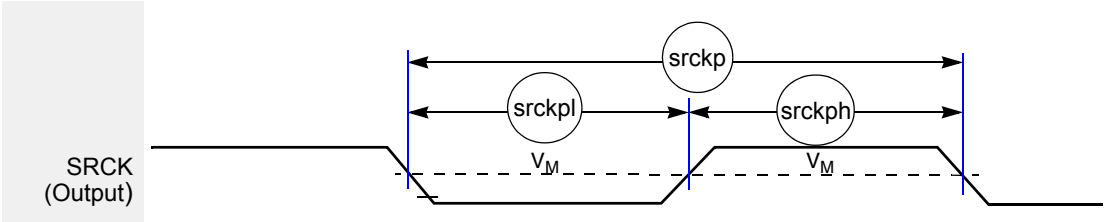


Figure 36. S/PDIF SRCK Timing Diagram

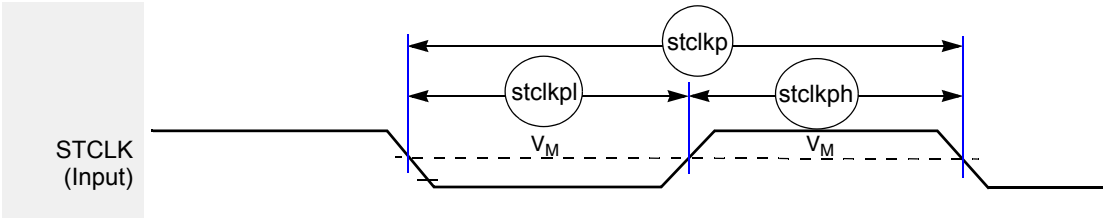


Figure 37. S/PIDF STCLK Timing Diagram

2.2.11 EMC Timing (DSP56720 only)

The DSP56721 device does not have an EMC module. For EMC timing parameters in DSP56720 devices, see Table 20, Table 21, and Table 22; for timing diagrams, see Figure 38, Figure 39, and Figure 40.

Table 20. EMC Timing Parameters (EMC PLL Enabled; LCRR[CLKDIV] = 2)

Parameter	Symbol	Min	Max	Unit
LCLK cycle time	T_{clk}	10	–	ns
LCLK skew to LSYNC_OUT	T_{clk_skew}	–	160	ps
Input setup to LSYNC_IN (except $\overline{\text{LGTA}}$/LUPWAIT)	T_{in_s}	2	–	ns
Input hold from LSYNC_IN (except $\overline{\text{LGTA}}$/LUPWAIT)	T_{in_h}	2	–	ns
$\overline{\text{LGTA}}$ valid time	T_{gta}	12	–	ns
LUPWAIT valid time	T_{upwait}	12	–	ns
LALE negedge to LAD(address phase) invaild (address latch hold time)	T_{ale_h}	3	–	ns
LALE valid time	T_{ale}	3.8	–	ns
Output setup from LSYNC_IN (except LAD[23:0] and LALE)	T_{out_s}	4	–	ns
Output hold from LSYNC_IN (except LAD[23:0] and LALE)	T_{out_h}	2	–	ns
LAD[23:0] output setup from LSYNC_IN	T_{ad_s}	3.5	–	ns
LAD[23:0] output hold from LSYNC_IN	T_{ad_h}	1.5	–	ns
LSYNC_IN to output high impedance for LAD[23:0]	T_{ad_z}	–	4.3	ns

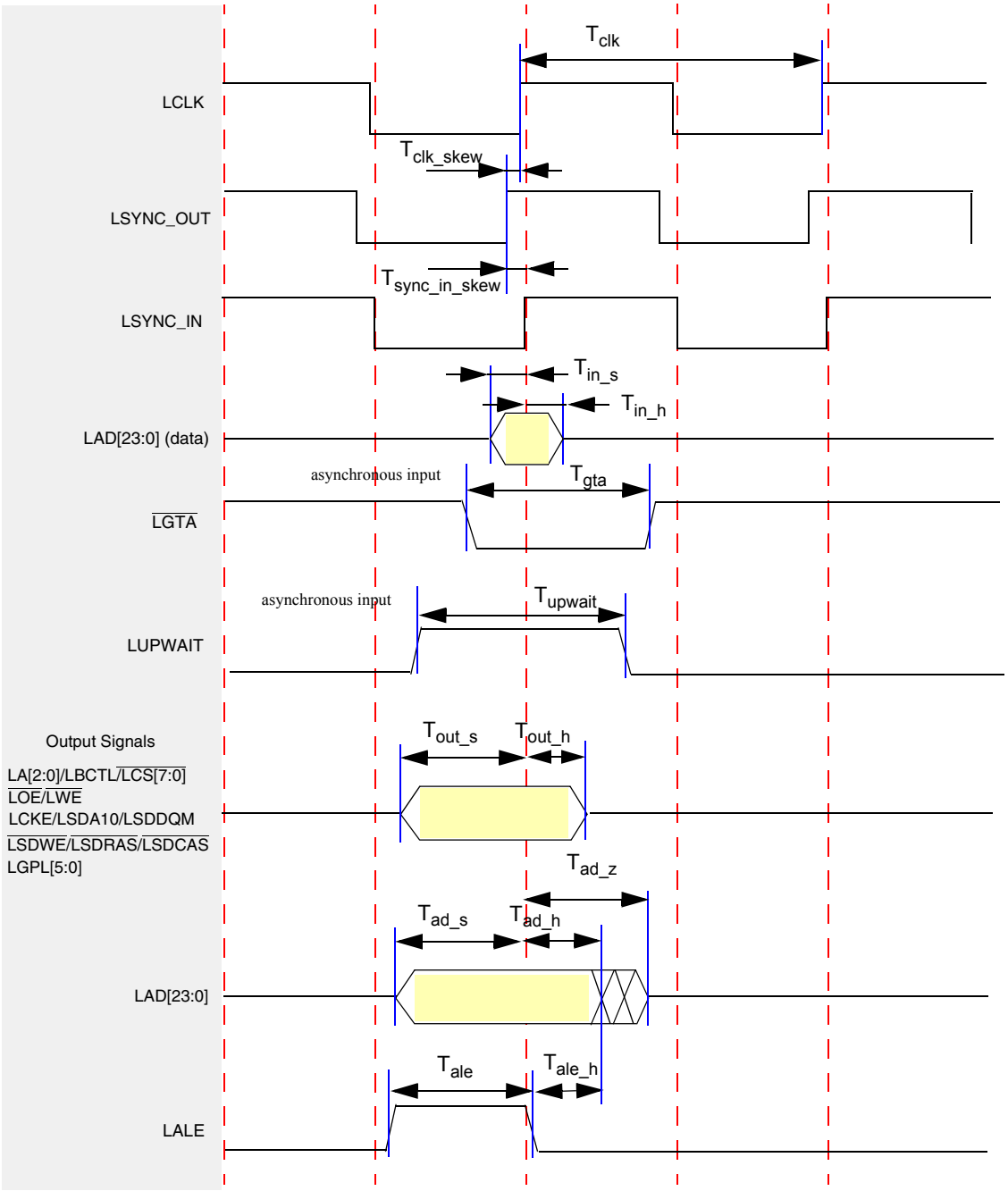


Figure 38. EMC Signals (EMC PLL Enabled; LCRR[CLKDIV] = 2)

Table 21. EMC Timing Parameters (EMC PLL Bypassed; LRCC[CLKDIV] = 4)

Parameter	Symbol	Min	Max	Unit
LCLK cycle time	T_{clk}	20	–	ns
Input setup to LCLK (except $\overline{LGTA}$/LUPWAIT)	T_{in_s}	8	–	ns
Input hold from LCLK (except $\overline{LGTA}$/LUPWAIT)[1]	T_{in_h}	-1	–	ns
$\overline{LGTA}$ valid time	T_{gta}	22	–	ns
LUPWAIT valid time	T_{upwait}	22	–	ns
LALE negedge to LAD (address phase) invalid (address latch hold time)	T_{ale_h}	4	–	ns
LALE valid time	T_{ale}	14	–	ns
Output setup from LCLK (except LAD[23:0] and LALE)	T_{out_s}	9	–	ns
Output hold from LCLK (except LAD[23:0] and LALE)	T_{out_h}	8	–	ns
LAD[23:0] output setup from LCLK	T_{ad_s}	8	–	ns
LAD[23:0] output hold from LCLK	T_{ad_h}	7	–	ns
LCLK to output high impedance for LAD[23:0]	T_{ad_z}	–	9	ns

Notes:
1. A negative hold time means that the signal could be invalid before the LCLK rising edge.

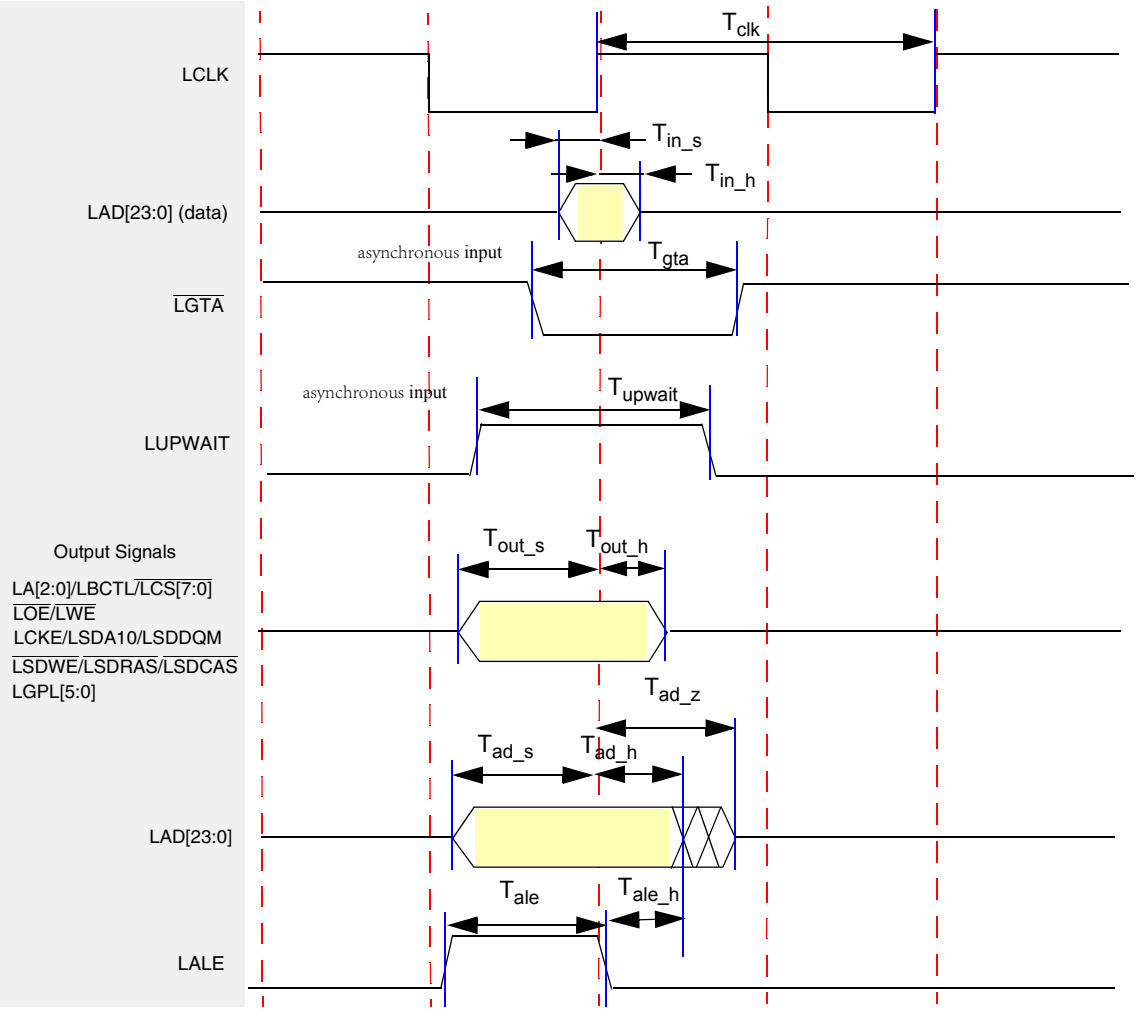


Figure 39. EMC Signals (EMC PLL Bypassed; LRCC[CLKDIV] = 4)

Table 22. EMC Timing Parameters (EMC PLL Bypassed; LRCC[CLKDIV] = 8)

Parameter	Symbol	Min	Max	Unit
LCLK cycle time	T_{clk}	40	–	ns
Input setup to LCLK (except $\overline{LGTA}$/LUPWAIT)	T_{in_s}	8	–	ns
Input hold from LCLK (except $\overline{LGTA}$/LUPWAIT)[1]	T_{in_h}	-1	–	ns
$\overline{LGTA}$ valid time	T_{gta}	42	–	ns
LUPWAIT valid time	T_{upwait}	42	–	ns
LALE negedge to LAD (address phase) invalid (address latch hold time)	T_{ale_h}	5	–	ns
LALE valid time	T_{ale}	34	–	ns
Output setup from LCLK (except LAD[23:0] and LALE)	T_{out_s}	19	–	ns
Output hold from LCLK (except LAD[23:0] and LALE)	T_{out_h}	18	–	ns

Table 22. EMC Timing Parameters (EMC PLL Bypassed; LRCC[CLKDIV] = 8) (Continued)

Parameter	Symbol	Min	Max	Unit
LAD[23:0] output setup from LCLK	T_{ad_s}	18	–	ns
LAD[23:0] output hold from LCLK	T_{ad_h}	17	–	ns
LCLK to output high impedance for LAD[23:0]	T_{ad_z}	–	19	ns
Notes: 1. A negative hold time means that the signal could be invalid before the LCLK rising edge.				

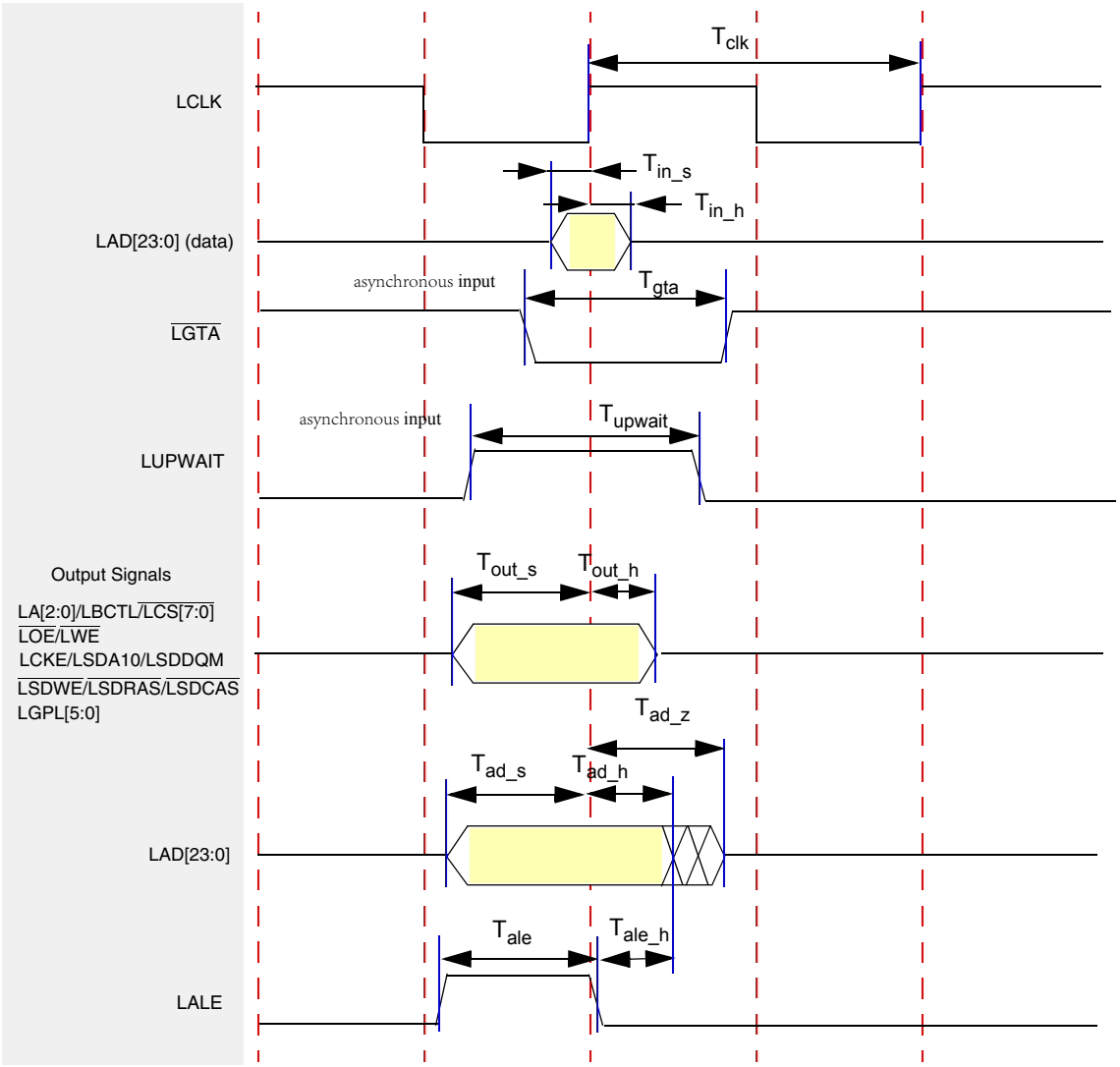


Figure 40. EMC Signals (EMC PLL Bypassed; LRCC[CLKDIV] = 8)

3 Functional Description and Application Information

See the DSP56720 Reference Manual (DSP56720RM) for detailed functional and applications information.

4 Hardware Design Considerations

For design considerations, also see Section 2.1.3, "Power Requirements."

5 Ordering Information

Table 23 provides ordering information for both the DSP56720 and DSP56721.

Table 23. Ordering Information

Product	ROM Version	Package	Part Number
DSP56720	A	144-pin plastic LQFP	DSPA56720AG
	B	144-pin plastic LQFP	DSPB56720AG
DSP56721	A	144-pin plastic LQFP	DSPA56721AG
	B	144-pin plastic LQFP	DSPB56721AG
	A	80-pin plastic LQFP	DSPA56721AF
	B	80-pin plastic LQFP	DSPB56721AF

6 Package Information

For the outline drawings of available device packages, see Table 24 and sections 6.1–6.2.

Table 24. Package Outline Drawings

Device	Package	See
DSP56720	144-pin plastic LQFP	Figure 43 on page 51 and Figure 44 on page 52
DSP56721	80-pin plastic LQFP	Figure 41 on page 49 and Figure 42 on page 50
	144-pin plastic LQFP	Figure 43 on page 51 and Figure 44 on page 52

6.1 80-Pin Package Outline Drawing

For the 80-pin package outline drawings, see Figure 41 and Figure 42.

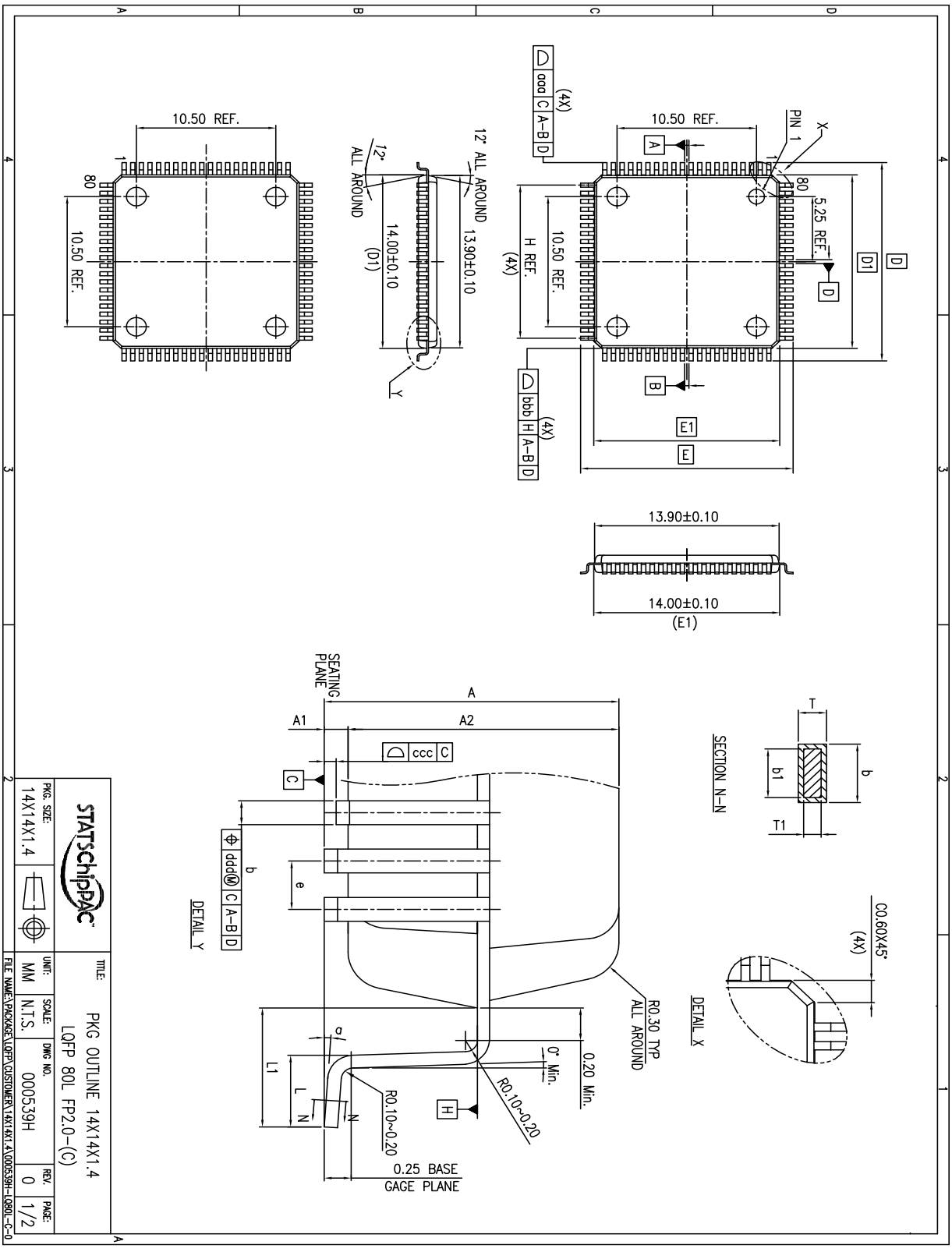


Figure 41. 80-Pin Package Outline Drawing (1 of 2)

Figure 42. 80-Pin Package Outline Drawing (2 of 2)

6.2 144-Pin Package Outline Drawing

For the 144-pin package drawings, see figures Figure 43 and Figure 44.

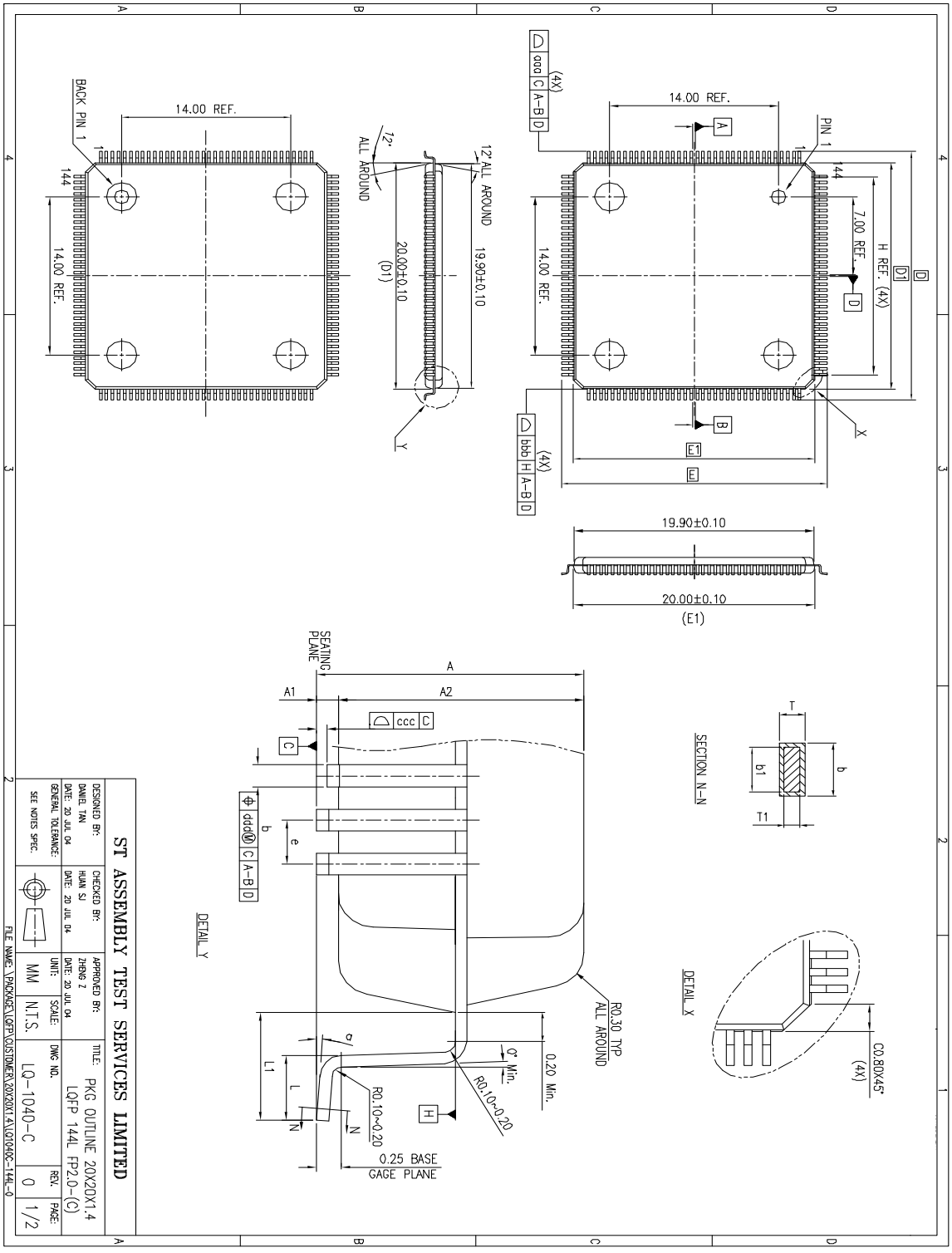


Figure 43. 144-Pin Package Outline Drawing (1 of 2)

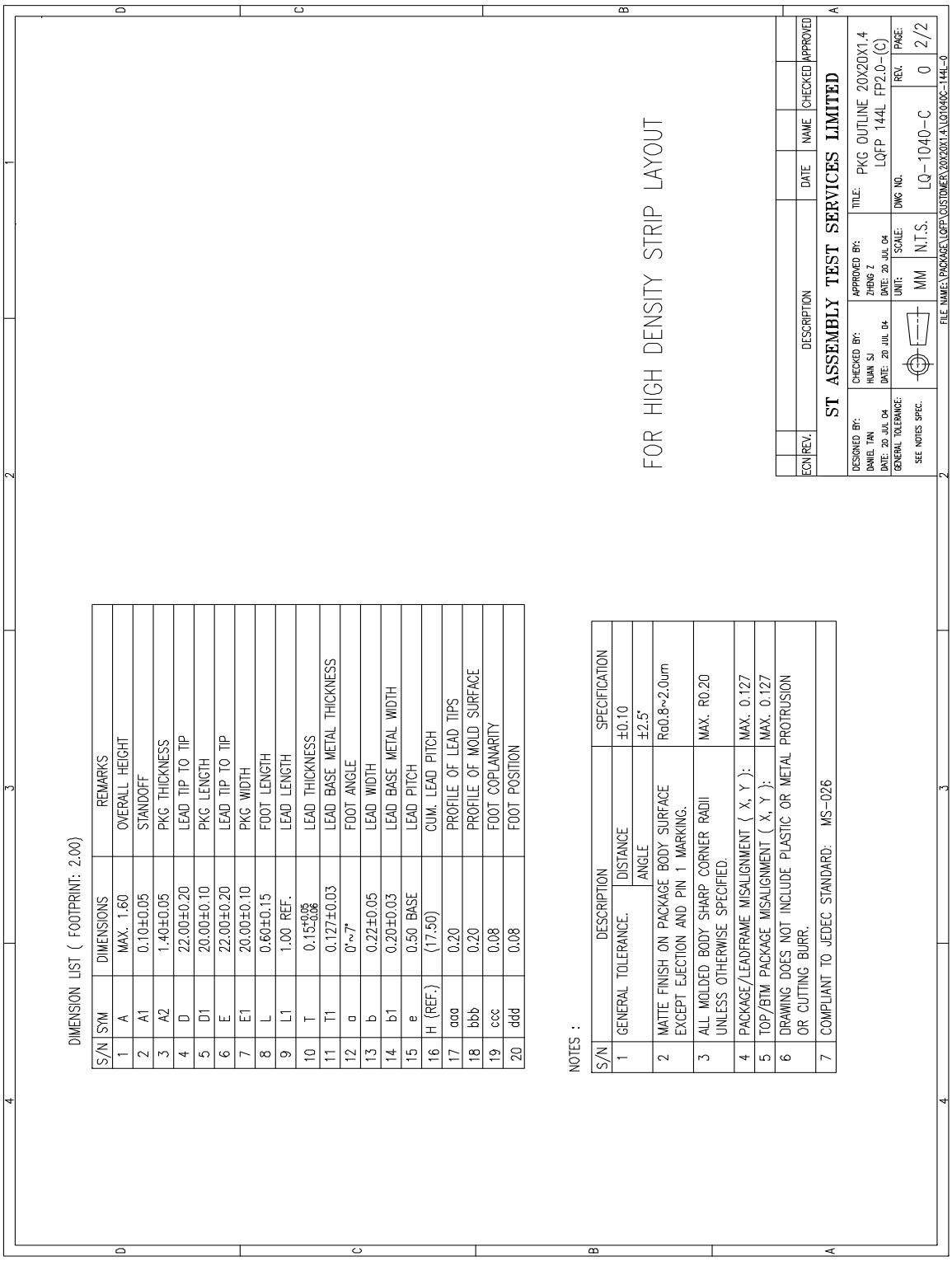


Figure 44. 144-Pin Package Outline Drawing (2 of 2)

7 Product Documentation

This Data Sheet is labeled as a particular type: Product Preview, Advance Information, or Technical Data. Definitions of these types are available at: http://www.freescale.com. Documentation is available from a local Freescale Semiconductor, Inc. distributor, semiconductor sales office, Literature Distribution Center, or through the Freescale DSP home page on the Internet (the source for the latest information).

The following documents are required for a complete description of the device and are necessary to design properly with the parts:

DSP56300 Family Manual (document number DSP56300FM). Detailed description of the 56300-family architecture and the 24-bit core processor and instruction set.

DSP56720/DSP56721 Reference Manual (document number DSP56720RM). Detailed description of memory, peripherals, and interfaces.

DSP56720 Product Brief (DSP56720PB). Brief description of the DSP56720 device.

DSP56721 Product Brief (DSP56721PB). Brief description of the DSP56721 device.

8 Revision History

Table 25 summarizes revisions to this document.

Table 25. Revision History

Revision	Date	Description
1	December 2007	• Initial public release.

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