TPS65266 2.7- to 6.5-V Input Voltage, 3-A/2-A/2-A Output Current Triple Synchronous Step-Down Converter

1 Features

- Operating Input Voltage Range 2.7 to 6.5 V
- Feedback Reference Voltage 0.6 V ±1%
- Maximum Continuous Output Current 3 A/2 A/2 A
- Dedicated Enable and Soft Start
- Accurate Start-Up Timing Control With Enable Pins Discharge
- Forced Continuous Current (FCC) Mode at Light Load
- Cycle-by-Cycle Current Limiting With Hiccup Mode Overcurrent Protection
- Adjustable Clock Frequency 250 kHz to 2.4 MHz
- External Clock Synchronization
- Power-Good Indicator
- Overtemperature Protection

2 Applications

- Printer and Scanner
- Digital TV
- Set Top Box
- Home Gateway and Access Point Networks
- Surveillance

3 Description

The TPS65266 incorporates 3 channels of high-efficiency synchronous buck converter for applications operating off the adaptor or battery with input voltage lower than 6.5 V.

The buck DC/DC converter integrates power MOSFETs for optimized power efficiency and reduces external component counts. The peak current mode control simplifies the compensation and fast transient response. High clock frequency allows smaller and low-value inductors and capacitors. External compensation supports optimized loop compensation and fast transient response. In light load condition, the buck converter operates in FCC mode for a reduction in noise susceptibility and RF interference. Cycle-by-cycle overcurrent limiting with hiccup mode limits MOSFET power dissipation in short circuit or overloading fault conditions.

The TPS65266 features a power-good supervisor circuit that monitors all converter outputs. The PGOOD pin is asserted after the output voltages in each channel are in regulation and sequencing is done.

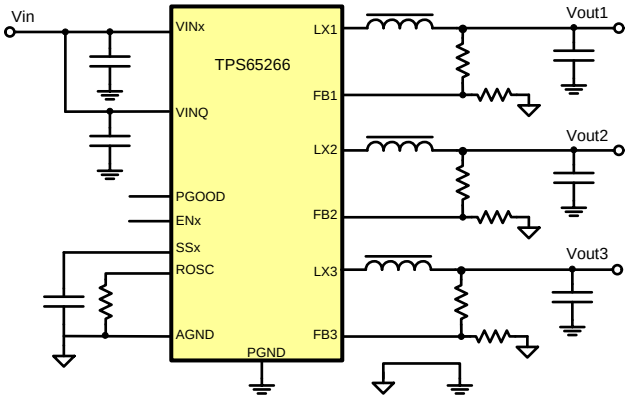
When continuous heavy overload or short circuit increases power dissipation in the buck converter, internal thermal protection circuit shuts off the device to prevent damage. Recovery from a thermal shutdown is automatic after the device has cooled sufficiently.

Device Information(1)

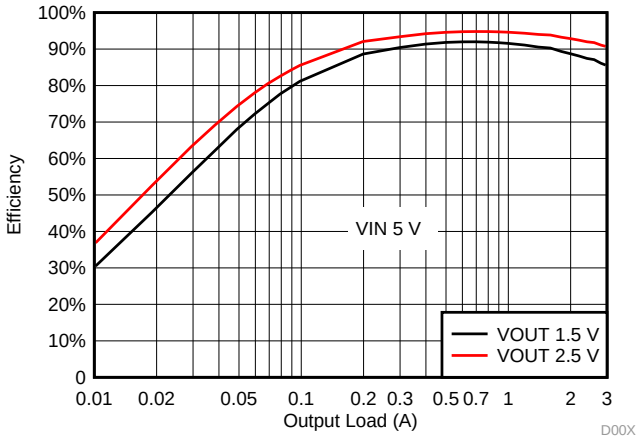
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS65266	VQFN (32)	5.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application Schematic



Efficiency vs Output Load



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

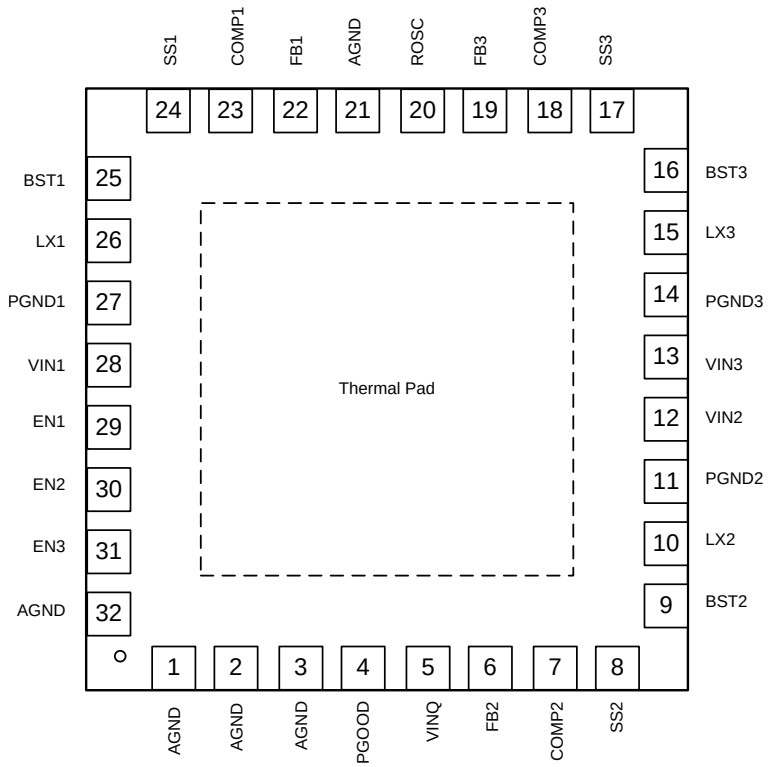
Changes from Revision A (December 2014) to Revision B	Page
• Updated device status to production data	1

Changes from Original (November 2014) to Revision A	Page
• Added note to $G_{m_PS1/2/3}$	6
• Added a step for type III compensation	26

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5 Pin Configuration and Functions

RHB PACKAGE
Top View



A. There is no electric signal down bonded to thermal pad inside IC. Exposed thermal pad must be soldered to PCB for optimal thermal performance.

Pin Functions

PIN		DESCRIPTION
NO.	NAME	
1	AGND	Analog ground pin
2	AGND	Analog ground pin
3	AGND	Analog ground pin
4	PGOOD	An open-drain output; asserts low if output voltage of bucks beyond regulation range due to thermal shutdown, over-current, under-voltage, or ENx low.
5	VINQ	Input voltage of converter controller and reference power supply bias. TI recommends to connect a 1-µF capacitor from the pin to analog ground and put the capacitor as near as possible to this pin.
6	FB2	Feedback Kelvin sensing pin for buck2 output voltage. Connect this pin to buck2 feedback resistor divider.
7	COMP2	Error amplifier output and loop compensation pin for buck2. Connect a series resistor and capacitor to compensate the control loop of buck converter 2 with peak current PWM mode.
8	SS2	Soft-start and tracking input for buck2 converter. An internal 5.5-µA pullup current source is connected to this pin. The soft-start time of buck2 can be programmed by connecting a capacitor between this pin and ground.
9	BST2	Boot strapped supply to the high-side floating gate driver in buck2 converter. Connect a capacitor (47 nF recommended) from BST2 pin to LX2 pin.
10	LX2	Switching node connection to the inductor and bootstrap capacitor for buck2 converter. The voltage swing at this pin is from a diode voltage below the ground up to VIN2 voltage.
11	PGND2	Power ground connection of buck2. Connect PGND2 pin as close as practical to the (–) terminal of VIN2 input ceramic capacitor.
12	VIN2	Input power supply for buck2. Connect VIN2 pin as close as practical to the (+) terminal of an input ceramic capacitor (10 µF suggested).

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Pin Functions (continued)

PIN		DESCRIPTION
NO.	NAME	
13	VIN3	Input power supply for buck3. Connect VIN3 pin as close as practical to the (+) terminal of an input ceramic capacitor (10 µF suggested).
14	PGND3	Power ground connection of buck3. Connect PGND3 pin as close as practical to the (–) terminal of VIN3 input ceramic capacitor.
15	LX3	Switching node connection to the inductor and bootstrap capacitor for buck3 converter. The voltage swing at this pin is from a diode voltage below the ground up to VIN3 voltage.
16	BST3	Boot strapped supply to the high-side floating gate driver in buck3 converter. Connect a capacitor (47 nF recommended) from BST3 pin to LX3 pin.
17	SS3	Soft-start and tracking input for buck3 converter. An internal 5.5-µA pullup current source is connected to this pin. The soft-start time of buck3 can be programmed by connecting a capacitor between this pin and ground.
18	COMP3	Error amplifier output and loop compensation pin for buck3. Connect a series resistor and capacitor to compensate the control loop of buck converter 3 with peak current PWM mode.
19	FB3	Feedback Kelvin sensing pin for buck3 output voltage. Connect this pin to buck3 feedback resistor divider.
20	ROSC	Oscillator frequency programmable pin. Connect an external resistor to set the switching frequency.
21	AGND	Analog ground common to buck controllers and other analog circuits. It must be routed separately from high-current power grounds to the (–) terminal of bypass capacitor of input voltage VINQ.
22	FB1	Feedback Kelvin sensing pin for buck1 output voltage. Connect this pin to buck1 feedback resistor divider.
23	COMP1	Error amplifier output and loop compensation pin for buck1. Connect a series resistor and capacitor to compensate the control loop of buck converter 1 with peak current PWM mode.
24	SS1	Soft-start and tracking input for buck1 converter. An internal 5.5-µA pullup current source is connected to this pin. The soft-start time of buck1 can be programmed by connecting a capacitor between this pin and ground.
25	BST1	Boot strapped supply to the high-side floating gate driver in buck1 converter. Connect a capacitor (47 nF recommended) from BST1 pin to LX1 pin.
26	LX1	Switching node connection to the inductor and bootstrap capacitor for buck1 converter. The voltage swing at this pin is from a diode voltage below the ground up to VIN1 voltage.
27	PGND1	Power ground connection of buck1. Connect PGND1 pin as close as practical to the (–) terminal of VIN1 input ceramic capacitor.
28	VIN1	Input power supply for buck1. Connect VIN1 pin as close as practical to the (+) terminal of an input ceramic capacitor (suggest 10 µF).
29	EN1	Enable for buck1 converter. Float to enable. Can use this pin to adjust the input undervoltage lockup of buck1 with resistors divider.
30	EN2	Enable for buck2 converter. Float to enable. Can use this pin to adjust the input undervoltage lockup of buck2 with resistors divider.
31	EN3	Enable for buck3 converter. Float to enable. Can use this pin to adjust the input undervoltage lockup of buck3 with resistors divider.
32	GND	Ground pin
—	Thermal PAD	No electric connection to any signal. Soldered to the ground in PCB for better thermal performance.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage at	VIN1, VIN2, VIN3, VINQ	–0.3	7	V
	LX1, LX2, LX3 (maximum withstand voltage transient <20 ns)	–1.0	7	
	BST1, BST2, BST3 referenced to LX1, LX2, LX3 pins respectively	–0.3	7	
	EN1, EN2, EN3, PGOOD	–0.3	7	
	FB1, FB2, FB3, COMP1 , COMP2, COMP3, SS1, SS2, SS3, ROSC	–0.3	3.6	
	AGND, PGND1, PGND2, PGND3	–0.3	0.3	
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Voltage at	VIN1, VIN2, VIN3, VINQ	2.7	6.5	V
	LX1, LX2, LX3 (maximum withstand voltage transient <20 ns)	–0.8	6.5	
	BST1, BST2, BST3 referenced to LX1, LX2, LX3 pins respectively	–0.1	6.5	
	EN1, EN2, EN3, PGOOD	–0.1	6.5	
	FB1, FB2, FB3, COMP1 , COMP2, COMP3, SS1, SS2, SS3, ROSC	–0.1	3	
T_J	Operating junction temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC (1)		TPS65266 RHB 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	27.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	8.3	
ψ_{JT}	Junction-to-top characterization parameter	0.4	
ψ_{JB}	Junction-to-board characterization parameter	8.3	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

T_A = 25°C, V_{IN} = 5 V, F_{SW} = 1 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY VOLTAGE						
VIN	Input voltage range		2.7		6.5	V
UVLO	VIN undervoltage lockout	VIN rising	2.35	2.45	2.6	V
		VIN falling	2.15	2.25	2.35	V
		Hysteresis		200		mV
IDD_{SDN}	Shutdown supply current	EN1 = EN2 = EN3 = 0 V		9		µA
IDD_{Q_NSW}	Input quiescent current without buck1/2/3 switching	EN1 = EN2 = EN3 = 5 V, FB1 = FB2 = FB3 = 0.8 V		790		µA
IDD_{Q_NSW1}		EN1 = 5 V, EN2 = EN3 = 0 V, FB1 = 0.8 V		340		µA
IDD_{Q_NSW2}		EN2 = 5 V, EN1 = EN3 = 0 V, FB2 = 0.8 V		340		µA
IDD_{Q_NSW3}		EN3 = 5 V, EN1 = EN2 = 0 V, FB3 = 0.8 V		340		µA
BUCK1, BUCK2, BUCK3						
V_{FB}	Feedback voltage	V_{COMP} = 1.2 V	0.594	0.6	0.606	V
V_{ENXH}	EN1/2/3 high-level input voltage			1.2	1.26	V
V_{ENXL}	EN1/2/3 low-level input voltage		1.1	1.15		V
I_{ENX1}	EN1/2/3 pullup current	ENx = 1 V	1.8	2.1	2.4	µA
I_{ENX2}	EN1/2/3 pullup current	ENx = 1.3 V		5.3		µA
I_{ENhys}	Hysteresis current			3.2		µA
I_{SSX}	Soft-start charging current		4.5	5.5	6.5	µA
t_{ON_MIN}	Minimum on-time			80	100	ns
G_{m_EA}	Error amplifier transconductance	–2 µA < I_{COMPX} < 2 µA		290		µS
$G_{m_PS1/2/3}$	COMP1/2/3 voltage to inductor current G_m (1)	I_{LX} = 0.5 A		10		A/V
I_{LIMIT1}	Buck1 peak inductor current limit		3.9	4.6	5.3	A
$I_{LIMITSINK1}$	Buck1 low-side sink current limit			1.4		
$I_{LIMIT2/3}$	Buck2/3 peak inductor current limit		2.5	3.1	3.7	A
$I_{LIMITSINK2/3}$	Buck2/3 low-side sink current limit			1.2		A
Rdson_HS1	Buck1 high-side switch resistance	VINQ = 5 V		45		mΩ
Rdson_LS1	Buck1 low-side switch resistance	VINQ = 5 V		50		mΩ
Rdson_HS2	Buck2 high-side switch resistance	VINQ = 5 V		60		mΩ
Rdson_LS2	Buck2 low-side switch resistance	VINQ = 5 V		60		mΩ
Rdson_HS3	Buck3 high-side switch resistance	VINQ = 5 V		60		mΩ
Rdson_LS3	Buck3 low-side switch resistance	VINQ = 5 V		60		mΩ
HICCUP TIMING						
t_{Hiccup_wait}	Overcurrent wait time (1)			512		cycles
t_{Hiccup_re}	Hiccup time before restart (1)			16382		cycles
POWER GOOD						
V_{th_PG}	Feedback voltage threshold	FBx undervoltage falling		92.5		%VREF
		FBx undervoltage rising		95		%VREF
$t_{DEGLITCH(PG)_F}$	PGOOD falling edge deglitch time			128		cycles
$t_{RDEGLITCH(PG)_R}$	PGOOD rising edge deglitch time			16350		cycles
I_{PG}	PGOOD pin leakage				1	µA
V_{LOW_PG}	PGOOD pin low voltage	I_{SINK} = 1 mA			0.4	V

(1) Lab validation result

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Electrical Characteristics (continued)

T_A = 25°C, V_{IN} = 5 V, F_{SW} = 1 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OSCILLATOR						
F_{SW}	Switching frequency	R_{OSC} = 51.1 kΩ	920	1000	1080	kHz
F_{SW_range}	Switching frequency		250		2400	kHz
F_{SYNC}	Clock sync frequency range		250		2400	kHz
t_{SYNC_w}	Clock sync minimum pulse duration		80			ns
F_{SYNC_HI}	Clock sync high threshold				2	V
V_{SYNC_LO}	Clock sync low threshold		0.4			V
THERMAL PROTECTION						
T_{TRIP_OTP} (1)	Thermal protection trip point	Temperature rising		160		°C
T_{HYST_OTP} (1)		Hysteresis		20		°C

6.6 Typical Characteristics

T_A = 25°C, V_{IN} = 5 V, V_{OUT1} = 1.0 V, V_{OUT2} = 1.5 V, V_{OUT3} = 1.8 V F_{SW} = 1 MHz (unless otherwise noted)

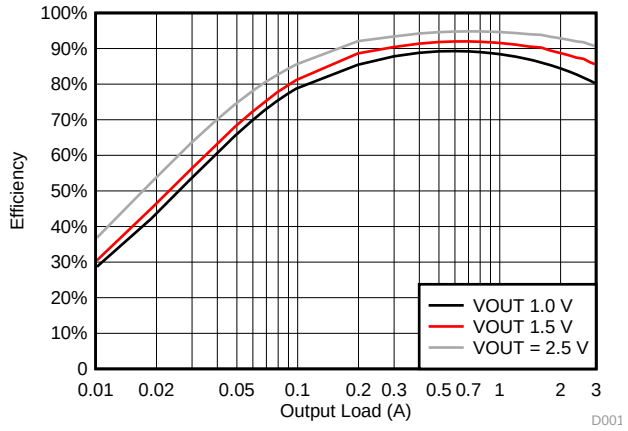


Figure 1. Buck1 Efficiency

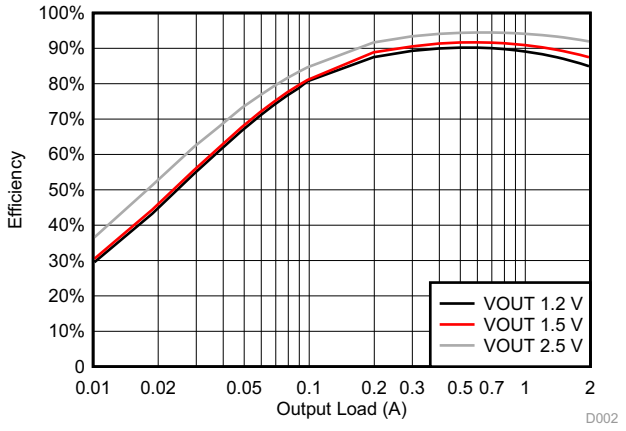


Figure 2. Buck2 Efficiency

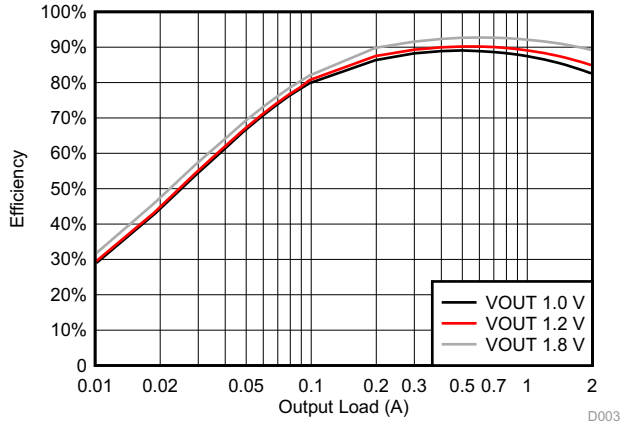


Figure 3. Buck3 Efficiency

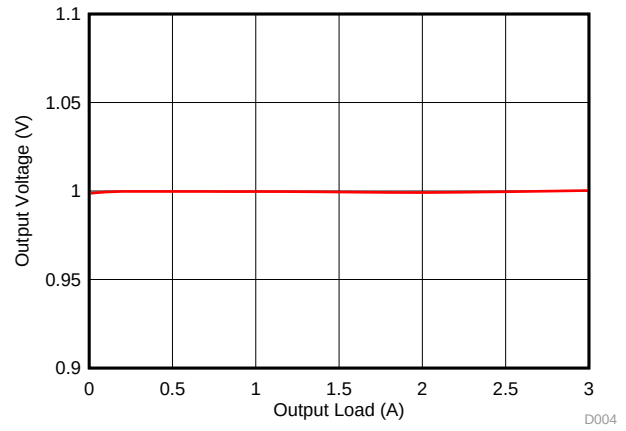


Figure 4. Buck1, Load Regulation

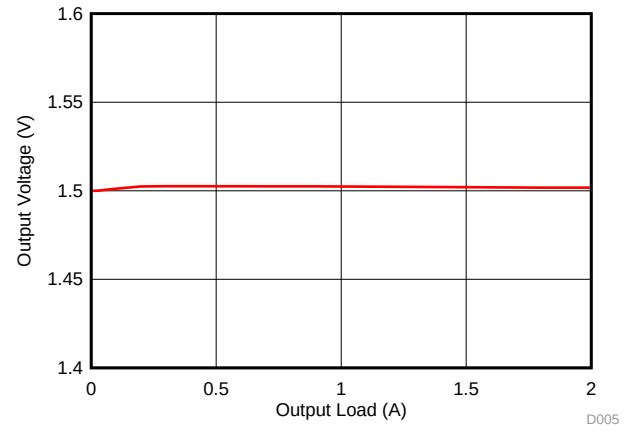


Figure 5. Buck2, Load Regulation

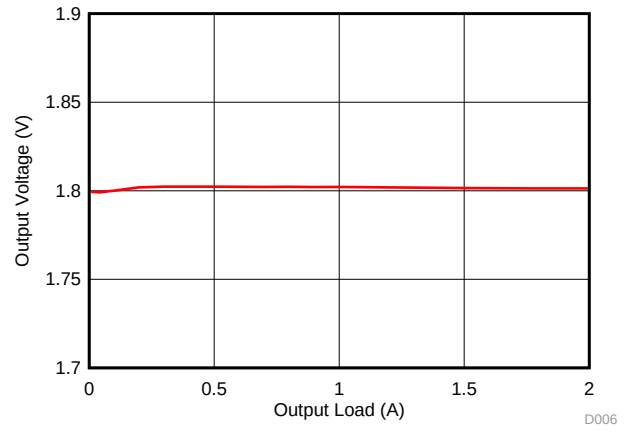


Figure 6. Buck3, Load Regulation

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Typical Characteristics (continued)

T_A = 25°C, V_{IN} = 5 V, V_{OUT1} = 1.0 V, V_{OUT2} = 1.5 V, V_{OUT3} = 1.8 V F_{SW} = 1 MHz (unless otherwise noted)

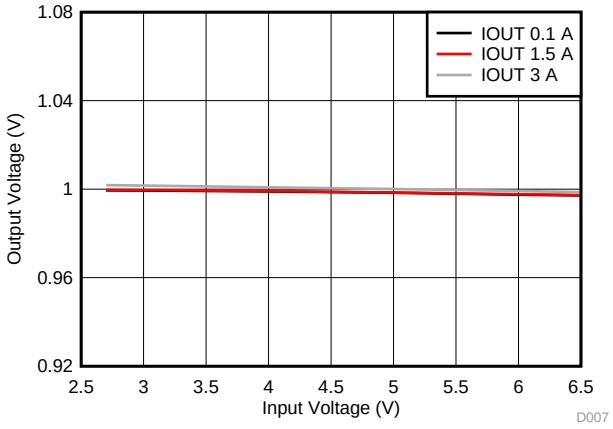


Figure 7. Buck1, Line Regulation

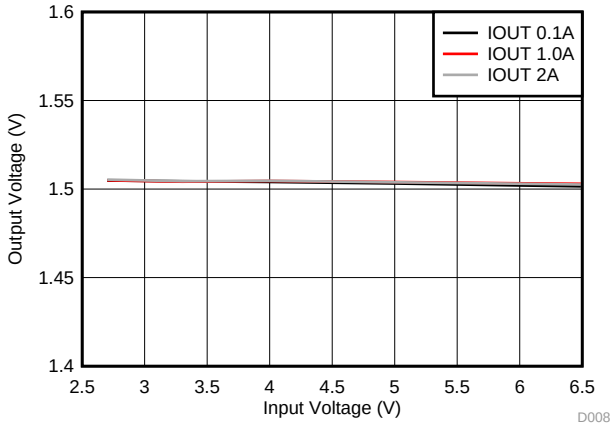


Figure 8. Buck2, Line Regulation

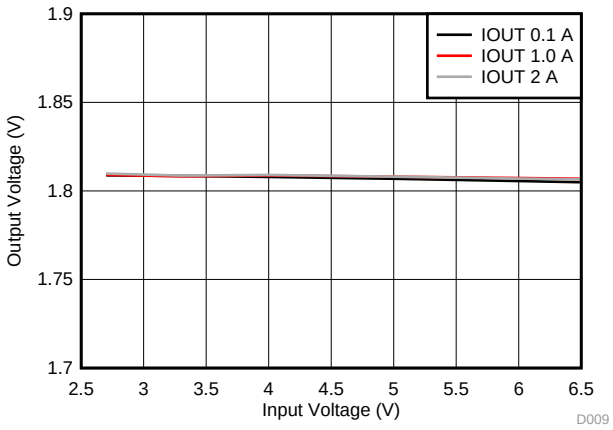


Figure 9. Buck3, Line Regulation

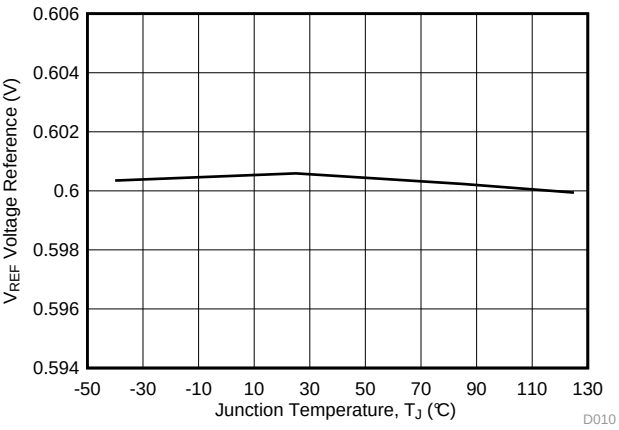


Figure 10. Voltage Reference vs Temperature

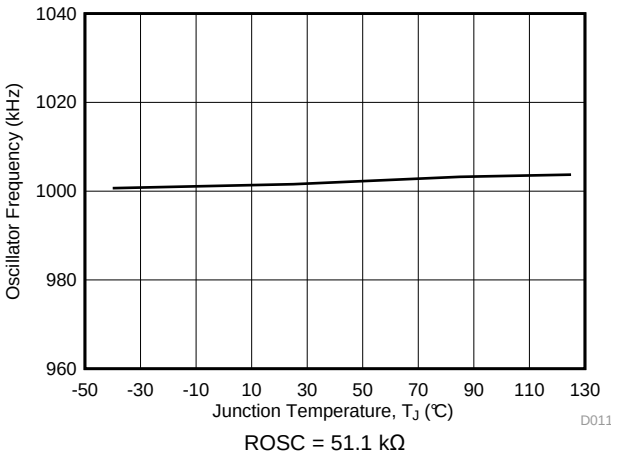


Figure 11. Oscillator Frequency vs Temperature

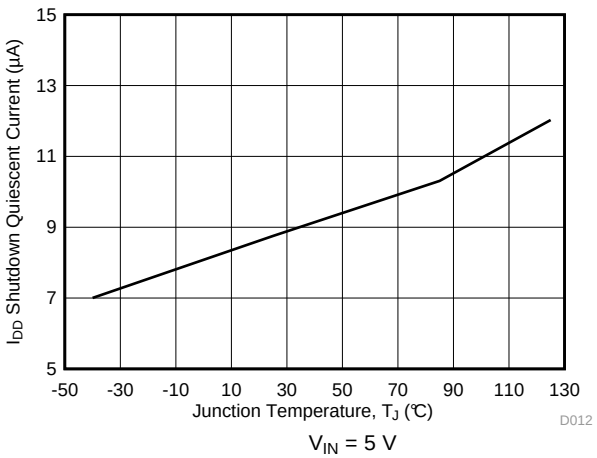


Figure 12. Shutdown Quiescent Current vs Temperature

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Typical Characteristics (continued)

T_A = 25°C, V_{IN} = 5 V, V_{OUT1} = 1.0 V, V_{OUT2} = 1.5 V, V_{OUT3} = 1.8 V F_{SW} = 1 MHz (unless otherwise noted)

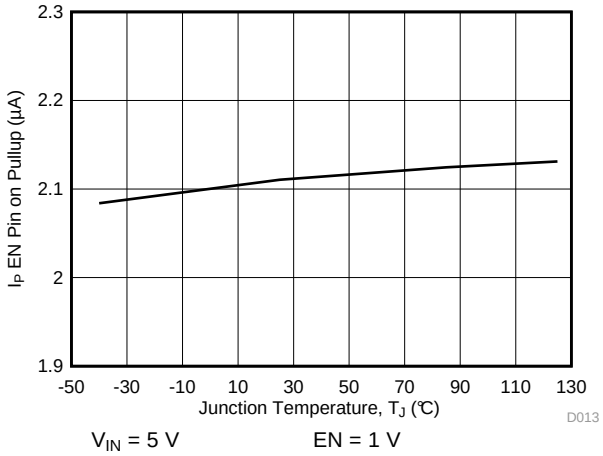


Figure 13. EN Pin Pullup Current vs Temperature, EN = 1 V

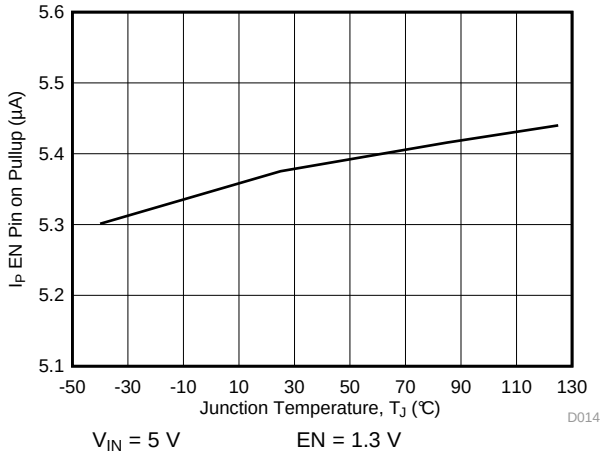


Figure 14. EN Pin Pullup Current vs Temperature, EN = 1.3 V

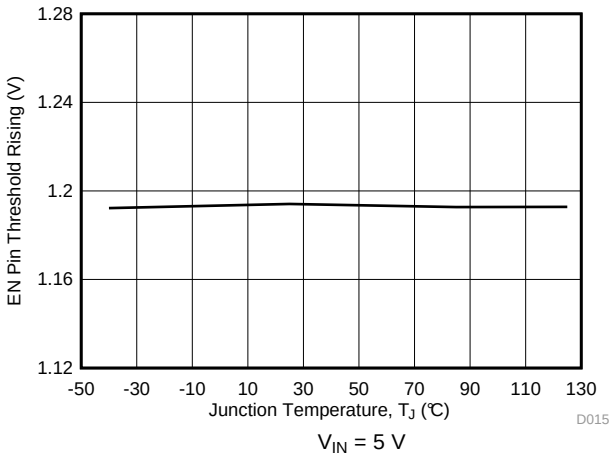


Figure 15. EN Pin Threshold Rising vs Temperature

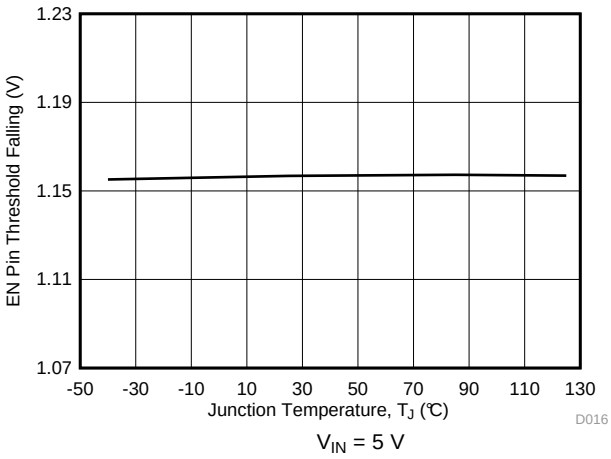


Figure 16. EN Pin Threshold Falling vs Temperature

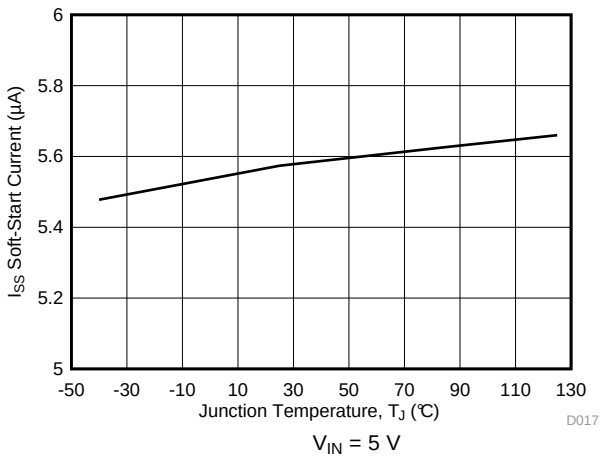


Figure 17. SS Pin Charge Current vs Temperature

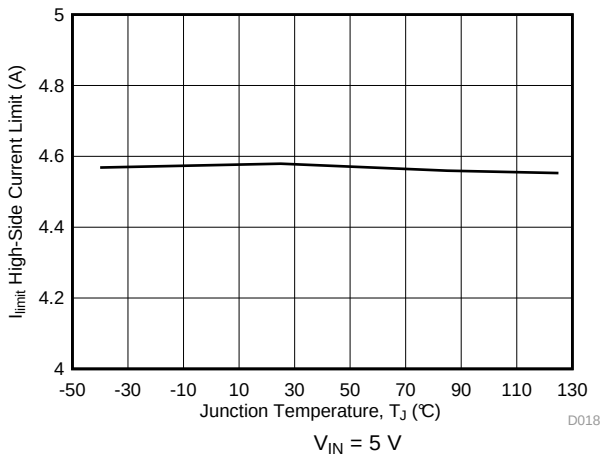


Figure 18. Buck1 High-Side Current Limit vs Temperature

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Typical Characteristics (continued)

T_A = 25°C, V_{IN} = 5 V, V_{OUT1} = 1.0 V, V_{OUT2} = 1.5 V, V_{OUT3} = 1.8 V F_{SW} = 1 MHz (unless otherwise noted)

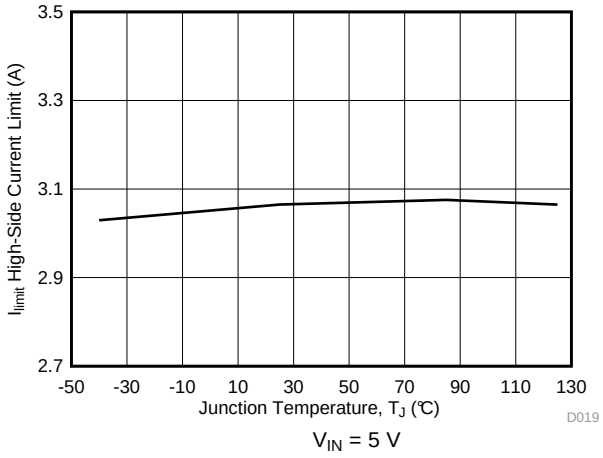


Figure 19. Buck2 High-Side Current Limit vs Temperature

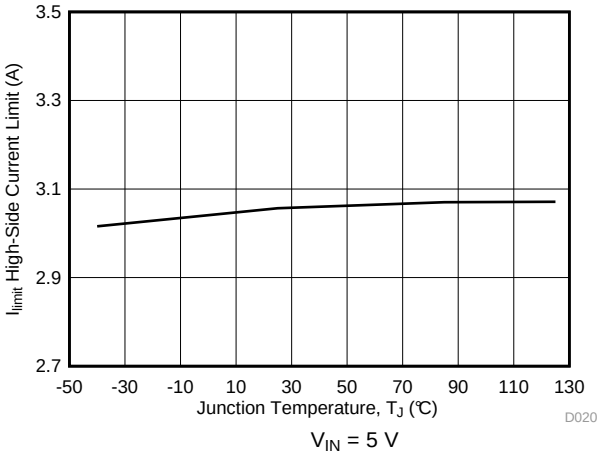


Figure 20. Buck3 High-Side Current Limit vs Temperature

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7 Detailed Description

7.1 Overview

The TPS65266 is a triple 3-A/2-A/2-A output current, synchronous step-down (buck) converter for applications operating off the adaptor or battery with input voltage lower than 6.5 V. The feedback voltage reference for each buck is 0.6 V. Each buck is independent with dedicated enable, soft-start, and loop compensation. The TPS65266 implements a constant frequency, peak current mode control that simplifies external loop compensation. The switch clock of buck1 is 180° out-of-phase operation from the clock of buck2 and buck3 channels to reduce input current ripple, input capacitor size and power-supply-induced noise.

The TPS65266 has been designed for safe monotonic startup into prebiased loads. The default start-up is when VIN is typically 2.45 V. The ENx pin has an internal pullup current source that can be used to adjust the input voltage undervoltage lockout (UVLO) with two external resistors. In addition, the EN pin can be floating for automatically starting up the converters with the internal pullup current.

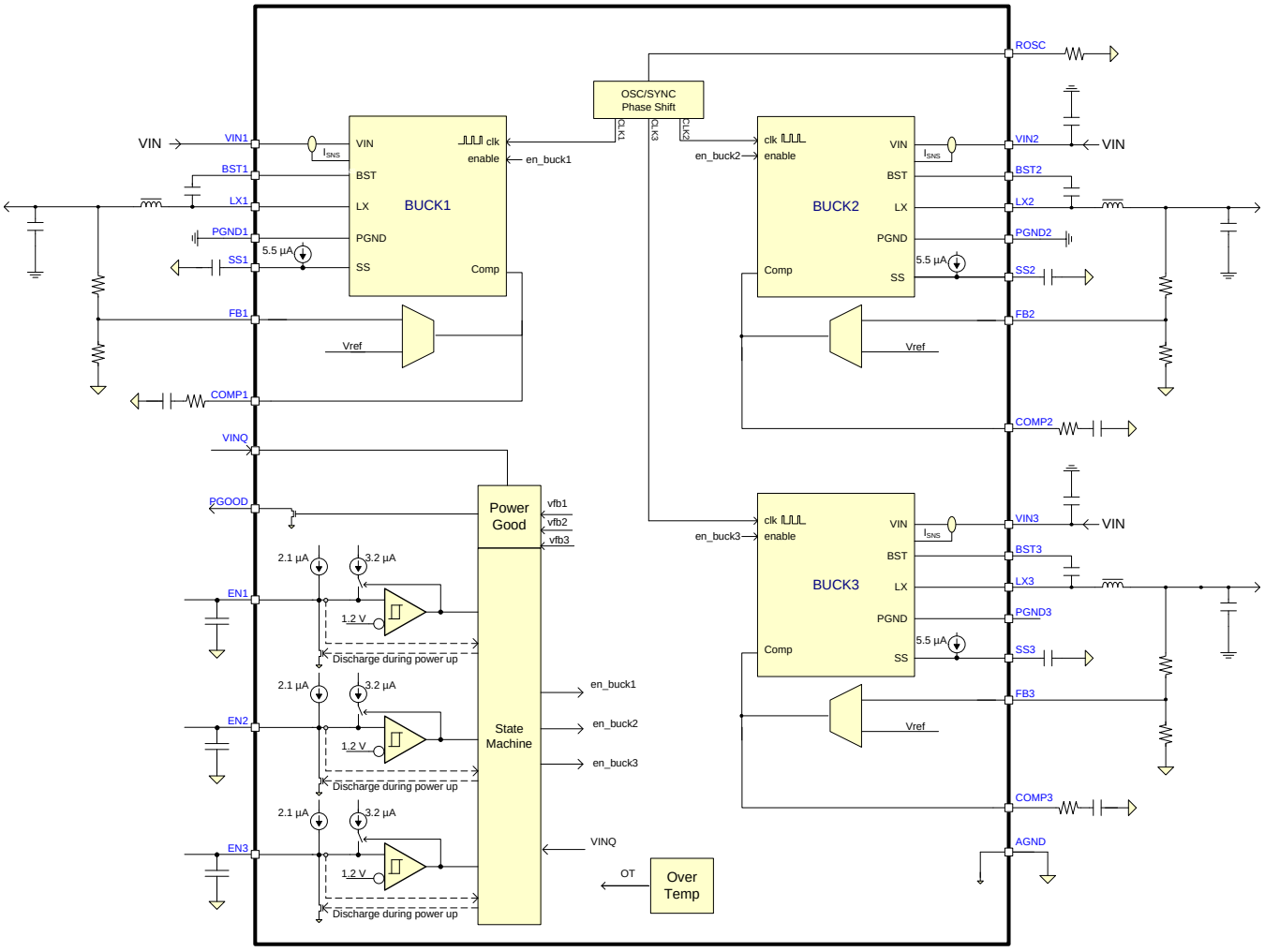
The TPS65266 features PGOOD pin to supervise output voltages of buck converter. The TPS65266 has power-good comparators with hysteresis, which monitor the output voltages through internal feedback voltages. When all bucks are in regulation range and power sequence is done, PGOOD is asserted high.

The SS (soft-start/tracking) pin is used to minimize inrush currents or provide power-supply sequencing during power up. A small-value capacitor or resistor divider should be coupled to the pin for soft start or critical power-supply sequencing requirements.

The TPS65266 is protected from overload and thermal fault conditions.

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7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Adjusting the Output Voltage

The output voltage of each buck is set with a resistor divider from the output of buck to the FB pin. TI recommends to use 1% tolerance or better resistors.

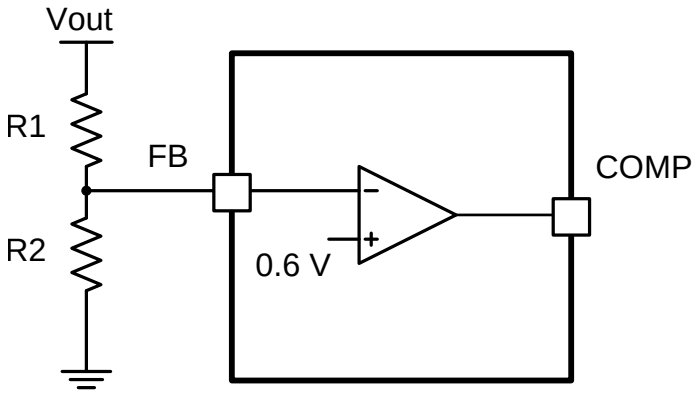


Figure 21. Voltage Divider Circuit

Feature Description (continued)

$$R_2 = R_1 \times \frac{0.6}{V_{out} - 0.6} \quad (1)$$

To improve efficiency at light loads, consider using larger-value resistors. If the values are too high, the regulator is more sensitive to noise. Table 1 shows the recommended resistor values.

Table 1. Output Resistor Divider Selection

Output Voltage (V)	R1 (kΩ)	R2 (kΩ)
1	10	15
1.2	10	10
1.5	15	10
1.8	20	10
2.5	31.6	10
3.3	45.3	10
3.3	22.6	4.99
5	73.2	10
5	36.5	4.99

7.3.2 Enable and Adjusting UVLO

The EN1/2/3 pin provides electrical on and off control of the device. After the EN1/2/3 pin voltage exceeds the threshold voltage, the device starts operation. If each ENx pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low I_q state.

The EN pin has an internal pullup current source, allowing the user to float the EN pin for enabling the device. If an application requires controlling the EN pin, use open-drain or open-collector output logic to interface with the pin.

The device implements internal UVLO circuitry on the VINQ pin. The device is disabled when the VINQ pin voltage falls below the internal VIN UVLO threshold. The internal VIN UVLO threshold has a hysteresis of 200 mV. If an application requires either a higher UVLO threshold on the VINQ pin or a secondary UVLO on the VINx, in split-rail applications, then the ENx pin can be configured as shown in Figure 22, Figure 23, and Figure 24. When using the external UVLO function, TI recommends to set the hysteresis to be >200 mV.

The EN pin has a small pullup current I_p, which sets the default state of the pin to enable when no external components are connected. The pullup current is also used to control the voltage hysteresis for the UVLO function because it increases by I_h after the EN pin crosses the enable threshold. Calculate the UVLO thresholds using Equation 2 and Equation 3.

$$R_1 = \frac{V_{START}\left(\frac{V_{ENFALLING}}{V_{ENRISING}}\right) - V_{STOP}}{I_P\left(1 - \frac{V_{ENFALLING}}{V_{ENRISING}}\right) + I_h}$$

$$R_2 = \frac{R_1 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R_1(I_h + I_p)} \quad (2)$$

where

- I_h = 3.2 µA
- I_p = 2.1 µA
- $V_{ENRISING}$ = 1.2 V
- $V_{ENFALLING}$ = 1.15 V (3)

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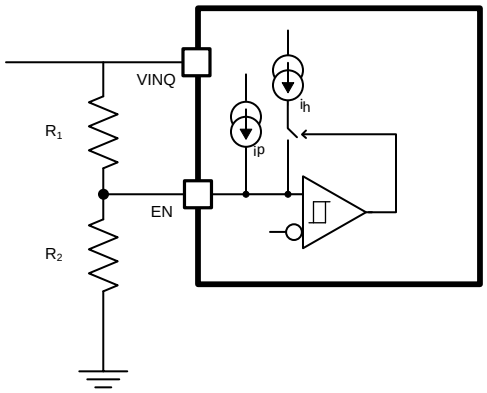


Figure 22. Adjustable VINQ UVLO

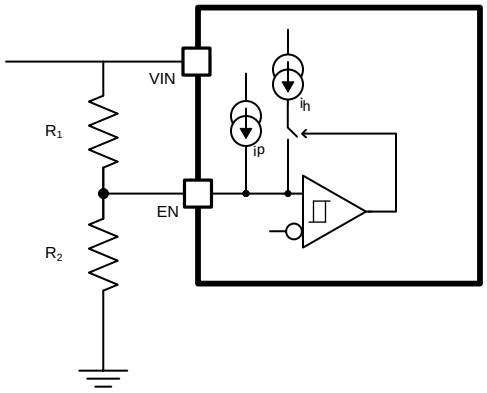


Figure 23. Adjustable VIN UVLO, VINQ > 2.7 V

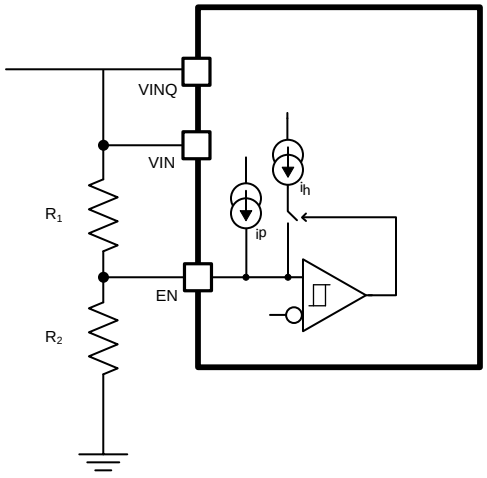


Figure 24. Adjustable VIN and VINQ UVLO

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7.3.3 Soft-Start Time

The voltage on the respective SS pin controls the start-up of buck output. When the voltage on the SS pin is less than the internal 0.6-V reference, the TPS65266 regulates the internal feedback voltage to the voltage on the SS pin instead of 0.6 V. The SS pin can be used to program an external soft-start function or to allow output of buck to track another supply during start-up. The device has an internal pullup current source of 5.5 µA (typical) that charges an external soft-start capacitor to provide a linear ramping voltage at SS pin. The TPS65266 regulates the internal feedback voltage to the voltage on the SS pin, allowing VOUT to rise smoothly from 0 V to its regulated voltage without inrush current. Calculate the approximate soft-start time with Equation 4.

$$t_{ss}\,(ms) = \frac{Css\,(nF) \times Vref\,(V)}{Iss\,(\mu A)} \tag{4}$$

Many of the common power-supply sequencing methods can be implemented using the SSx and ENx pins. Figure 25 shows the method implementing ratiometric sequencing by connecting the SSx pins of three buck channels together. The regulator outputs ramp up and reach regulation at the same time. When calculating the soft-start time, the pullup current source must be tripled in Equation 4.

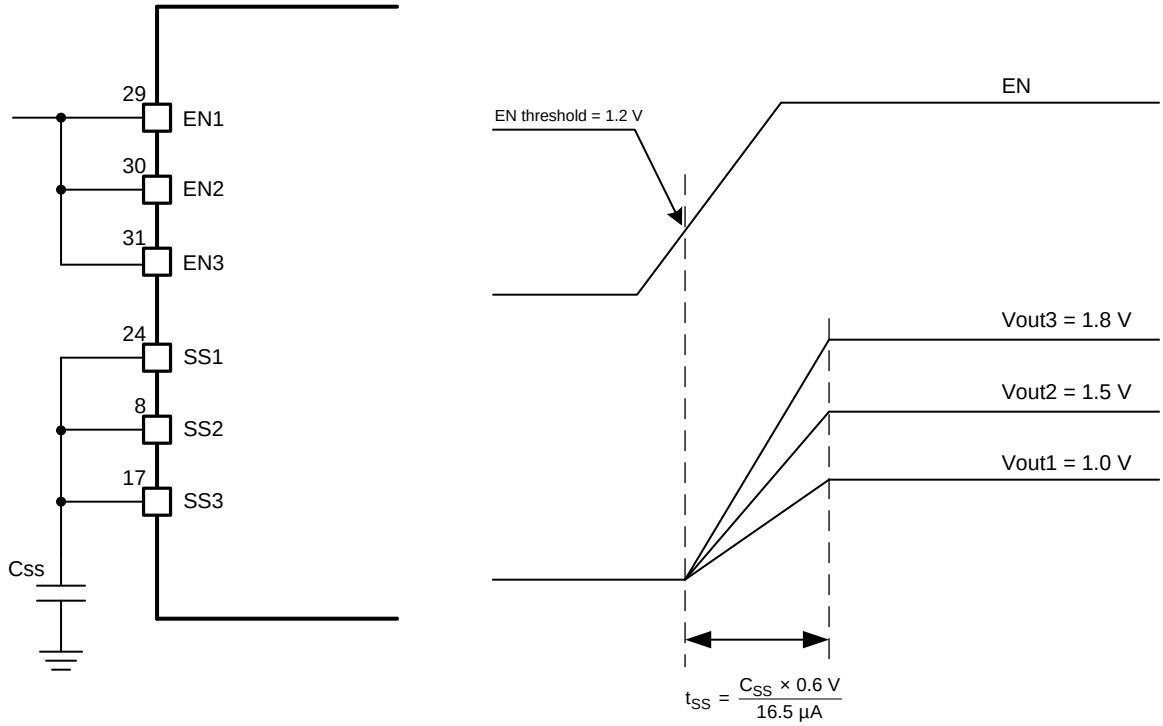


Figure 25. Ratiometric Power-Up Using SSx Pins

Simultaneous power-supply sequencing can be implemented by connecting capacitor to SSx pin, shown in Figure 26. Using Equation 4 and Equation 5, calculate the capacitors.

$$\frac{Css1}{Vout1} = \frac{Css2}{Vout2} = \frac{Css3}{Vout3} \tag{5}$$

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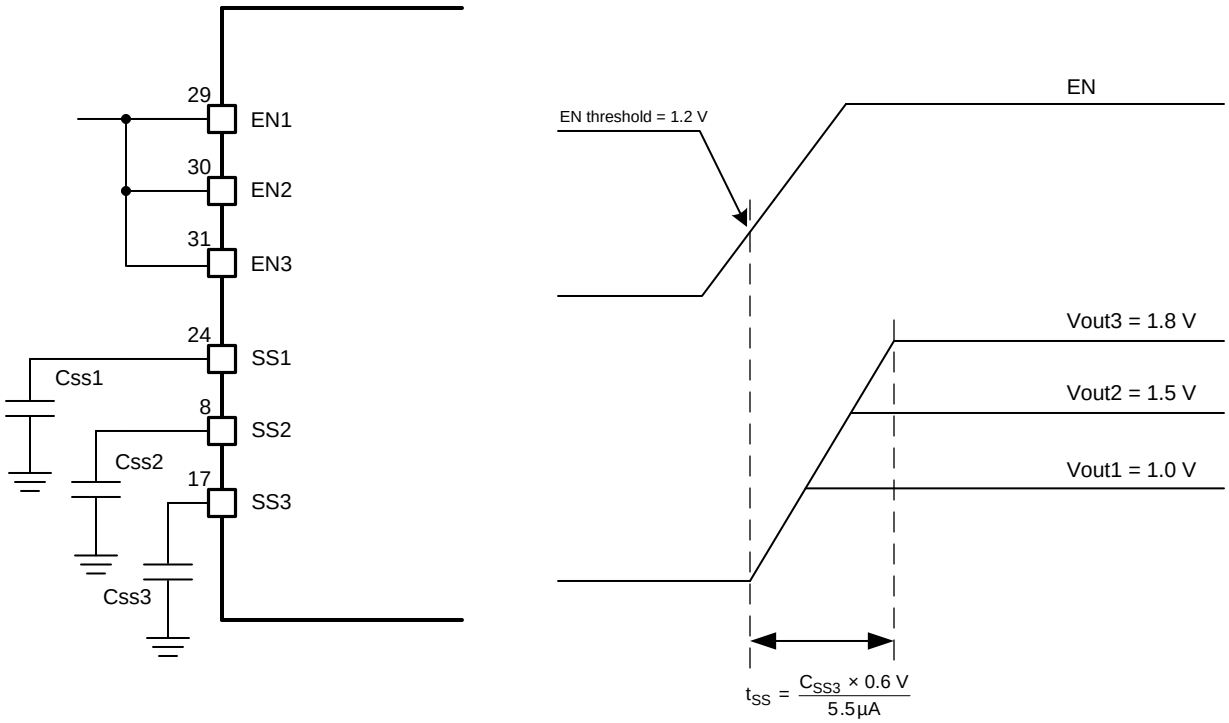


Figure 26. Simultaneous Startup Sequence Using SSx Pins

7.3.4 Power-Up Sequencing

The TPS65266 has a dedicated enable pin and soft-start pin for each converter. The converter enable pins are biased by a current source that allows for easy sequencing by the addition of an external capacitor. Enable pins have a discharge function, which ensures power-up sequencing is effective at quickly powering down and up status. Disabling the converter with an active pulldown transistor on the ENs pin allows for a predictable power-down timing operation. Figure 27 shows the timing diagram of a typical buck power-up sequence with connecting a capacitor at ENx pin.

When VINQ pin voltage rises to about 1 V, the internal EN turns on and a typical 1.4-µA current is charging ENx pin from input supply. If any of the EN pin voltages reaches 0.5 V when powered up, three EN pin discharge functions are triggered and keep 2 ms with discharge resistor around 1.2 kΩ to GND, then a 2.1-µA pullup current is sourcing ENx. After ENx pin voltage reaches to ENx enabling threshold, 3.2-µA hysteresis current sources to the pin to improve noise sensitivity.

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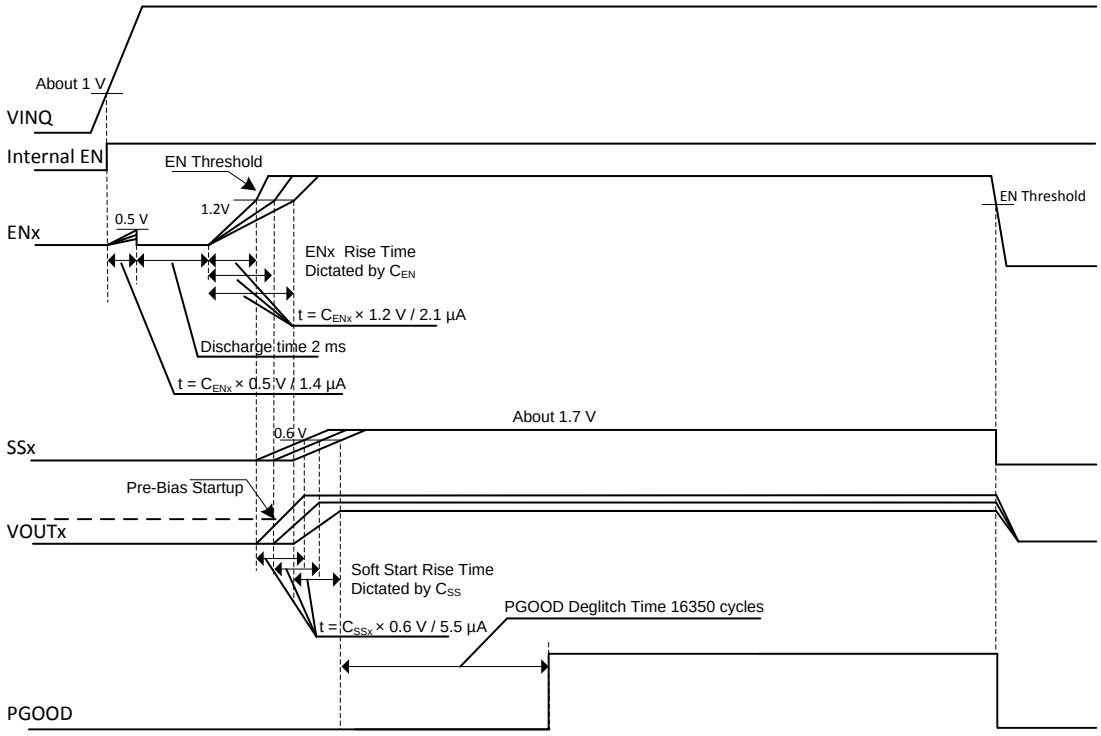


Figure 27. Startup Power Sequence

7.3.5 Boostrap Voltage and BST-LX UVLO

Each high-side MOSFET driver is biased from the floating bootstrap capacitor, CB, shown in Figure 28, which is normally recharged during each cycle through an internal low-side MOSFET or the body diode of a low-side MOSFET when the high-side MOSFET turns off. The boot capacitor is charged when the BST pin voltage is less than VIN and BST-LX voltage is below regulation. The recommended value of this ceramic capacitor is 47 nF. TI recommends a ceramic capacitor with an X7R- or X5R-grade dielectric with a voltage rating of 10 V or higher because of the stable characteristics over temperature and voltage.

To improve dropout, the device is designed to operate at 100% duty cycle as long as the BST to LX pin voltage is greater than the BST-LX UVLO threshold, which is typically 2.1 V. When the voltage between BST and LX drops below the BST-LX UVLO threshold, the high-side MOSFET is turned off and the low-side MOSFET is turned on allowing the boot capacitor to be recharged.

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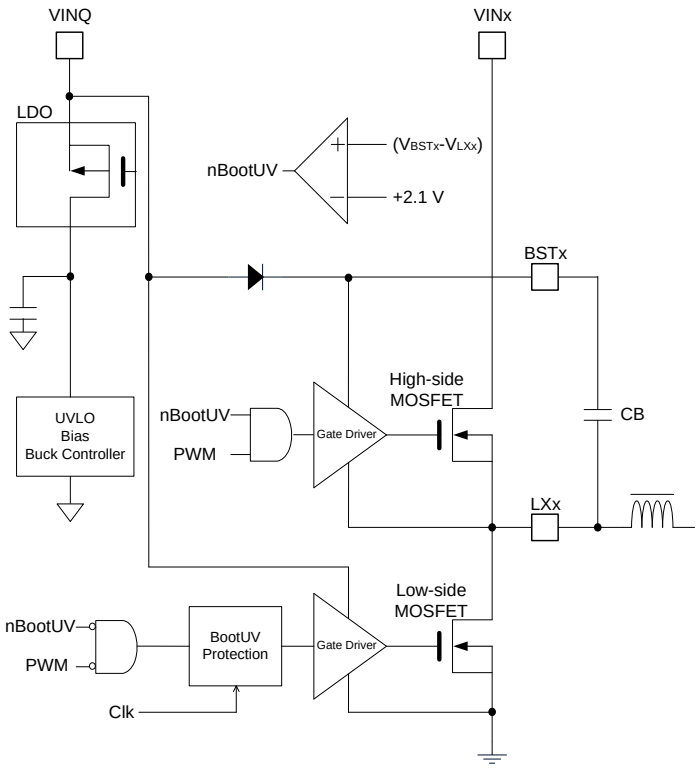


Figure 28. Bootstrap Voltage and Diagram

7.3.6 Out of Phase Operation

To reduce input ripple current, the switch clock of buck1 is 180° out-of-phase from the clock of buck2 and buck3. This enables the system by having less input current ripple to reduce input capacitors' size, cost, and EMI.

7.3.7 Output Overvoltage Protection (OVP)

The device incorporates an OVP circuit to minimize output voltage overshoot. When the output is overloaded, the error amplifier compares the actual output voltage to the internal reference voltage. If the FB pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier demands maximum output current. After the condition is removed, the regulator output rises and the error amplifier output transitions to the steady-state voltage. In some applications with small output capacitance, the load can respond faster than the error amplifier. This leads to the possibility of an output overshoot. Each buck compares the FB pin voltage to the OVP threshold. If the FB pin voltage is greater than the OVP threshold, the high-side MOSFET is turned off preventing current from flowing to the output and minimizing output overshoot. When the FB voltage drops lower than the OVP threshold, the high-side MOSFET turns on at the next clock cycle.

7.3.8 Slope Compensation

To prevent the subharmonic oscillations when the device operates at duty cycles greater than 50%, the TPS65266 adds built-in slope compensation, which is a compensating ramp to the switch current signal.

7.3.9 Overcurrent Protection

The device is protected from overcurrent conditions by cycle-by-cycle current limiting on both the high-side MOSFET and low-side MOSFET.

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7.3.9.1 High-Side MOSFET Overcurrent Protection

The device implements current mode control, which uses the COMP pin voltage to control the turn off of the high-side MOSFET and the turn-on of the low-side MOSFET on a cycle-by-cycle basis. Each cycle the switch current and the current reference generated by the COMP pin voltage are compared, when the peak switch current intersects the current reference, the high-side switch is turned off.

7.3.9.2 Low-Side MOSFET Overcurrent Protection

While the low-side MOSFET is turned on, its conduction current is monitored by the internal circuitry. During normal operation the low-side MOSFET sources current to the load. At the end of every clock cycle, the low-side MOSFET sourcing current is compared to the internally set low-side sourcing current limit. If the low-side sourcing current is exceeded, the high-side MOSFET is not turned on and the low-side MOSFET stays on for the next cycle. The high-side MOSFET is turned on again when the low-side current is below the low-side sourcing current limit at the start of a cycle.

The low-side MOSFET may also sink current from the load. If the low-side sinking current limit is exceeded, the low-side MOSFET is turned off immediately for the rest of that clock cycle. In this scenario, both MOSFETs are off until the start of the next cycle.

Furthermore, if an output overload condition (as measured by the COMP pin voltage) has lasted for more than the hiccup wait time, which is programmed for 512 cycles (typical) shown in Figure 29, the device shuts down itself and restarts after the hiccup time of 16382 cycles (typical). The hiccup mode helps to reduce the device power dissipation under a severe overcurrent condition.

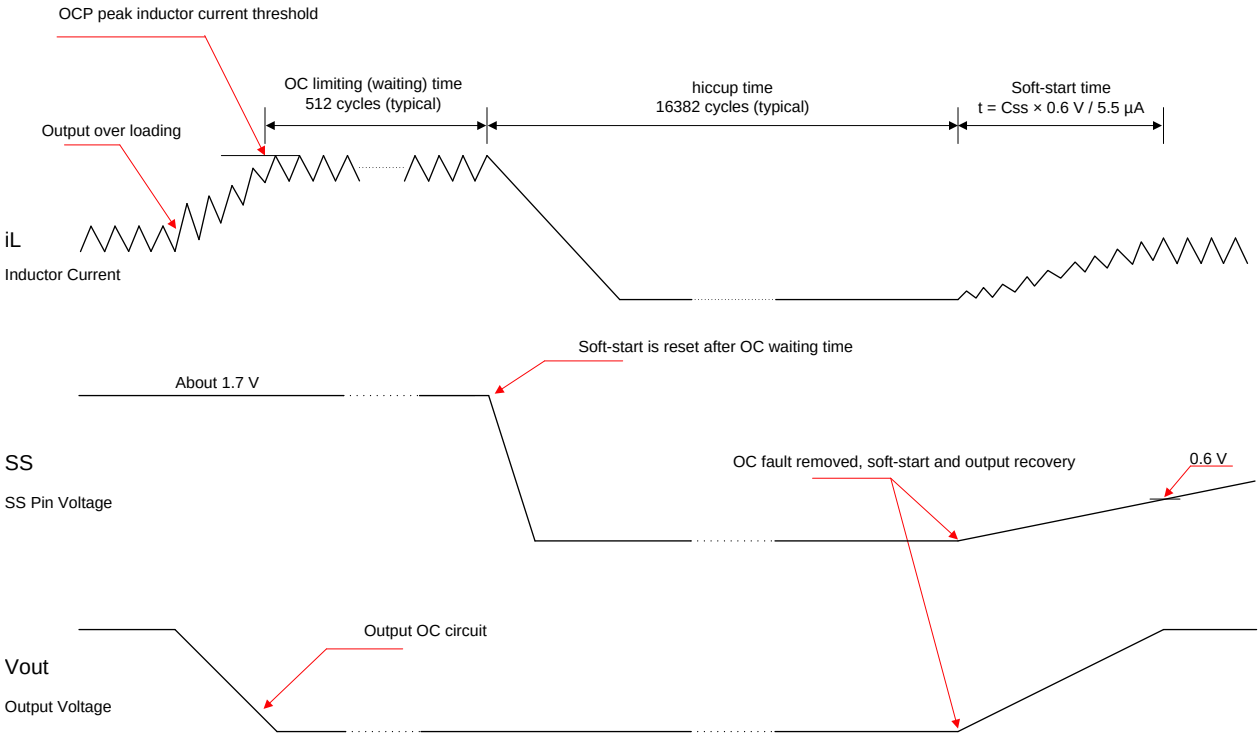


Figure 29. Overcurrent Protection

7.3.10 Power Good

The PGOOD pin is an open-drain output. After the feedback voltage of each buck is higher than 95% (rising) of the internal voltage reference, the PGOOD pin pulldown is deasserted and the pin floats. TI recommends to use a pullup resistor between the values of 10 kΩ and 100 kΩ to a voltage source that is 5.0 V or less.

The PGOOD pin is pulled low when any feedback voltage of a buck is lower than 92.5% (falling) of the nominal internal reference voltage. Also, the PGOOD is pulled low if the input voltage is undervoltage locked up, thermal shutdown is asserted, the EN pin is pulled low, or the converter is in a soft-start period.

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7.3.11 Adjustable Switching Frequency

The ROSC pin can be used to set the switching frequency by connecting a resistor to GND. The switching frequency of the device is adjustable from 250 kHz to 2.4 MHz.

To determine the ROSC resistance for a given switching frequency, use Equation 6 or the curve in Figure 30. To reduce the solution size, the user should set the switching frequency as high as possible, but consider the tradeoffs of the supply efficiency and minimum controllable on-time.

$$f_{osc}\,(\text{kHz}) = 46657 \times R\,(\text{k}\Omega)^{-0.976} \quad (6)$$

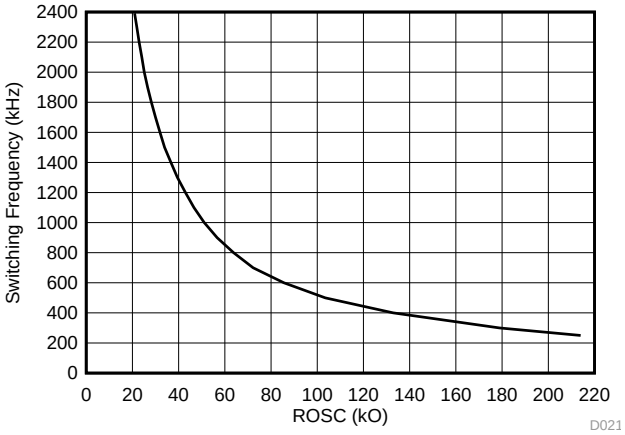


Figure 30. ROSC vs Switching Frequency

When an external clock applies to the ROSC pin, the internal phase locked loop (PLL) has been implemented to allow internal clock synchronizing to an external clock between 250 kHz and 2.4 MHz. To implement the clock synchronization feature, connect a square wave clock signal to the ROSC pin with a duty cycle between 20% to 80%. The clock signal amplitude must transition lower than 0.4 V and higher than 2.0 V. The start of the switching cycle is synchronized to the falling edge of the ROSC pin.

In applications where both resistor mode and synchronization mode are needed, the device can be configured as shown in Figure 31. Before an external clock is present, the device works in resistor mode and ROSC resistor sets the switching frequency. When an external clock is present, the synchronization mode overrides the resistor mode. The first time the ROSC pin is pulled above the ROSC high threshold (2.0 V), the device switches from the resistor mode to the synchronization mode and the ROSC pin becomes high impedance as the PLL starts to lock onto the frequency of the external clock. TI does not recommended to switch from synchronization mode back to resistor mode because the internal switching frequency drops to 100 kHz first before returning to the switching frequency set by ROSC resistor.

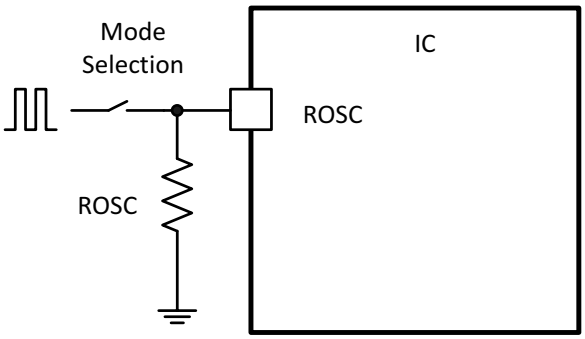


Figure 31. Works With Resistor Mode and Synchronization Mode

7.3.12 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 160°C typically. The device reinitiates the power-up sequence when the junction temperature drops below 140°C typically.

7.4 Device Functional Modes

7.4.1 Operation With V_{IN} < 2.6 V (Minimum V_{IN})

The device operates with input voltages above 2.6 V. The maximum UVLO voltage is 2.6 V and will operate at input voltages above 2.6 V. The typical UVLO voltage is 2.45 V and the device may operate at input voltages above that point. The device also may operate at lower input voltages, the minimum UVLO voltage is 2.35 V (rising) and 2.15V (falling). At input voltages below the UVLO minimum voltage, the devices will not operate.

7.4.2 Operation With EN Control

The enable rising edge threshold voltage is 1.2 V typical and 1.26 V maximum. With EN held below that voltage the device is disabled and switching is inhibited. The IC quiescent current is reduced in this state. When input voltage is above the UVLO threshold and the EN voltage is increased above the rising edge threshold, the device becomes active. Switching is enabled, and the soft start sequence is initiated. The device will start at the soft start time determined by the external soft start capacitor as shown in Figure 34 to Figure 36.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The device is a triple-synchronous step-down DC/DC converter. It is typically used to convert a higher DC voltage to lower DC voltages with a continuously available output current of 3 A/2 A/2 A. The following design procedure can be used to select component values for the TPS65266. This section presents a simplified discussion of the design process.

8.2 Typical Application

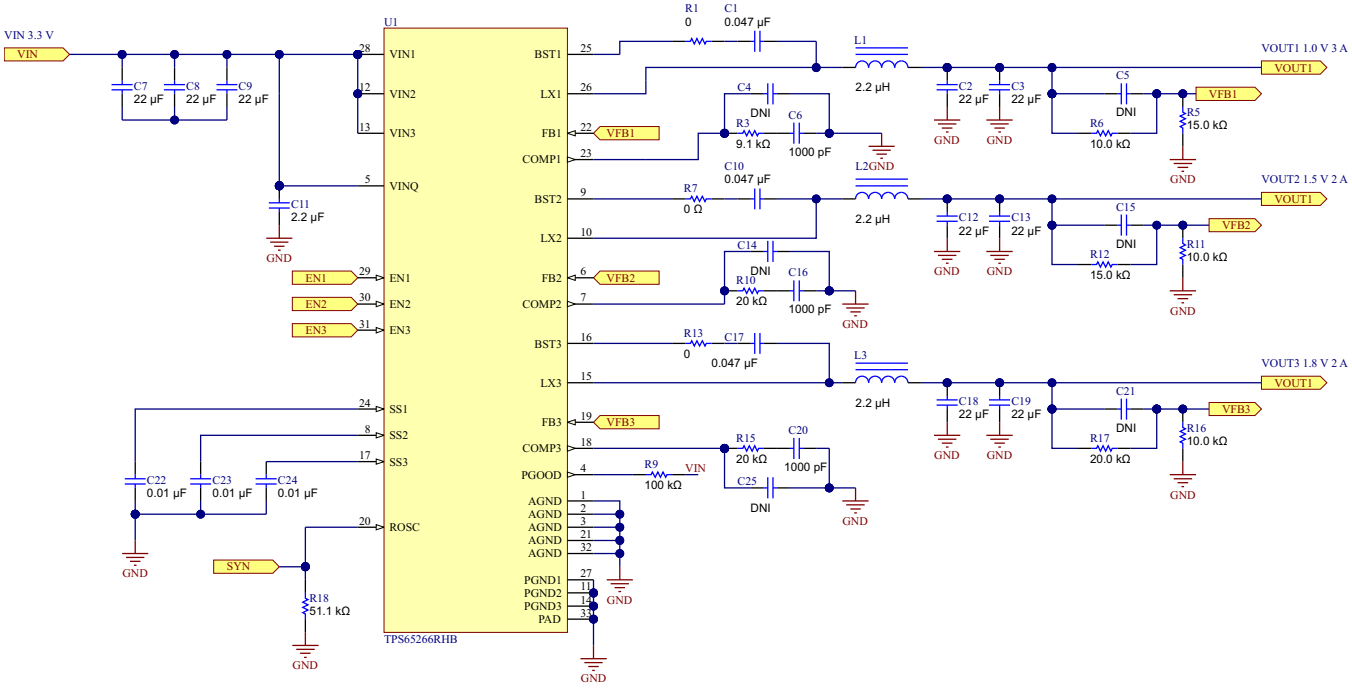


Figure 32. Typical Application Schematic

Typical Application (continued)

8.2.1 Design Requirements

This example details the design of a triple-synchronous step-down converter. The designer must know a few parameters to start the design process. These parameters are typically determined at the system level. For this example, start with the following known parameters in Table 2.

Table 2. Design Parameters

Parameter	Value
Vout1	1.0 V
Iout1	3 A
Vout2	1.5 V
Iout2	2 A
Vout3	1.8 V
Iout3	2 A
Transient response 1-A load step	±5%
Input voltage	5.0 V normal, 2.7 to 6.5 V
Output voltage ripple	±1%
Switching frequency	1 MHz

8.2.2 Detailed Design Procedure

8.2.2.1 Output Inductor Selection

To calculate the value of the output inductor, use Equation 7. LIR is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current is filtered by the output capacitor. Therefore, choosing high inductor ripple currents impact the selection of the output capacitor because the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer; however, LIR is normally from 0.1 to 0.3 for the majority of applications.

$$L = \frac{V_{inmax} - V_{out}}{I_o \times LIR} \times \frac{V_{out}}{V_{inmax} \times f_{sw}} \quad (7)$$

For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS and peak inductor current can be found from Equation 9 and Equation 10.

$$I_{ripple} = \frac{V_{inmax} - V_{out}}{L} \times \frac{V_{out}}{V_{inmax} \times f_{sw}} \quad (8)$$

$$I_{Lrms} = \sqrt{I_O^2 + \frac{\left(\frac{V_{out} \times (V_{inmax} - V_{out})}{V_{inmax} \times L \times fsw}\right)^2}{12}} \quad (9)$$

$$I_{Lpeak} = I_{out} + \frac{I_{ripple}}{2} \quad (10)$$

The current flowing through the inductor is the inductor ripple current plus the output current. During power-up, faults, or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated previously. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

8.2.2.2 Output Capacitor Selection

The three primary considerations for selecting the value of the output capacitor are: the output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance must be selected based on the most stringent of these three criteria.

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The first criterion is the desired response to a large change in the load current. The output capacitor needs to supply the load with current when the regulator cannot. This situation would occur if there are desired hold-up times for the regulator where the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator is also temporarily not able to supply sufficient output current if there is a large, fast increase in the current needs of the load such as a transition from no load to full load. The regulator usually needs two or more clock cycles for the control loop to see the change in load current and output voltage and adjust the duty cycle to react to the change. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for two clock cycles while only allowing a tolerable amount of droop in the output voltage. Equation 11 shows the minimum output capacitance necessary to accomplish this.

$$C_o = \frac{2 \times \Delta I_{out}}{f_{sw} \times \Delta V_{out}}$$

where

- ΔIout is the change in output current.
- f_{sw} is the regulator's switching frequency.
- ΔVout is the allowable change in the output voltage. (11)

Equation 12 calculates the minimum output capacitance needed to meet the output voltage ripple specification.

$$C_o > \frac{1}{8 \times f_{sw}} \times \frac{1}{\frac{V_{oripple}}{I_{oripple}}}$$

where

- f_{sw} is the switching frequency.
- V_{ripple} is the maximum allowable output voltage ripple.
- I_{ripple} is the inductor ripple current. (12)

Equation 13 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification.

$$R_{ESR} < \frac{V_{oripple}}{I_{oripple}} \quad (13)$$

Additional capacitance deratings for aging, temperature, and DC bias should be factored in, which increase this minimum value. Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. Some capacitor data sheets specify the root mean square (RMS) value of the maximum ripple current. Equation 14 can be used to calculate the RMS ripple current the output capacitor needs to support.

$$I_{corms} = \frac{V_{out} \times (V_{inmax} - V_{out})}{\sqrt{12} \times V_{inmax} \times L \times f_{sw}} \quad (14)$$

8.2.2.3 Input Capacitor Selection

The TPS65266 requires a high-quality ceramic, type X5R or X7R, input decoupling capacitor of at least 10 µF of effective capacitance on the VIN input voltage pins. In some applications, additional bulk capacitance may also be required for the VIN input. The effective capacitance includes any DC bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the TPS65266. Calculate the input ripple current using Equation 15.

$$I_{inrms} = I_{out} \times \sqrt{\frac{V_{out}}{V_{inmin}} \times \frac{(V_{inmin} - V_{out})}{V_{inmin}}} \quad (15)$$

The value of a ceramic capacitor varies significantly over temperature and the amount of DC bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are usually selected for power regulator capacitors because they have a high capacitance-to-volume ratio and are fairly stable over temperature. The output capacitor must also be selected with the DC bias taken into account. The capacitance value of a capacitor decreases as the DC bias across a capacitor increases. The input capacitance value determines the input ripple voltage of the regulator. Calculate the input voltage ripple using Equation 16.

$$\Delta V_{in} = \frac{I_{outmax} \times 0.25}{C_{in} \times f_{sw}} \quad (16)$$

8.2.2.4 Loop Compensation

The TPS65266 incorporates a peak current mode control scheme. The error amplifier is a transconductance amplifier with a gain of 290 µS. A typical type II compensation circuit adequately delivers a phase margin between 30° and 90°. C_b adds a high-frequency pole to attenuate high-frequency noise when needed. To calculate the external compensation components, follow these steps.

1. Select switching frequency, f_{SW}, that is appropriate for application depending on L and C sizes, output ripple, EMI, and so forth. Switching frequency between 500 kHz to 1.5 MHz gives best trade-off between performance and cost. To optimize efficiency, lower switching frequency is desired.
2. Set up crossover frequency, f_c, which is typically between 1 / 5 and 1 / 20 of f_{SW}.
3. R_C can be determined by:

$$R_C = \frac{2\pi \times f_C \times V_O \times C_O}{G_{m-EA} \times Vref \times G_{m-PS}} \quad (17)$$

   where
   - G_{m_EA} is the error amplifier gain (290 µS).
   - G_{m_PS} is the power stage voltage to current conversion gain (10 A/V).

4. Calculate C_C by placing a compensation zero at or before the dominant pole $f_p = \frac{1}{C_O \times R_L \times 2\pi}$

$$C_C = \frac{R_L \times C_O}{R_C} \quad (18)$$

5. Optional C_b can be used to cancel the zero from the ESR associated with C_O.

$$C_b = \frac{R_{ESR} \times C_O}{R_C} \quad (19)$$

6. Type III compensation can be implemented with the addition of one capacitor, C_1. This allows for slightly higher loop bandwidths and higher phase margins. If used, C_1 is calculated from Equation 20.

$$C_1 = \frac{1}{2\pi \times R_1 \times f_c} \quad (20)$$

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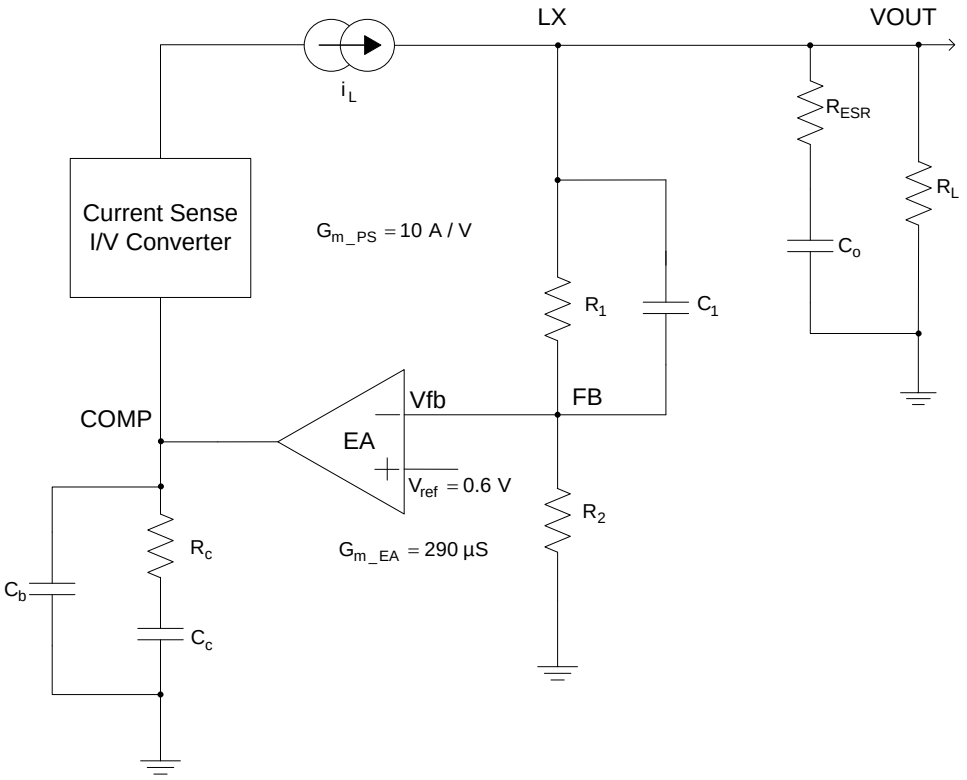


Figure 33. DC/DC Loop Compensation

8.2.3 Application Curves

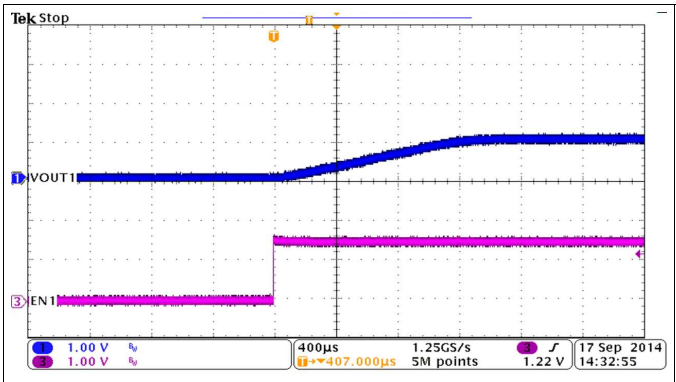


Figure 34. Buck1, Soft-Start, Iout = 3 A

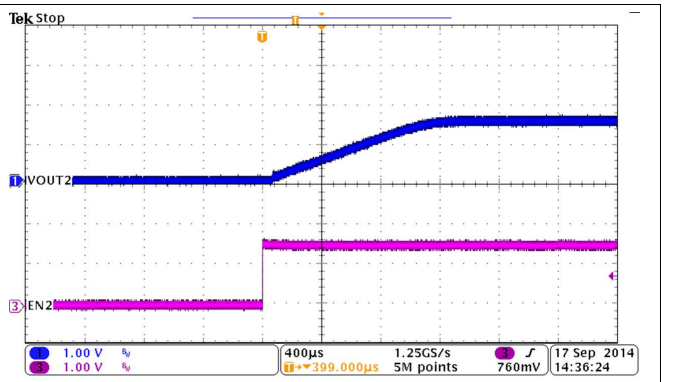


Figure 35. Buck2, Soft-Start, Iout = 2 A

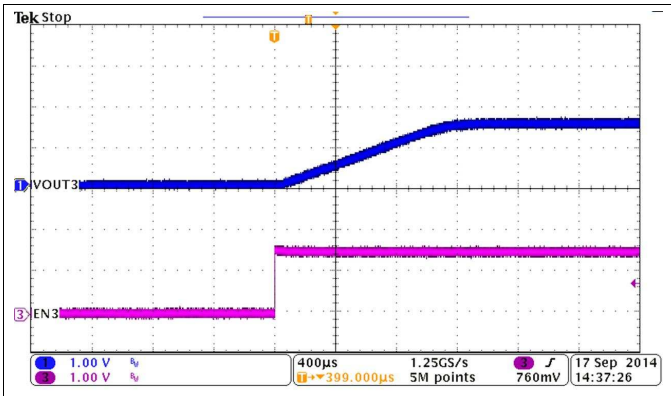


Figure 36. Buck3, Soft-Start, Iout = 2 A

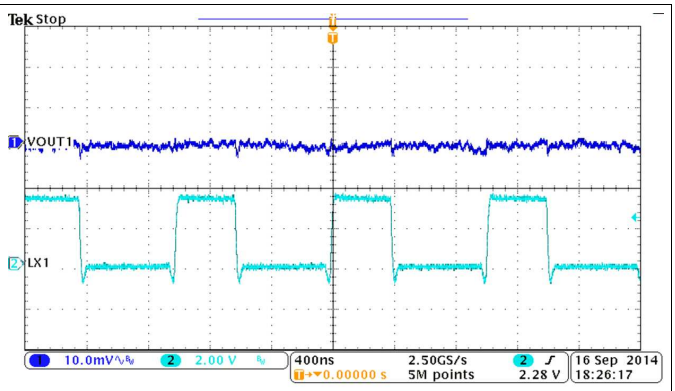


Figure 37. Buck1, Output Voltage Ripple, Iout = 3 A

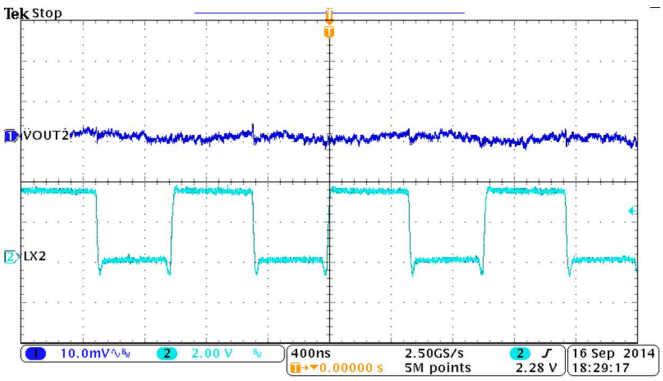


Figure 38. Buck2, Output Voltage Ripple, Iout = 2 A

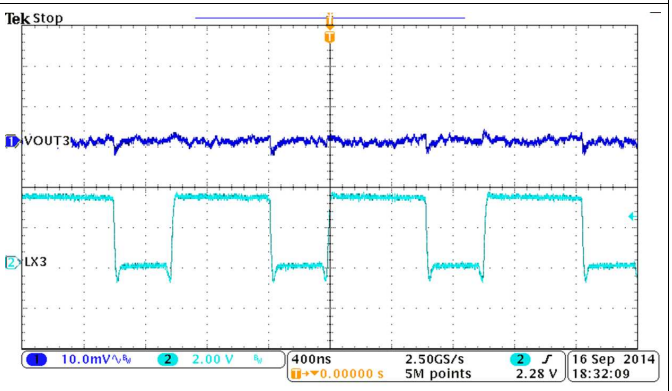
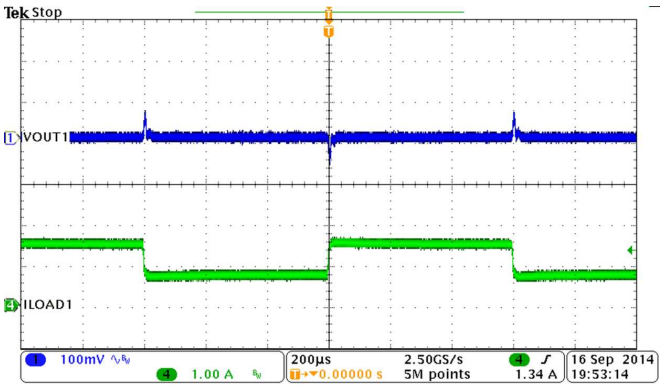
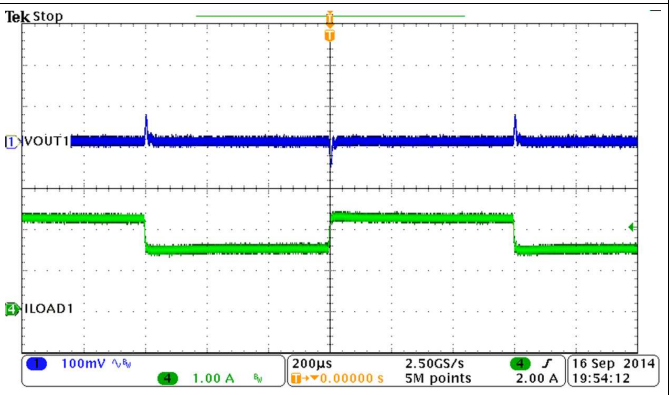


Figure 39. Buck3, Output Voltage Ripple, Iout = 2 A



SR = 0.25 A/µs

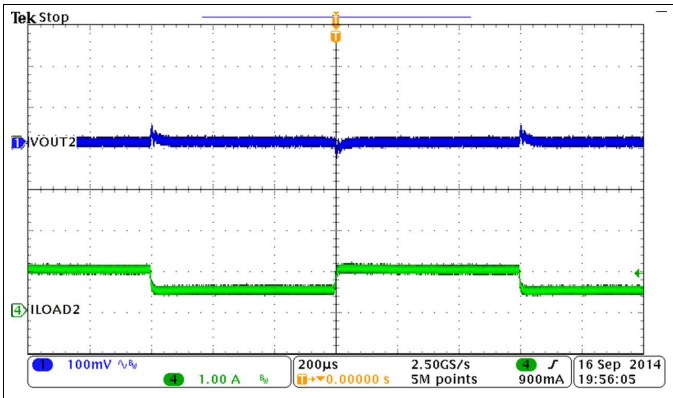
Figure 40. Buck1, Load Transient, 0.75 to 1.5 A



SR = 0.25 A/µs

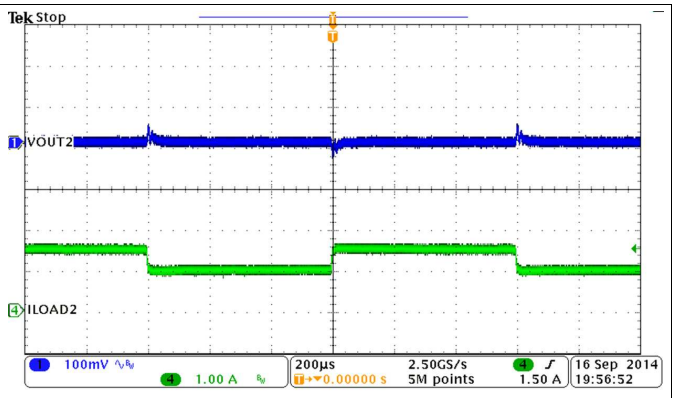
Figure 41. Buck1, Load Transient, 1.5 to 2.25 A

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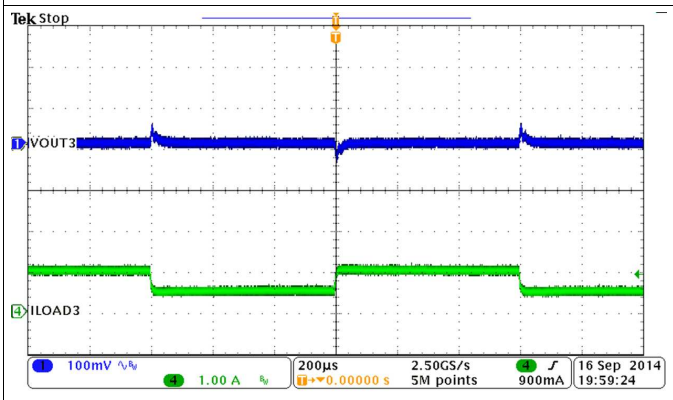
SR = 0.25 A/µs

Figure 42. Buck2, Load Transient, 0.5 to 1.0 A



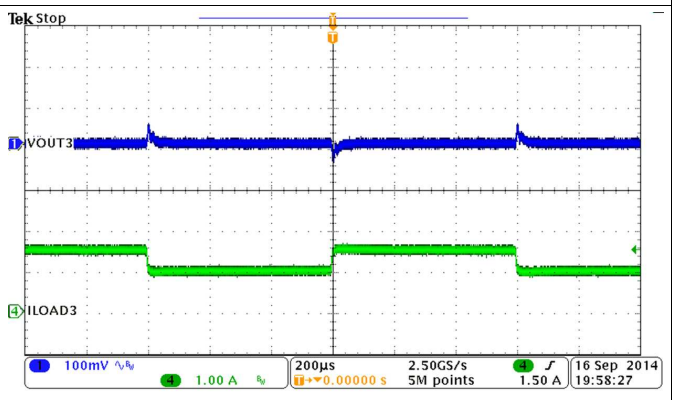
SR = 0.25 A/µs

Figure 43. Buck2, Load Transient, 1.0 to 1.5 A



SR = 0.25 A/µs

Figure 44. Buck3, Load Transient, 0.5 to 1.0 A



SR = 0.25 A/µs

Figure 45. Buck3, Load Transient, 1.0 to 1.5 A

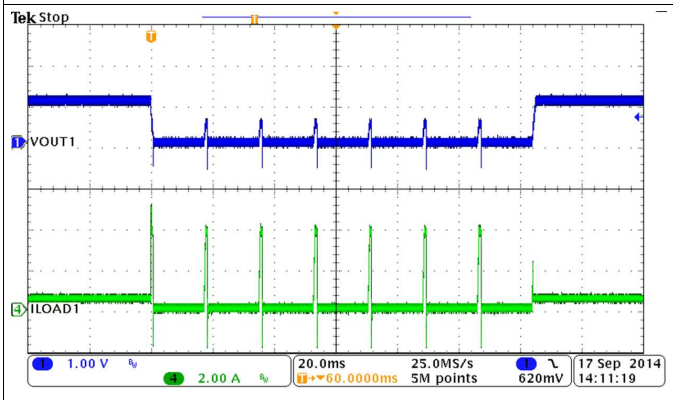


Figure 46. Buck1, Hiccup and Recovery

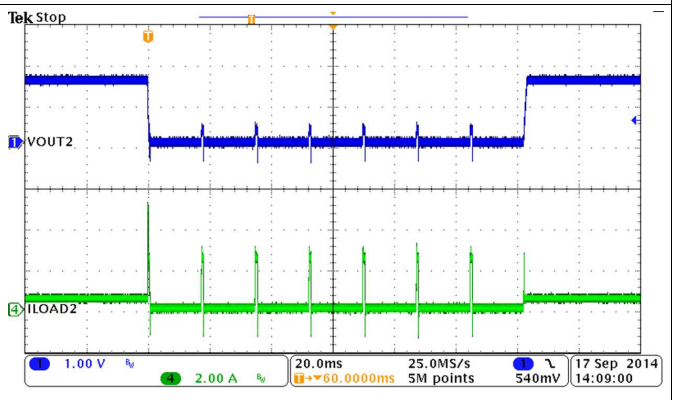


Figure 47. Buck2, Hiccup and Recovery

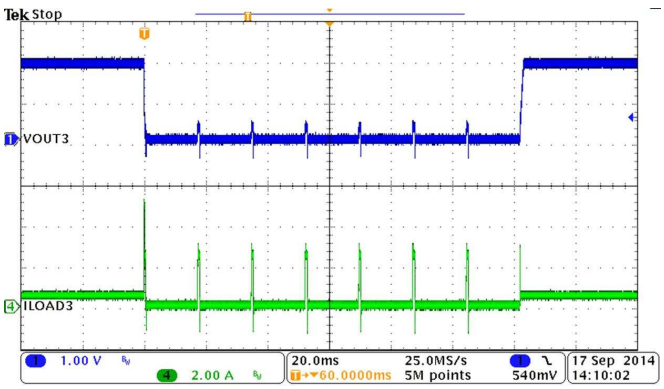


Figure 48. Buck3, Hiccup and Recovery

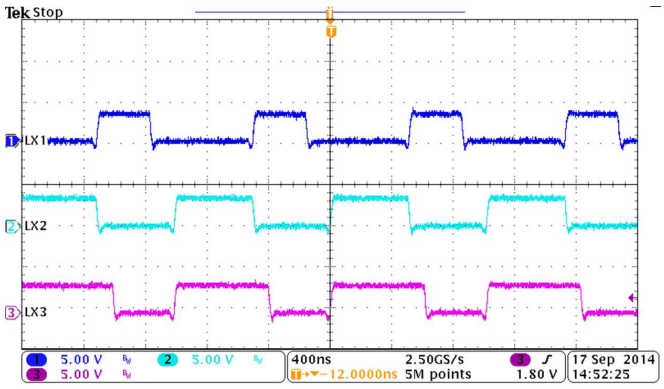


Figure 49. 180° Out of Phase

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9 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 2.7 and 6.5 V. This input power supply should be well regulated. If the input supply is located more than a few inches from the TPS65266 converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 47 µF is a typical choice.

10 Layout

10.1 Layout Guidelines

The TPS65266 supports a 2-layer PCB layout, shown in Figure 50.

Layout is a critical portion of good power supply design. See Figure 50 for a PCB layout example. The top contains the main power traces for VIN, VOUT, and LX. The top layer also has connections for the remaining pins of the TPS65266 and a large top-side area filled with ground. The top-layer ground area should be connected to the bottom layer ground using vias at the input bypass capacitor, the output filter capacitor, and directly under the TPS65266 device to provide a thermal path from the exposed thermal pad land to ground. The bottom layer acts as ground plane connecting analog ground and power ground.

For operation at full-rated load, the top-side ground area together with the bottom-side ground plane must provide an adequate heat dissipating area. Several signals paths conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies' performance. To help eliminate these problems, the VIN pin should be bypassed to ground with a low-ESR ceramic bypass capacitor with X5R or X7R dielectric. Take care to minimize the loop area formed by the bypass capacitor connections, the VIN pins, and the ground connections. The VIN pin must also be bypassed to ground using a low-ESR ceramic capacitor with X5R or X7R dielectric.

Because the LX connection is the switching node, the output inductor should be located close to the LX pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. The output filter capacitor ground should use the same power ground trace as the VIN input bypass capacitor. Try to minimize this conductor length while maintaining adequate width. The small signal components should be grounded to the analog ground path.

The FB and COMP pins are sensitive to noise so the resistors and capacitors should be located as close as possible to the IC and routed with minimal lengths of trace. Place the additional external components approximately as shown in Figure 50.

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10.2 Layout Example

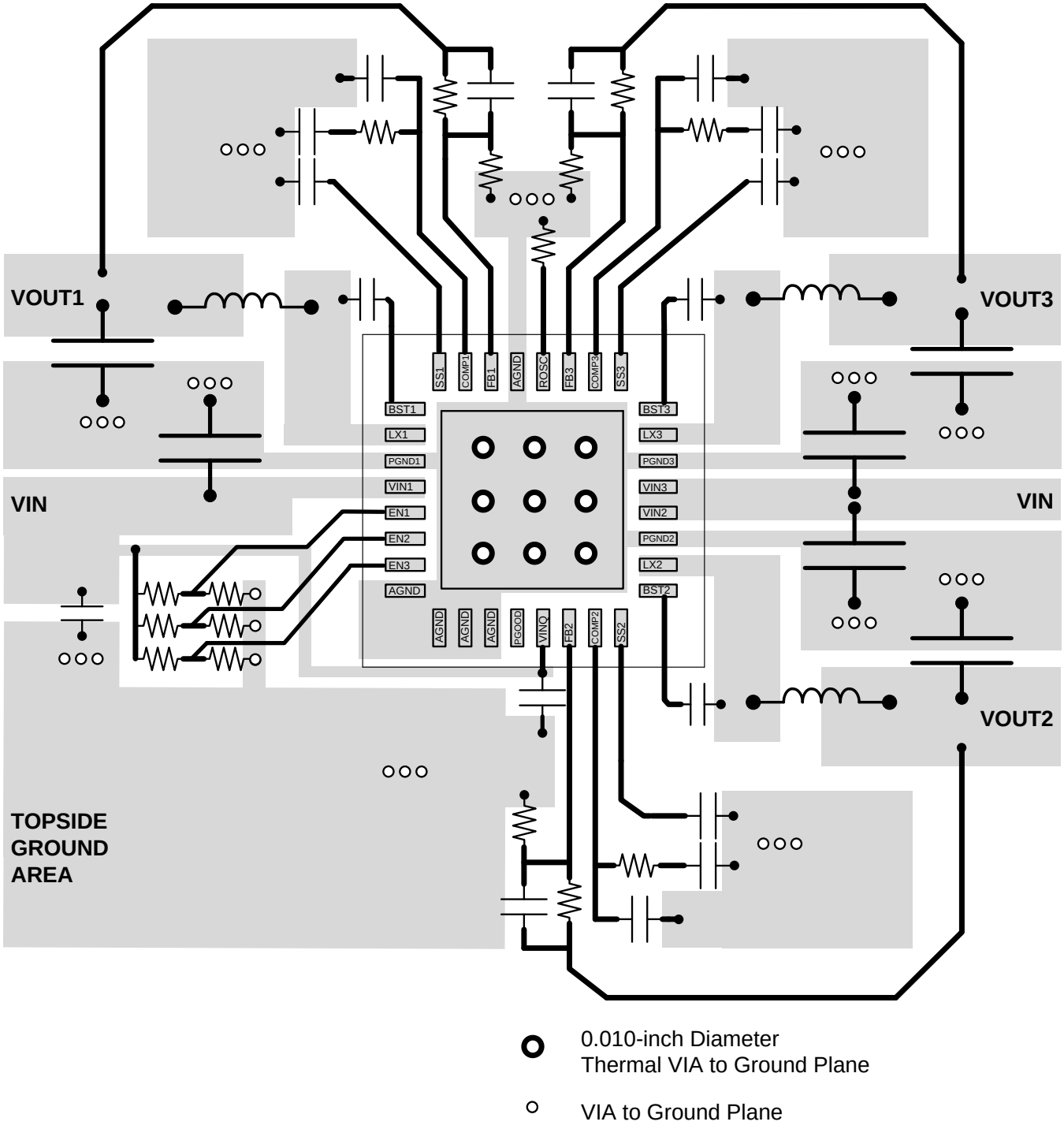


Figure 50. PCB Layout

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Related Parts

PART NUMBER	DESCRIPTION	COMMENTS
TPS65261 TPS65261-1	4.5 to 18 V, triple bucks with input voltage power failure indicator	Triple bucks 3-A/2-A/2-A output current, features an open-drain RESET signal to monitor input power failure, automatic power sequencing
TPS65262 TPS65262-1	4.5 to 18 V, triple bucks with dual adjustable LDOs	Triple bucks 3-A/1-A/1-A output current, automatic power sequencing. Dual LDOs: TPS65262, 200 mA/100 mA TPS65262-1, 350 mA/150 mA
TPS65263	4.5 to 18 V, triple buck with I^2C interface	Triple buck 3-A/2-A/2-A output current, I^2C-controlled dynamic voltage scaling (DVS)

11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65266RHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65266	Samples
TPS65266RHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65266	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

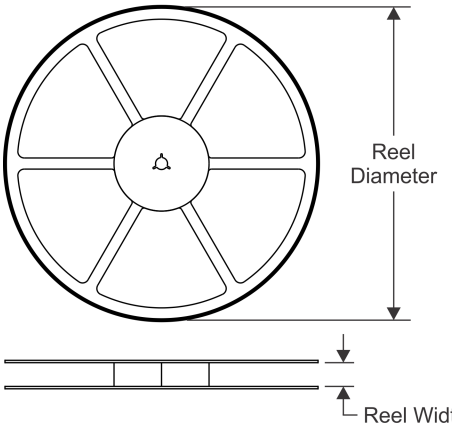
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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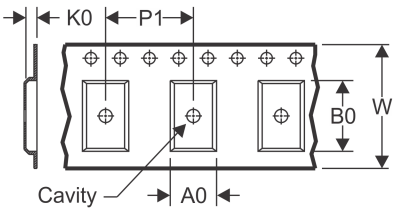
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

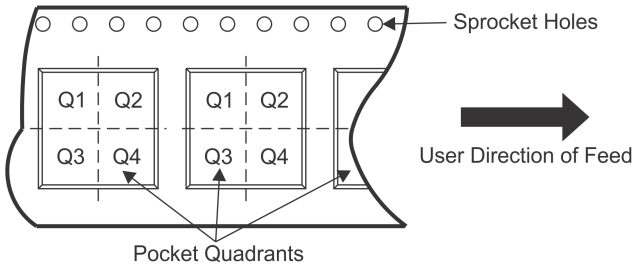


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

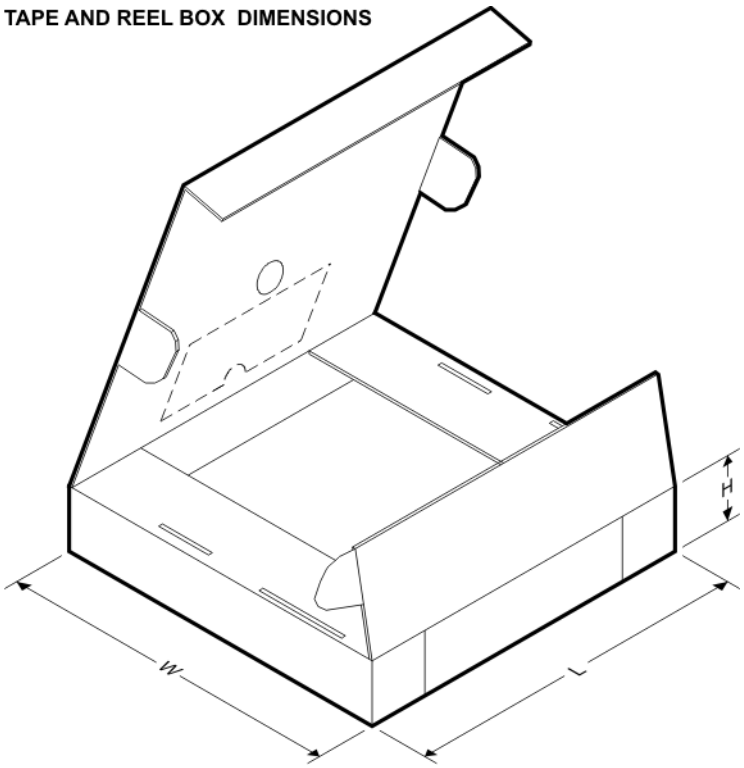
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65266RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS65266RHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

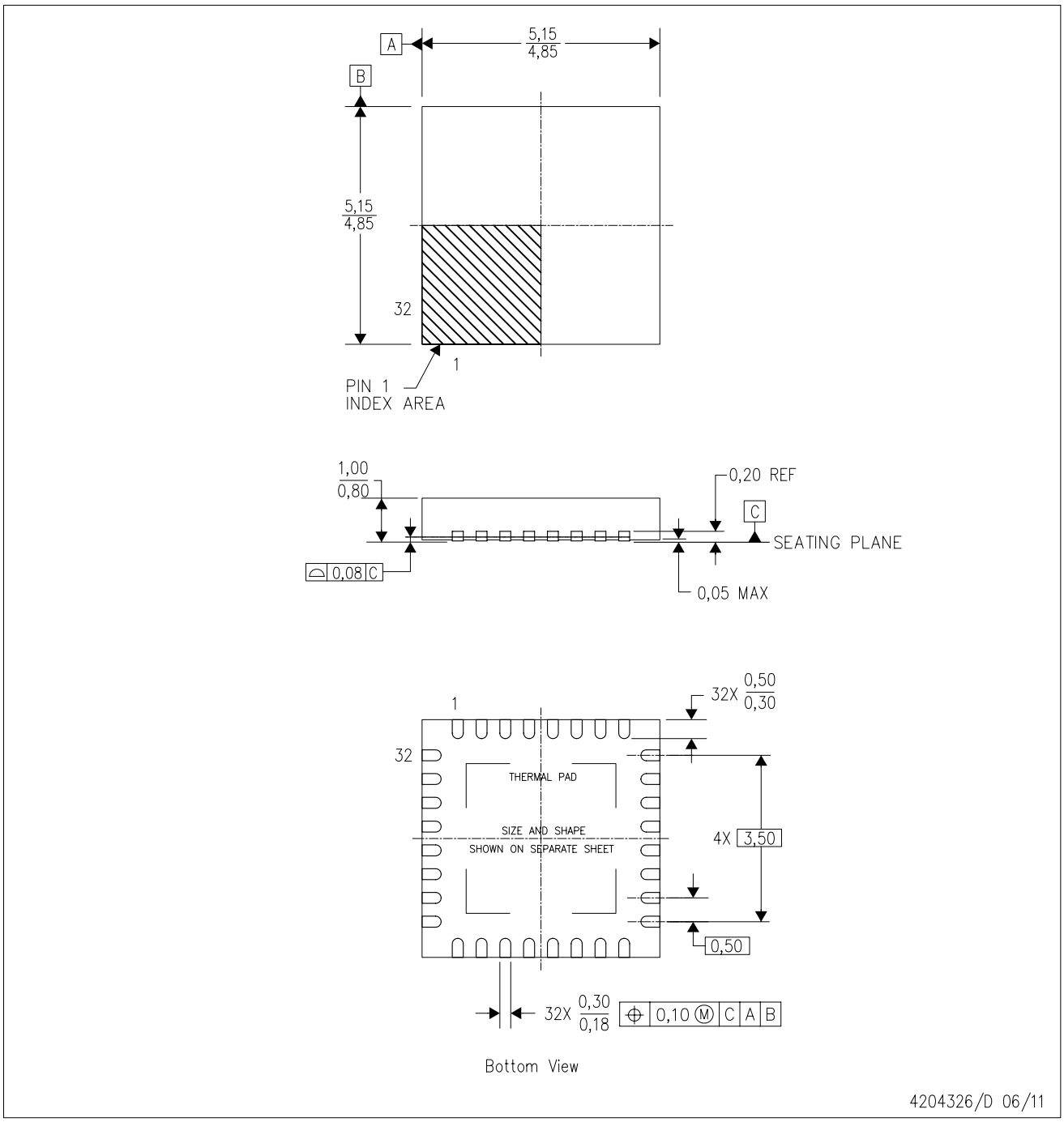
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65266RHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
TPS65266RHBT	VQFN	RHB	32	250	210.0	185.0	35.0

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

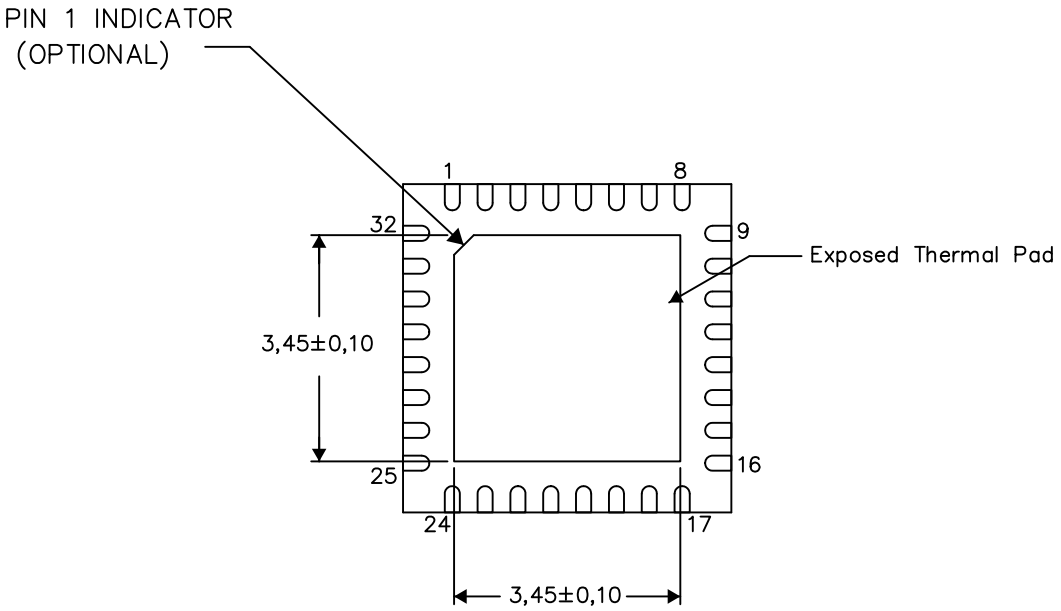
RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



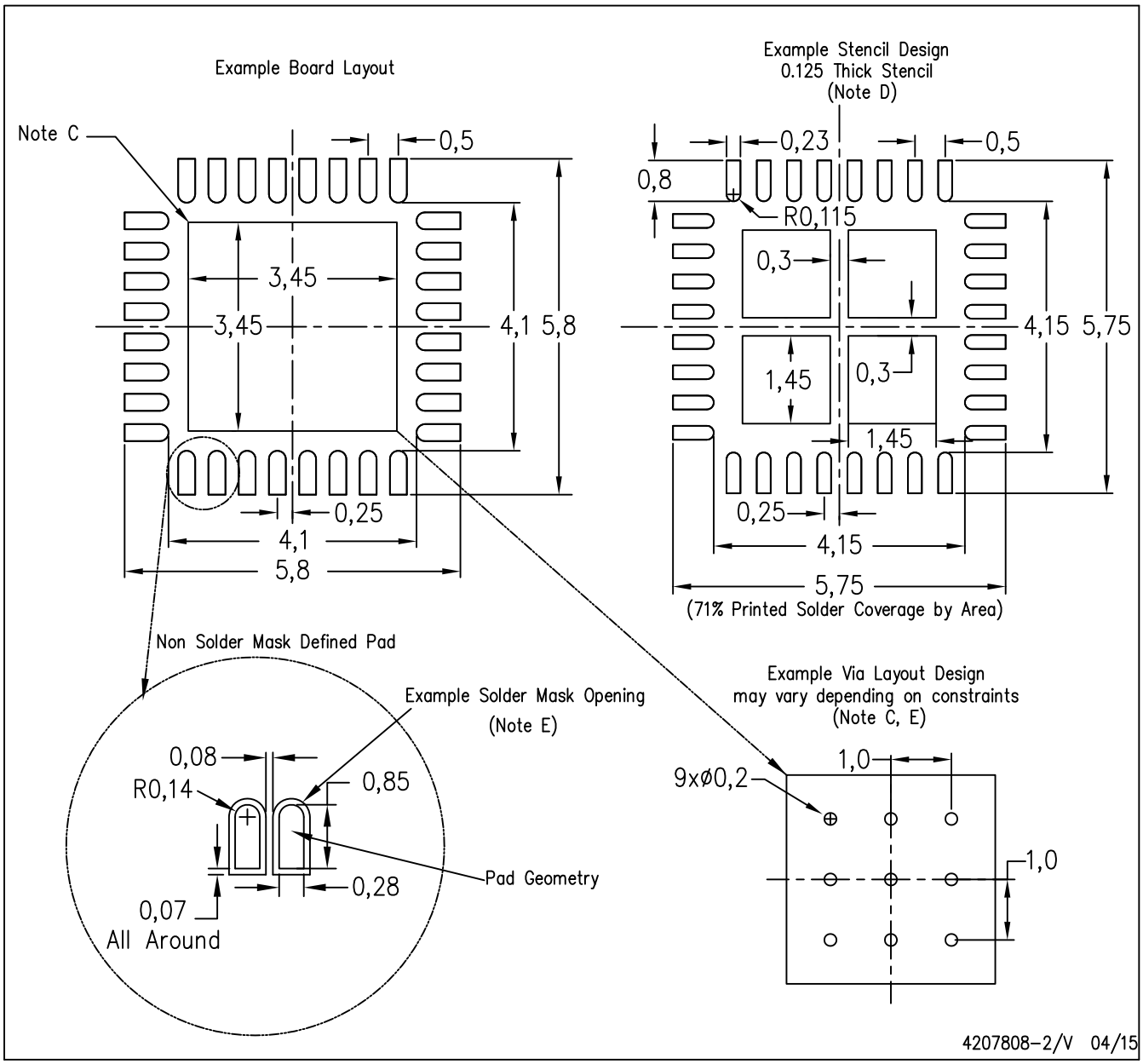
Bottom View

Exposed Thermal Pad Dimensions

4206356–2/AC 05/15

NOTE: A. All linear dimensions are in millimeters

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for any larger diameter vias placed in the thermal pad.

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