ADS7861



SBAS110D – DECEMBER 1998 – REVISED AUGUST 2007

Dual, 500kSPS, 12-Bit, 2 + 2 Channel, Simultaneous Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 4 INPUT CHANNELS
- FULLY DIFFERENTIAL INPUTS
- 2μs TOTAL THROUGHPUT PER CHANNEL
- NO MISSING CODES
- 1MHz EFFECTIVE SAMPLING RATE
- LOW POWER: 40mW
- SSI SERIAL INTERFACE
- OPERATING TEMPERATURE RANGE: –40°C to +125°C

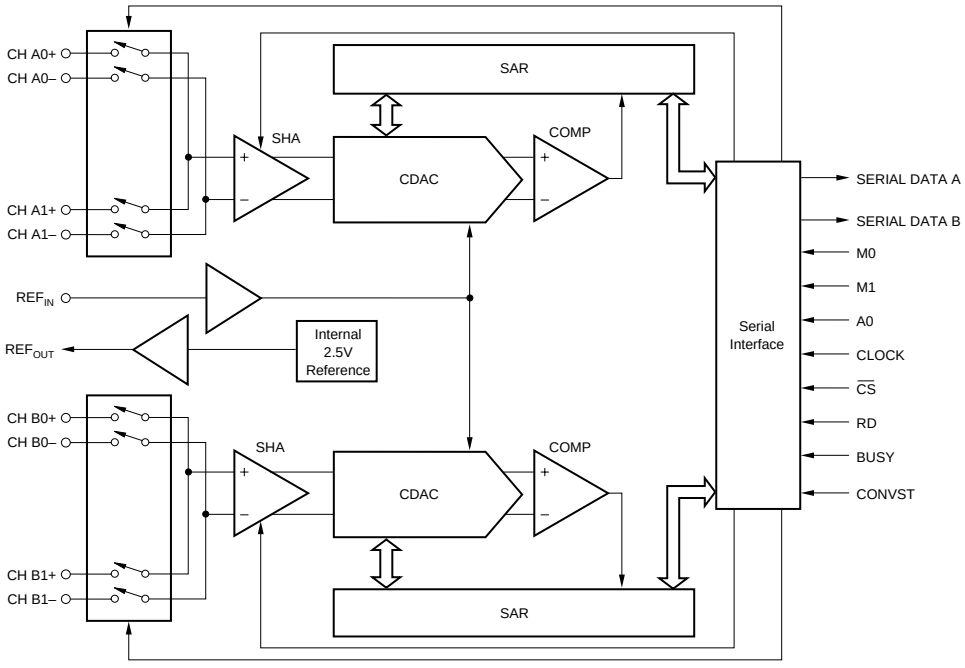
APPLICATIONS

- MOTOR CONTROL
- MULTI-AXIS POSITIONING SYSTEMS
- 3-PHASE POWER CONTROL

DESCRIPTION

The ADS7861 is a dual, 12-bit, 500kSPS, Analog-to-Digital (A/D) converter with four fully differential input channels grouped into two pairs for high speed, simultaneous signal acquisition. Inputs to the sample-and-hold amplifiers are fully differential and are maintained differential to the input of the A/D converter. This provides excellent common-mode rejection of 80dB at 50kHz which is important in high noise environments.

The ADS7861 offers a high-speed, dual serial interface and control inputs to minimize software overhead. The output data for each channel is available as a 12-bit word. The ADS7861 is offered in both an SSOP-24 and a QFN-32 package and is fully specified over the –40°C to +125°C operating range.



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ABSOLUTE MAXIMUM RATINGS[1]

Analog Inputs to AGND, Any Channel Input	–0.3V to ($+V_D$ + 0.3V)
REF_{IN}	–0.3V to ($+V_D$ + 0.3V)
Digital Inputs to DGND	–0.3V to ($+V_D$ + 0.3V)
Ground Voltage Differences: AGND, DGND	±0.3V
$+V_D$ to AGND	–0.3V to +6V
Power Dissipation	325mW
Maximum Junction Temperature	+150°C
Operating Temperature Range	–40°C to +125°C
Storage Temperature Range	–65°C to +150°C

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

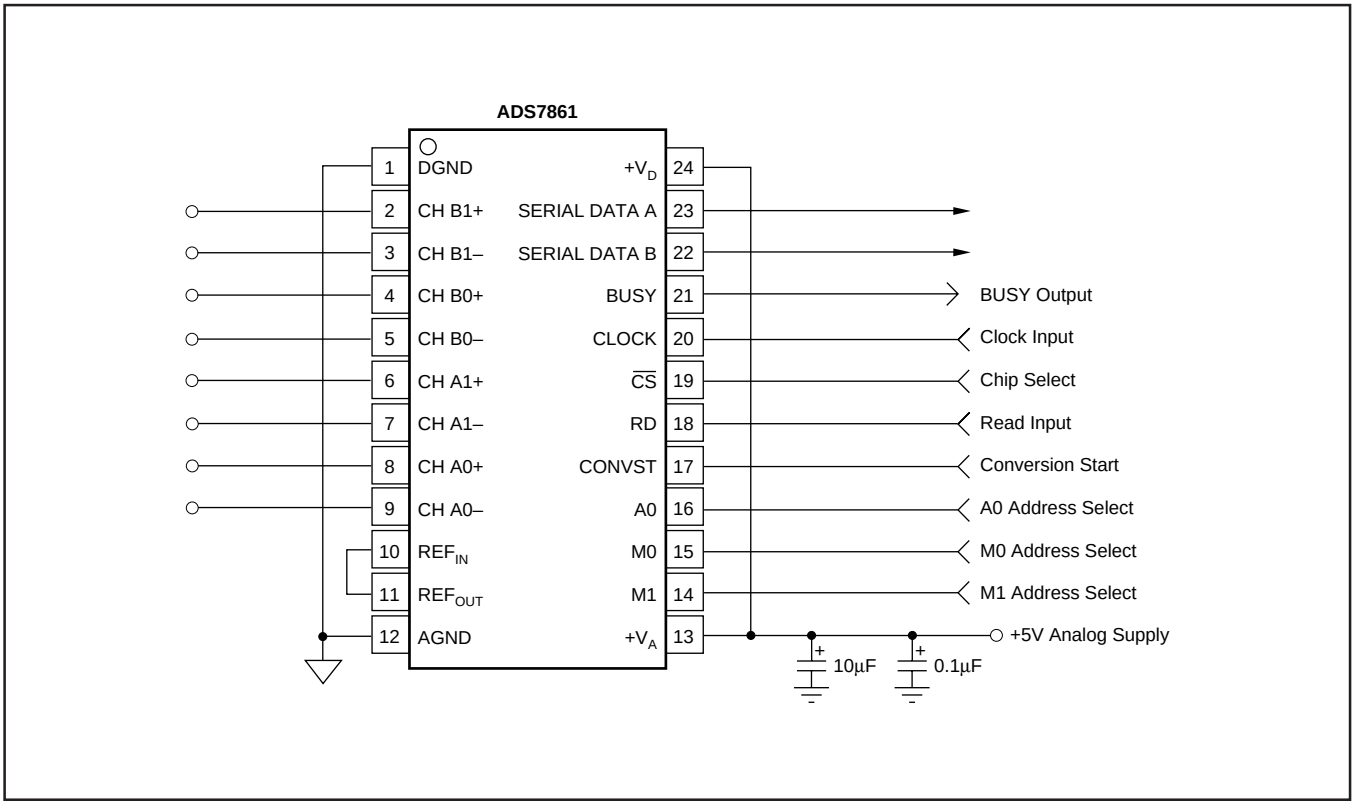
For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

TRUTH TABLE

M0	M1	A0	TWO-CHANNEL/FOUR-CHANNEL OPERATION	DATA ON SERIAL OUTPUTS	CHANNELS CONVERTED
0	0	0	Two Channel	A and B	A0, B0
0	0	1	Two Channel	A and B	A1, B1
0	1	0	Two Channel	A Only	A0, B0
0	1	1	Two Channel	A Only	A1, B1
1	0	X	Four Channel	A and B	Sequential
1	1	X	Four Channel	A Only	Sequential

X = Don't Care.

BASIC CIRCUIT CONFIGURATION



ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range at T_A = –40°C to +125°C, $+V_A + V_D$ = +5V, V_{REF} = internal +2.5V, f_{CLK} = 8MHz, and f_{SAMPLE} = 500kSPS, unless otherwise noted.

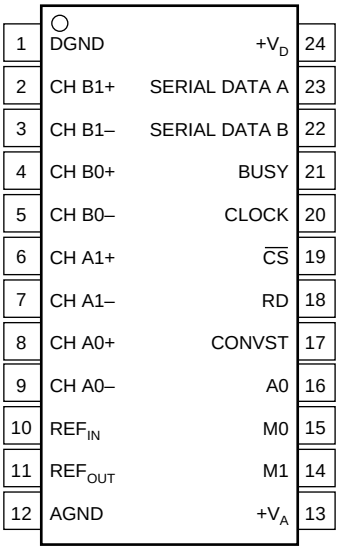
PARAMETER	CONDITIONS	ADS7861I, E			ADS7861IB, EB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION				12			*	Bits
ANALOG INPUT								
Input Voltage Range-Bipolar	V_{CENTER} = Internal V_{REF} at 2.5V	$–V_{REF}$		$+V_{REF}$	*		*	V
Input Capacitance			15			*		pF
Input Leakage Current			±1			*		µA
SYSTEM PERFORMANCE								
No Missing Codes		12			*			Bits
Integral Linearity			±0.75	±2		±0.5	±1	LSB
Integral Linearity Match			0.5	±1		*	*	LSB
Differential Linearity			±1			±0.5	±1	LSB
Bipolar Offset Error	T_A = –40°C to +85°C		±0.5	±3		*	*	LSB
	T_A = –40°C to +125°C		±0.5	±3.5		*	*	LSB
Bipolar Offset Error Match				3			2	LSB
Positive Gain Error	Referenced to REF_{IN}		±0.15	±0.75		±0.10	±0.50	% of FSR
Positive Gain Error Match				2			1	LSB
Negative Gain Error	Referenced to REF_{IN}		±0.15	±0.75		±0.10	±0.50	% of FSR
Negative Gain Error Match				2			1	LSB
Common-Mode Rejection Ratio	At DC		80			*		dB
	V_{IN} = ±1.25V_{PP} at 50kHz		80			*		dB
Noise			120			*		µVrms
Power Supply Rejection Ratio			0.5	2		*	*	LSB
SAMPLING DYNAMICS								
Conversion Time per A/D			1.625			*		µs
Acquisition Time			0.375			*		µs
Throughput Rate		500			*			kSPS
Aperture Delay			3.5			*		ns
Aperture Delay Matching			100			*		ps
Aperture Jitter			50			*		ps
Small-Signal Bandwidth			40			*		MHz
DYNAMIC CHARACTERISTICS (V_{IN} = ±2.5V_{PP} at 100kHz)								
Total Harmonic Distortion	T_A = –40°C to +85°C			–72			–76	dB
	T_A = –40°C to +125°C			–71			–75	dB
SINAD		70			*			dB
Spurious Free Dynamic Range	T_A = –40°C to +85°C	72			76			dB
	T_A = –40°C to +125°C	71			75			dB
Channel-to-Channel Isolation				–80			*	dB
VOLTAGE REFERENCE								
Internal		2.475	2.5	2.525	*	*	*	V
Internal Drift			±25			*		ppm/°C
Internal Noise			50			*		$µV_{PP}$
Internal Source Current			2			*		mA
Internal Load Rejection			0.005			*		mV/µA
Internal PSRR			80			*		dB
External Voltage Range		1.2	2.5	2.6	*	*	*	V
Input Current			0.05	1		*	*	µA
Input Capacitance			5			*		pF
DIGITAL INPUT/OUTPUT								
Logic Family			CMOS			*		
Logic Levels: V_{IH}	I_{IH} = +5µA	3.0		$+V_{DD}$ + 0.3	*		*	V
V_{IL}	I_{IL} = +5µA	–0.3		1	*		*	V
V_{OH}	I_{OH} = –0.5mA	3.5			*			V
V_{OL}	I_{OL} = –0.5mA			0.4			*	V
External Clock, Optional		0.2		8	*		*	MHz
Data Format			Binary Two's Complement			*		
POWER SUPPLY REQUIREMENTS								
Power Supply Voltage, +V		4.75	5	5.25	*	*	*	V
Quiescent Current, $+V_A$	T_A = –40°C to +85°C		5	8		*	*	mA
	T_A = –40°C to +125°C		5	8.5		*	*	mA
Power Dissipation	T_A = –40°C to +85°C		25	40		*	*	mW
	T_A = –40°C to +125°C		25	42.5		*	*	mW

* Specifications same as ADS7861I, ADS7861E.

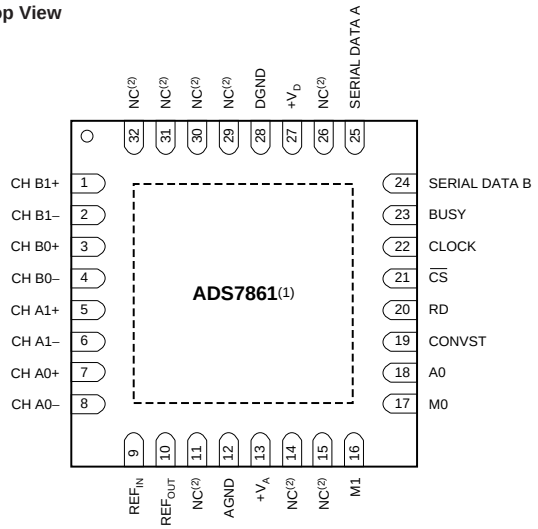
PIN CONFIGURATIONS

Top View **SSOP**

ADS7861



Top View **QFN**



NOTE: (1) The thermal pad is internally connected to the substrate. This pad can be connected to the analog ground or left floating. Keep the thermal pad separate from the digital ground, if possible.
(2) NC = Not Connected.

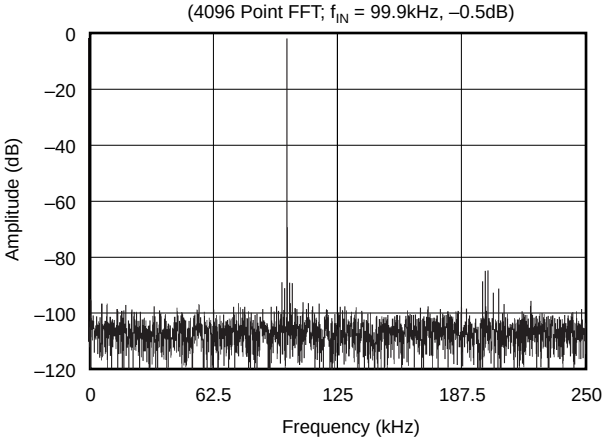
PIN DESCRIPTIONS

SSOP PIN	QFN PIN	NAME	DESCRIPTION
1	28	DGND	Digital Ground. Connect directly to analog ground (pin 12).
2	1	CH B1+	Noninverting Input Channel B1
3	2	CH B1–	Inverting Input Channel B1
4	3	CH B0+	Noninverting Input Channel B0
5	4	CH B0–	Inverting Input Channel B0
6	5	CH A1+	Noninverting Input Channel A1
7	6	CH A1–	Inverting Input Channel A1
8	7	CH A0+	Noninverting Input Channel A0
9	8	CH A0–	Inverting Input Channel A0
10	9	REF$_{IN}$	Reference Input
11	10	REF$_{OUT}$	2.5V Reference Output
12	12	AGND	Analog Ground. Connect directly to digital ground (pin 1).
13	13	+V$_A$	Analog Power Supply, +5VDC. Connect directly to digital power supply (pin 24). Decouple to analog ground with a 0.1µF ceramic capacitor and a 10µF tantalum capacitor.
14	16	M1	Selects between the Serial Outputs. When M1 is LOW, both Serial Output A and Serial Output B are selected for data transfer. When M1 is HIGH, Serial output A is configured for both Channel A data and Channel B data; Serial Output B goes into tri-state (i.e., high impedance).
15	17	M0	Selects between two-channel and four-channel operation. When M0 is LOW, two-channel operation is selected and operates in conjunction with A0. When A0 is HIGH, Channel A1 and Channel B1 are being converted. When A0 is LOW, Channel A0 and Channel B0 are being converted. When M0 is HIGH, four-channel operation is selected. In this mode, all four channels are converted in sequence starting with Channels A0 and B0, followed by Channels A1 and B1.
16	18	A0	A0 operates in conjunction with M0. With M0 LOW and A0 HIGH, Channel A1 and Channel B1 are converted. With M0 LOW and A0 LOW, Channel A0 and Channel B0 are converted.
17	19	CONVST	Convert Start. When CONVST switches from LOW to HIGH, the device switches from the sample to hold mode, independent of the status of the external clock.
18	20	RD	Synchronization Pulse for the Serial Output.
19	21	$\overline{CS}$	Chip Select. When LOW, the Serial Output A and Serial Output B outputs are active; when HIGH, the serial outputs are tri-stated.
20	22	CLOCK	An external CMOS-compatible clock can be applied to the CLOCK input to synchronize the conversion process to an external source. The CLOCK pin controls the sampling rate by the equation: CLOCK = 16 • f_{SAMPLE}.
21	23	BUSY	BUSY goes HIGH during a conversion and returns LOW after the third LSB has been transmitted on either the Serial A or Serial B output pin.
22	24	SERIAL DATA B	The Serial Output data word is comprised of channel information and 12 bits of data. In operation, data is valid on the falling edge of DCLOCK for 16 edges after the rising edge of RD.
23	25	SERIAL DATA A	The Serial Output data word is comprised of channel information and 12 bits of data. In operation, data is valid on the falling edge of DCLOCK for 16 edges after the rising edge of RD. When M1 is HIGH, both Channel A data and Channel B data are available.
24	27	+V$_D$	Digital Power Supply, +5VDC. Connect directly to pin 13. Must be ≤ +V$_A$.

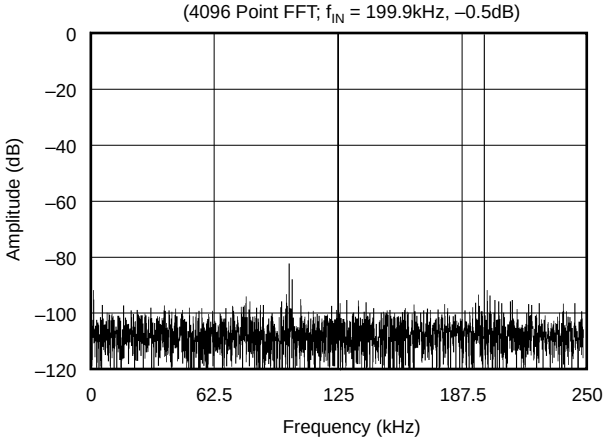
TYPICAL CHARACTERISTICS

At T_A = +25°C, $+V_A$ + V_D = +5V, and V_{REF} = internal +2.5V, f_{CLK} = 8MHz, f_{SAMPLE} = 500kSPS, unless otherwise noted.

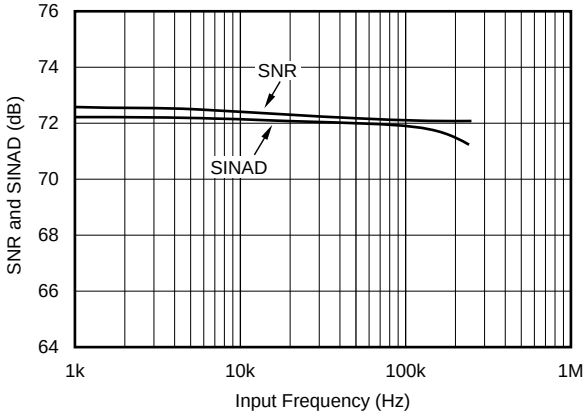
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 99.9kHz, –0.5dB)



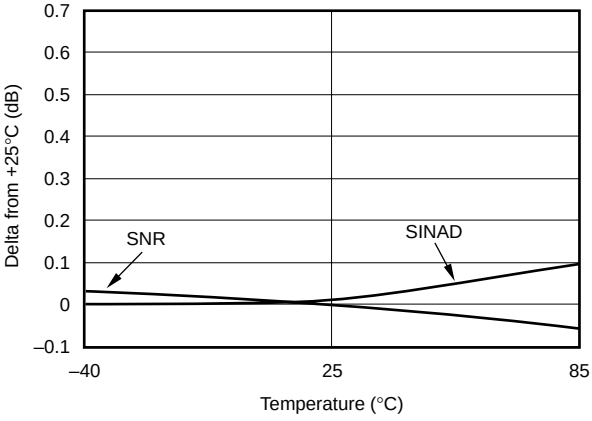
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 199.9kHz, –0.5dB)



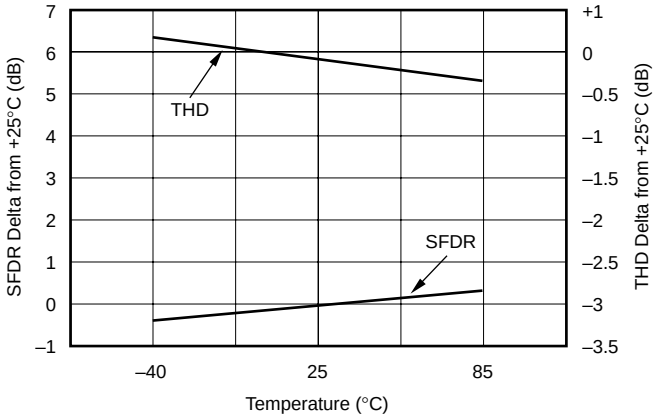
SIGNAL-TO-NOISE RATIO and
SIGNAL-TO-(NOISE+DISTORTION)
vs INPUT FREQUENCY



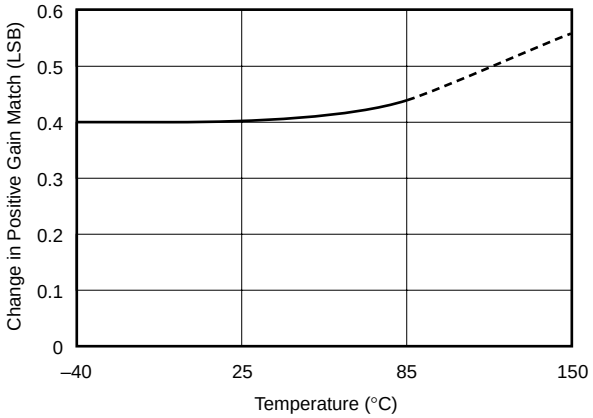
CHANGE IN SIGNAL-TO-NOISE RATIO
AND SIGNAL-TO-(NOISE+DISTORTION)
vs TEMPERATURE



CHANGE IN SPURIOUS FREE DYNAMIC RANGE
AND TOTAL HARMONIC DISTORTION
vs TEMPERATURE



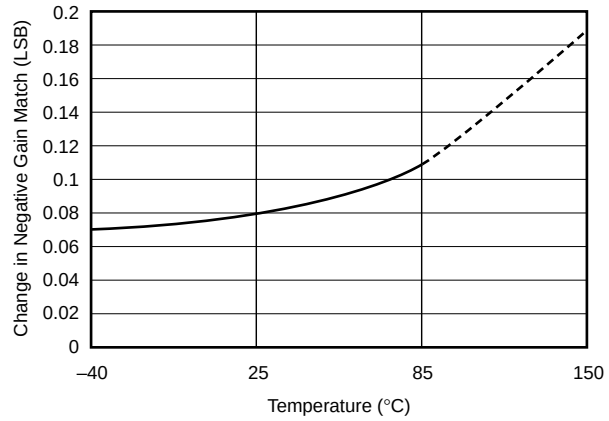
CHANGE IN POSITIVE GAIN MATCH
vs TEMPERATURE
(Maximum Deviation for All Four Channels)



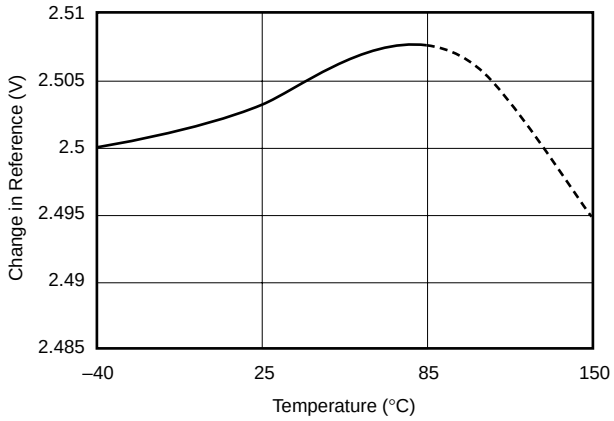
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, $+V_A$ + V_D = +5V, and V_{REF} = internal +2.5V, f_{CLK} = 8MHz, f_{SAMPLE} = 500kSPS, unless otherwise noted.

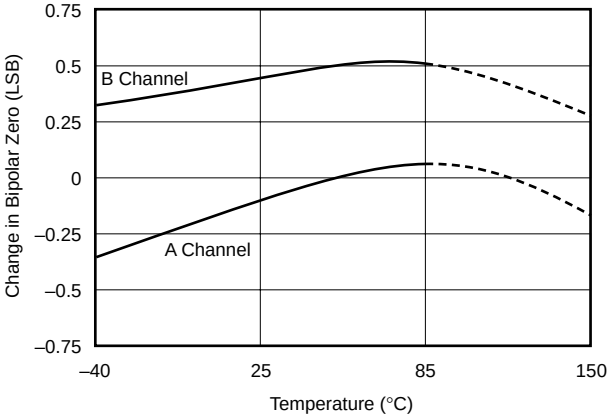
CHANGE IN NEGATIVE GAIN MATCH
vs TEMPERATURE
(Maximum Deviation for All Four Channels)



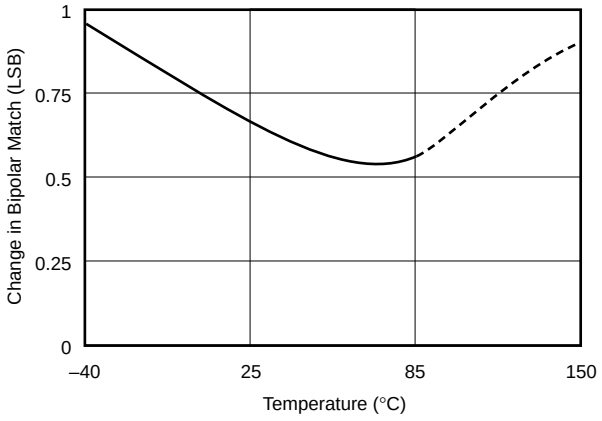
CHANGE IN REFERENCE VOLTAGE
vs TEMPERATURE



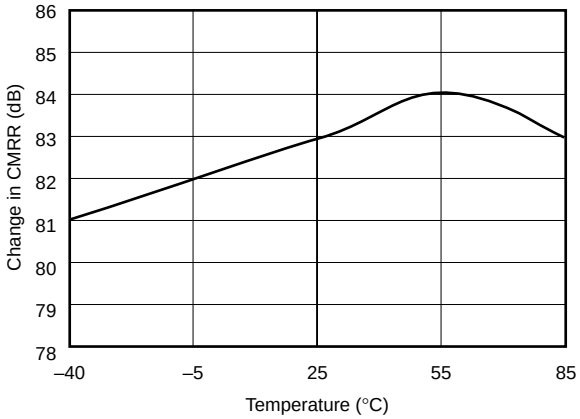
CHANGE IN BIPOLAR ZERO
vs TEMPERATURE



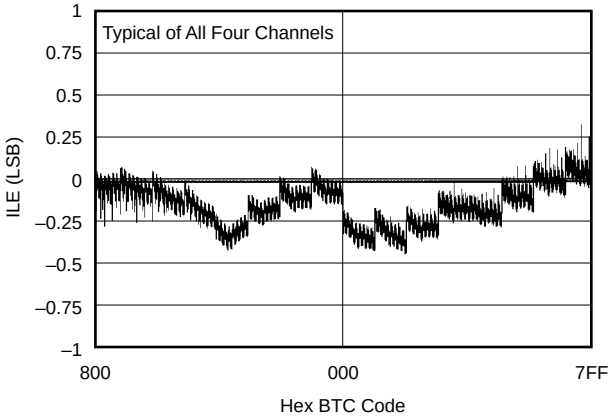
CHANGE IN BPZ MATCH vs TEMPERATURE



CHANGE IN CMRR vs TEMPERATURE



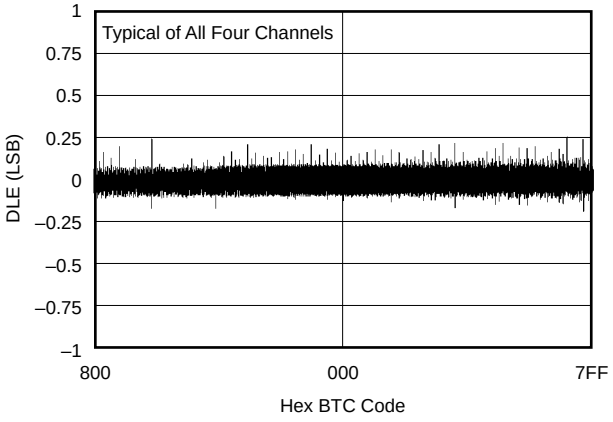
INTEGRAL LINEARITY ERROR vs CODE



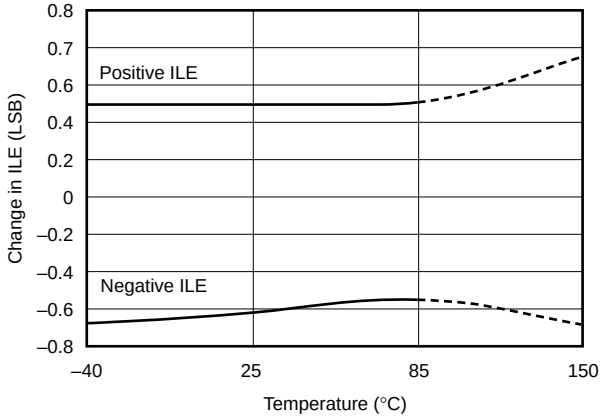
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, $+V_A$ + V_D = +5V, and V_{REF} = internal +2.5V, f_{CLK} = 8MHz, f_{SAMPLE} = 500kSPS, unless otherwise noted.

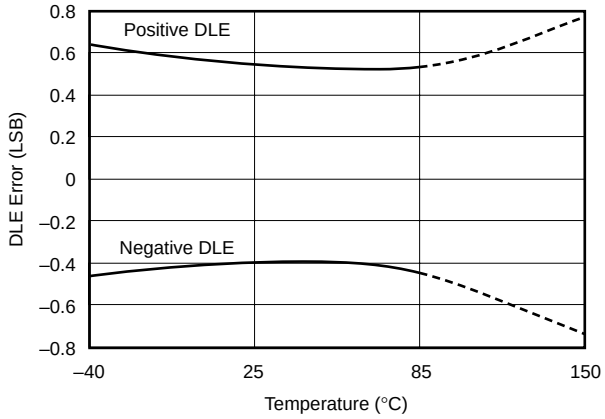
DIFFERENTIAL LINEARITY ERROR vs CODE



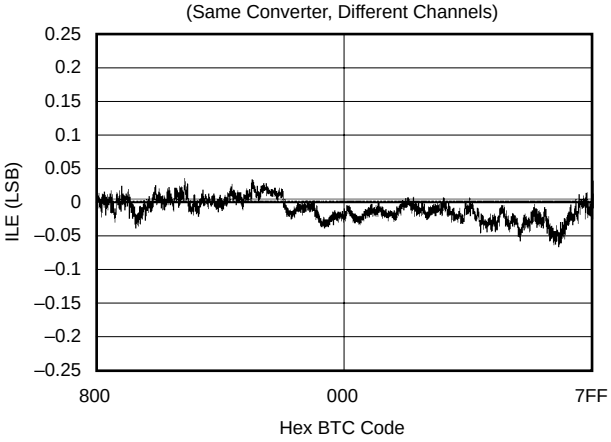
INTEGRAL LINEARITY ERROR vs TEMPERATURE



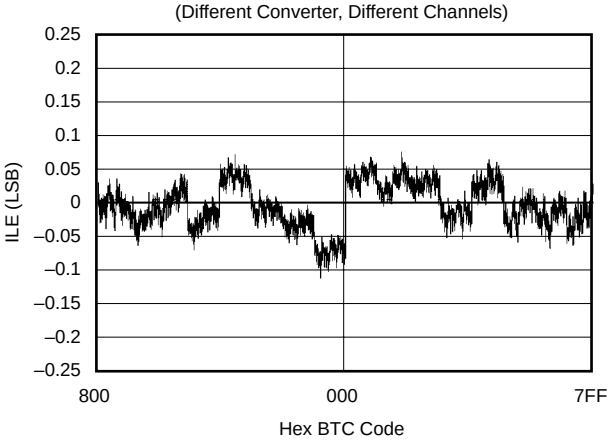
DIFFERENTIAL LINEARITY ERROR
vs TEMPERATURE



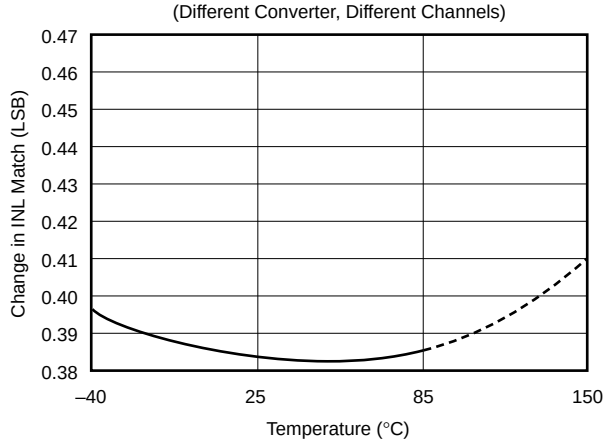
INTEGRAL LINEARITY ERROR MATCH
vs CODE CHANNEL A0/CHANNEL A1
(Same Converter, Different Channels)



INTEGRAL LINEARITY ERROR MATCH
vs CODE CHANNEL A0/CHANNEL B1
(Different Converter, Different Channels)



INTEGRAL LINEARITY ERROR MATCH
vs TEMPERATURE
Channel A0/Channel B0
(Different Converter, Different Channels)



INTRODUCTION

The ADS7861 is a high-speed, low power, dual, 12-bit A/D converter that operates from a single +5V supply. The input channels are fully differential with a typical common-mode rejection of 80dB. The part contains dual, 2µs successive approximation ADCs, two differential sample-and-hold amplifiers, an internal +2.5V reference with REF_{IN} and REF_{OUT} pins and a high-speed parallel interface. The ADS7861 requires an external clock. In order to achieve the maximum throughput rate of 500kSPS, the master clock must be set at 8MHz. A minimum of 16 clock cycles are required for each 12-bit conversion.

There are four analog inputs that are grouped into two channels (A and B). Channel selection is controlled by the M0, M1 and A0 pins. Each channel has two inputs (A0 and A1 and B0 and B1) that can be sampled and converted simultaneously, thus preserving the relative phase information of the signals on both analog inputs. The part accepts an analog input voltage in the range of $-V_{REF}$ to $+V_{REF}$, centered around the internal +2.5V reference. The part will also accept bipolar input ranges when a level shift circuit is used at the front end (see Figure 7).

All conversions are initiated on the ADS7861 by bringing the CONVST pin HIGH for a minimum of 15ns. CONVST HIGH places both sample-and-hold amplifiers in the hold state simultaneously and the conversion process is started on both channels. The RD pin can be connected to CONVST to simplify operation. Depending on the status of the M0, M1 and A0 pins, the ADS7861 will (a) operate in either two-channel or four-channel mode and (b) output data on both the Serial A and Serial B output or both channels can be transmitted on the A output only.

NOTE: See the Timing and Control section of this data sheet for more information.

SAMPLE-AND-HOLD SECTION

The sample-and-hold amplifiers on the ADS7861 allow the ADCs to accurately convert an input sine wave of full-scale amplitude to 12-bit accuracy. The input bandwidth of the sample-and-hold is greater than the Nyquist rate (Nyquist equals one-half of the sampling rate) of the ADC even when the ADC is operated at its maximum throughput rate of 500kSPS. The typical small-signal bandwidth of the sample-and-hold amplifiers is 40MHz.

Typical aperture delay time or the time it takes for the ADS7861 to switch from the sample to the hold mode following the CONVST pulse is 3.5ns. The average delta of repeated aperture delay values is typically 50ps (also known as aperture jitter). These specifications reflect the ability of the ADS7861 to capture AC input signals accurately at the exact same moment in time.

REFERENCE

Under normal operation, the REF_{OUT} pin should be directly connected to the REF_{IN} pin to provide an internal +2.5V reference to the ADS7861. The ADS7861 can operate, however, with an external reference in the range of 1.2V to 2.6V for a corresponding full-scale range of 2.4V to 5.2V.

The internal reference of the ADS7861 is double-buffered. If the internal reference is used to drive an external load, a buffer is provided between the reference and the load applied to pin 2 (the internal reference can typically source 2mA of current load—capacitance should not exceed 100pF). If an external reference is used, the second buffer provides isolation between the external reference and the CDAC. This buffer is also used to recharge all of the capacitors of both CDACs during conversion.

ANALOG INPUT

The analog input is bipolar and fully differential. There are two general methods of driving the analog input of the ADS7861: single-ended or differential (see Figures 1 and 2). When the input is single-ended, the –IN input is held at the common-mode voltage. The +IN input swings around the same common voltage and the peak-to-peak amplitude is the (common-mode $+V_{REF}$) and the (common-mode $-V_{REF}$). The value of V_{REF} determines the range over which the common-mode voltage may vary (see Figure 3).

When the input is differential, the amplitude of the input is the difference between the +IN and –IN input, or (+IN) – (–IN). The peak-to-peak amplitude of each input is $\pm 1/2V_{REF}$ around this common voltage. However, since the inputs are 180° out of phase, the peak-to-peak amplitude of the differential voltage is $+V_{REF}$ to $-V_{REF}$. The value of V_{REF} also determines the range of the voltage that may be common to both inputs (see Figure 4).

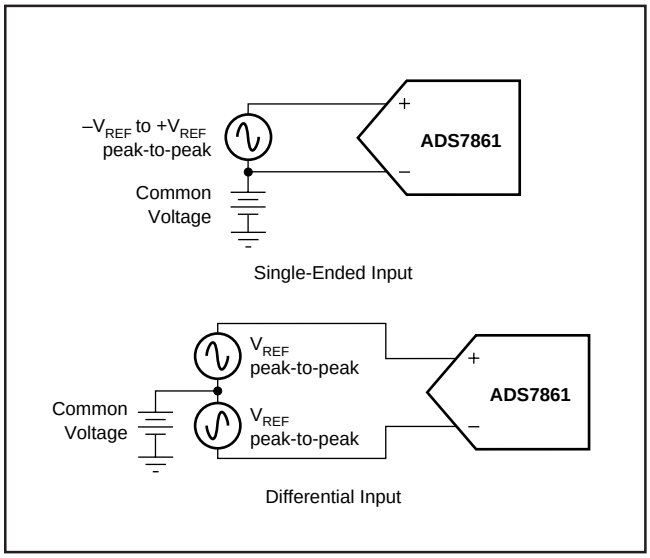
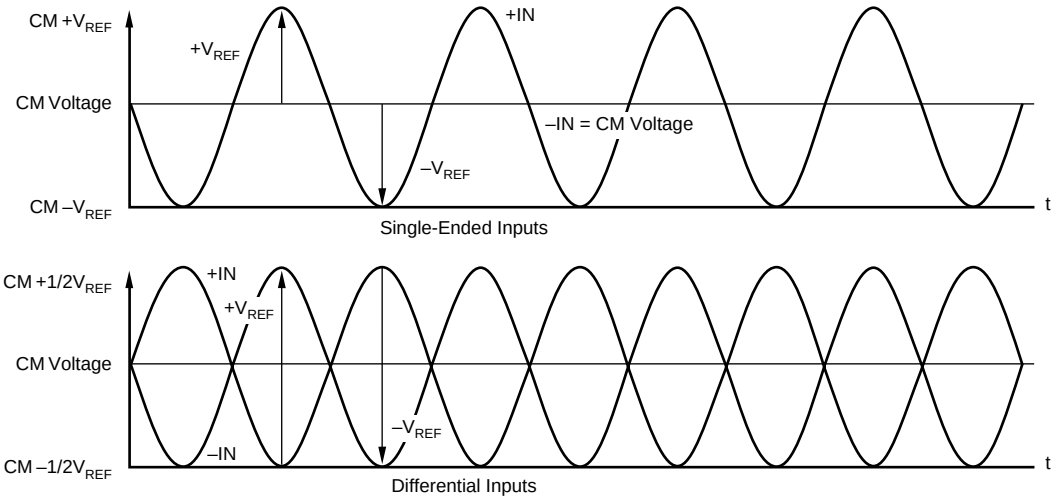


FIGURE 1. Methods of Driving the ADS7861 Single-Ended or Differential.



NOTES: Common-Mode Voltage (Differential Mode) = $\frac{(IN+) + (IN-)}{2}$ Common-Mode Voltage (Single-Ended Mode) = IN–.

The maximum differential voltage between +IN and –IN of the ADS7861 is V_{REF}. See Figures 3 and 4 for a further explanation of the common voltage range for single-ended and differential inputs.

FIGURE 2. Using the ADS7861 in the Single-Ended and Differential Input Modes.

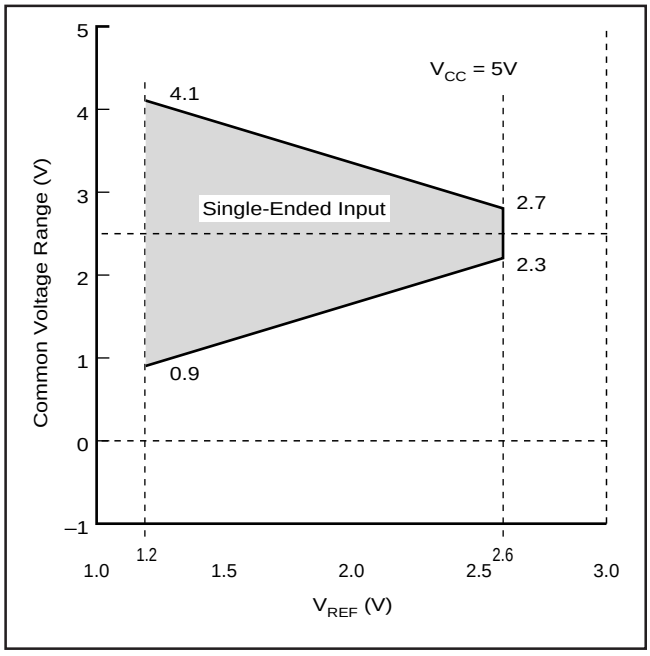


FIGURE 3. Single-Ended Input: Common-Mode Voltage Range vs V_{REF}.

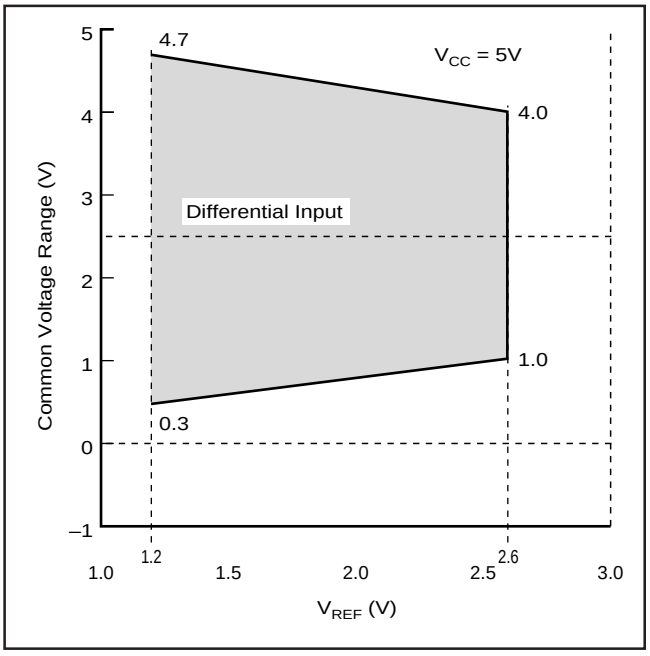


FIGURE 4. Differential Input: Common-Mode Voltage Range vs V_{REF}.

In each case, care should be taken to ensure that the output impedance of the sources driving the +IN and –IN inputs are matched. Otherwise, this may result in offset error, gain error and linearity error which will change with both temperature and input voltage.

The input current on the analog inputs depend on a number of factors: sample rate, input voltage, and source impedance. Essentially, the current into the ADS7861 charges the internal capacitor array during the sampling period. After this capacitance has been fully charged, there is no further input current. The source of the analog input voltage must be able to charge the input capacitance (15pF) to a 12-bit settling level within 2 clock cycles. When the converter goes into the hold mode, the input impedance is greater than 1GΩ.

Care must be taken regarding the absolute analog input voltage. The +IN input should always remain within the range of GND – 300mV to V_{DD} + 0.3V.

TRANSITION NOISE

Figure 5 shows a histogram plot for the ADS7861 following 8,000 conversions of a DC input. The DC input was set at output code 2046. All but one of the conversions had an output code result of 2046 (one of the conversions resulted in an output of 2047). The histogram reveals the excellent noise performance of the ADS7861.

BIPOLAR INPUTS

The differential inputs of the ADS7861 were designed to accept bipolar inputs ($-V_{REF}$ and $+V_{REF}$) around the internal reference voltage (2.5V), which corresponds to a 0V to 5V input range with a 2.5V reference. By using a simple op amp circuit featuring a single amplifier and four external resistors, the ADS7861 can be configured to except bipolar inputs. The conventional ±2.5V, ±5V, and ±10V input ranges can be interfaced to the ADS7861 using the resistor values shown in Figure 7.

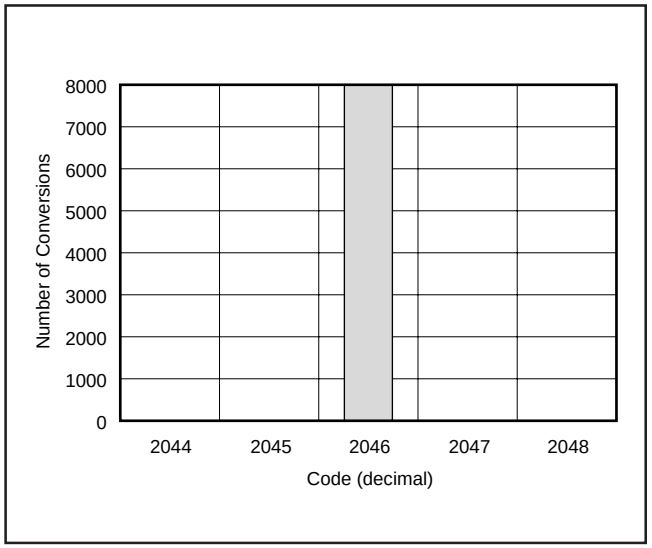


FIGURE 5. Histogram of 8,000 Conversions of a DC Input.

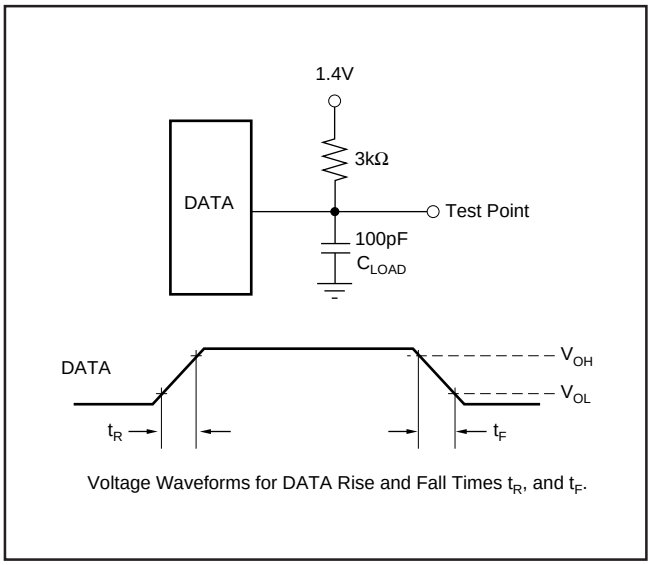


FIGURE 6. Test Circuits for Timing Specifications.

DESCRIPTION	ANALOG INPUT	DIGITAL OUTPUT BINARY TWO'S COMPLEMENT	
Full-Scale Input Span	$-V_{REF}$ to $+V_{REF}$ (1)		
Least Significant Bit (LSB)	$(-V_{REF}$ to $+V_{REF})/4096$ (2)	BINARY CODE	HEX CODE
+Full Scale	4.99878V	0111 1111 1111	7FF
Midscale	2.5V	0000 0000 0000	000
Midscale – 1 LSB	2.49878V	1111 1111 1111	FFF
–Full Scale	0V	1000 0000 0000	800

NOTES: (1) $-V_{REF}$ to $+V_{REF}$ around V_{REF}. With a 2.5V reference, this corresponds to a 0V to 5V input span. (2) 1.22mV with a 2.5V reference.

TABLE I. Ideal Input Voltages and Output Codes.

TIMING AND CONTROL

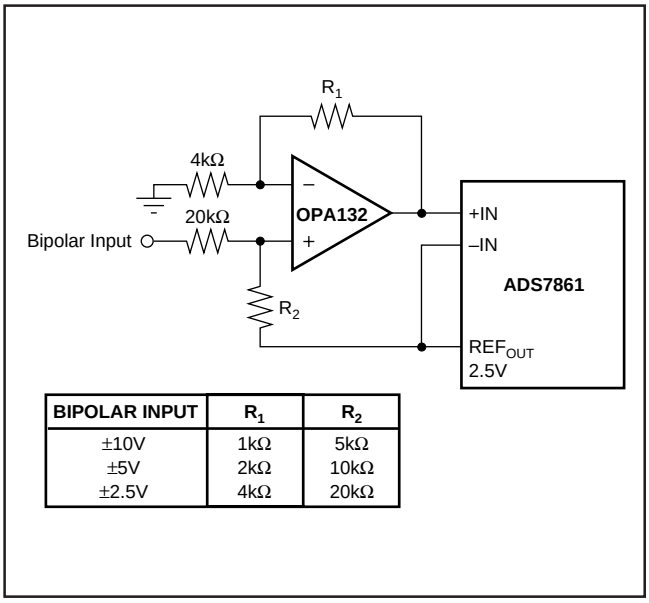
The operation of the ADS7861 can be configured in four different modes by using the address pins M0, M1 and A0.

The M0 pin selects between two- and four-channel operation (in two-channel operation, the A0 pin selects between Channels 0 and 1; in four-channel operation the A0 pin is ignored and the channels are switched automatically after each conversion). The M1 pin selects between having serial data transmitted simultaneously on both the Serial A data output and the Serial B data output or having both channels output data through the Serial A port. The A0 pin selects either Channel 0 or Channel 1 (see Pin Descriptions and Serial Output Truth Table for more information).

The next four sections will explain the four different modes of operation.

Mode I (M0 = 0, M1 = 0)

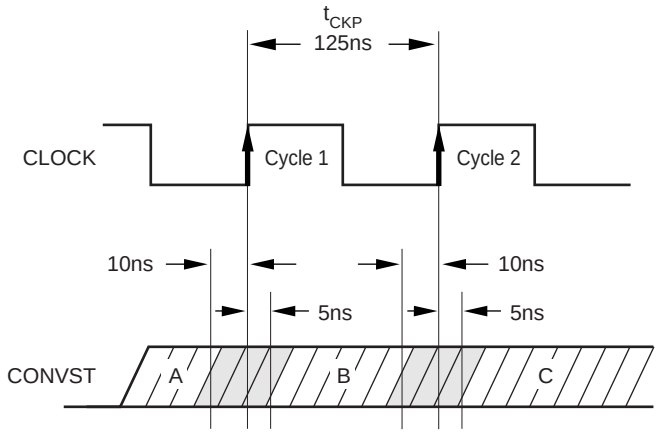
With the M0 and M1 pins both set to '0', the ADS7861 will operate in two-channel operation (the A0 pin must be used to switch between Channels A and B). A conversion is initiated by bringing CONVST HIGH for a minimum of 15ns. It is very important that CONVST be brought HIGH a minimum of 10ns prior to a rising edge of the external clock or 5ns after the rising edge. If CONVST is brought



BIPOLAR INPUT	R_1	R_2
±10V	1kΩ	5kΩ
±5V	2kΩ	10kΩ
±2.5V	4kΩ	20kΩ

FIGURE 7. Level Shift Circuit for Bipolar Input Ranges.

HIGH within this window, it is then uncertain as to when the ADS7861 will initiate conversion (see Figure 8 for a more detailed description). Sixteen clock cycles are required to perform a single conversion. Immediately following CONVST switching to HIGH, the ADS7861 will switch from the sample mode to the hold mode asynchronous to the external clock. The BUSY output pin will then go HIGH and remain HIGH for the duration of the conversion cycle. On the falling edge of the first cycle of the external clock, the ADS7861 will latch in the address for the next conversion cycle depending on the status of the A0 pin (HIGH = Channel 1, LOW = Channel 0). The address must be selected 15ns prior to the falling edge of cycle one of the external clock and must remain 'held' for 15ns following the clock edge. For maximum throughput time, the CONVST and RD pins should be tied together. CS must be brought LOW to enable the two serial outputs. Data will be valid on the falling edge of all 16 clock cycles per conversion. The first bit of data will be a status flag for either Channel 0 or 1, the second bit will be a second status flag for either Channel A or B. The subsequent data will be MSB-first through the LSB, followed by two zeros (see Table II and Figures 9 and 10).



NOTE: All CONVST commands which occur more than 10ns before the rising edge of cycle '1' of the external clock (Region 'A') will initiate a conversion on the rising edge of cycle '1'. All CONVST commands which occur 5ns after the rising edge of cycle '1' or 10ns before the rising edge of cycle 2 (Region 'B') will initiate a conversion on the rising edge of cycle '2'. All CONVST commands which occur 5ns after the rising edge of cycle '2' (Region 'C') will initiate a conversion on the rising edge of the next clock period. The CONVST pin should never be switched from LOW to HIGH in the region 10ns prior to the rising edge of the CLOCK and 5ns after the rising edge (gray areas). If CONVST is toggled in this gray area, the conversion could begin on either the same rising edge of the CLOCK or the following edge.

FIGURE 8. Conversion Mode.

TIMING SPECIFICATIONS

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS	COMMENTS
t_{CONV}	Conversion Time	1.75			µs	When T_{CKP} = 125ns
t_{ACQ}	Acquisition Time	0.25			µs	When T_{CKP} = 125ns
t_{CKP}	Clock Period	125		5000	ns	
t_{CKL}	Clock LOW	40			ns	
t_{CKH}	Clock HIGH	40			ns	
t_F	DOUT Fall Time			25	ns	
t_R	DOUT Rise Time			30	ns	
t_1	CONVST HIGH	15			ns	
t_2	Address Setup Time	15			ns	Address latched on falling edge of CLK cycle '2'
t_3	Address Hold Time	15				
t_4	RD Setup Time	15			ns	Before falling edge of CLOCK
t_5	RD to $\overline{CS}$ Hold Time	15			ns	After falling edge of CLOCK
t_6	CONVST LOW	20			ns	
t_7	RD LOW	20			ns	
t_8	$\overline{CS}$ to Data Valid			25	ns	
t_9	CLOCK to Data Valid Delay			30	ns	Maximum delay following rising edge of CLOCK
t_{10}	Data Valid After CLOCK(1)			1	ns	Time data is valid after second rising edge of CLOCK

NOTE: (1) 'n – 1' data will remain valid 1ns after rising edge of next CLOCK cycle.

CLOCK CYCLE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
SERIAL DATA	CH0 OR CH1	CHA OR CHB	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	0	0

TABLE II. Serial Data Output Format.

Mode II (M0 = 0, M1 = 1)

With M1 set to '1', the ADS7861 will output data on the Serial Data A pin only. All other pins function in the same manner as Mode I except that the Serial Data B output will tri-state (i.e., high impedance) after a conversion following M1 going HIGH. Another difference in this mode involves the CONVST pin. Since it takes 32 clock cycles to output the results from both A/D converters (rather than 16 when M1 = 0), the ADS7861 will take 4µs to complete a conversion on both A/Ds (See Figure 11).

Mode III (M0 = 1, M1 = 0)

With M0 set to '1', the ADS7861 will cycle through Channels 0 and 1 sequentially (the A0 pin is ignored). At the same time, setting M1 to '0' places both Serial Outputs, A and B, in the active mode (See Figure 12).

Mode IV (M0 = 1, M1 = 1)

Similar to Mode II, Mode IV uses the Serial A output line to transmit data exclusively. Following the first conversion after M1 goes HIGH, the serial B output will go into tri-state. See Figure 13. As in Mode II, the second CONVST command is always ignored when M1 = 1.

READING DATA

In all four timing diagrams, the CONVST pin and the RD pins are tied together. If so desired, the two lines can be separated. Data on the Serial Output pins (A and B) will become valid following the third rising SCLK edge following RD rising edge. Refer to Table II for data output format.

LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS7861 circuitry. This is particularly true if the CLOCK input is approaching the maximum throughput rate.

The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections and digital inputs that occur just prior to latching the output of the analog comparator. Thus, driving any single conversion for an n-bit SAR converter, there are n "windows" in which large external transient voltages can affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic or high power devices. The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. Their error can change if the external event changes in time with respect to the CLOCK input.

With this in mind, power to the ADS7861 should be clean and well-bypassed. A 0.1µF ceramic bypass capacitor should be placed as close to the device as possible. In addition, a 1µF to 10µF capacitor is recommended. If needed, an even larger capacitor and a 5Ω or 10Ω series resistor may be used to low pass filter a noisy supply. On average, the ADS7861 draws very little current from an external reference as the reference voltage is internally buffered. However, glitches from the conversion process appear at the V_{REF} input and the reference source must be able to handle this. Whether the reference is internal or external, the V_{REF} pin should be bypassed with a 0.1µF capacitor. An additional larger capacitor may also be used, if desired. If the reference voltage is external and originates from an op amp, make sure that it can drive the bypass capacitor or capacitors without oscillation. No bypass capacitor is necessary when using the internal reference (tie pin 10 directly to pin 11).

The GND pin should be connected to a clean ground point. In many cases, this will be the 'analog' ground. Avoid connections which are too near the grounding point of a microcontroller or digital signal processor. If required, run a ground trace directly from the converter to the power supply entry point. The ideal layout will include an analog ground plane dedicated to the converter and associated analog circuitry.

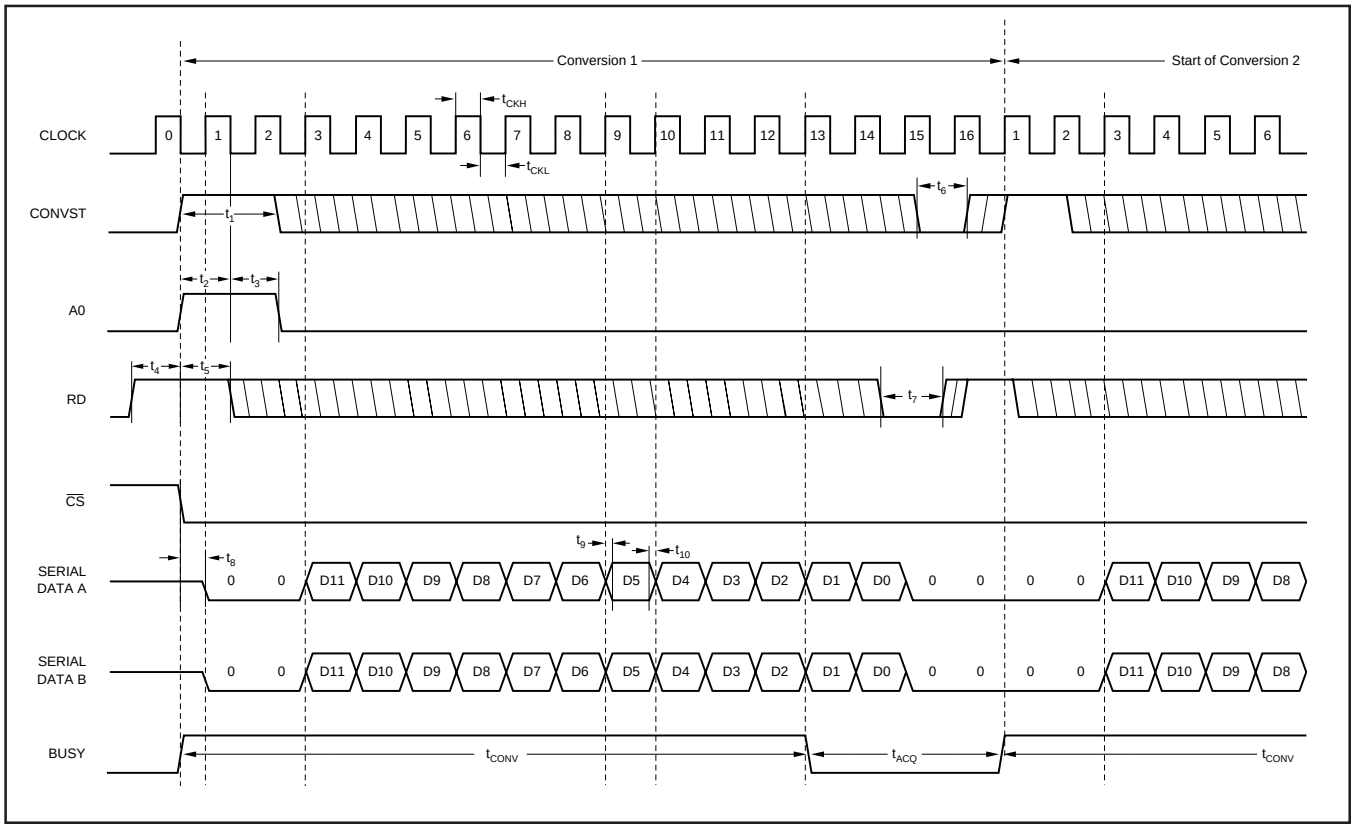


FIGURE 9. Mode I with Timing Specifications.

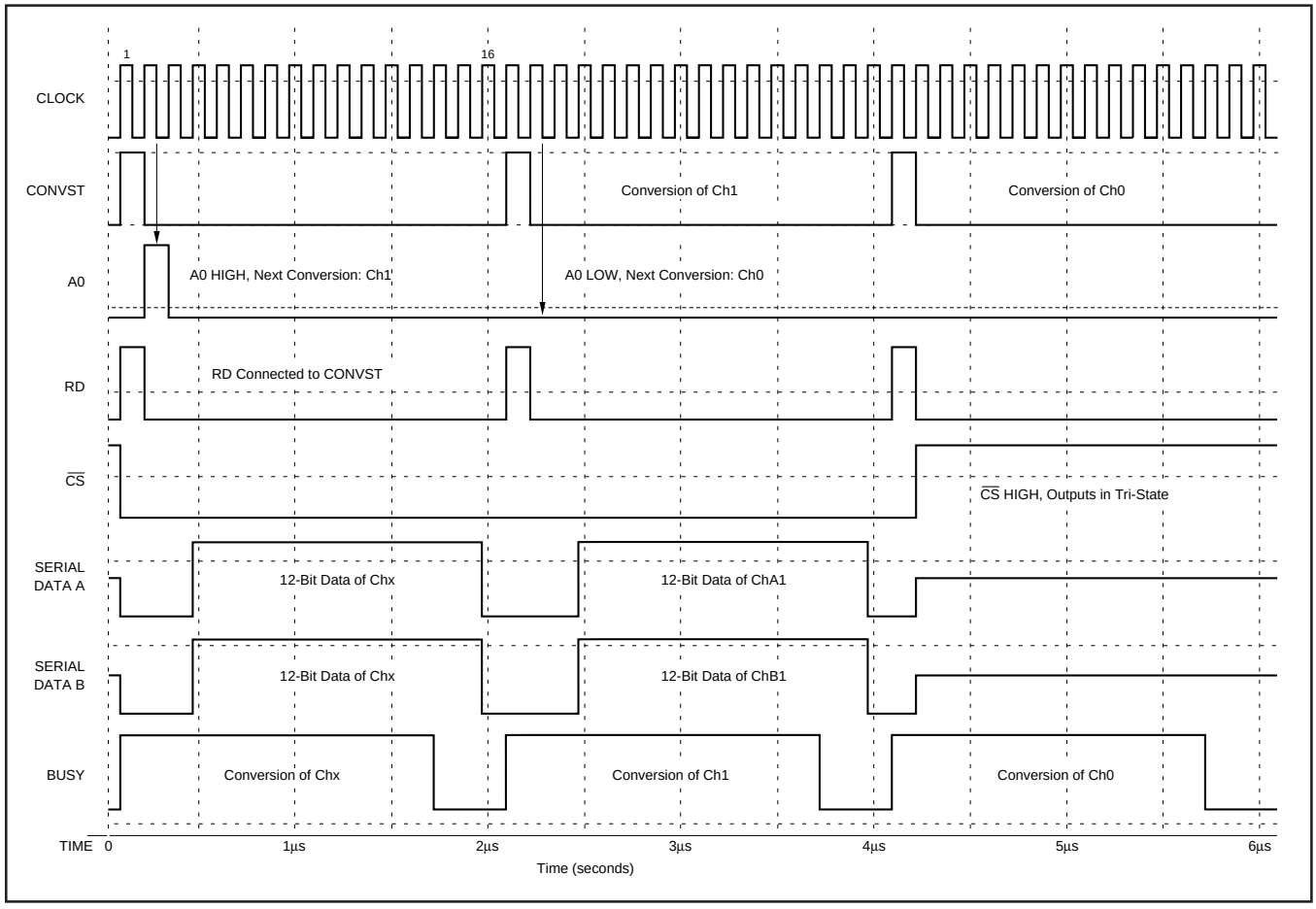


FIGURE 10. Mode I, Timing Diagram for M0 = 0 and M1 = 0.

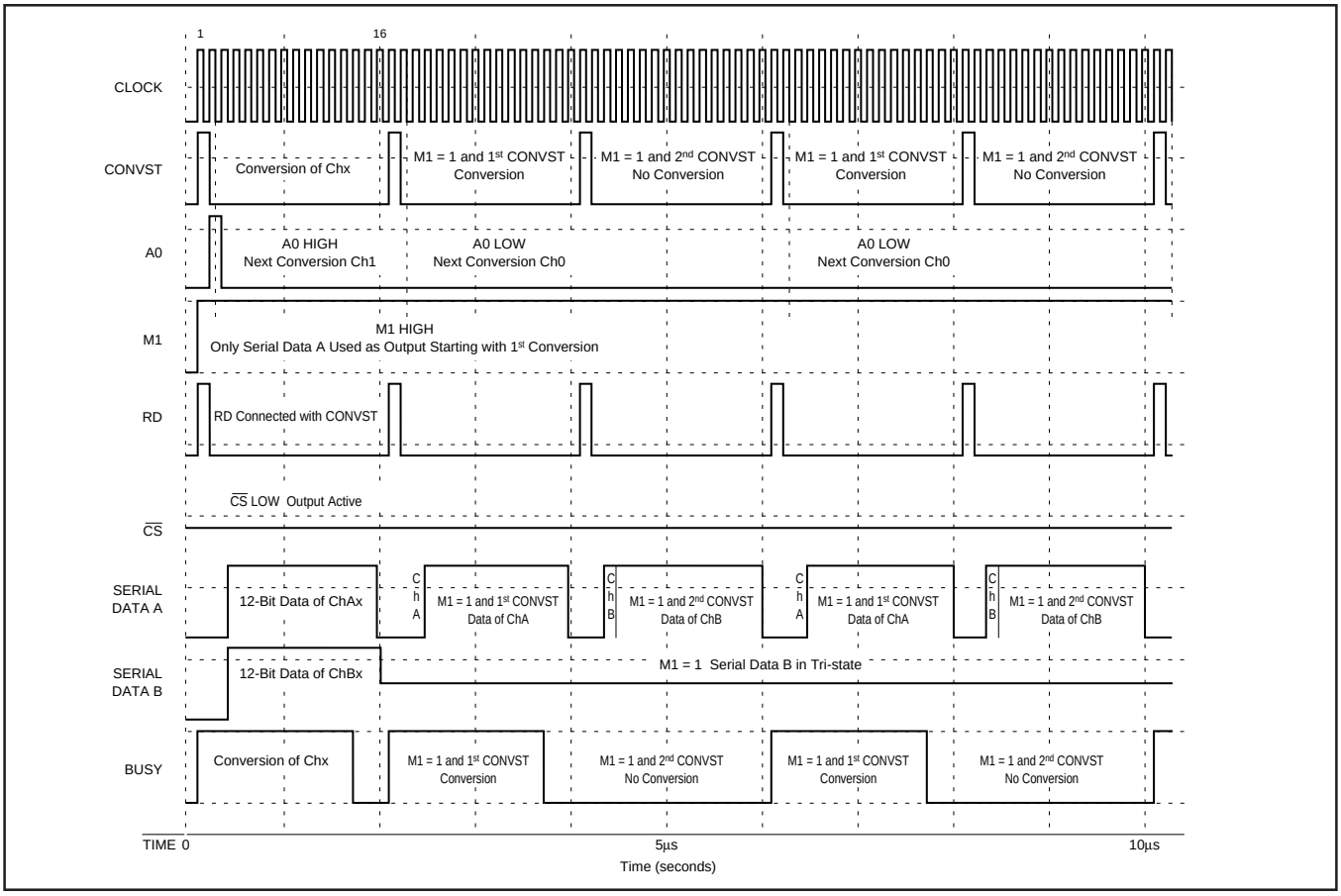


FIGURE 11. Mode II, Timing Diagram for M0 = 0 and M1 = 1.

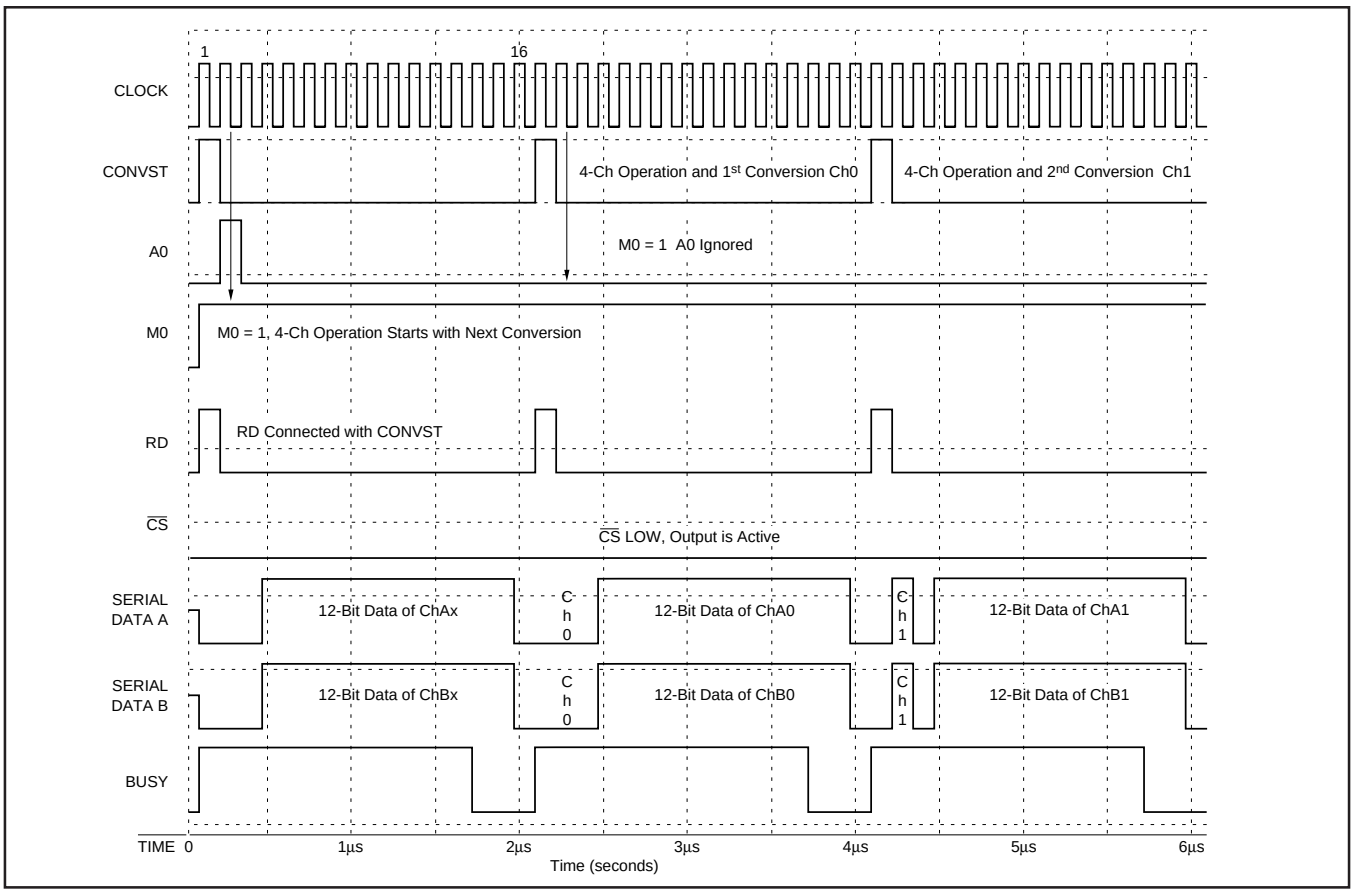


FIGURE 12. Mode III, Timing Diagram for M0 = 1 and M1 = 0.

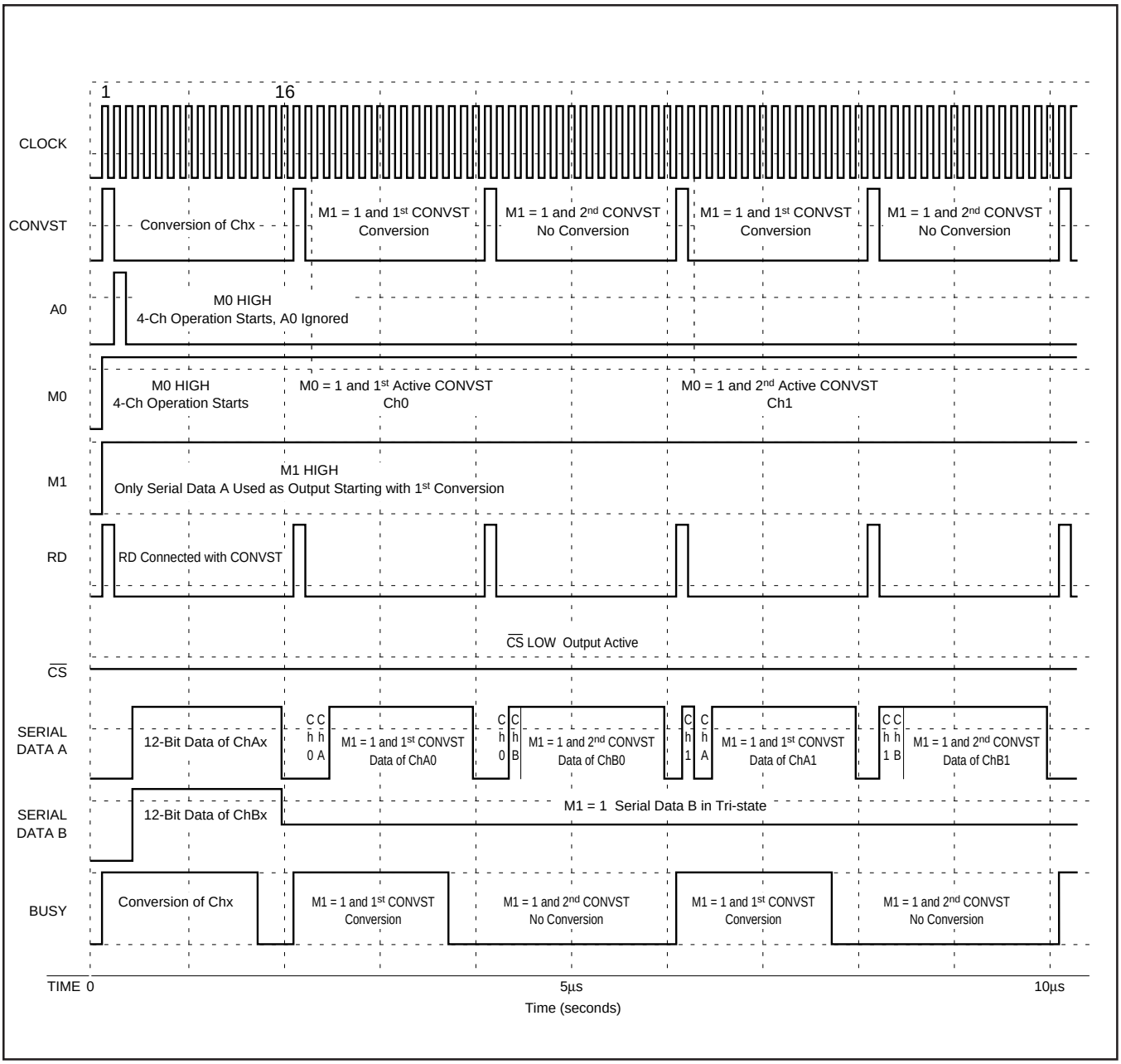


FIGURE 13. Mode IV, Timing Diagram for M0 = 1 and M1 = 1.

Revision History

DATE	REVISION	PAGE	SECTION	DESCRIPTION
8/07	D	6	Pin Configuration	Added Note (1) to QFN package.
8/06	C	1	Entire Document	Changed Throughput Rate from 500kHz to 500kSPS throughout document.
		1	Features	Added Operating Temperature Range: –40°C to +125°C.
		1	Description	Changed Operating Temperature Range upper limit from +85°C to +125°C.
		2	Absolute Maximum Ratings	Changed Operating Temperature Range upper limit from +85°C to +125°C.
		3	Electrical Characteristics	Changed top-of-page header condition to begin with: "Over recommended operating free-air temperature range at..."
				Changed "T_{MIN} to T_{MAX}" to "T_A = –40°C to +125°C" in several locations.
				Added T_A = –40°C to +85°C to conditions for these parameters: Bipolar Offset Error, Total Harmonic Distortion, Spurious-Free Dynamic Range, Quiescent Current, and Power Dissipation.
				Added new row for T_A = –40°C to +125°C condition for these parameters: Bipolar Offset Error, Total Harmonic Distortion, Spuriouse-Free Dynamic Range, Quiescent Current, and Power Dissipation.
				Moved "V_{IN} = ±2.5V_{PP} at 100kHz" from conditions of Dynamic Characteristics to section header.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
ADS7861E	ACTIVE	SSOP/ QSOP	DBQ	24	56	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7861E/2K5	ACTIVE	SSOP/ QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7861E/2K5G4	ACTIVE	SSOP/ QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7861EB	ACTIVE	SSOP/ QSOP	DBQ	24	56	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7861EB/2K5	ACTIVE	SSOP/ QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7861EB/2K5G4	ACTIVE	SSOP/ QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7861EBG4	ACTIVE	SSOP/ QSOP	DBQ	24	56	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7861EG4	ACTIVE	SSOP/ QSOP	DBQ	24	56	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7861IBRHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7861IBRHBRG4	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7861IBRHBT	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7861IBRHBTG4	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7861IRHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7861IRHBRG4	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7861IRHBT	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7861IRHBTG4	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

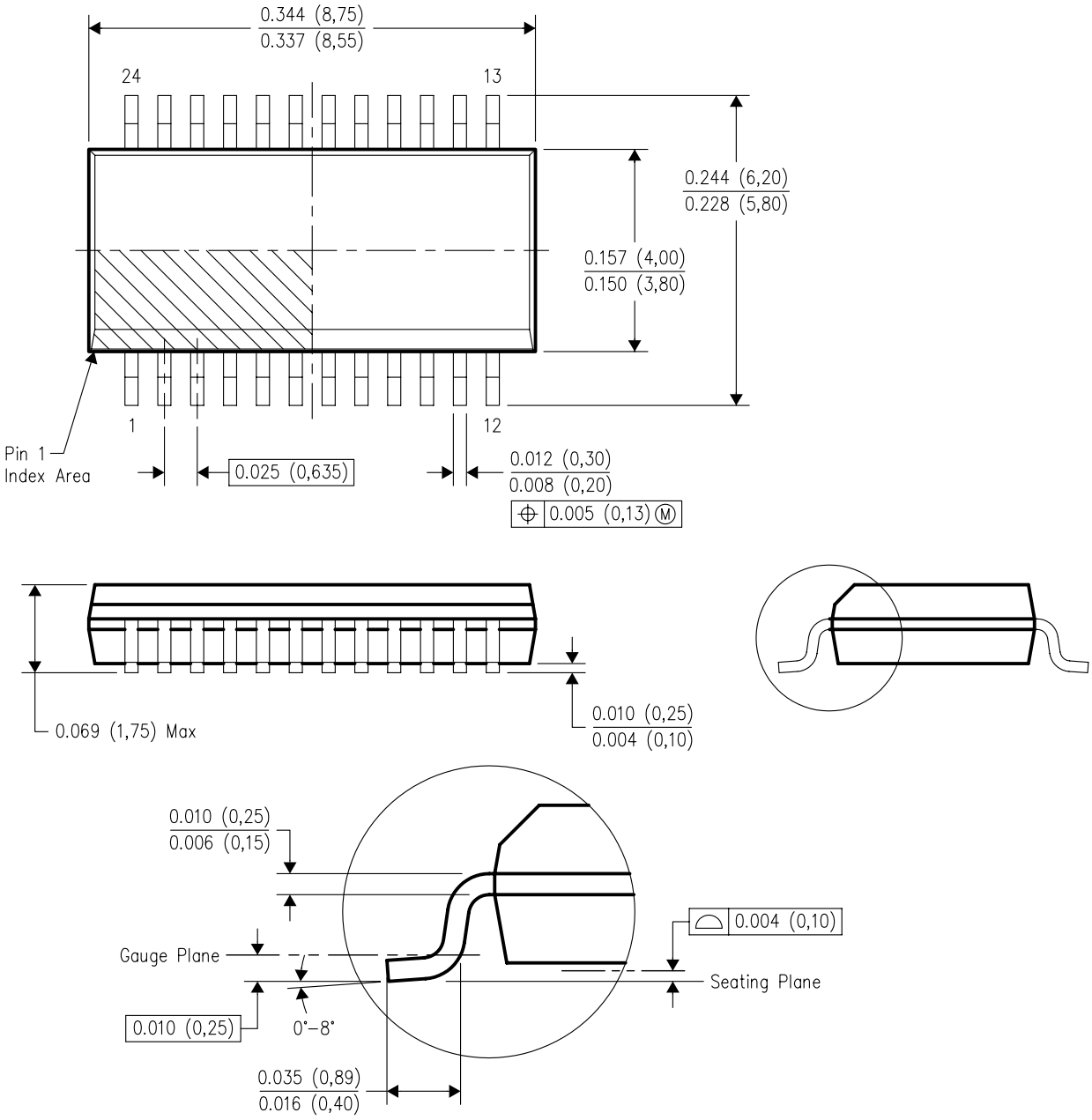
[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

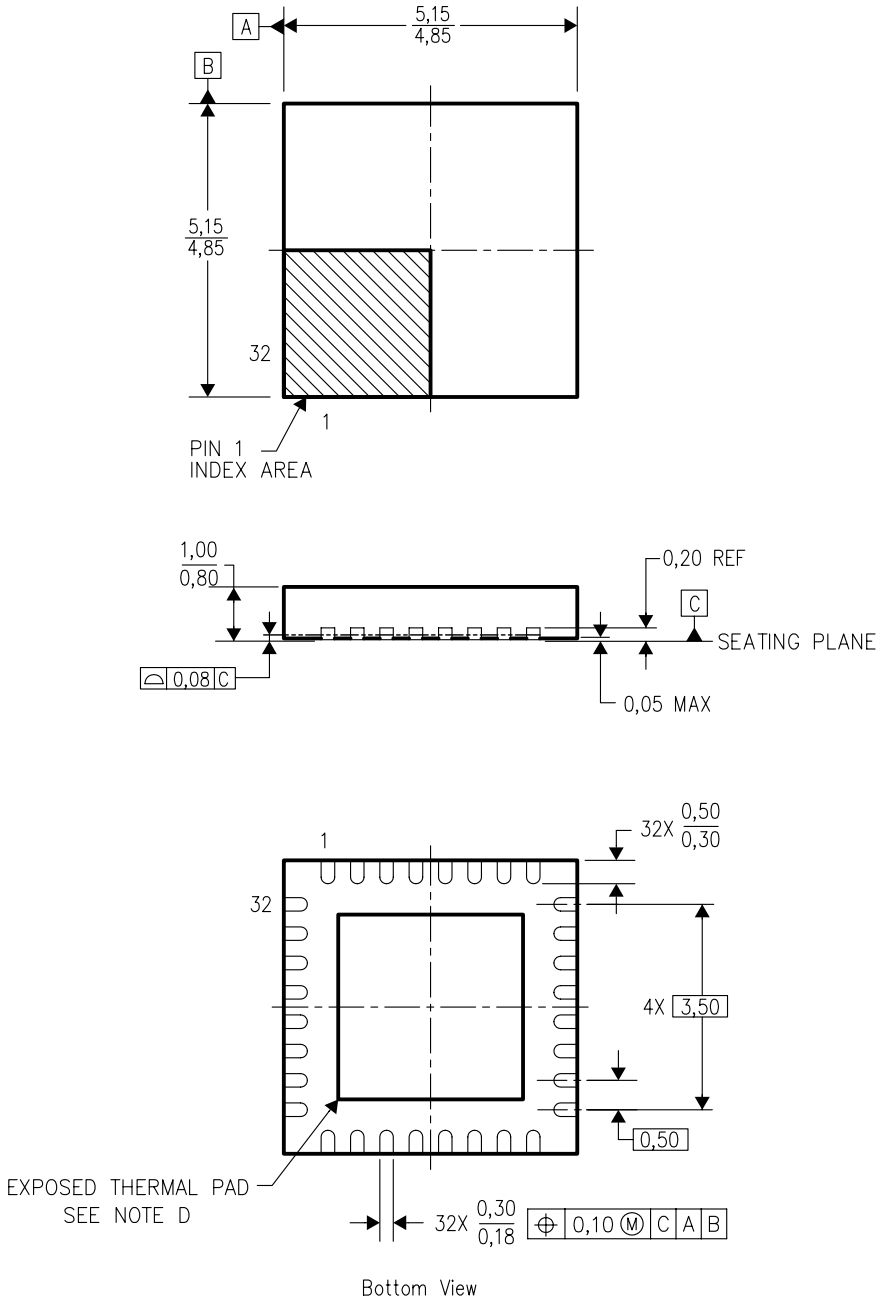
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DBQ (R–PDSO–G24) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AE.

RHB (S–PQFP–N32) PLASTIC QUAD FLATPACK



4204326/C xx/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D The Package thermal pad must be soldered to the board for thermal and mechanical performance. See product data sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

THERMAL PAD MECHANICAL DATA

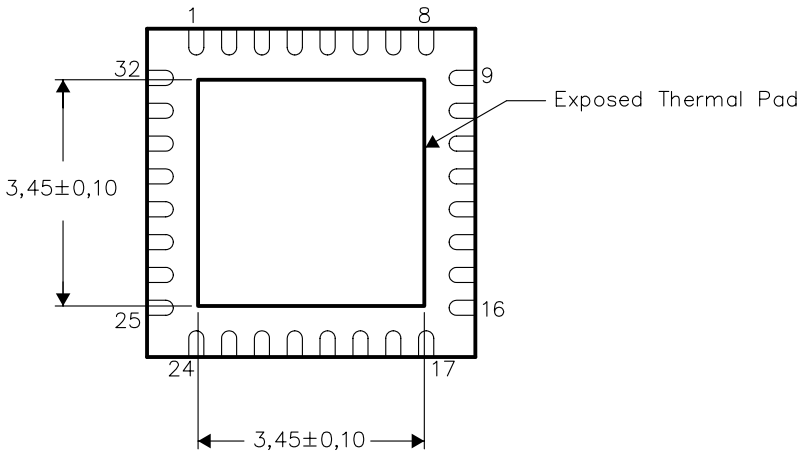
RHB (S–PQFP–N32)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

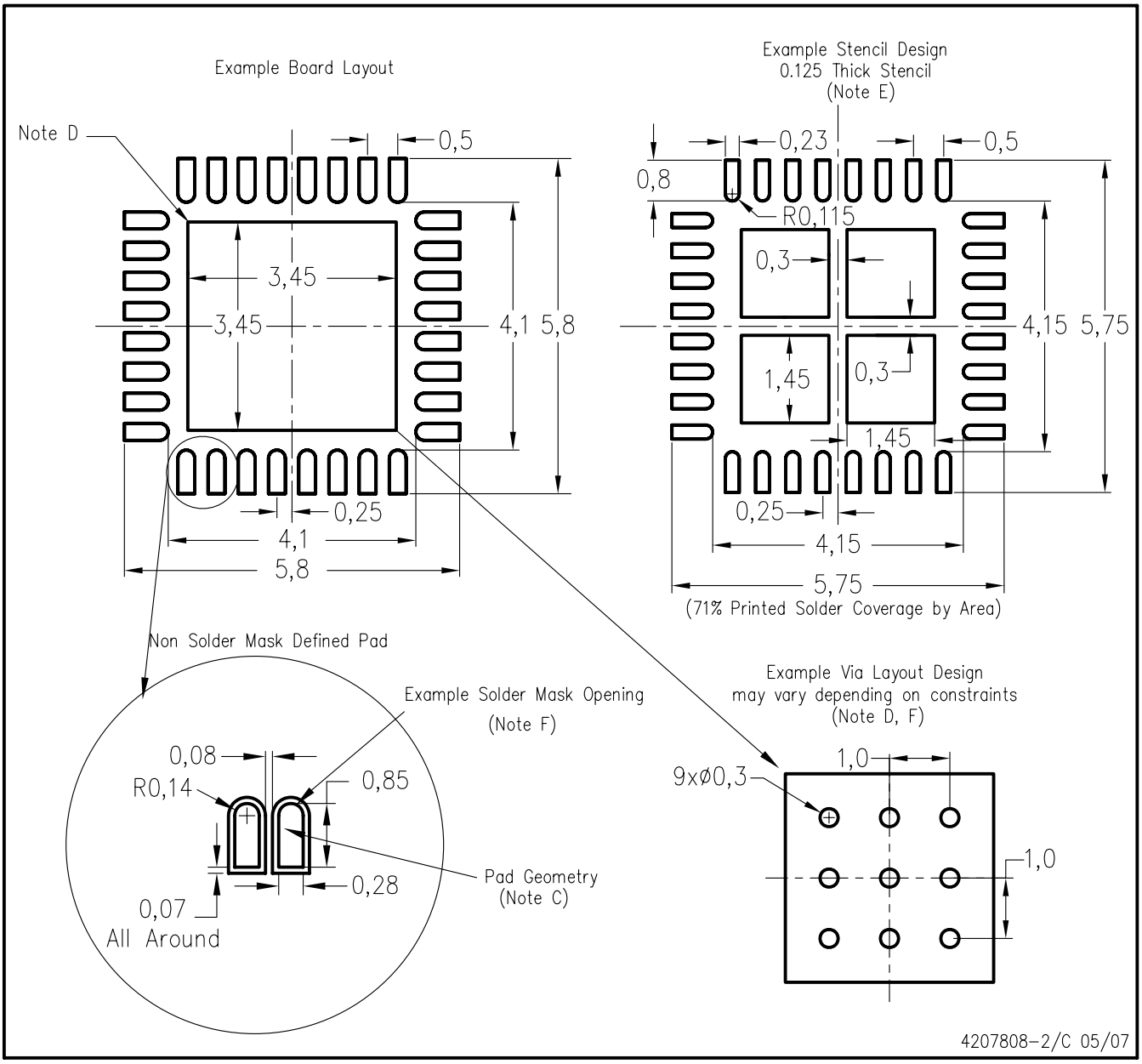


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RHB (S–PQFP–N32)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7861E	ACTIVE	SSOP	DBQ	24	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		ADS7861E	Samples
ADS7861E/2K5	ACTIVE	SSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		ADS7861E	Samples
ADS7861E/2K5G4	ACTIVE	SSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		ADS7861E	Samples
ADS7861EB	ACTIVE	SSOP	DBQ	24	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		ADS7861E B	Samples
ADS7861EB/2K5	ACTIVE	SSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		ADS7861E B	Samples
ADS7861EB/2K5G4	ACTIVE	SSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		ADS7861E B	Samples
ADS7861EBG4	ACTIVE	SSOP	DBQ	24	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		ADS7861E B	Samples
ADS7861EG4	ACTIVE	SSOP	DBQ	24	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		ADS7861E	Samples
ADS7861IBRHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		ADS 7861I B	Samples
ADS7861IBRHBRG4	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		ADS 7861I B	Samples
ADS7861IBRHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		ADS 7861I B	Samples
ADS7861IBRHBTG4	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		ADS 7861I B	Samples
ADS7861IRHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		ADS 7861I	Samples
ADS7861IRHBRG4	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		ADS 7861I	Samples
ADS7861IRHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		ADS 7861I	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7861IRHBTG4	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		ADS 7861I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

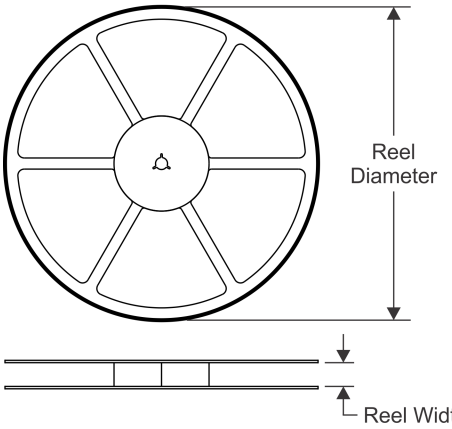
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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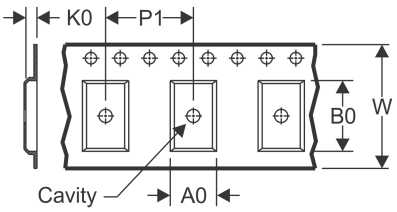
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

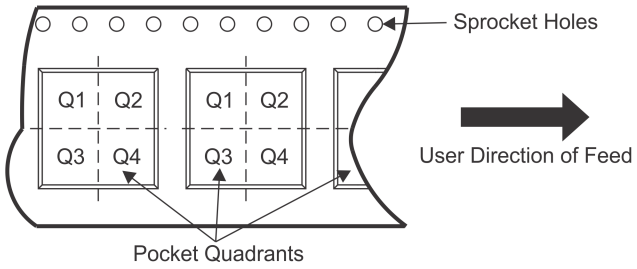


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

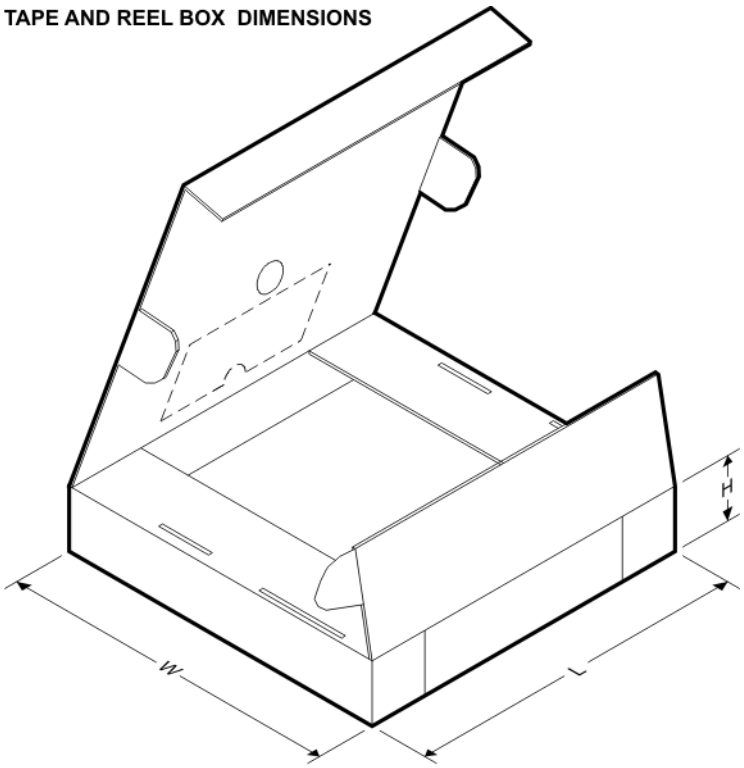
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7861E/2K5	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
ADS7861EB/2K5	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
ADS7861IBRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
ADS7861IBRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
ADS7861IRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
ADS7861IRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

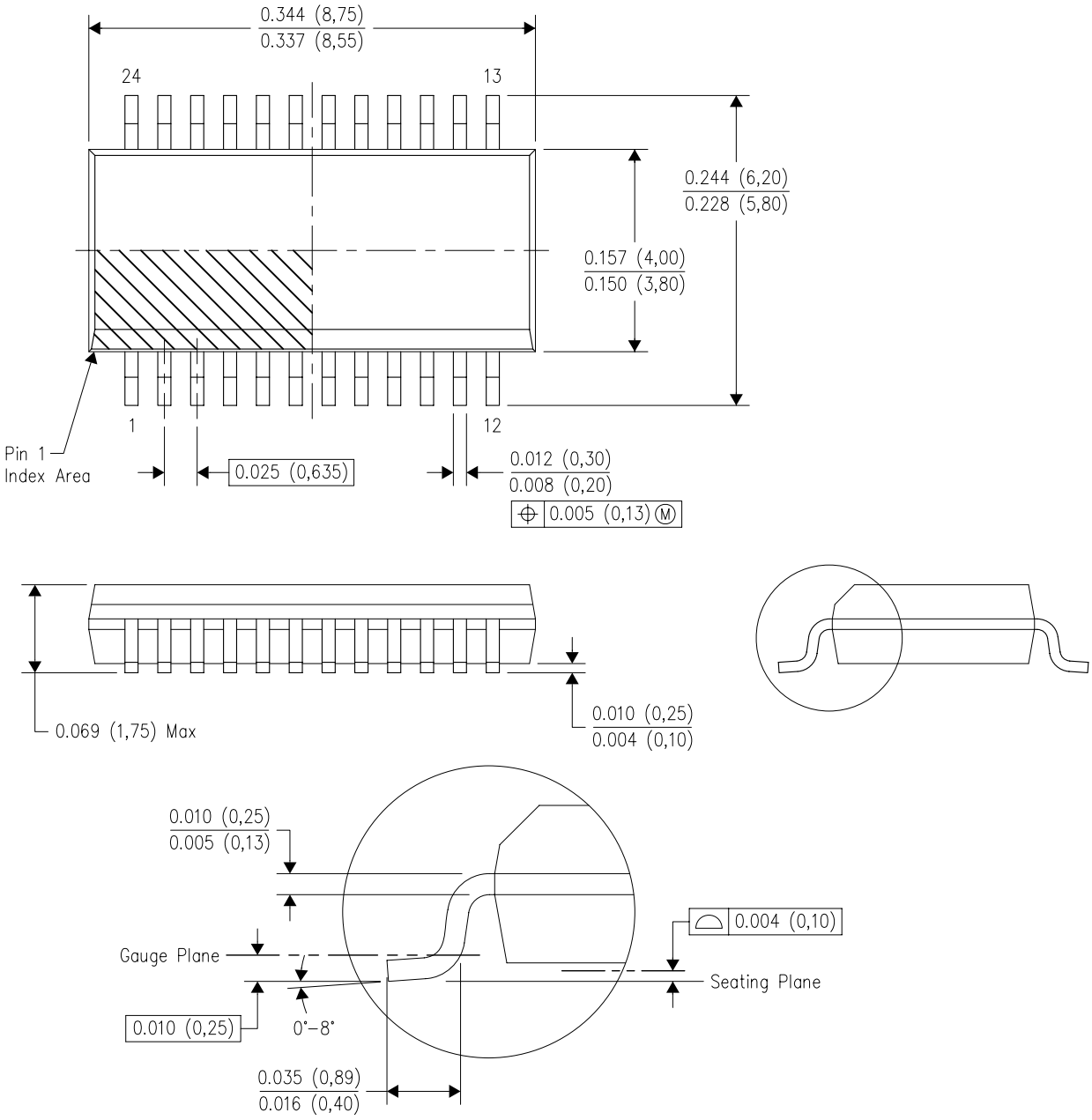
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

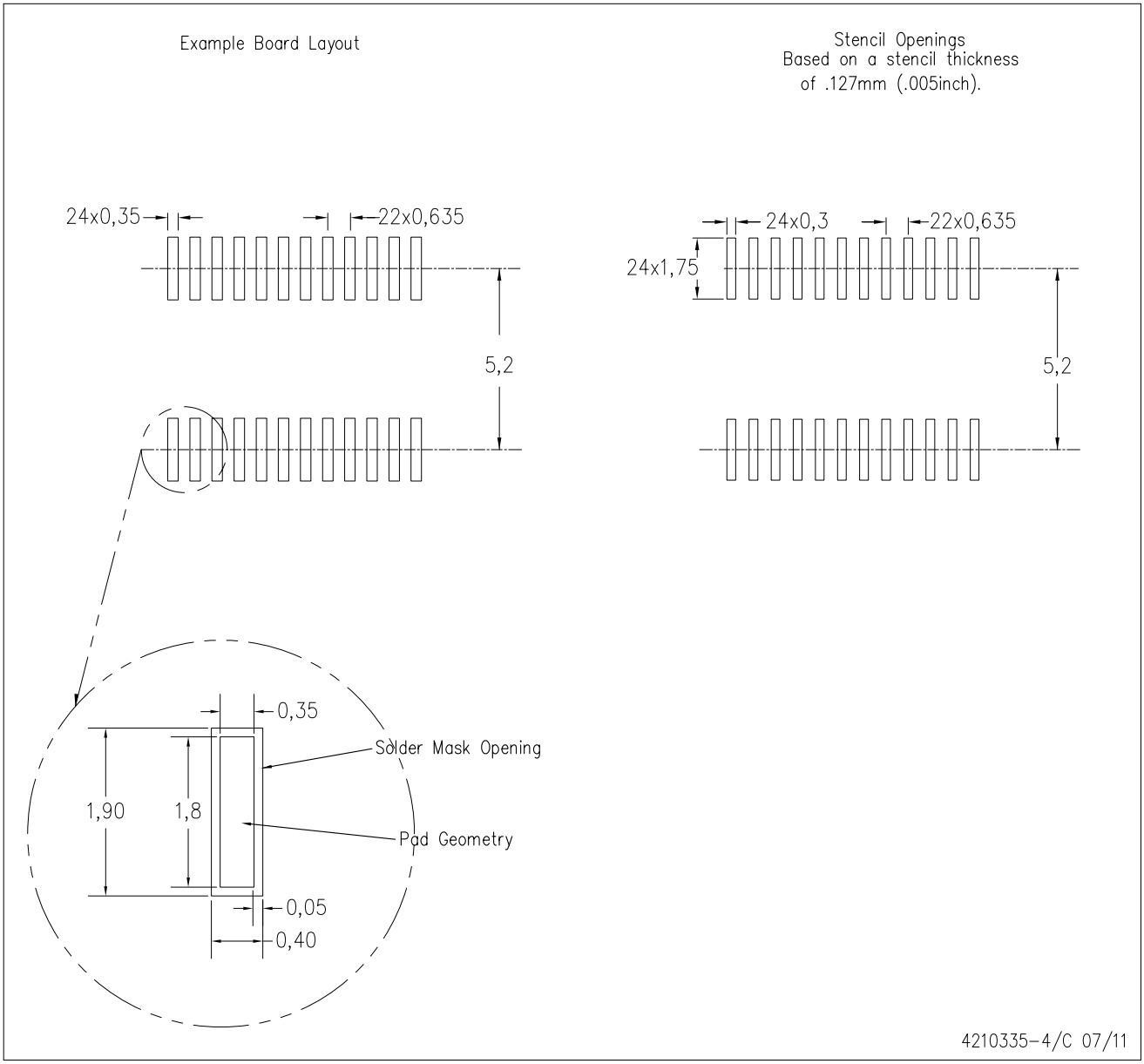
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7861E/2K5	SSOP	DBQ	24	2500	367.0	367.0	38.0
ADS7861EB/2K5	SSOP	DBQ	24	2500	367.0	367.0	38.0
ADS7861IBRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
ADS7861IBRHBT	VQFN	RHB	32	250	210.0	185.0	35.0
ADS7861IRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
ADS7861IRHBT	VQFN	RHB	32	250	210.0	185.0	35.0

DBQ (R–PDSO–G24) PLASTIC SMALL–OUTLINE PACKAGE



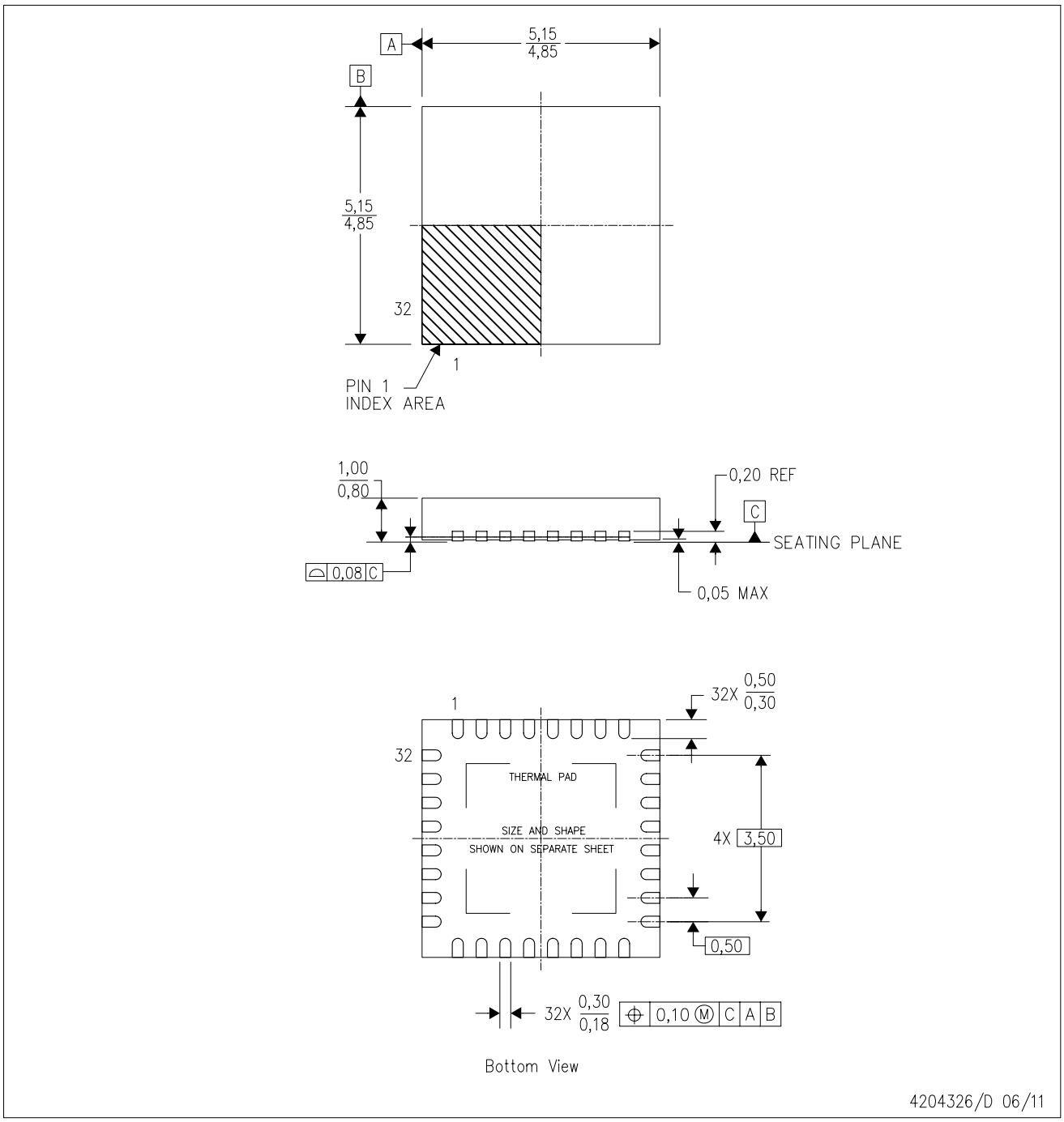
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AE.

DBQ (R–PDSO–G24) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

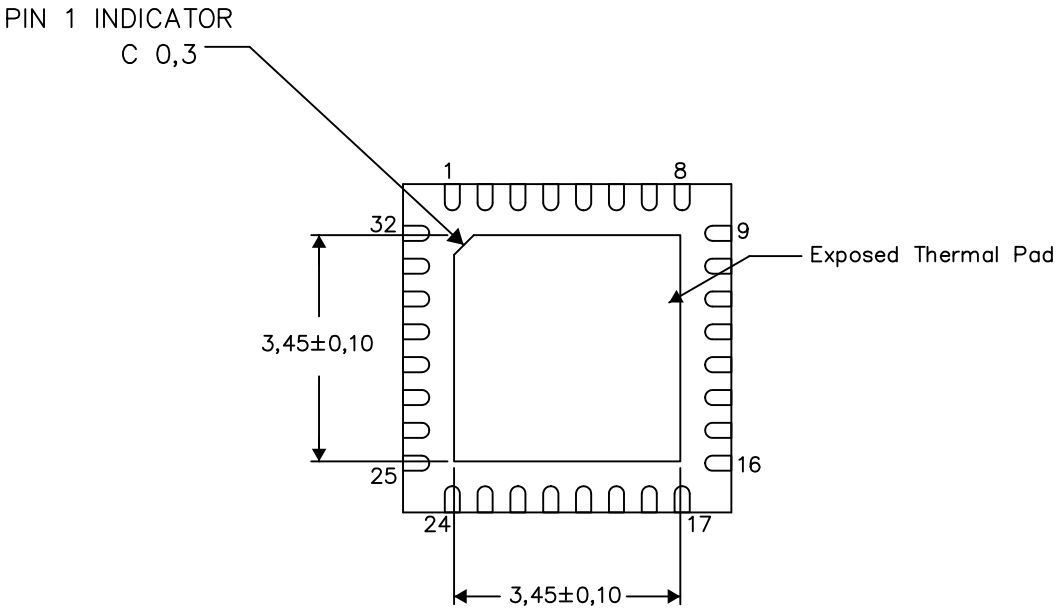
RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



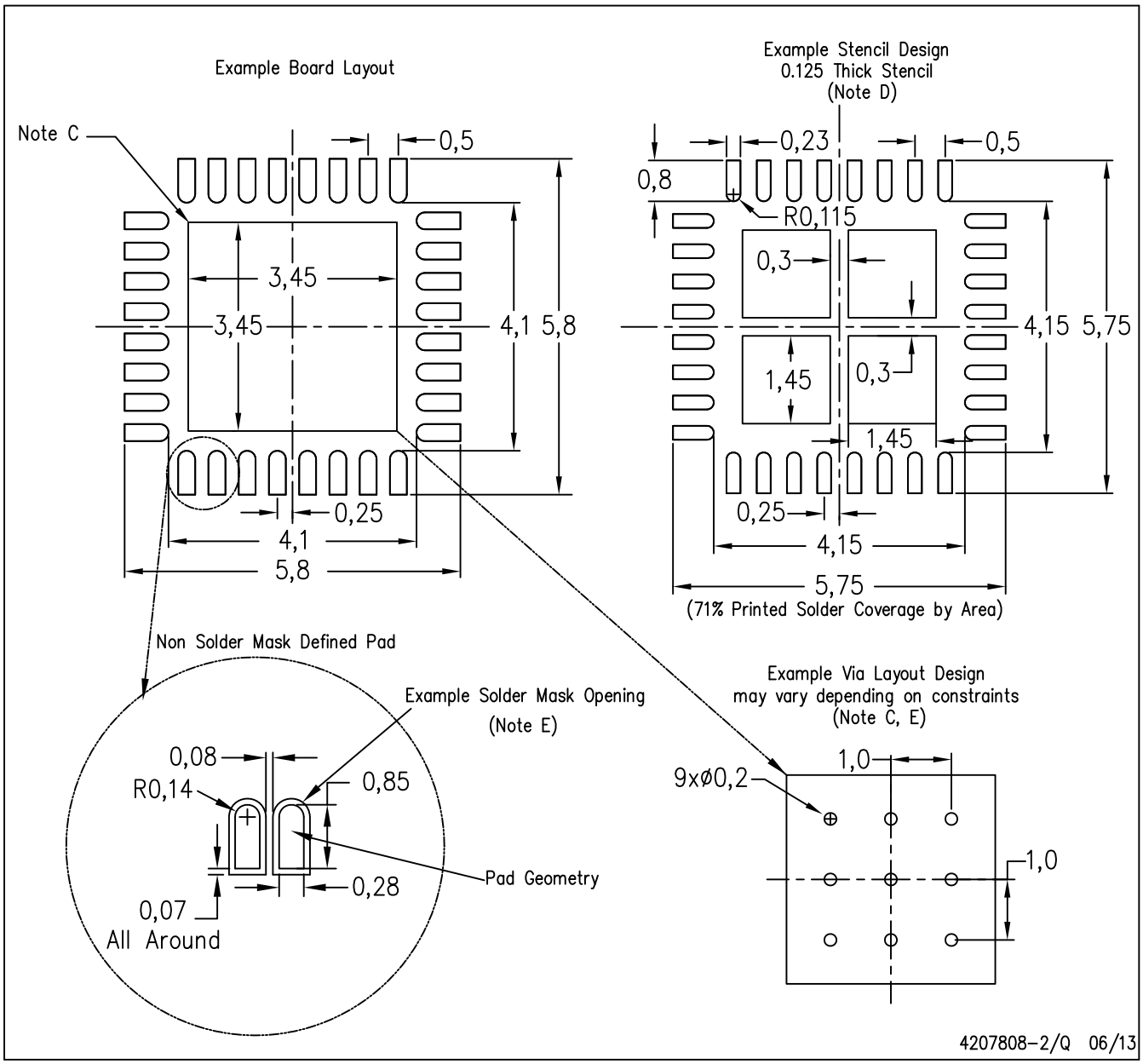
Bottom View

Exposed Thermal Pad Dimensions

4206356–2/Y 06/13

NOTE: A. All linear dimensions are in millimeters

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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