E-Band Upconverter SiP, 81 GHz to 86 GHz

Data Sheet

ADMV7320

FEATURES

- Maximum conversion gain: 33 dB typical
- Gain tuning range: 40 dB minimum
- P_{SAT}: 26 dBm typical for a gain = 23.5 dB and 19.5 dB
- OIP3: 31 dBm typical for a gain = 23.5 dB and P_{OUT} = 16.5 dBm per tone
- OP1dB: 25 dBm typical for a gain = 23.5 dB and 19.5 dB
- Built-in power detector
- Built-in envelope detector for LO nulling
- Fully integrated, surface-mount, 50-terminal, 16.00 mm × 14.00 mm LGA_CAV package

APPLICATIONS

- E-band communication systems
- High capacity wireless backhauls
- Test and measurement
- Aerospace and defense

GENERAL DESCRIPTION

The ADMV7320 is a fully integrated system in package (SiP), in phase/quadrature (I/Q) upconverter that operates between an intermediate frequency (IF) input range of dc and 2 GHz and a radio frequency (RF) output range of 81 GHz and 86 GHz. The device uses an image rejection mixer that is driven by a 6× local oscillator (LO) multiplier. The mixer RF output is followed by a variable gain amplifier (VGA) and a power amplifier (PA), providing a conversion gain of 33 dB typical. Differential I and Q mixer inputs are provided and can be driven with differential I and Q baseband waveforms for direct conversion applications. Alternatively, the inputs can be driven using an external 90° hybrid and two external 180 hybrids for single-ended applications.

The ADMV7320 comes in a fully integrated, surface-mount, 50-terminal, 16.00 mm × 14.00 mm, chip array small outline no lead cavity (LGA_CAV) package. The ADMV7320 operates over the −40°C to +85°C temperature range.

FUNCTIONAL BLOCK DIAGRAM

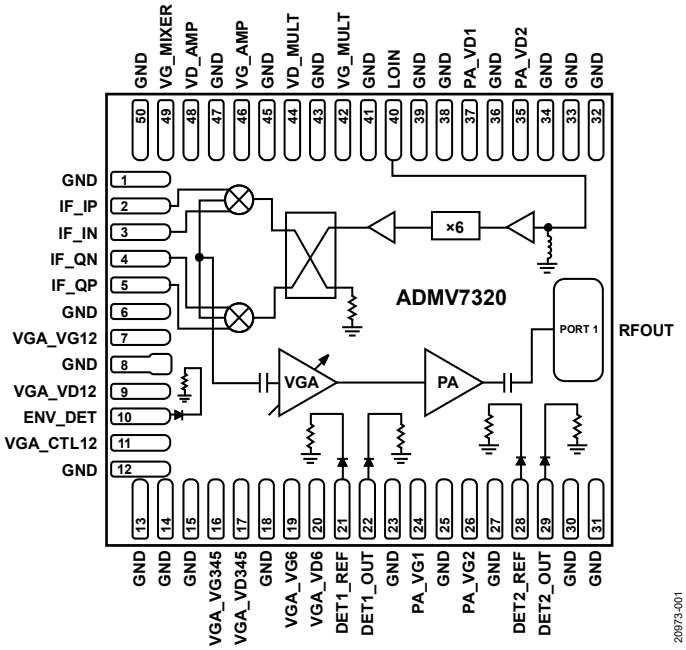


Figure 1.

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REVISION HISTORY

12/2020—Rev. B to Rev. C

Changes to Figure 79 ... 21

3/2020—Rev. A to Rev. B

Changes to Power-Up Bias Sequence Section ... 25
Change to Table 5 ... 26

10/2019—Revision A: Initial Version

SPECIFICATIONS

T_A = −40°C to +85°C, IF = 1 GHz, LO power = 4 dBm, VD_AMP = +4 V, VGA_CTL12 = −5 V, VG_MIXER = −1 V, VD_MULT = +1.5 V, VGA_VD12 = VGA_VD345 = VGA_VD6 = +4 V, and PA_VD1 = PA_VD2 = +4 V, unless otherwise noted. Measurements performed as upconverter with upper sideband selected and an external 90° hybrid followed by two external 180° hybrids at the IF ports.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OPERATING CONDITIONS					
Frequency Range					
Output RF		81		86	GHz
LO		13.4		14.6	GHz
Input IF		DC		2	GHz
LO Drive Level Range		0	4	8	dBm
Input Signal Level	Total baseband power		−4		dBm
PERFORMANCE					
Maximum Conversion Gain	−20 dBm input	23.5	33	43.5	dB
Gain Tuning Range		40			dB
Gain Flatness			3		dB
Sideband Rejection	−4 dBm input	15	20		dBc
Output Power for 1 dB Compression (OP1dB)					
	Gain = 23.5 dB	21.5	25		dBm
	Gain = 19.5 dB	21.5	25		dBm
	Gain = 10.5 dB	16.5	24		dBm
	Gain = 3.5 dB	9.5	18		dBm
Saturated Output Power (P_{SAT})					
	Gain = 23.5 dB	23	26		dBm
	Gain = 19.5 dB	23	26		dBm
	Gain = 10.5 dB	17.5	25		dBm
	Gain = 3.5 dB	10.5	19		dBm
Noise Figure (NF)					
	Gain = 23.5 dB		26		dB
	Gain = 19.5 dB		26		dB
	Gain = 10.5 dB		29		dB
	Gain = 3.5 dB		31		dB
6× LO to RF Rejection	RF port (uncalibrated)				
	Gain = 23.5 dB		5		dBc
	Gain = 19.5 dB		5		dBc
	Gain = 10.5 dB		5		dBc
	Gain = 3.5 dB		5		dBc
Output Third-Order Intercept (OIP3)					
	Gain = 23.5 dB, output power (P_{OUT}) = 16.5 dBm per tone	27	31		dBm
	Gain = 19.5 dB, P_{OUT} = 12.5 dBm per tone	26	28.5		dBm
	Gain = 10.5 dB, P_{OUT} = 3.5 dBm per tone	22	24		dBm
	Gain = 3.5 dB, P_{OUT} = −3.5 dBm per tone	16	20		dBm
Output Waveguide Port Return Loss			7		dB
Baseband Input Return Loss			15		dB
LO Port Return Loss			8		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Minimum Power Amplifier Detector Sensitivity					
	−5 dBm ≤ P_{OUT} ≤ 0 dBm		1		mV/dB
	0 dBm ≤ P_{OUT} ≤ 23 dBm		3		mV/dB
Power Amplifier Detector Voltage					
Minimum (DET2_REF − DET2_OUT)	−5 dBm ≤ P_{OUT} ≤ 0 dBm		5		mV
Maximum (DET2_REF − DET2_OUT)	0 dBm ≤ P_{OUT} ≤ 23 dBm		800		mV
DET2_REF	−5 dBm ≤ P_{OUT} ≤ 23 dBm	0	0.9	2.5	V
DET2_OUT	−5 dBm ≤ P_{OUT} ≤ 23 dBm	−1		2.5	V
Envelope Detector	Load resistance (R_{LOAD}) = 200 Ω				
Minimum AC Detected Signal	−4 dBm ≤ input power (P_{IN}) ≤ 9.5 dBm		45		mV p-p
3 dB Bandwidth			750		MHz
Second Harmonic			24		dBc
DIFFERENTIAL BASEBAND INPUT PORT IMPEDANCE			100		Ω
LO INPUT PORT IMPEDANCE			50		Ω
POWER SUPPLY					
DC Power Dissipation			5		W
PA (PA_VD1 and PA_VD2) Drain Voltage		3.88	4	4.12	V
PA (PA_VG1 and PA_VG2) Gate Voltage		−2		+0.2	V
VGA (VGA_VG12, VGA_VG345, and VGA_VG6) Gate Voltage		−2		+0.2	V
Multiplier Drain Voltage (VD_MULT)		1.46	1.5	1.55	V
VGA Voltage Control (VGA_CTL12)		−5		0	V
PA (I_{PA_VD1} and I_{PA_VD2}) Drain Current			800		mA
VGA (I_{VGA_VD12}, I_{VGA_VD345}, and I_{VGA_VD6}) Drain Current			250		mA
Amplifier Drain (VD_AMP) Current (I_{VD_AMP})			175		mA
Multiplier Drain (VD_MULT) Current (I_{VD_MULT})			80		mA

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VD_AMP	4.5 V
VD_MULT	3 V
VGA_VD12, VGA_VD345, and VGA_VD6	4.5 V
PA_VD1 and PA_VD2	4.5 V
VG_AMP	−3 V to +0.2 V
VG_MULT	−3 V to +0.2 V
VGA_VG12, VGA_VG345, and VGA_VG6	−3 V to +0.2 V
PA_VG1 and PA_VG2	−3 V to +0.2 V
VGA_CTL12	−6 V to 0 V
LO Drive	10 dBm
Baseband Input (IF_IP, IF_IN, IF_QP, and IF_QN)	4 dBm
IF Source and Sink Current	3 mA
Nominal Junction Temperature (T_A = 85°C)	160°C
Maximum Junction Temperature (to Maintain 1 Million Hours Mean Time to Failure (MTTF))	190°C
Maximum Junction Temperature (to Maintain 3 Million MTTF)	175°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−55°C to +150°C
Maximum Peak Reflow Temperature (Moisture Sensitivity Level 3 (MSL3))	260°C
Thermal Humidity Bias (THB)	JESD22-A101[1, 2, 3]
Thermal Humidity Storage (THS)	JESD22-A101[1, 3]
Electrostatic Discharge (ESD) Sensitivity	
Human Body Model (HBM)	200 V
Field Induced Charged Device Model (FICDM)	300 V

[1] Samples subject to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: bake for 24 hours at 125°C, unbiased soak for 192 hours at 30°C and 60% relative humidity (RH), and reflow of three passes through an oven with a peak temperature of 260°C.
[2] Results valid for 600 mW of nominal dc power dissipation for all active devices. Analog Devices, Inc., recommends that users perform their own THB test for all other bias conditions.
[3] Valid for package vent hole solder sealed or unsealed during test.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case (or die to package) thermal resistance.

Table 3. Thermal Resistance[1]

Package Type	θ_{JC}	Unit
CE-50-2	15	°C/W

[1] Thermal impedance simulated values are based on a JEDEC 2S2P test board with 16 mm × 14 mm thermal vias. Refer to JEDEC standard JESD51-2 for additional information.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

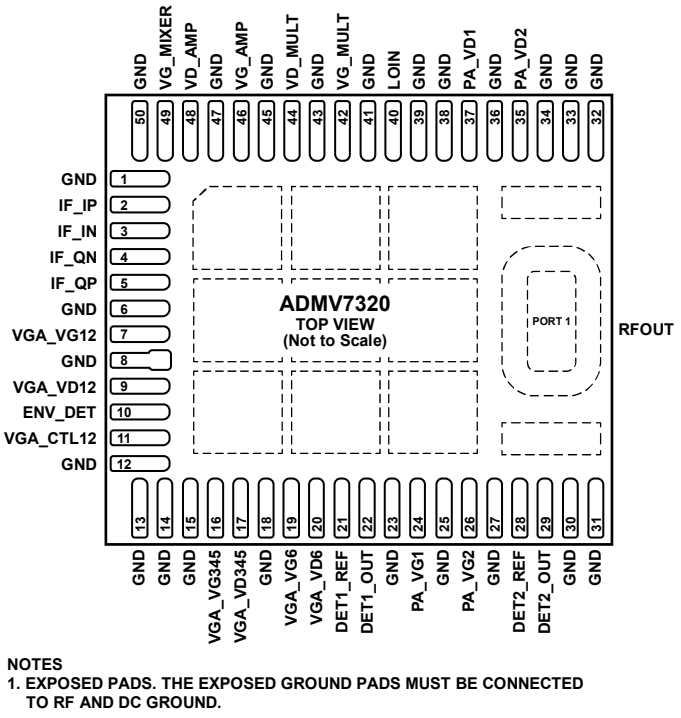


Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 6, 8, 12 to 15, 18, 23, 25, 27, 30 to 34, 36, 38, 39, 41, 43, 45, 47, 50	GND	Ground Connections. These pins must be connected to RF and dc ground.
2	IF_IP	Positive IF In Phase Input. This pin is dc-coupled. When operation to dc is not required, block this pin externally using a series capacitor with a value chosen to pass the necessary frequency range. For operation to dc, this pin must not source or sink more than 3 mA of current or device malfunction and device failure may result.
3	IF_IN	Negative IF In Phase Input. This pin is dc-coupled. When operation to dc is not required, block this pin externally using a series capacitor with a value chosen to pass the necessary frequency range. For operation to dc, this pin must not source or sink more than 3 mA of current or device malfunction and device failure may result.
4	IF_QN	Negative IF Quadrature Input. This pin is dc-coupled. When operation to dc is not required, block this pin externally using a series capacitor with a value chosen to pass the necessary frequency range. For operation to dc, this pin must not source or sink more than 3 mA of current or device malfunction and device failure may result.
5	IF_QP	Positive IF Quadrature Input. This pin is dc-coupled. When operation to dc is not required, block this pin externally using a series capacitor with a value chosen to pass the necessary frequency range. For operation to dc, this pin must not source or sink more than 3 mA of current or device malfunction and device failure may result.
7	VGA_VG12	Gate Control for the First and Second Stage Variable Gain Amplifier. See Figure 86 for the recommended external components.
9	VGA_VD12	Drain Voltage for the First and Second Stage Variable Gain Amplifier. See Figure 86 for recommended external components.
10	ENV_DET	Envelope Detector. See Figure 86 for the recommended external components.

Pin No.	Mnemonic	Description
11	VGA_CTL12	Gain Control Voltage for the First and Second Stage Variable Gain Amplifier. See Figure 86 for the recommended external components.
16	VGA_VG345	Gate Control for the Third, Fourth, and Fifth Stage Variable Gain Amplifier. See Figure 86 for the recommended external components.
17	VGA_VD345	Drain Voltage for the Third, Fourth, and Fifth Stage Variable Gain Amplifier. See Figure 86 for the recommended external components.
19	VGA_VG6	Gate Control for the Sixth Stage Variable Gain Amplifier. See Figure 86 for the recommended external components.
20	VGA_VD6	Drain Voltage for the Sixth Stage Variable Gain Amplifier. See Figure 86 for the recommended external components.
21	DET1_REF	Reference Voltage for the VGA Power Detector. DET1_REF is the dc bias of the diode biased through an external resistor used for the temperature compensation of DET1_OUT.
22	DET1_OUT	Detector Voltage for the VGA Power Detector. DET1_OUT is the dc voltage representing the RF output power rectified by the diode, which is biased through an external resistor.
24	PA_VG1	Gate Voltage for the First Power Amplifier. See Figure 86 for the recommended external components.
26	PA_VG2	Gate Voltage for the Second Power Amplifier. See Figure 86 for the recommended the external components.
28	DET2_REF	Reference Voltage for the PA Power Detector. DET2_REF is the dc bias of the diode biased through an external resistor used for the temperature compensation of DET2_OUT.
29	DET2_OUT	Detector Voltage for the VGA Power Detector. DET2_OUT is the dc voltage representing the RF output power rectified by the diode, which is biased through an external resistor.
35	PA_VD2	Drain Voltage for the Second Power Amplifier. See Figure 86 for the recommended external components.
37	PA_VD1	Drain Voltage for the First Power Amplifier. See Figure 86 for the recommended external components.
40	LOIN	LO Input. This pin is dc-coupled and matched to 50 Ω.
42	VG_MULT	Gate Voltage for the LO Multiplier. See Figure 86 for the recommended external components.
44	VD_MULT	Drain Voltage for the LO Multiplier. See Figure 86 for the recommended external components.
46	VG_AMP	Gate Voltage for the LO Amplifier. See Figure 86 for the recommended external components.
48	VD_AMP	Drain Voltage for the LO Amplifier. See Figure 86 for the recommended external components.
49	VG_MIXER	Gate Voltage for the Field Effect Transistor (FET) Mixer. See Figure 86 for the recommended external components.
PORT 1	RFOUT	WR-12 Waveguide Port. This port is ac-coupled and matched to the waveguide output impedance.
	EPAD	Exposed Pads. The exposed ground pads must be connected to RF and dc ground.

INTERFACE SCHEMATICS



Figure 3. GND Interface Schematic

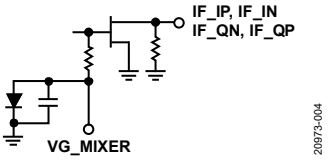


Figure 4. IF_IP, IF_IN, IF_QN, IF_QP, and VG_MIXER Interface Schematic

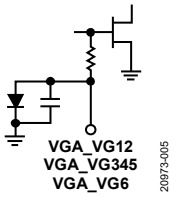


Figure 5. VGA_VG12, VGA_VG345, and VGA_VG6 Interface Schematic

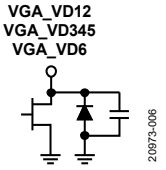


Figure 6. VGA_VD12, VGA_VD345, and VGA_VD6 Interface Schematic



Figure 7. ENV_DET Interface Schematic

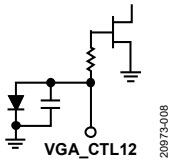


Figure 8. VGA_CTL12 Interface Schematic

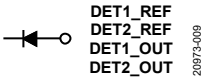


Figure 9. DET1_REF, DET2_REF, DET1_OUT, and DET2_OUT Interface Schematic

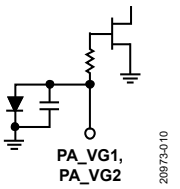


Figure 10. PA_VG1, PA_VG2 Interface Schematic

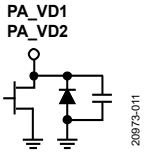


Figure 11. PA_VD1, PA_VD2 Interface Schematic

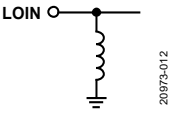


Figure 12. LOIN Interface Schematic

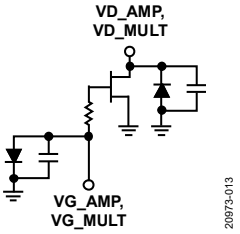


Figure 13. VD_AMP, VD_MULT, VG_AMP, and VG_MULT Interface Schematic

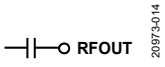


Figure 14. RFOUT Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, IF = 1 GHz, IF input power = −4 dBm combined, LO power = +4 dBm, gain adjusted per the Applications Information section, and upper sideband selected, unless otherwise noted.

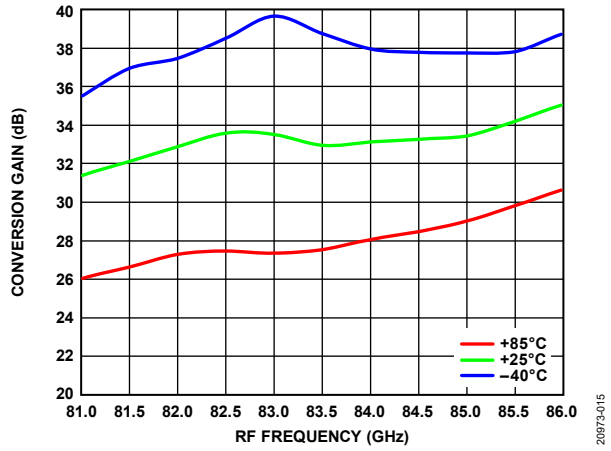


Figure 15. Maximum Conversion Gain vs. RF Frequency over Temperature, IF Input Power = −20 dBm

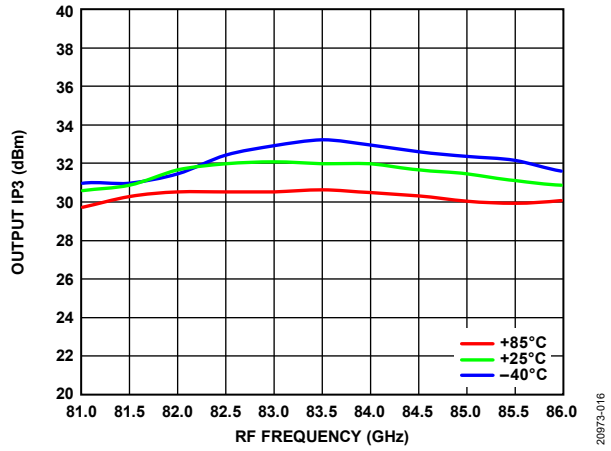


Figure 16. Output IP3 vs. RF Frequency over Temperature, Gain = 23.5 dB

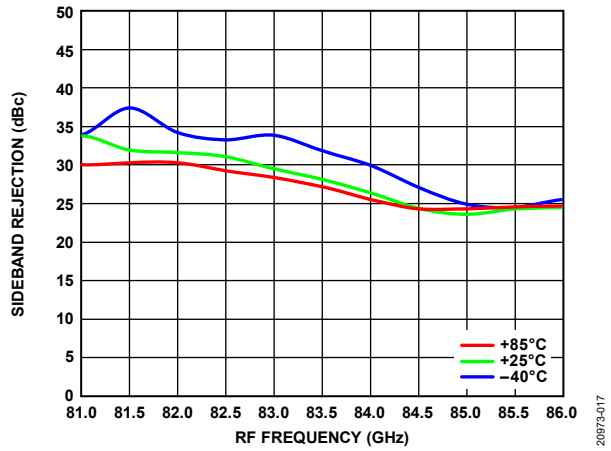


Figure 17. Sideband Rejection vs. RF Frequency over Temperature, Gain = 23.5 dB

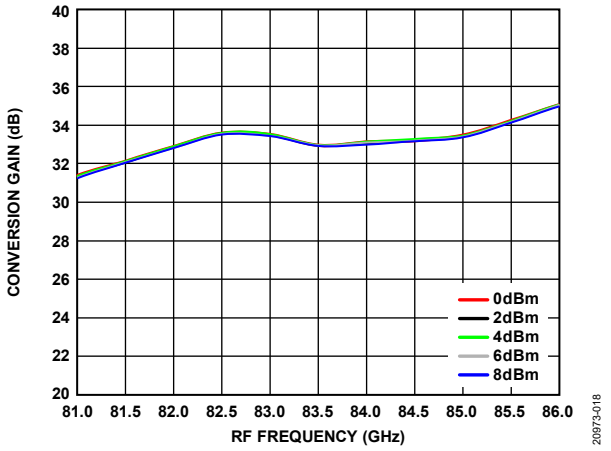


Figure 18. Maximum Conversion Gain vs. RF Frequency over LO Power, IF Input Power = −20 dBm

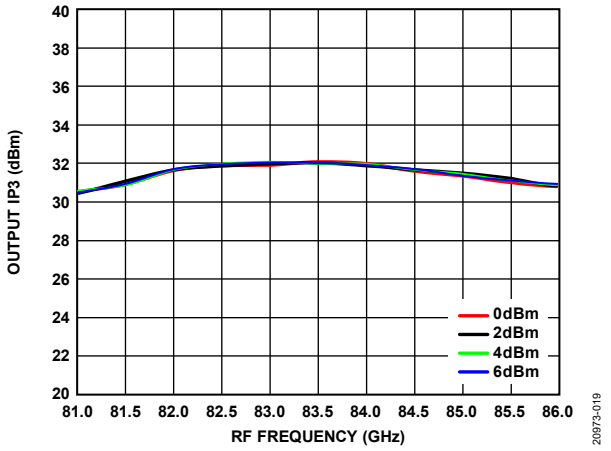


Figure 19. Output IP3 vs. RF Frequency over LO Power, Gain = 23.5 dB

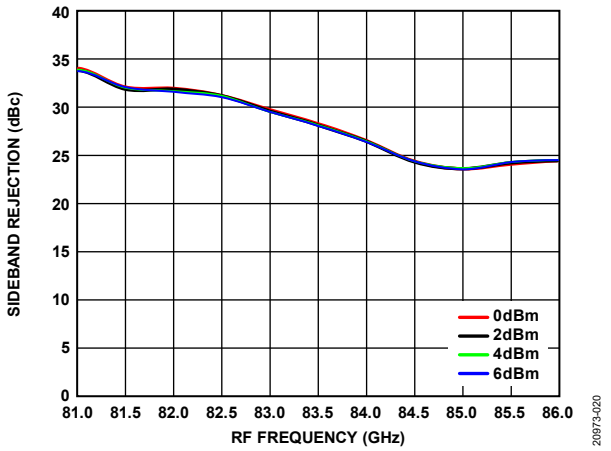


Figure 20. Sideband Rejection vs. RF Frequency over LO Power, Gain = 23.5 dB

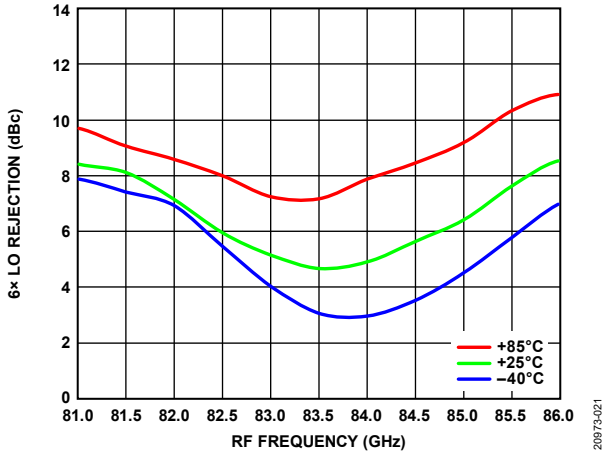


Figure 21. 6× LO Rejection vs. RF Frequency over Temperature, Gain = 23.5 dB

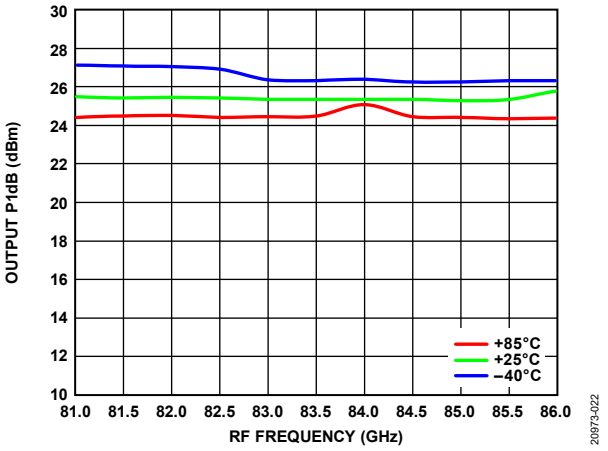


Figure 22. Output P1dB vs. RF Frequency over Temperature, Gain = 23.5 dB

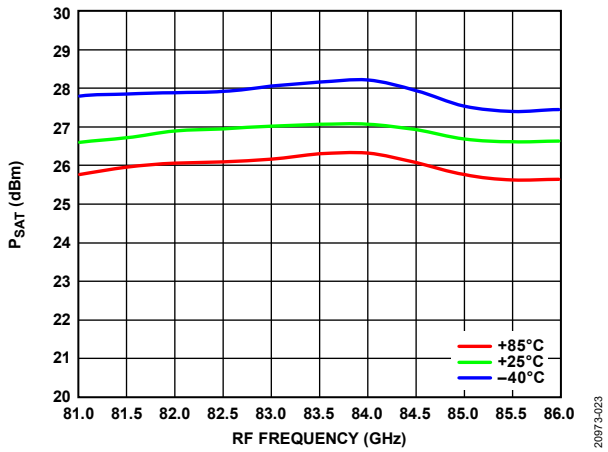


Figure 23. P_{SAT} vs. RF Frequency over Temperature, Gain = 23.5 dB

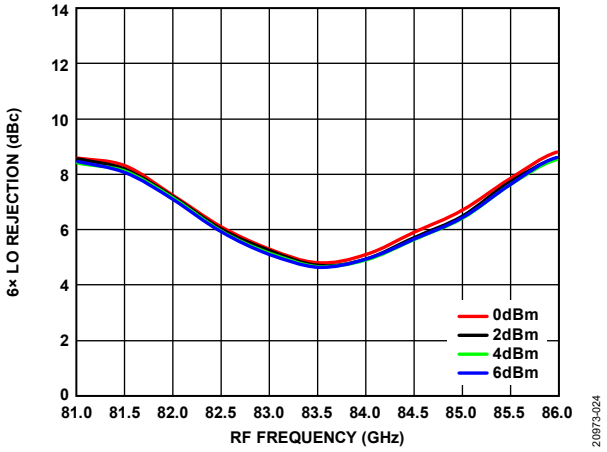


Figure 24. 6× LO Rejection vs. RF Frequency over LO Power, Gain = 23.5 dB

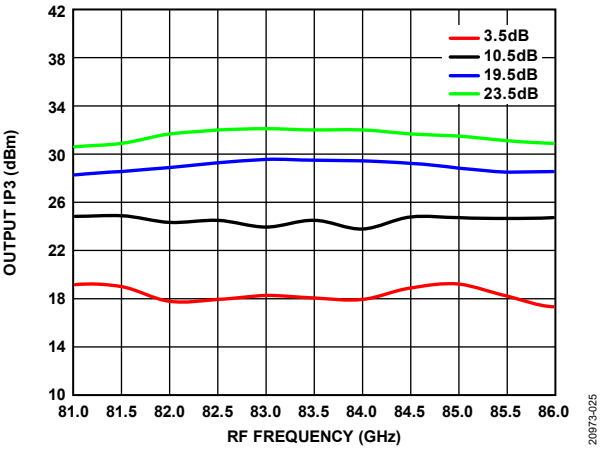


Figure 25. Output IP3 vs. RF Frequency at Various Gains

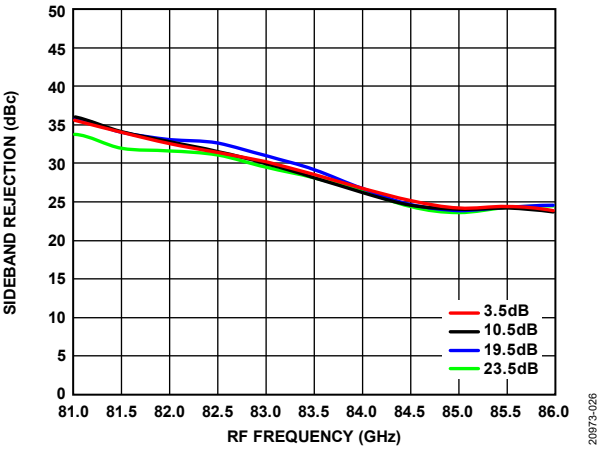


Figure 26. Sideband Rejection vs. RF Frequency at Various Gains

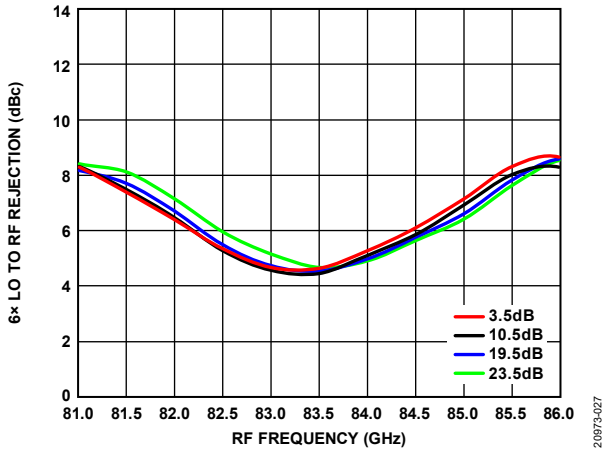


Figure 27. 6× LO to RF Rejection vs. RF Frequency at Various Gains

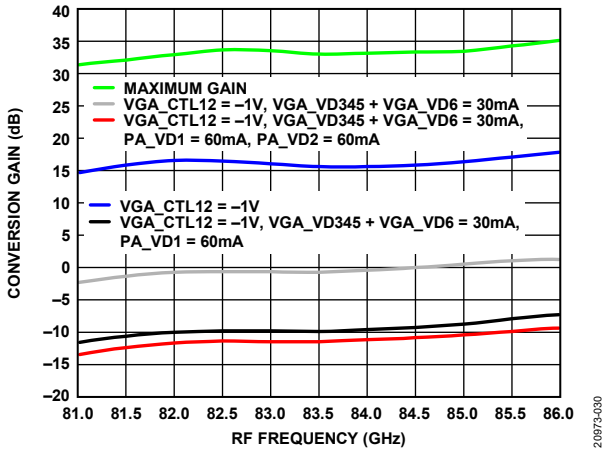


Figure 30. Conversion Gain vs. RF Frequency at Various Gain Tuning Modes

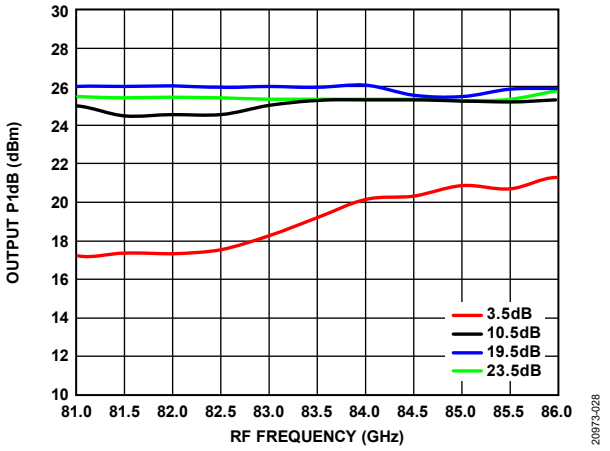


Figure 28. Output P1dB vs. RF Frequency at Various Gains

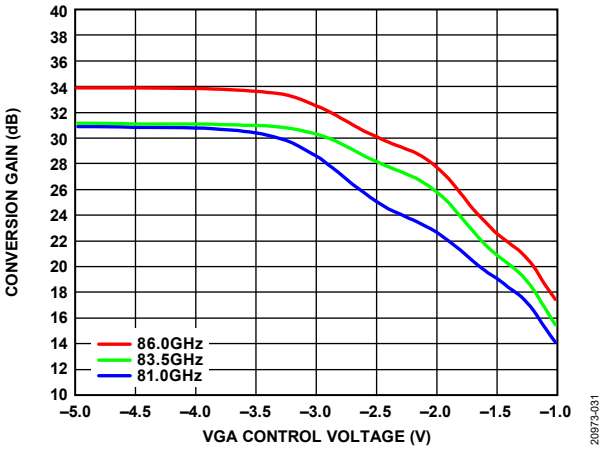


Figure 31. Conversion Gain vs. VGA Control Voltage at Various RF Frequencies

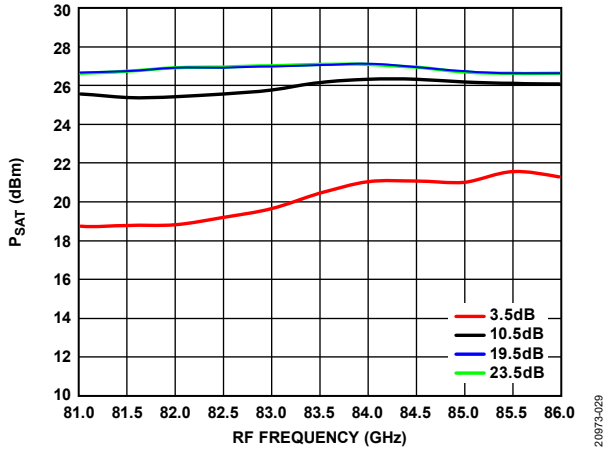


Figure 29. P_{SAT} vs. RF Frequency at Various Gains

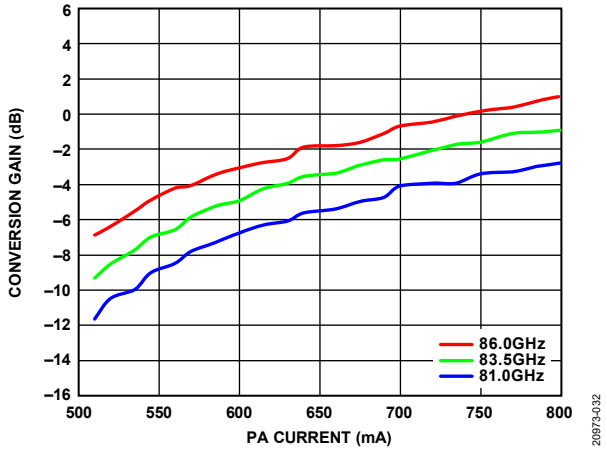


Figure 32. Conversion Gain vs. PA Current at Various RF Frequencies, VGA_CTL12 = −1 V, VGA_VD12 = 75 mA, VGA_VD345 = 75 mA, and VGA_VD6 = 75 mA

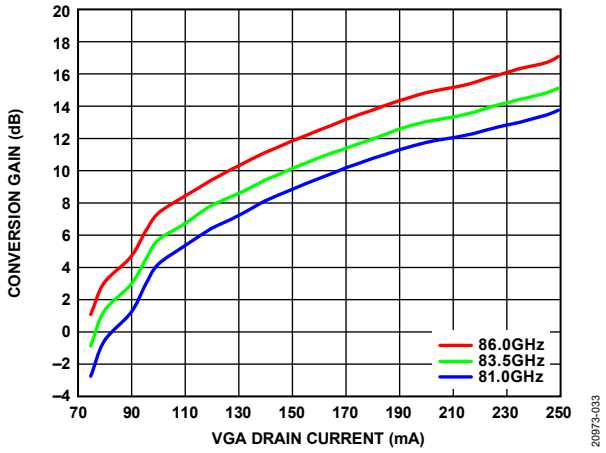


Figure 33. Conversion Gain vs. VGA Drain Current at Various RF Frequencies, VGA_CTL12 = −1 V

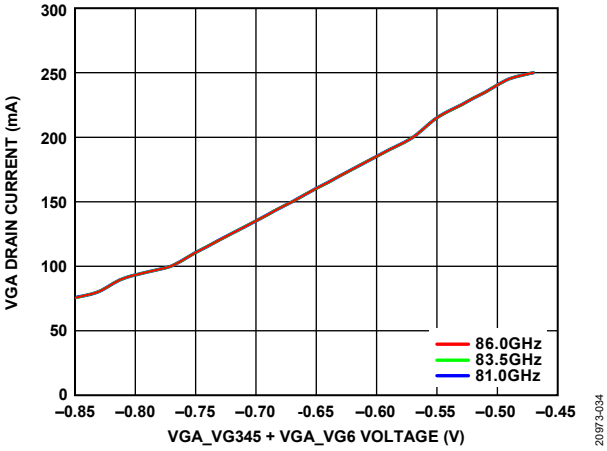


Figure 34. VGA Drain Current vs. VGA_VG345 + VGA_VG6 Voltage at Various Frequencies

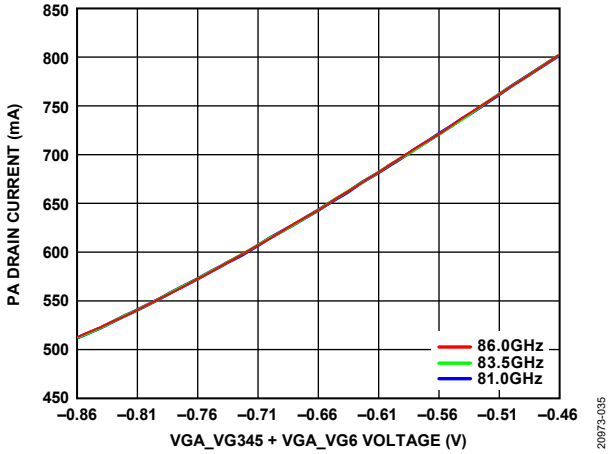


Figure 35. PA Drain Current vs. VGA_VG345 + VGA_VG6 Voltage at Various Frequencies

T_A = 25°C, IF = 0.1 GHz, IF input power = −4 dBm combined, LO power = +4 dBm, gain adjusted per the Applications Information section, and upper sideband selected, unless otherwise noted.

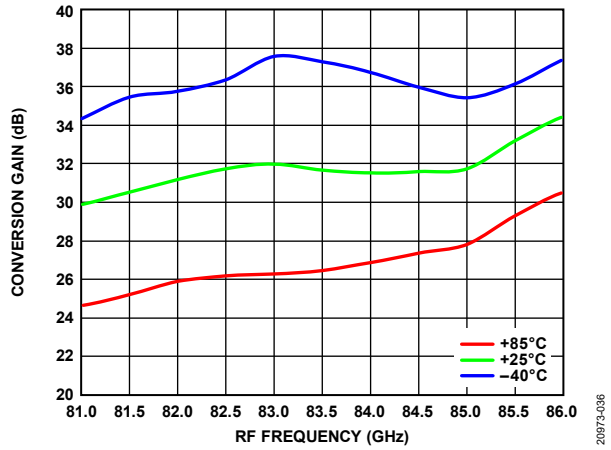


Figure 36. Maximum Conversion Gain vs. RF Frequency over Temperature, IF Input Power = −20 dBm

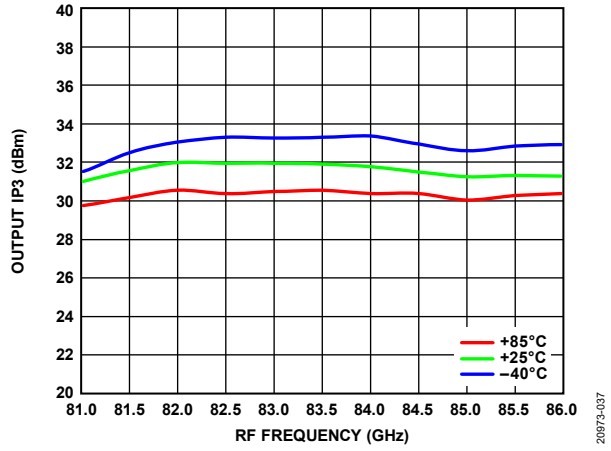


Figure 37. Output IP3 vs. RF Frequency over Temperature, Gain = 23.5 dB

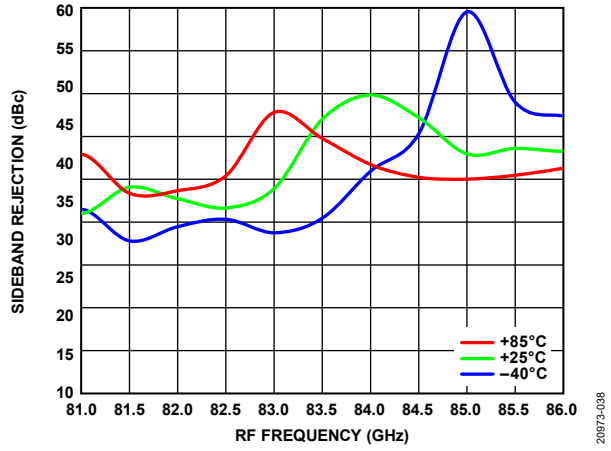


Figure 38. Sideband Rejection vs. RF Frequency over Temperature, Gain = 23.5 dB

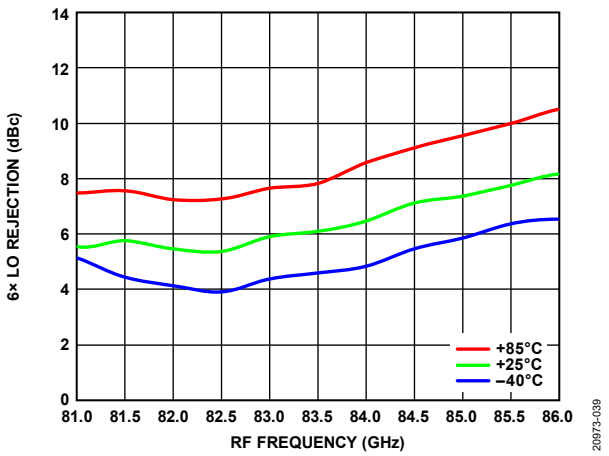


Figure 39. 6× LO Rejection vs. RF Frequency over Temperature, Gain = 23.5 dB

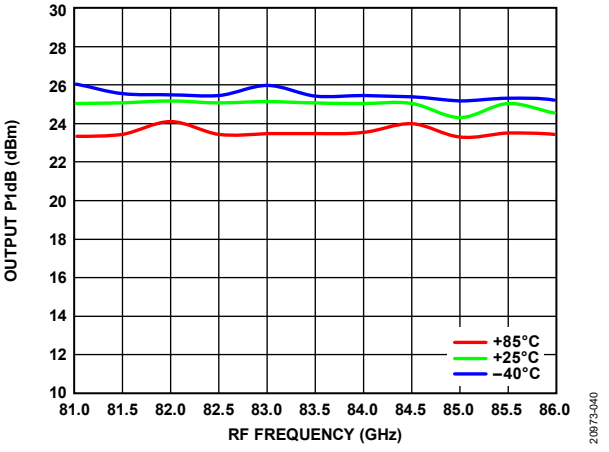


Figure 40. Output P1dB vs. RF Frequency over Temperature, Gain = 23.5 dB

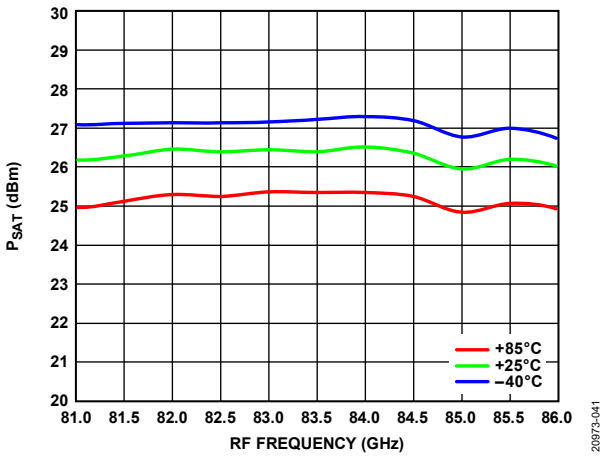


Figure 41. P_{SAT} vs. RF Frequency over Temperature, Gain = 23.5 dB

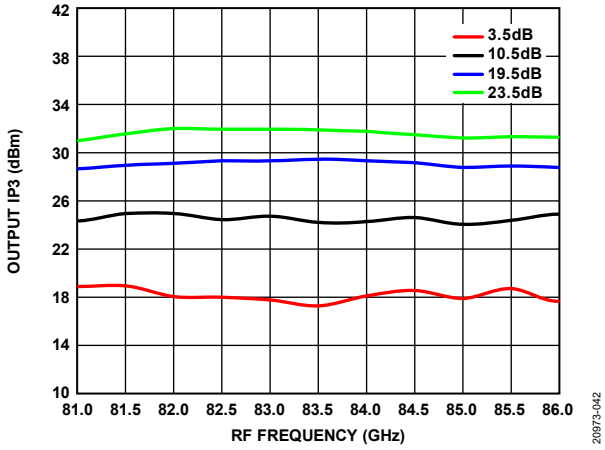


Figure 42. Output IP3 vs. RF Frequency at Various Gains

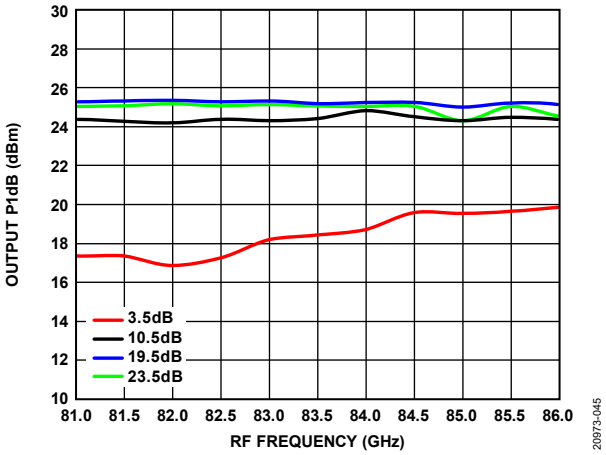


Figure 45. Output P1dB vs. RF Frequency at Various Gains

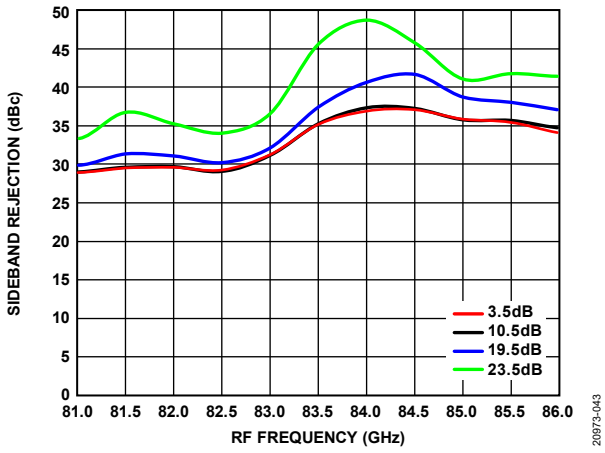


Figure 43. Sideband Rejection vs. RF Frequency at Various Gains

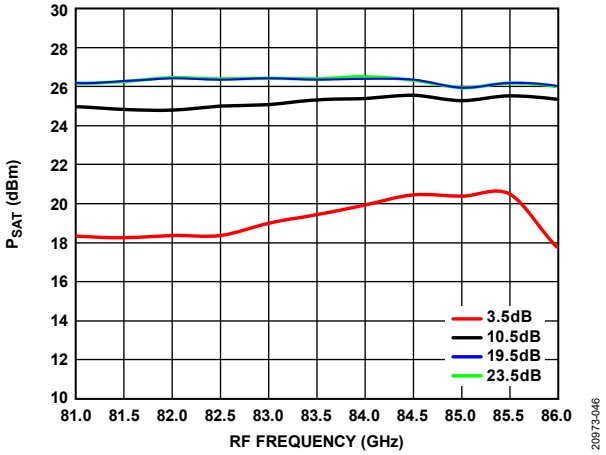


Figure 46. P_{SAT} vs. RF Frequency at Various Gains

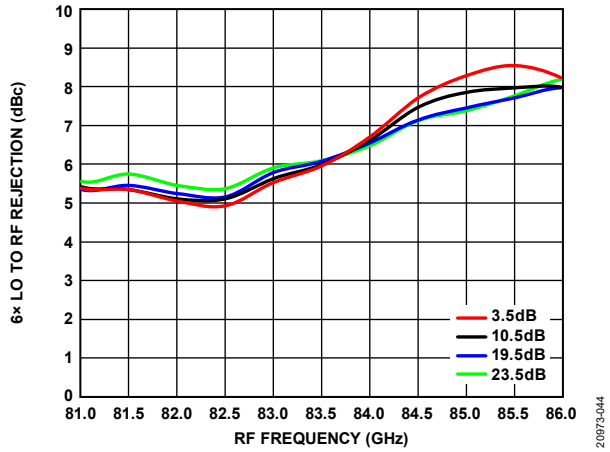


Figure 44. 6× LO to RF Rejection vs. RF Frequency at Various Gains

T_A = 25°C, IF = 0.5 GHz, IF input power = −4 dBm combined, LO power = +4 dBm, gain adjusted per the Applications Information section, and upper sideband selected, unless otherwise noted.

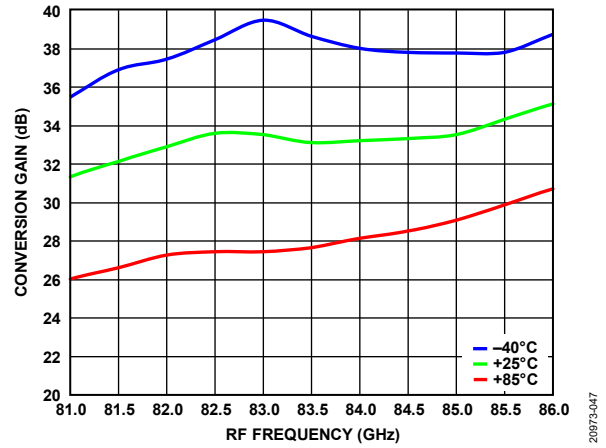


Figure 47. Maximum Conversion Gain vs. RF Frequency over Temperature, IF Input Power = −20 dBm

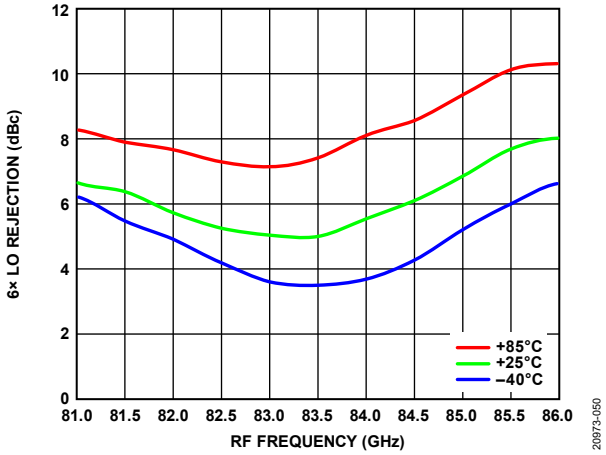


Figure 50. 6× LO Rejection vs. RF Frequency over Temperature, Gain = 23.5 dB

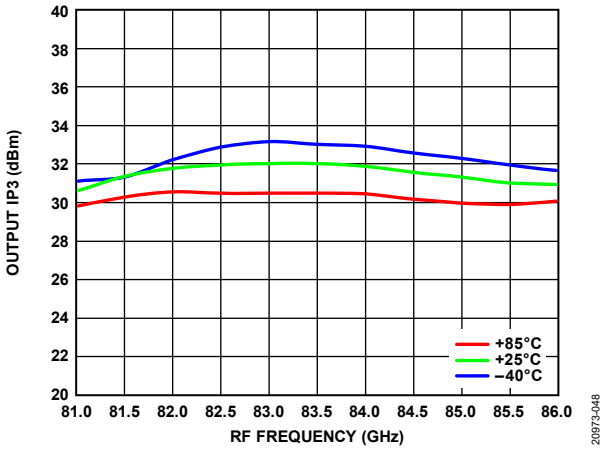


Figure 48. Output IP3 vs. RF Frequency over Temperature, Gain = 23.5 dB

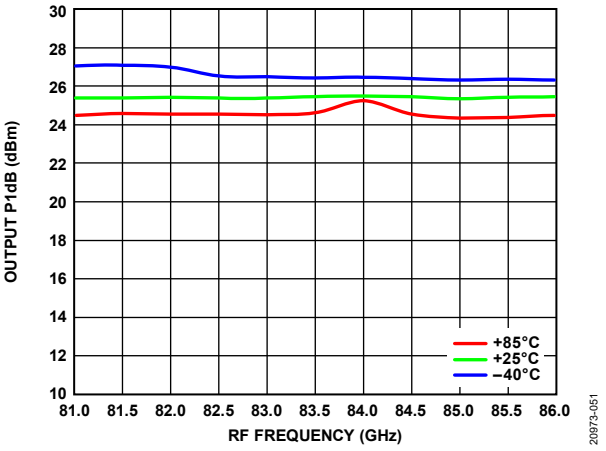


Figure 51. Output P1dB vs. RF Frequency over Temperature, Gain = 23.5 dB

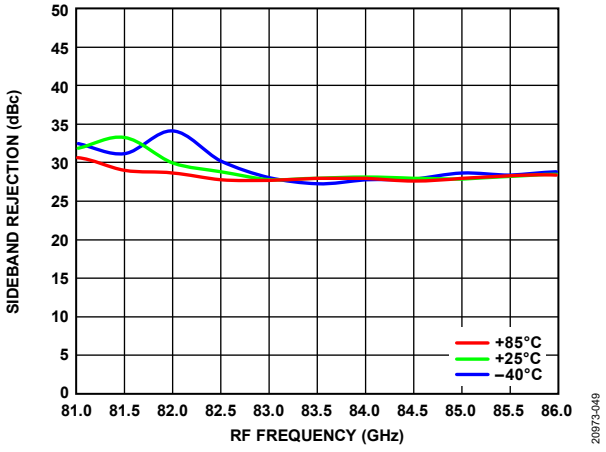


Figure 49. Sideband Rejection vs. RF Frequency over Temperature, Gain = 23.5 dB

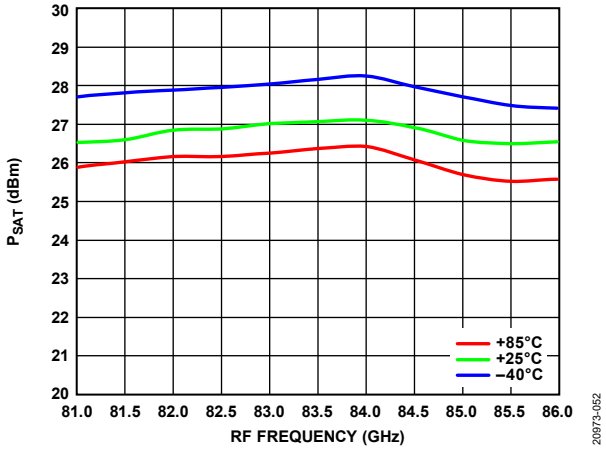


Figure 52. P_{SAT} vs. RF Frequency over Temperature, Gain = 23.5 dB

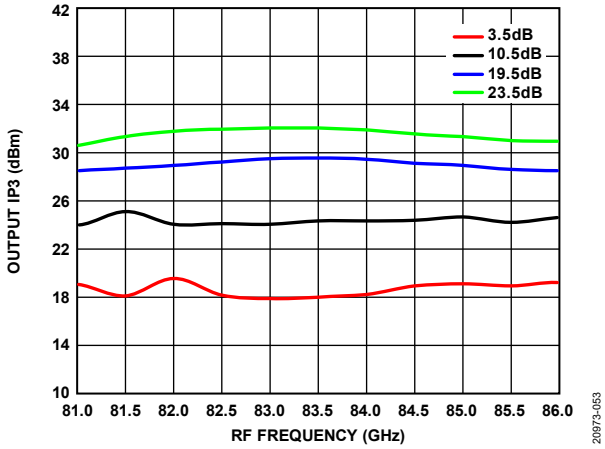


Figure 53. Output IP3 vs. RF Frequency at Various Gains

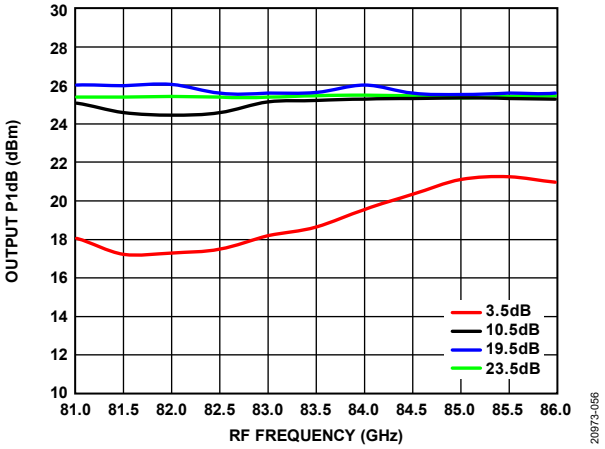


Figure 56. Output P1dB vs. RF Frequency at Various Gains

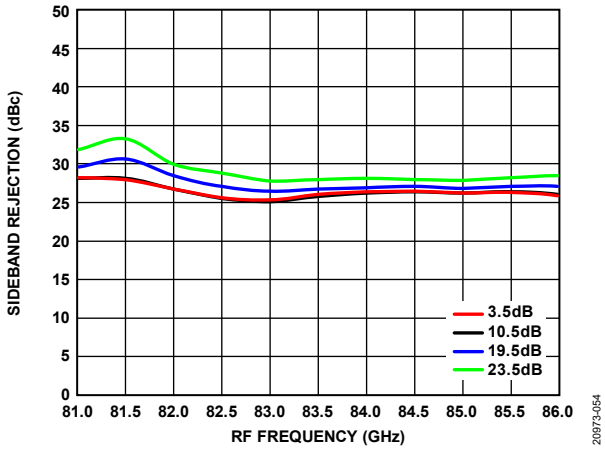


Figure 54. Sideband Rejection vs. RF Frequency at Various Gains

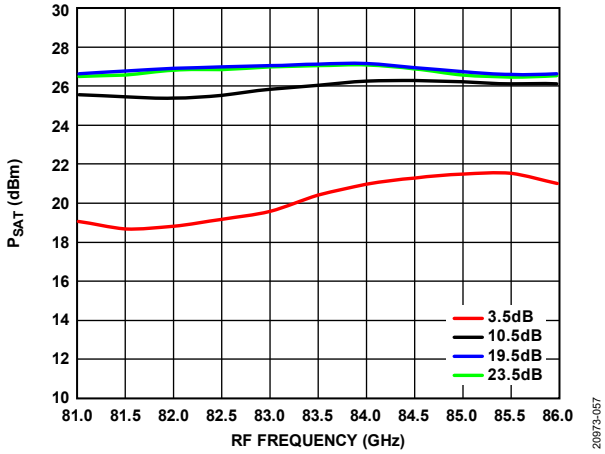


Figure 57. P_{SAT} vs. RF Frequency at Various Gains

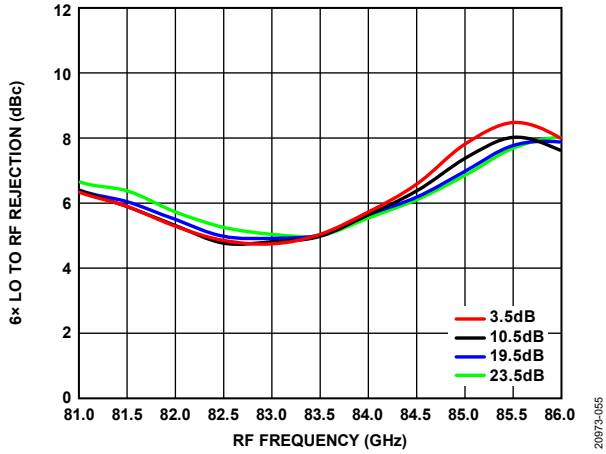


Figure 55. 6× LO to RF Rejection vs. RF Frequency at Various Gains

T_A = 25°C, IF = 2 GHz, IF input power = −4 dBm combined, LO power = +4 dBm, gain adjusted per the Applications Information section, and upper sideband selected, unless otherwise noted.

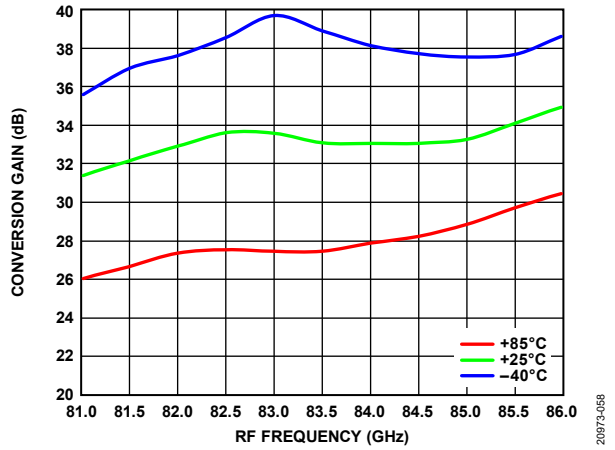


Figure 58. Maximum Conversion Gain vs. RF Frequency over Temperature, IF Input Power = −20 dBm

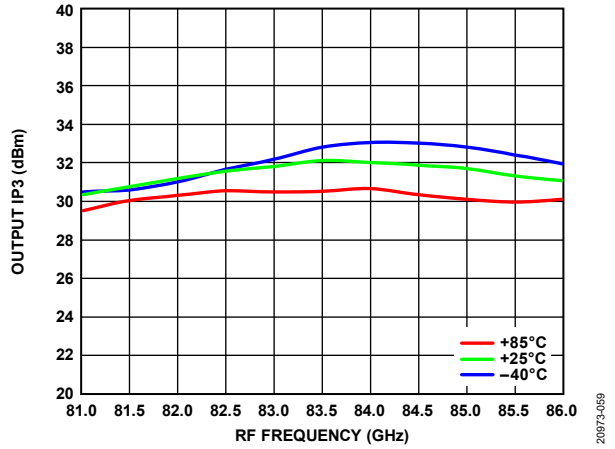


Figure 59. Output IP3 vs. RF Frequency over Temperature, Gain = 23.5 dB

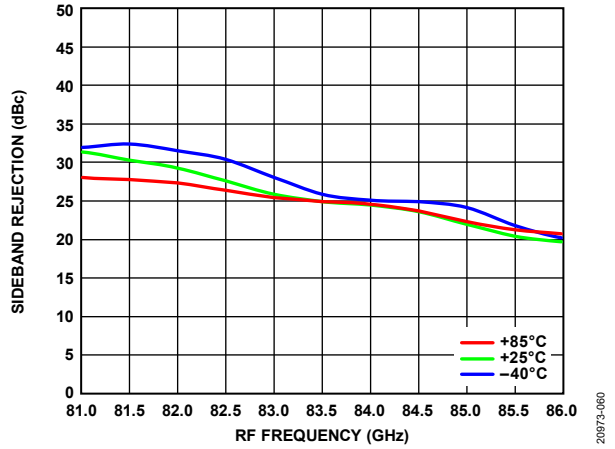


Figure 60. Sideband Rejection vs. RF Frequency over Temperature, Gain = 23.5 dB

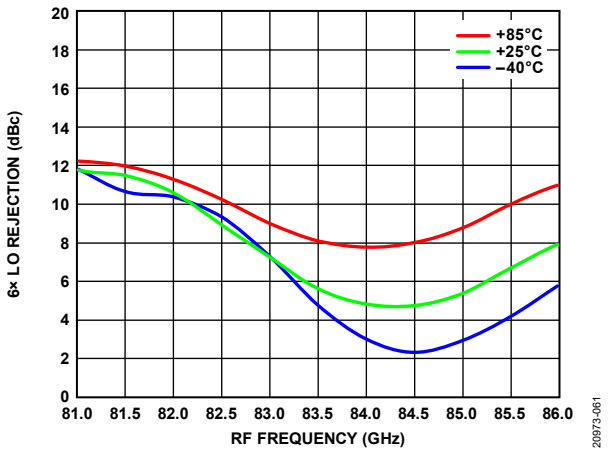


Figure 61. 6× LO Rejection vs. RF Frequency over Temperature, Gain = 23.5 dB

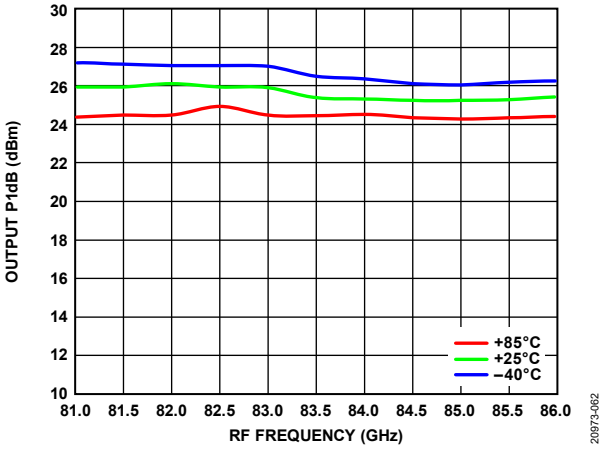


Figure 62. Output P1dB vs. RF Frequency over Temperature, Gain = 23.5 dB

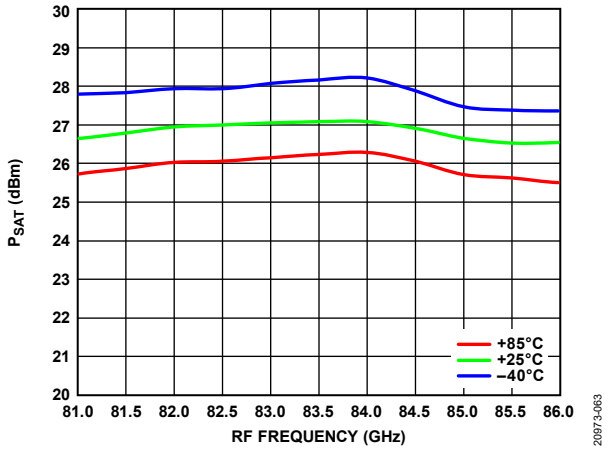


Figure 63. P_{SAT} vs. RF Frequency over Temperature, Gain = 23.5 dB

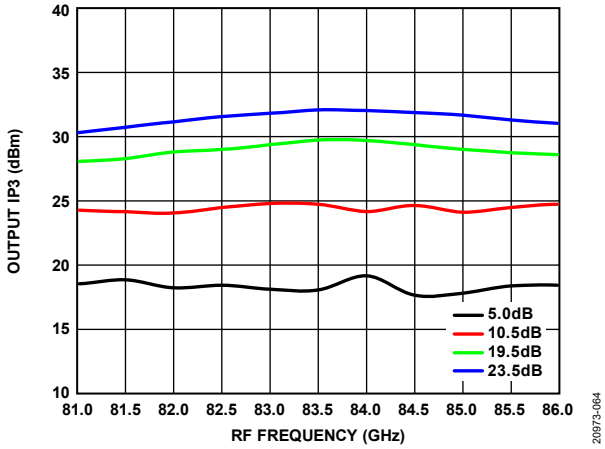


Figure 64. Output IP3 vs. RF Frequency at Various Gains

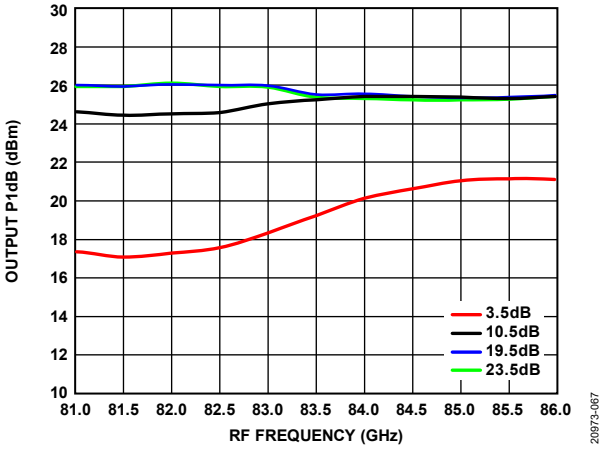


Figure 67. Output P1dB vs. RF Frequency at Various Gains

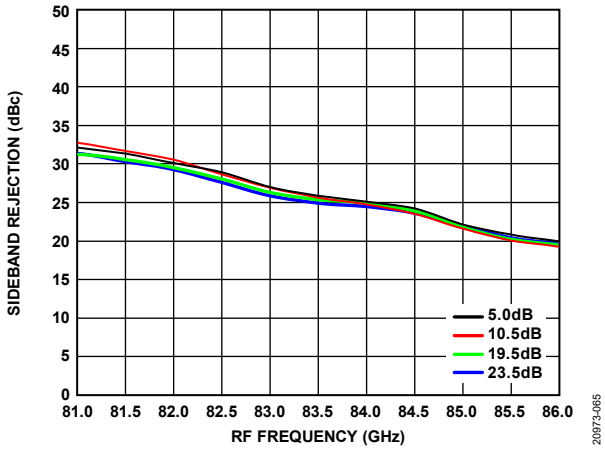


Figure 65. Sideband Rejection vs. RF Frequency at Various Gains

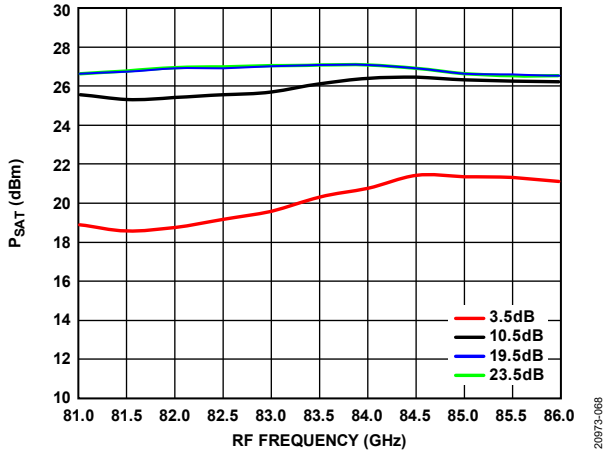


Figure 68. P_{SAT} vs. RF Frequency at Various Gains

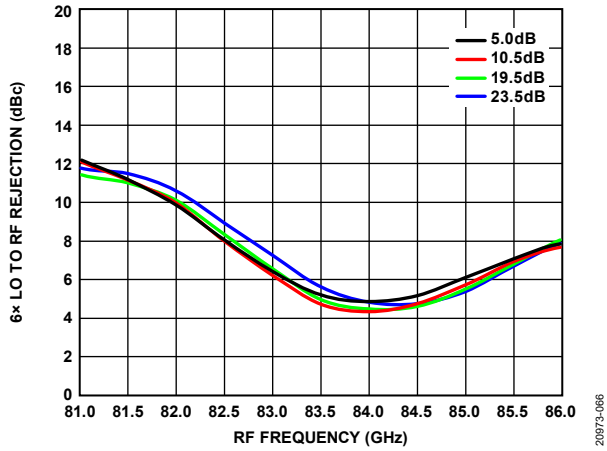


Figure 66. 6× LO to RF Rejection vs. RF Frequency at Various Gains

DETECTOR PERFORMANCE

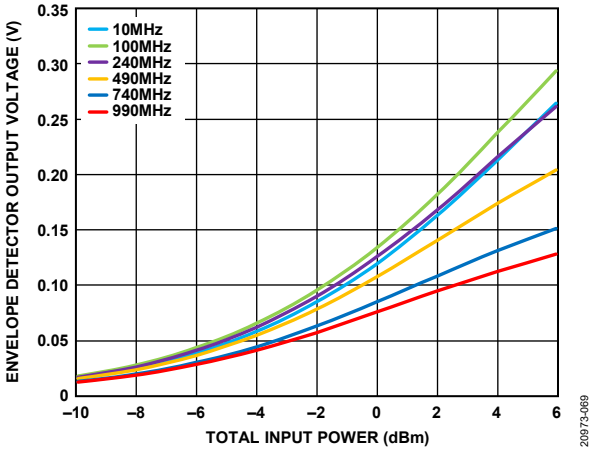


Figure 69. Envelope Detector Output Voltage vs. Total Input Power for Various Input Tone Spacings, RF = 81 GHz

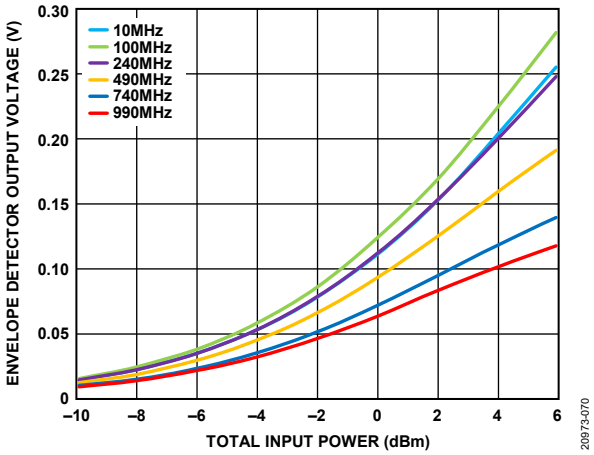


Figure 70. Envelope Detector Output Voltage vs. Total Input Power for Various Input Tone Spacings, RF = 83.5 GHz

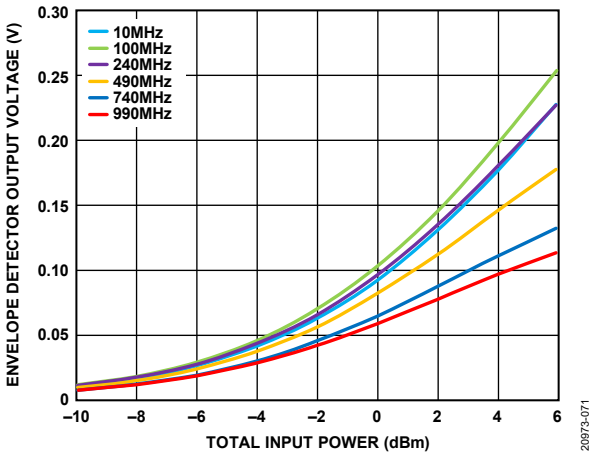


Figure 71. Envelope Detector Output Voltage vs. Total Input Power for Various Input Tone Spacings, RF = 86 GHz

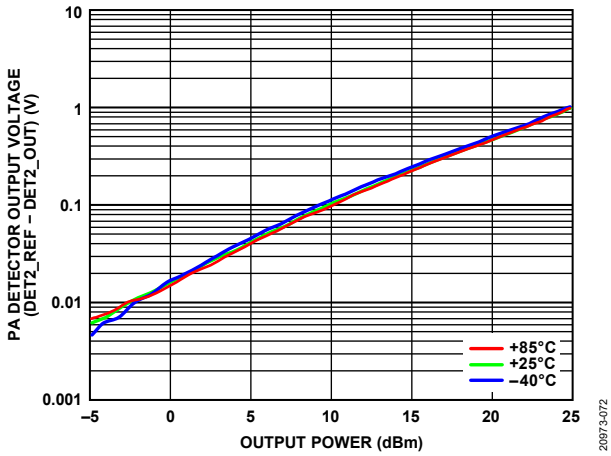


Figure 72. PA Detector Output Voltage (DET2_REF – DET2_OUT) vs. Output Power over Temperatures, RF = 81 GHz

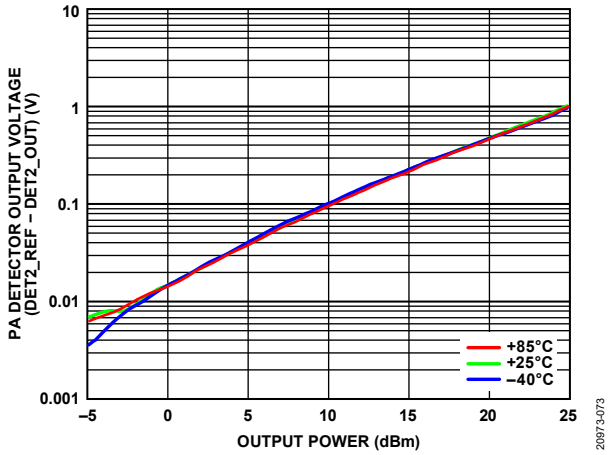


Figure 73. PA Detector Output Voltage (DET2_REF – DET2_OUT) vs. Output Power over Temperatures, RF = 83.5 GHz

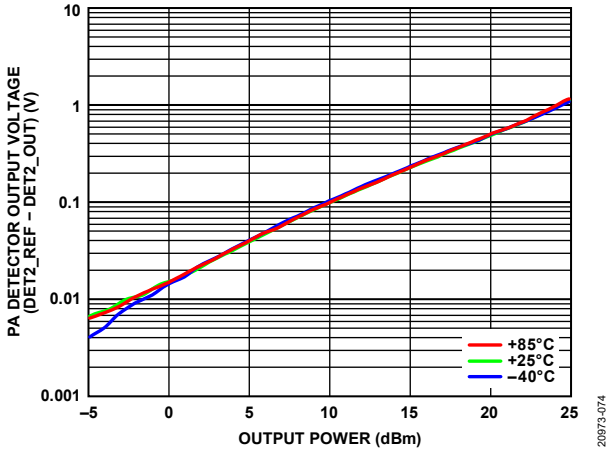


Figure 74. PA Detector Output Voltage (DET2_REF – DET2_OUT) vs. Output Power over Temperatures, RF = 86 GHz

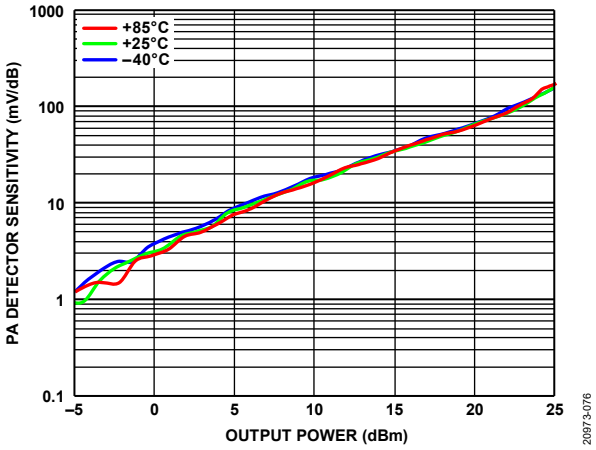


Figure 75. PA Detector Sensitivity vs. Output Power over Temperature, RF = 81 GHz

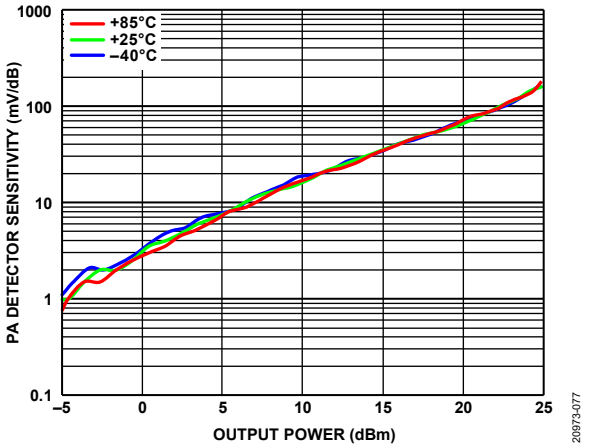


Figure 76. PA Detector Sensitivity vs. Output Power over Temperature, RF = 83.5 GHz

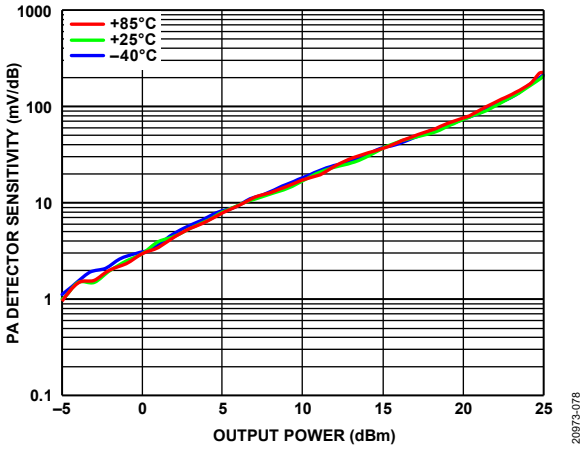


Figure 77. PA Detector Sensitivity vs. Output Power over Temperature, RF = 86 GHz

RETURN LOSS PERFORMANCE

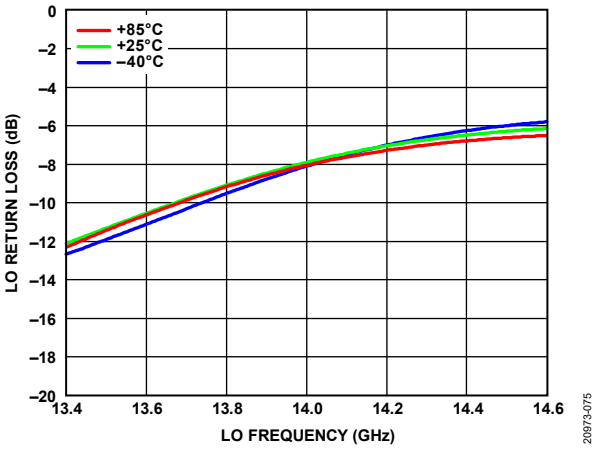


Figure 78. LO Return Loss vs. LO Frequency over Temperature

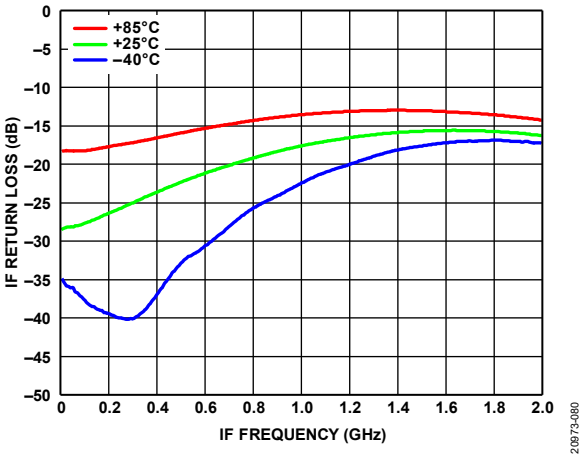


Figure 80. IF Return Loss vs. IF Frequency over Temperature

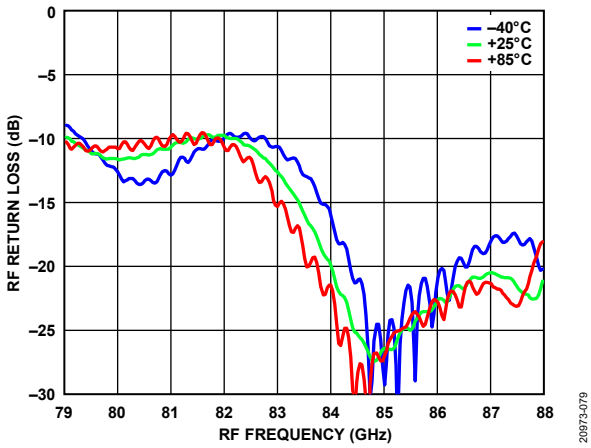


Figure 79. RF Return Loss vs. RF Frequency over Temperature

SPURIOUS PERFORMANCE

T_A = 25°C, IF = 1 GHz, IF input power = −4 dBm, and LO power = 4 dBm, unless otherwise noted. Mixer spurious products are measured in dBc from the RF output power for 60 GHz to 90 GHz due to the waveguide bandwidth. Spur values are (M × IF) + (N × LO). N/A means not applicable.

M × N Spurious Outputs, RF = 81 GHz, LO = 13.333 GHz

		N × LO		
		5	**6**	**7**
M × IF	**−5**	<−80	−79	−67
	−4	<−80	−79	−67
	−3	<−80	−77	N/A
	−2	<−80	−63	N/A
	−1	<−80	−39	N/A
	0	−79	−9	N/A
	+1	<−80	0	N/A
	+2	<−80	−30	N/A
	+3	<−80	−50	N/A
	+4	<−80	−69	N/A
	+5	<−80	−70	N/A

M × N Spurious Outputs, RF = 83.5 GHz, LO = 13.75 GHz

		N × LO		
		5	**6**	**7**
M × IF	**−5**	N/A	<−80	−79
	−4	N/A	<−80	−72
	−3	N/A	<−80	−69
	−2	N/A	<−80	−54
	−1	N/A	<−80	−33
	0	N/A	<−80	−5
	+1	N/A	<−80	0
	+2	N/A	<−80	−32
	+3	N/A	<−80	−46
	+4	N/A	<−80	−64
	+5	<−80	−78	−68

M × N Spurious Outputs, RF = 86 GHz, LO = 14.167 GHz

		N × LO		
		5	**6**	**7**
M × IF	**−5**	N/A	<−80	−71
	−4	N/A	<−80	−71
	−3	N/A	<−80	−64
	−2	N/A	<−80	−70
	−1	N/A	−79	−26
	0	N/A	−75	−9
	+1	N/A	−74	0
	+2	N/A	−79	−33
	+3	N/A	−80	−47
	+4	<−80	−79	−60
	+5	<−80	−77	−65

THEORY OF OPERATION

The ADMV7320 is a fully integrated SiP, I/Q upconverter that is made up of three functional blocks: a mixer and LO path, an envelope detector, a VGA, and a power detector, and a power amplifier and power detector.

MIXER AND LO PATH

The first functional block is a gallium arsenide (GaAs) I/Q upconverter driven by a 6× LO multiplier. The 6× multiplier allows the use of a lower frequency range LO input signal between 13.4 GHz and 14.6 GHz. The 6× multiplier is implemented using a cascade of 3× and 2× multipliers. LO buffer amplifiers are included on chip to allow a typical LO drive level of 4 dBm for typical performance. The LO path feeds a quadrature splitter followed by on-chip baluns that drive the I and Q mixer cores. The mixer cores comprise of singly balanced passive mixers. The RF outputs of the I and Q mixers are then summed through an on-chip Wilkinson power combiner, which is then fed into the second functional block.

ENVELOPE DETECTOR, VGA, AND POWER DETECTOR

The second functional block is a VGA (see Figure 81). The VGA utilizes multiple gain stages and staggered voltage variable attenuation stages to form a low noise, high linearity variable gain amplifier. The first stage of the VGA is a low noise preamp. A portion of the signal is coupled away and further amplified before driving an on-chip envelope detector. The envelope detector provides an output that is proportional to the peak envelope power of the incoming signal.

The preamp is followed by the first voltage variable attenuator in the signal path. Then, a second stage amplifier provides additional gain and isolation before driving the second variable attenuator block. Three cascaded gain stages follow the second variable attenuator.

At the output of the second stage, another coupler taps off a small portion of the output signal. The coupled signal is presented to an on-chip diode detector for external monitoring of the output power. A matched reference diode, Detector 1 (DET1), is included to help correct for detector temperature dependencies. A typical application circuit for the power detector is shown in Figure 83.

See the Applications Information section for further details on biasing the different blocks. The output of the VGA then feeds into the third functional block of the ADMV7320.

POWER AMPLIFIER AND POWER DETECTOR

The third block is a power amplifier that uses four cascaded gain stages to form the amplifier, see Figure 82.At the output of the last stage, a coupler taps off a small portion of the output signal. The coupled signal is presented to an on-chip diode detector for external monitoring of the output power. A matched reference diode, Detector 2 (DET2), is included to help correct for detector temperature dependencies.

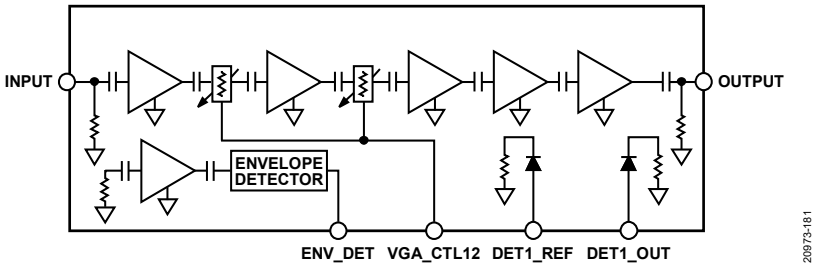


Figure 81. Variable Gain Amplifier Circuit Architecture

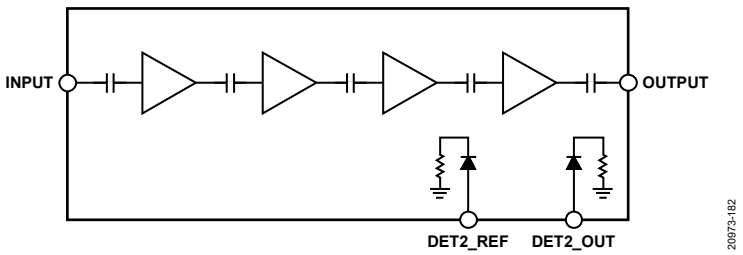


Figure 82. Power Amplifier Circuit Architecture

A typical application circuit for the power detector is shown in Figure 83. See the Applications Information section for further details on biasing the different blocks.

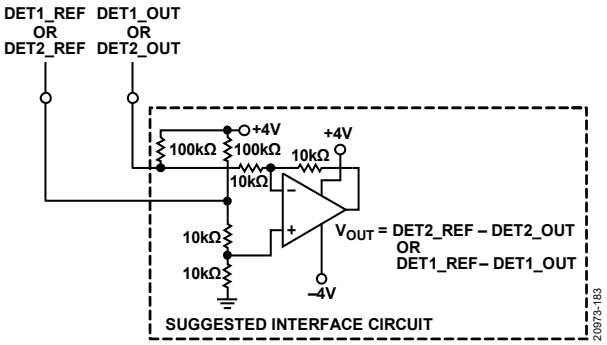


Figure 83. Typical Application Circuit for Power Detector

APPLICATIONS INFORMATION

POWER-UP BIAS SEQUENCE

The ADMV7320 functional blocks use active multiple amplifier and multiplier stages that all use depletion mode pseudomorphic high electron mobility transistors (pHEMTs). To ensure transistor damage does not occur, use the following power-up bias sequence and do not apply RF power to the device on the LO or IF ports before powering up the device:

1. Apply −2 V bias to VG_MULT, VG_AMP, VGA_VG12, VGA_VG345, VGA_VG6, PA_VG1, and PA_VG2.
2. Apply −1 V bias to VG_MIXER.
3. Apply between −5 V (minimum attenuation) and −1 V (maximum attenuation) bias to VGA_CTL12.
4. Apply 1.5 V bias to VD_MULT.
5. Apply a 4 V bias to VD_AMP, VGA_VD12, VGA_VD345, VGA_VD6, PA_VD1, PA_VD2, DET1_REF_BIAS, DET1_OUT_BIAS, DET2_REF_BIAS and DET2_OUT_BIAS (see Figure 86).
6. Adjust VG_AMP between −2 V and 0 V to achieve a total I_{VD_AMP} current of 175 mA.
7. Adjust VGA_VG12 between −2 V and 0 V to achieve a total I_{VGA_VD12} current of 35 mA.
8. Adjust VGA_VG345 and VGA_VG6 between −2 V and 0 V to achieve a total I_{VGA_VD345} and I_{VGA_VD6} current of 215 mA.
9. Adjust PA_VG1 between −2 V and 0 V to achieve a total I_{PA_VD1} current of 400 mA.
10. Adjust PA_VG2 between −2 V and 0 V to achieve a total I_{PA_VD2} current of 400 mA.
11. Apply a LO input signal on the LO port and adjust VG_MULT between −2 V and 0 V to achieve a total I_{VD_MULT} current of 80 mA.

POWER-DOWN BIAS SEQUENCE

To power-down the ADMV7320, take the following steps:

1. Apply a 0 V bias to VD_MULT, VD_AMP, VGA_VD12, VGA_VD345, VGA_VD6, PA_VD1, PA_VD2, DET1_REF_BIAS, DET1_OUT_BIAS, DET2_REF_BIAS, and DET2_OUT_BIAS supply voltage per application circuit.
2. Apply a 0 V bias to VGA_CTL12.
3. Apply a 0 V bias to VG_MIXER.
4. Apply a 0 V bias to VG_MULT, VG_AMP, VGA_VG12, VGA_VG345, VGA_VG6, PA_VG1, and PA_VG2.

LO NULLING

LO nulling is required to achieve optimal overall RF performance, especially for LO to RF rejection. This nulling is achieved by applying dc voltages (V_{DC}) between −0.2 V and +0.2 V to the IF_IN, IF_IP, IF_QN, and IF_QP ports to suppress the 6× LO signal at the RFOUT port across the RF frequency band by approximately 40 dBc. To suppress the 6× LO signal at the RFOUT port, use the following nulling sequence:

1. Adjust IF_IN V_{DC} between −0.2 V and +0.2 V. Monitor the 6× LO leakage on the RFOUT port. When the desired or maximum level of suppression is achieved, proceed to Step 2.
2. Adjust IF_IP V_{DC} between −0.2 V and +0.2 V. Monitor the 6× LO leakage on the RFOUT port. When the desired or maximum level of suppression is achieved, proceed to Step 3.
3. Adjust IF_QN V_{DC} input between −0.2 V and +0.2 V. Monitor the 6× LO leakage on the RFOUT port. When the desired or maximum level of suppression is achieved, proceed to Step 4.
4. Adjust IF_QP V_{DC} between −0.2 V and +0.2 V. Monitor the 6× LO leakage on the RFOUT port. When the desired or maximum level of suppression is achieved, proceed to Step 5.
5. If the desired level of the 6× LO signal on the RFOUT port is still not achieved, further tune each dc voltage to the IF_IN, IF_IP, IF_QN, and IF_QP ports by repeating Step 1 through Step 4. The resolution of the voltage changed on the dc voltage of the inputs must be in the millivolt.
6. To ensure that the mixer core is not damaged during the LO nulling, limit each current to IF_IN, IF_IP, IF_QN, and IF_QP to 3 mA.
7. LO nulling must be conducted with any change in input LO frequency, temperature change, or when Gain Tuning Order 1 is conducted. The level of suppression changes as those conditions vary.

GAIN TUNING PROCEDURE

The ADMV7320 features three different mechanisms to control the total gain of the transmitter. The first mechanism is the variable gain control of the variable gain control amplifier of the transmitter. The variable gain control is controlled by the VGA_CTL12 pin. The voltage control range to achieve maximum and minimum gain from the VGA is −5 V to −1 V. The second mechanism for further gain control is to lower the I_{VGA_VD345} and I_{VGA_VD6} current consumption via the VGA_VG345 and VGA_VG6 pins from the nominal VGA_VG345 + VGA_VG6 voltage to achieve the nominal $I_{VGA_VD12} + I_{VGA_VD345} + I_{VGA_VD6}$ current consumption. The third mechanism is to lower the I_{PA_VD1} current consumption via PA_VG1 from the nominal PA_VG1 voltage to achieve the nominal $I_{PA_VD1} + I_{PA_VD2}$ current consumption.

See Table 5 for additional details as to which gain control mechanism to use per the desired gain control range required. The settings detailed in Table 5 are guidelines for a gain control approach and may need adjustment depending on application requirements over temperature and frequency.

Follow the gain tuning order to control the gain to achieve the correct gain level for optimal performance.

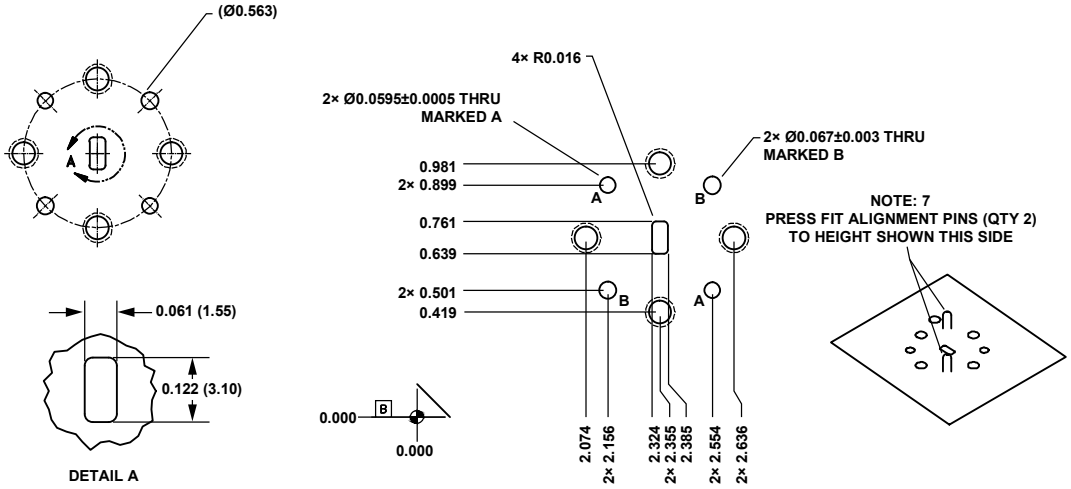
Table 5. Recommended Gain Settings

Gain Tuning Order	Gain Reduction Range (dB)	Gain Tuning	Recommended Gain Tuning Voltage Range (V)	Description of Gain Tuning Procedure
1	0 to 10	VGA_CTL12	−5 to −1	To achieve maximum gain, set VGA_CTL12 to −5 V. To achieve a gain reduction between 0 dB and 10 dB, adjust VGA_CTL12 between −5 V and −1 V (−1 V is the typical minimum gain for the VGA). For both of these conditions, follow the bias procedure in the Theory of Operation section to bias the ADMV7320 to the normal operating currents.
2	10 to 25	VGA_VG345 + VGA_VG6	−2 to 0	To achieve greater than 10 dB to 25 dB gain reduction, adjust VGA_CTL12 between −5 V and −1 V. If further gain reduction is required to achieve 25 dB gain reduction after conducting Gain Tuning Order 1, lower $I_{VGA_VD345} + I_{VGA_VD6}$ by adjusting VGA_VG345 + VGA_VG6 between −2 V and 0 V to achieve the correct gain level. The total current consumption of $I_{VGA_VD345} + I_{VGA_VD6}$ while adjusting the VGA_VG345 + VGA_VG6 to drop to 45 mA (nominal $I_{VGA_VD345} + I_{VGA_VD6}$ is 215 mA).
3	25 to 40	PA_VG1	−2 to 0	To achieve greater than 25 dB to 40 dB gain reduction, adjust VGA_CTL12 to −1 V and adjust the total current consumption of $I_{VGA_VD345} + I_{VGA_VD6}$ between 200 mA and 45 mA per Gain Tuning Order 2. If further gain reduction is needed to achieve 40 dB gain reduction after conducting Gain Tuning Order 2, lower I_{PA_VD1} by adjusting PA_VG1 between −2 V and 0 V to achieve the correct gain level. The total current consumption of I_{PA_VD1} while adjusting PA_VG1 must not drop below 100 mA (nominal I_{PA_VD1} is 400 mA).

LAYOUT

Solder the exposed pad on the underside of the ADMV7320 to a low thermal and electrical impedance ground plane. This pad is typically soldered to an exposed opening in the solder mask. Connect these ground vias to all other ground layers to maximize heat dissipation from the device package.

Figure 84 illustrates the recommended mechanical layout on the interface plate used to interface to the WR-12 waveguide opening of the ADMV7320. The recommended PCB land pattern footprint is shown in Figure 85.

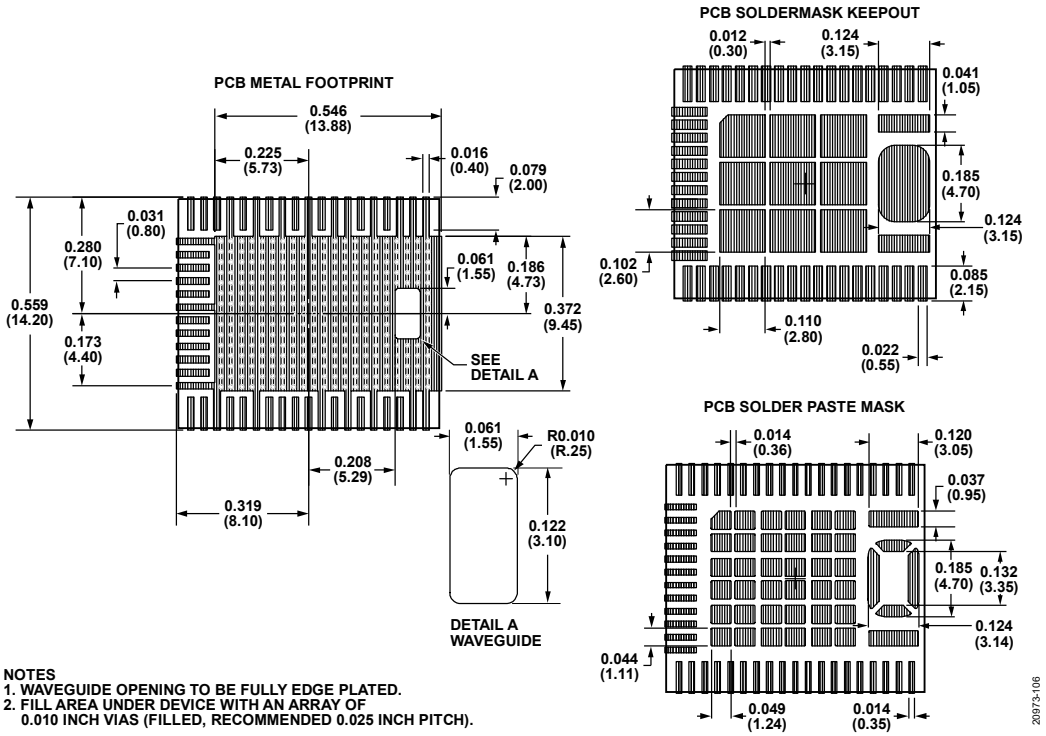


PART LIST				
ITEM	QTY	VENDOR	STOCK NUMBER	DESCRIPTION
1	2	VARIOUS	VARIOUS	PIN, ALIGNMENT, FLANGE, 0.0615 DIA

NOTES:
1. REMOVE BURRS AND BREAK SHARP EDGES.
2. ALL INTERNAL RADII ARE 0.090 UNLESS OTHERWISE NOTED.
3. SURFACE FINISH 32 RMS UNLESS OTHERWISE SPECIFIED.
4. DIMENSIONS APPLY AFTER PLATING.
5. MATERIAL: ALUMINUM 6061-T6 PER QQ-A-250/11.
6. FINISH: NONE.
7. INSTALL DOWEL PINS.
8. USE ELECTRONIC DATA FOR ALL GEOMETRY THAT IS NOT DIMENSIONED.

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Figure 84. Recommended Standard WR-12 Footprint



NOTES
1. WAVEGUIDE OPENING TO BE FULLY EDGE PLATED.
2. FILL AREA UNDER DEVICE WITH AN ARRAY OF 0.010 INCH VIAS (FILLED, RECOMMENDED 0.025 INCH PITCH).

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Figure 85. PCB Land Pattern Footprint

TYPICAL APPLICATION CIRCUIT

Figure 86 shows the typical application circuit.

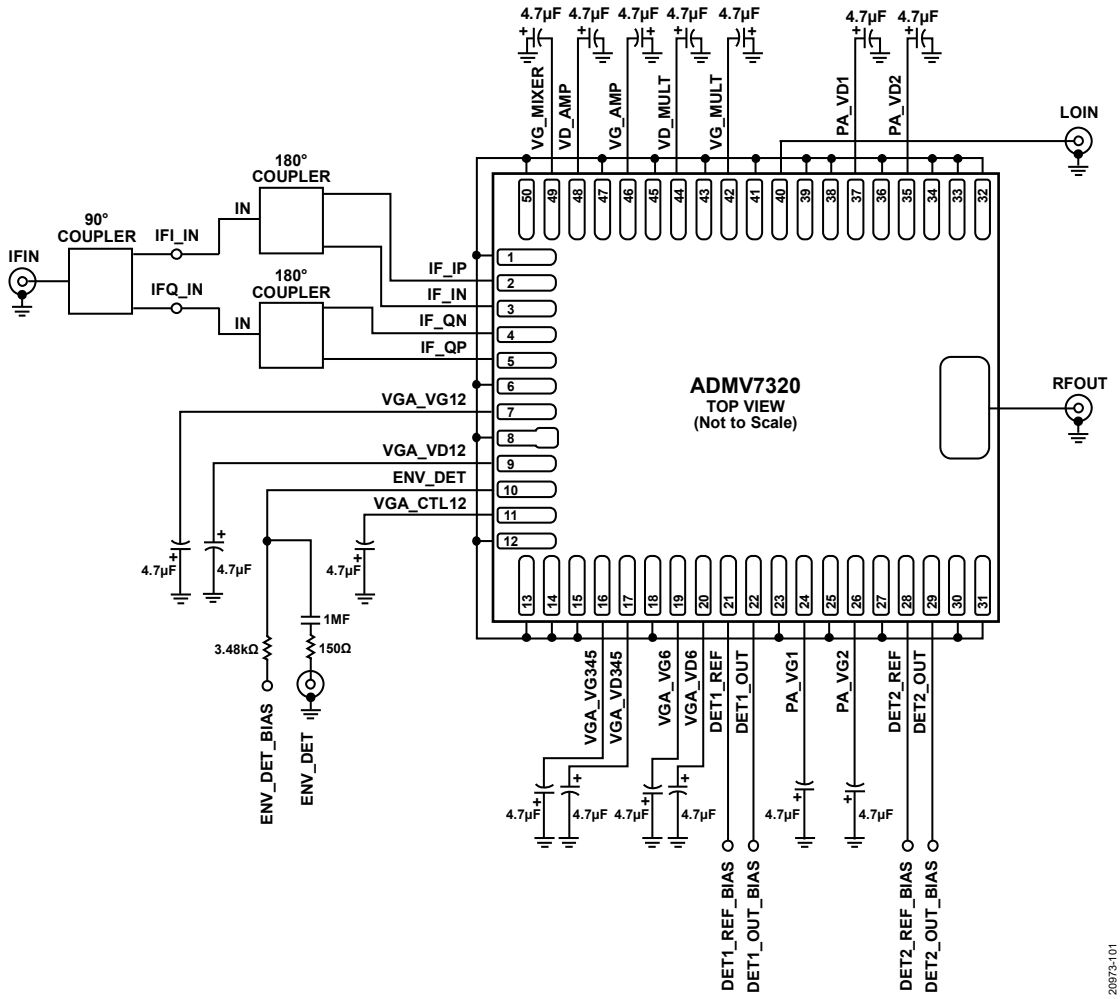


Figure 86. Typical Application Circuit

OUTLINE DIMENSIONS

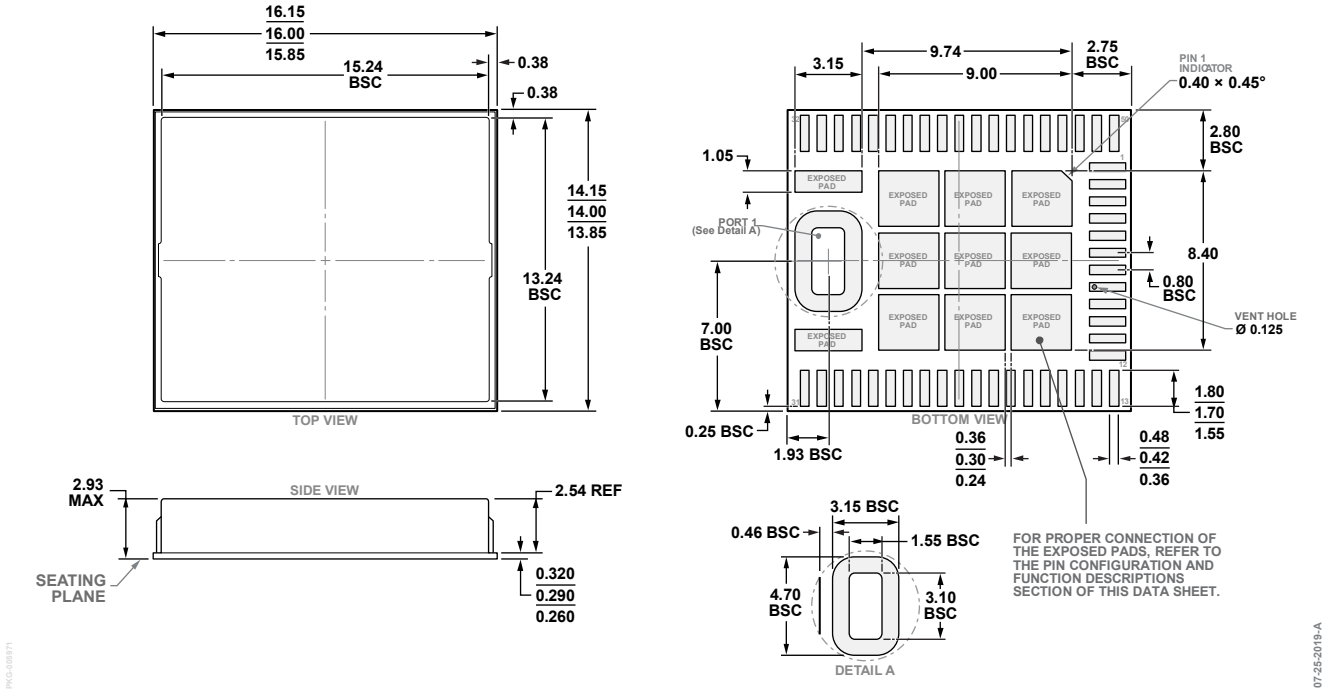


Figure 87. 50-Terminal Chip Array Small Outline No Lead Cavity [LGA_CAV]
16.00 mm × 14.00 mm Body and 2.93 mm Package Height
(CE-50-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADMV7320BCEZ	−40°C to +85°C	50-Terminal Chip Array Small Outline No Lead Cavity [LGA_CAV]	CE-50-2
ADMV7320-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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