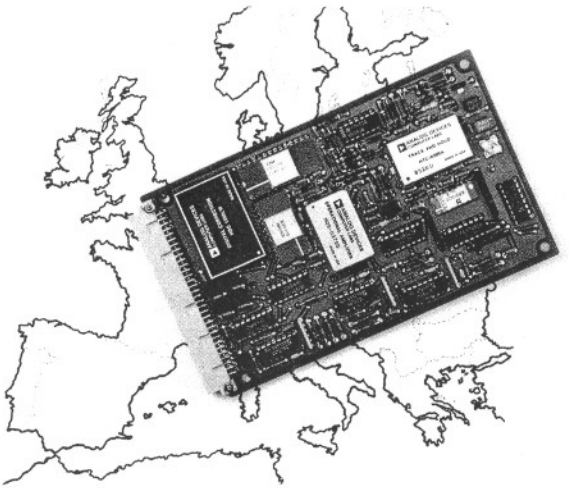
12-Bit Eurocard Analog-to-Digital Converter

CAV-1202

FEATURES
12-Bit Resolution
2MHz Word Rate
Single Eurocard Size
TTL Compatible
No External Support Circuits

APPLICATIONS
Radar Digitizing
Medical Instrumentation
Transient Analysis



GENERAL DESCRIPTION

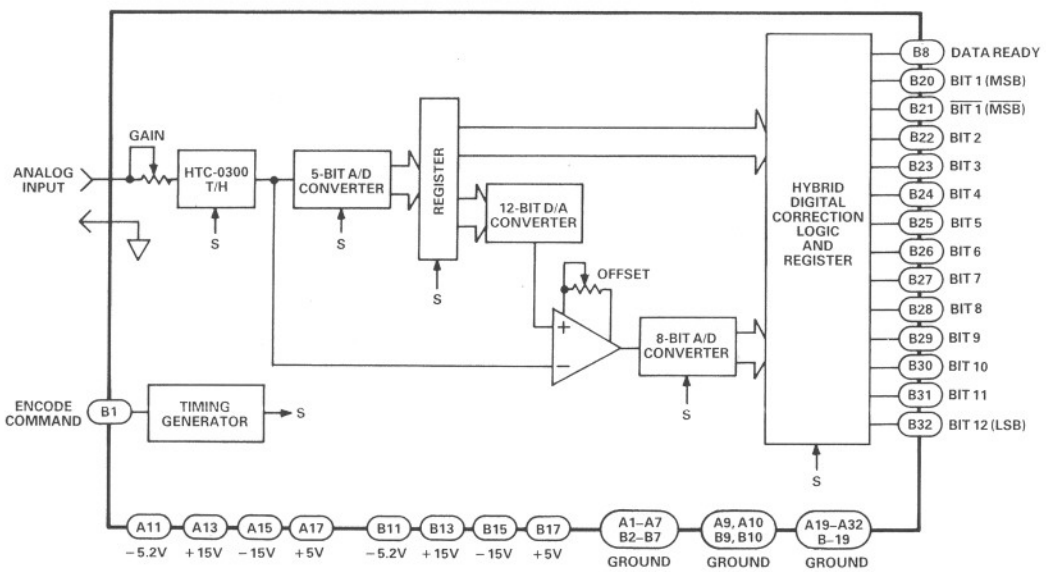
The Analog Devices Model CAV-1202 A/D Converter is a unique combination of 12-bit resolution, 2MHz word rates, and small size capable of being applied in a multitude of high-speed digitizing applications.

This remarkable, complete converter includes a track-and-hold along with encoding and timing circuits in a single "Eurocard" format. The unit requires only an encode command and external power supplies; no external support circuits are needed.

Increasingly, large scale electronic devices and systems are designed in modular form. This approach for combining complex circuits and subsystems is best served if all components of the systems share a common, standard geometry. When they do, it becomes possible to combine modules of various functions and manufacturers in one common subrack.

In Europe and many other parts of the world, Europa and double Europa size printed circuit boards are used extensively as the basis of a standardized 19″ system. The four levels of this system have evolved into a standard arrangement of dimensions which make it possible to combine components in one level and insert them into the components of the next higher level.

The design of the CAV-1202 is based on the Level 2 requirements for printed circuit board subunits and meets the standards established by DIN 41494, IEC 48D (sec) 12.



CAV-1202 Block Diagram

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SPECIFICATIONS (typical @ +25°C with nominal power supplies unless otherwise noted)

Parameter	Units	CAV-1202
RESOLUTION (FS = Full Scale)	Bits (% FS)	12 (0.024)
LSB WEIGHT	mV	1.0
ACCURACY		
(Including Linearity) @ dc	% FS ± 1/2LSB	0.0122
Monotonicity		Guaranteed Over Temperature
Diff. Nonlinearity vs. Temperature	ppm/°C (max)	2 (4)
Offset vs. Temperature	ppm/°C (max)	50 (100)
Gain vs. Temperature	ppm/°C (max)	75 (150)
DYNAMIC CHARACTERISTICS		
In-Band Harmonics[1]		
dc to 500kHz Input	dB Below FS (min)	74 (70)
500kHz to 1MHz Input	dB Below FS (min)	67 (60)
Conversion Time[2]	ns (max)	400 (± 25) + 2 Clock Periods
Conversion Rate[3]	MHz (max)	dc to 2 (2.2)
Aperture Uncertainty (Jitter)	ps, rms, max	30
Effective Aperture Delay Time[4]	ns (max)	− 19 (± 5)
Signal to Noise Ratio (SNR)[5]		
360kHz Input	dB (min)	66 (65)
Transient Response[6]	ns	500
Overvoltage Recovery[7]	ns	1000
Input Bandwidth (−3dB)[8]	MHz	5
Two-Tone Linearity (@ Input Frequencies)[9]		
(500kHz; 540kHz)	dB Below FS	65
ANALOG INPUT		
Voltage Range[10]		
Operating	V, FS	± 2.048
Maximum Without Damage	V, max	± 4
Input Type		Bipolar
Impedance	Ω	95
Offset[11]		
Initial	mV	± 2
ENCODE COMMAND INPUT[12]		
Logic Levels, TTL-Compatible	V	"0" = 0 to + 0.4
	V	"1" = + 2.5 to + 5.0
Impedance	Ω, min	100k
Rise and Fall Times	ns, max	10
Width		
Min	ns	20
Max	70% of Encode Command Period	
Frequency	MHz	dc to 2
DIGITAL OUTPUT		
Format	Data Bits	12 Parallel, Plus $\overline{\text{MSB}}$; NRZ
	Data Ready	1; RZ
Logic Levels, TTL-Compatible	V	"0" = 0 to + 0.5
		"1" = + 2.5 to + 4.0
Drive	LS Loads	10
Time Skew	ns, max	10
Coding		Binary (BIN); 2's Complement (2SC)
DATA READY OUTPUT		
Logic Levels, TTL-Compatible	V	"0" = 0 to + 0.5
		"1" = + 2.5 to + 4.0
Drive	LS Loads	10
Rise and Fall Times	ns, max	10
Duration	ns (max)	50 (± 10)
POWER REQUREMENTS[13]		
+ 15V ± 5%	mA (max)	105 (120)
− 15V ± 5%	mA (max)	70 (80)
+ 5V ± 5%	mA (max)	530 (550)
− 5.2V ± 5%	A (max)	1.0 (1.2)
Power Consumption	W (max)	10.5 (12)
TEMPERATURE RANGE		
Operating	°C	0 to + 70
Storage	°C	− 55 to + 85
Cooling Air Requirements	LFPM (Linear Feet Per Minute)	500
CONSTRUCTION		
Single Printed Circuit Card		
Including Connectors	Millimeters	167.3 × 100 × 13.13
	Inches	6.59 × 3.93 × 0.517
Board Only	Millimeters	160 × 100 × 1.57
	Inches	6.3 × 3.93 × 0.062
PRICE		
(1–4)	$	1940

For Applications Assistance, Call Computer Labs Division @ (919) 668-9511.

NOTES

[1] In-Band Harmonics expressed in terms of spurious in-band signals and related harmonics generated at 2MHz encode rate. Minimums shown guaranteed over operating temperature range of 0°C to + 70°C.
[2] Measured leading edge Encode Command to trailing edge of associated Data Ready; use trailing edge to strobe output data into external circuits (see text).
[3] For word rates below 100kHz, consult factory.
[4] See text for description of Effective Aperture Delay Time.
[5] Rms signal to rms noise ratio with full scale 540kHz analog input; minimums guaranteed over operating temperature range of 0°C to + 70°C (see Figure 3).
[6] For full-scale step input, 12-bit accuracy attained in specified time.
[7] Recovers to 12-bit accuracy in specified time after 2 × FS input overvoltage.
[8] Input bandwidth flat within 0.2dB, dc to 1MHz.
[9] Each input frequency applied at level 7dB below full scale.
[10] Standard bipolar input is adjustable ± 5% with on-card potentiometer (see text and Figure 1).
[11] Adjustable ± 15mV without performance degradation (see text and Figure 1).
[12] Transition from digital "0" to digital "1" initiates encoding.
[13] ± 15V must be equal and opposite within 200mV and track over temperature.

Specifications subject to change without notice.

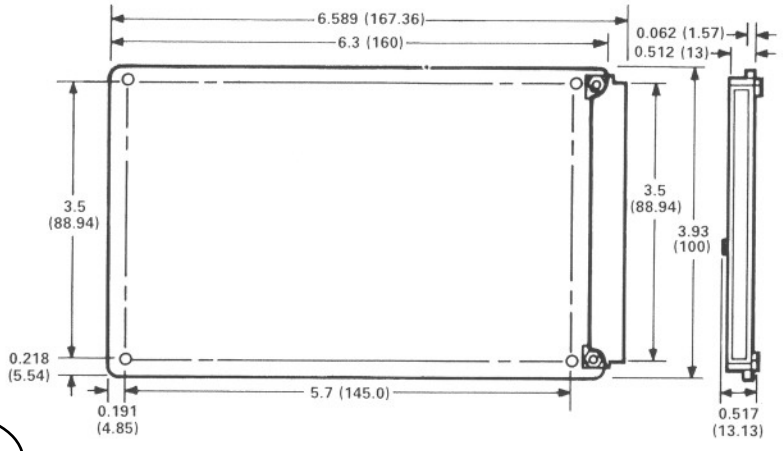
PIN DESIGNATIONS

ROW A		ROW B	
PIN	FUNCTION	PIN	FUNCTION
1	GROUND	1	ENCODE COMMAND
2	GROUND	2	GROUND
3	GROUND	3	GROUND
4	GROUND	4	GROUND
5	GROUND	5	GROUND
6	GROUND	6	GROUND
7	GROUND	7	GROUND
8	NO CONNECTION	8	DATA READY
9	GROUND	9	GROUND
10	GROUND	10	GROUND
11	− 5.2V	11	− 5.2V
12	− 5.2V SENSE	12	− 5.2V RETURN*
13	+ 15V	13	+ 15V
14	+ 15V SENSE	14	+ 15V RETURN*
15	− 15V	15	− 15V
16	− 15V SENSE	16	− 15V RETURN*
17	+ 5V	17	+ 5V
18	+ 5V SENSE	18	+ 5V RETURN*
19	GROUND	19	GROUND
20	GROUND	20	BIT 1 (MSB)
21	GROUND	21	$\overline{\text{BIT 1 (MSB)}}$
22	GROUND	22	BIT 2
23	GROUND	23	BIT 3
24	GROUND	24	BIT 4
25	GROUND	25	BIT 5
26	GROUND	26	BIT 6
27	GROUND	27	BIT 7
28	GROUND	28	BIT 8
29	GROUND	29	BIT 9
30	GROUND	30	BIT 10
31	GROUND	31	BIT 11
32	GROUND	32	BIT 12 (LSB)

*CONNECTED INTERNALLY TO GROUND PINS
ANALOG INPUT IS SMA CONNECTOR LABELED J2

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



THEORY OF OPERATION

Refer to the block diagram of the CAV-1202.

Analog input signals to be digitized are applied to a track-and-hold (T/H) amplifier which is normally operating as a buffer amplifier in the "track" mode, following all changes in analog input as they occur. The user of the CAV-1202 determines the point at which the analog signal is to be digitized by applying an Encode Command.

The transition from digital "0" to digital "1" of the TTL-compatible encode command causes the track-and-hold to switch momentarily to the "hold" mode of operation. This "freezes" the analog input signal long enough to begin the digitizing process. The instant this switching action occurs is affected by one of the parameters of the CAV-1202, called out as Effective Aperture Delay Time in the Specifications Table.

Basically, effective aperture delay time is a measure of the difference between the converter's digital and analog delays (t_d-t_a) and can assume a zero, positive, or negative value depending on the comparative lengths of the two delays. In the CAV-1202, the analog delay (t_a) is longer than the digital delay (t_d), and causes effective aperture delay to be typically -19ns.

The "held" value of analog signal at the output of the T/H is applied to a 5-bit encoder. It is also applied as one input to a fast-settling operational amplifier.

The output of the encoder is applied as a 5-bit input to a 12-bit D/A converter. Via registers, the same digital signal is directed to the digital correction logic circuits and a second set of registers. These data will represent Bits 1–5 of the 12-bit digital output of the CAV-1202.

This reconstructed output of the D/A converter becomes the second input to the operational amplifier mentioned earlier. The output of the wideband, fast-settling op amp represents the residue which remains after a 5-bit digital representation of the analog input has been subtracted from that input.

This residue, or error, signal is encoded by a second converter and is applied as 8-bit digital information to the digital correction logic circuits which contain Bits 1–5.

The correction circuits combine the 5-bit and 8-bit bytes of data to compensate for possible nonlinearities and other errors to assure the final 12-bit output of the CAV-1202 is 12-bit accurate.

Expressed in its simplest terms, the digital correction logic circuits use the information in the 8-bit signal to determine what modifications of Bits 1–5 may be necessary. The value of the MSB in the 8-bit byte establishes whether the 5-bit data are passed "as is" or whether they are increased by a value of binary "1". The remaining bits (2–8) of the 8-bit byte become Bits 6–12 of the CAV-1202 digital output.

Digitally-corrected subranging (DCS), the innovative technique described here, helps compensate for a wide range of potential errors which could otherwise be avoided only if the CAV-1202 design included expensive, high precision components.

OFFSET AND GAIN ADJUSTMENTS

The design and manufacture of the CAV-1202 A/D Converter are innovative and precise, and have resulted in a high-performance converter which is virtually adjustment-free. This elimination of variable controls helps make the unit less susceptible to performance degradation caused by vibration, shock, or inadvertent and/or incorrect adjustment.

Only two control settings are available to the user; factory adjustments use selected fixed resistors to assure optimum performance without a need for "tweaking" by the user.

OFFSET and GAIN controls are available, but even these are sealed before shipment. In those rare instances where they may require readjustment, the procedure below is the one to use.

Refer to Figure 1, the CAV-1202 Adjustment Controls.

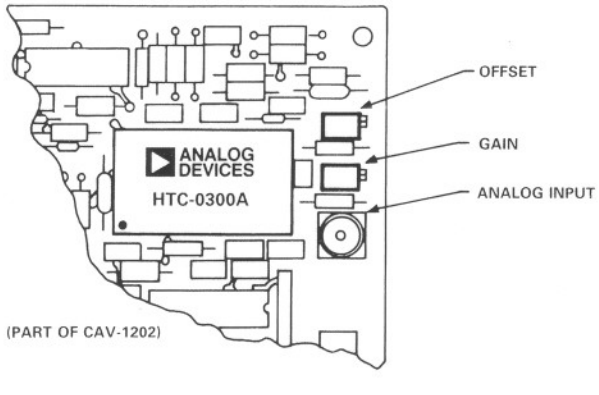


Figure 1. Offset and Gain Controls

When adjusting offset and gain of the CAV-1202 in the system, the OFFSET control should be adjusted first. The adjustment sequence is:

1. Apply to the analog input a precise (±0.25mV) dc level corresponding to midscale of the desired input range (0V input).
2. Adjust OFFSET control while observing MSB (Bit 1); adjust for MSB "toggling" between digital "0" and digital "1".
3. Apply a precise (±0.25mV) dc level corresponding to the most negative excursion of the desired input range. (For standard input, this is −2.048V.)
4. Adjust GAIN control while observing LSB (Bit 12); adjust for output of Bits 1–11 solid "0" with LSB "toggling".
5. Apply a precise (±0.25mV) dc level corresponding to the most positive excursion of the desired input range. (For standard input, this is +2.048V.)
6. Check digital output to assure Bits 1–11 are solid "1" with LSB "toggling".
7. Adjust OFFSET and GAIN controls alternately as necessary to obtain analog input range tolerance of ± 1/2LSB.

CAV-1202 TIMING

Refer to Figure 2, the CAV-1202 Timing Diagram.

The intervals which are shown represent a continuous update rate of 2MHz, and help illustrate the "pipeline delay" characteristic of the converter.

At this word rate, spacing between encode commands is 500 nanoseconds; and two additional encode commands have occurred before the data associated with the first command are valid. In Figure 2, this pipeline delay has a total time of approximately 1.4 microseconds (400ns + two encode periods of 500ns each). This interval will be different at other word rates, but will always include 400ns; at word rates lower than the converter's 2MHz maximum, it is longer.

After the initial delay, valid data will be available at the word rate dictated by encode commands. The spacing between Encode Command #1 and Encode Command #2 is one encode period, which is also the spacing between Data Ready #1 and Data Ready #2. In this illustration, the non-varying word rate causes the encode period to remain constant; note how the change from one group of valid data to the next also occurs with the same period.

System timing can be adjusted as necessary to take into account the pipeline delay effects and assure that the data of interest are strobed out of the converter at the appropriate time.

Figure 2 also illustrates why the trailing edge of the Data Ready pulse is recommended as the strobe for output data. Typically, data begin changing 5ns after the leading (rising) edge of each Data Ready pulse; they will be fully settled at the time of the trailing (falling) edge and available for use in external circuits.

DYNAMIC PERFORMANCE

Figure 3 shows typical performance on some of the dynamic characteristics which are important in systems using the CAV-1202 A/D Converter.

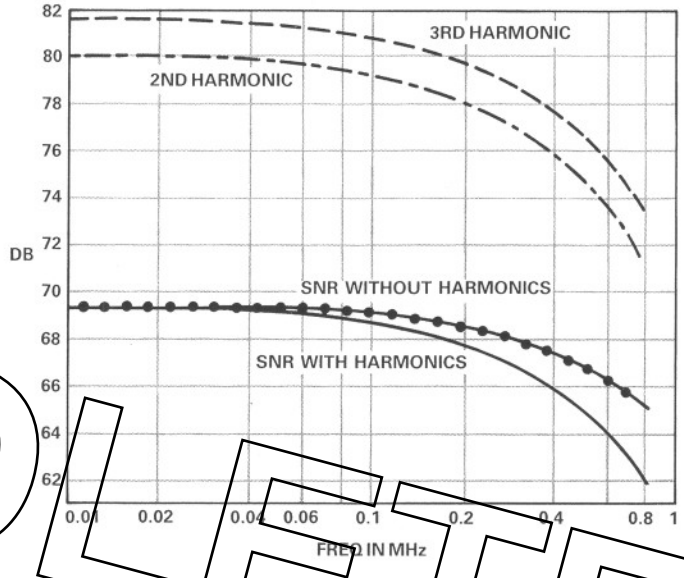


Figure 3. CAV-1202 SNR & Harmonics

The A/D was calibrated in final test for an encode rate of 2MHz. As shown, signal-to-noise ratio (SNR) with harmonics is typically better than 68dB at an input frequency of 100kHz; and remains greater than 60dB for full scale inputs of 800kHz. As expected, SNR without harmonics is better and is typically 65dB at 800kHz.

The level of 2nd and 3rd harmonics at word rates of 2MHz is also depicted; in these characteristics, too, the CAV-1202 has exceptional performance.

ORDERING INFORMATION

The standard CAV-1202 A/D Converter has the characteristics described within this data sheet and should be ordered by that number; there are no options to be specified by the user.

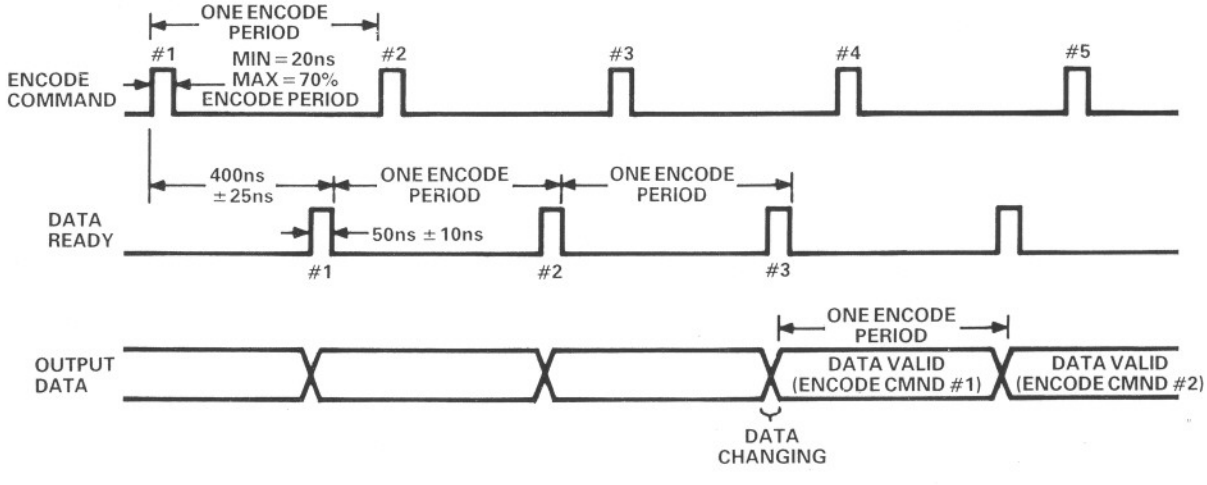


Figure 2. CAV-1202 Timing Diagram (2MHz Word Rate)

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