

Low-power / Low-voltage Precision Amplifier

Features

- Low Offset:
 - 10 μV Typ.
- Low Drift:
 - 0.05 $\mu\text{V}/^\circ\text{C}$ Max.
- Low Noise:
 - 22 $\text{nV}/\sqrt{\text{Hz}}$
- Open-loop Voltage Gain:
 - 135 dB Typ.
- Rail-to-Rail Inputs
- Rail-to-Rail Output Swing
 - to within 20 mV of supply voltage
- 1.0 mA Supply Current
- Slew rate:
 - 0.25 $\text{V}/\mu\text{s}$

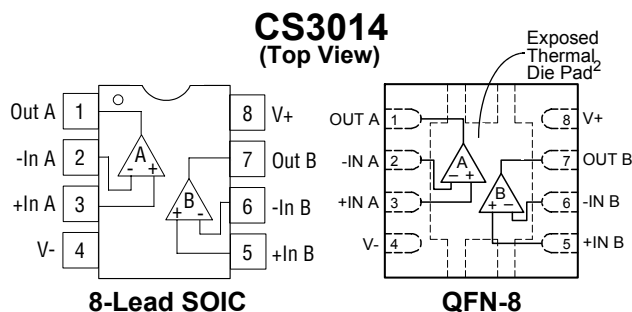
Applications

- Thermocouple/Thermopile Amplifiers
- Load Cell and Bridge Transducer Amplifiers
- Precision Instrumentation
- Battery-powered Systems

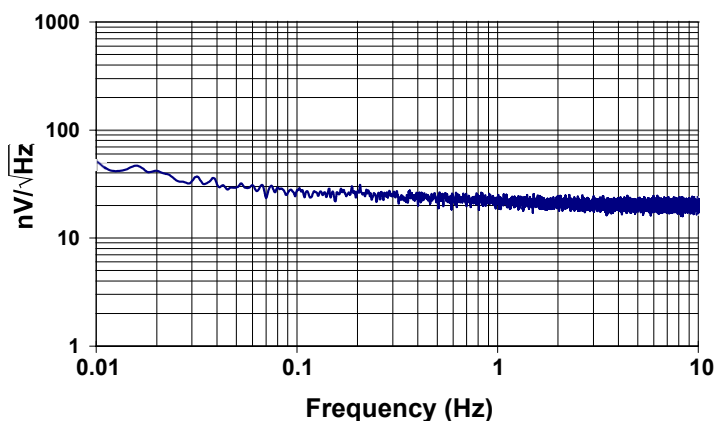
Description

The CS3004 dual amplifier is designed for precision amplification of low-level signals. These amplifiers achieve excellent offset stability, high open loop gain, and low noise. The devices also exhibit excellent CMRR and PSRR. The common mode input range includes the supply rails. The amplifiers operate with any supply voltage from 2.7 V to 5 V (± 1.35 V to ± 2.50 V).

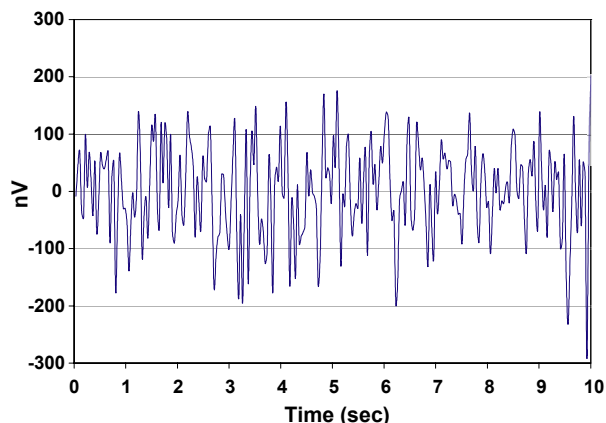
Pin Configurations



1. Must not be connected.
2. Connect thermal die pad to V-.



Noise vs. Frequency (Measured)



0.01 Hz to 10 Hz Noise Performance

TABLE OF CONTENTS

1. CHARACTERISTICS AND SPECIFICATIONS	3
1.1 5 V Electrical Characteristics	3
1.2 3 V Electrical Characteristics	4
1.3 Absolute Maximum Ratings	5
2. TYPICAL PERFORMANCE PLOTS	5
3. PACKAGE DRAWINGS	6
4. ORDERING INFORMATION	8
5. ENVIRONMENTAL, MANUFACTURING, & HANDLING INFORMATION ...	8

LIST OF FIGURES

Figure 1. Noise vs. Frequency (Measured)	5
Figure 2. 0.01 Hz to 10 Hz Noise	5
Figure 3. Gain & Phase vs. Frequency (2.7 V)	5
Figure 4. Gain & Phase vs. Frequency (5 V)	5
Figure 5. Supply Current vs. Supply Voltage	5
Figure 6. Supply Current vs. Temperature	5
Figure 7. Voltage Swing vs. Output Current (2.7 V)	6
Figure 8. Voltage Swing vs. Output Current (5 V)	6

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find one nearest you go to <http://www.cirrus.com>

IMPORTANT NOTICE

Cirrus Logic, Inc. and its subsidiaries ("Cirrus") believe that the information contained in this document is accurate and reliable. However, the information is subject to change without notice and is provided "AS IS" without warranty of any kind (express or implied). Customers are advised to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, indemnification, and limitation of liability. No responsibility is assumed by Cirrus for the use of this information, including use of this information as the basis for manufacture or sale of any items, or for infringement of patents or other rights of third parties. This document is the property of Cirrus and by furnishing this information, Cirrus grants no license, express or implied under any patents, mask work rights, copyrights, trademarks, trade secrets or other intellectual property rights. Cirrus owns the copyrights associated with the information contained herein and gives consent for copies to be made of the information only for use within your organization with respect to Cirrus integrated circuits or other products of Cirrus. This consent does not extend to other copying such as copying for general distribution, advertising or promotional purposes, or for creating any work for resale.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). CIRRUS PRODUCTS ARE NOT DESIGNED, AUTHORIZED OR WARRANTED FOR USE IN AIRCRAFT SYSTEMS, MILITARY APPLICATIONS, PRODUCTS SURGICALLY IMPLANTED INTO THE BODY, AUTOMOTIVE SAFETY OR SECURITY DEVICES, LIFE SUPPORT PRODUCTS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF CIRRUS PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK AND CIRRUS DISCLAIMS AND MAKES NO WARRANTY, EXPRESS, STATUTORY OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR PARTICULAR PURPOSE, WITH REGARD TO ANY CIRRUS PRODUCT THAT IS USED IN SUCH A MANNER. IF THE CUSTOMER OR CUSTOMER'S CUSTOMER USES OR PERMITS THE USE OF CIRRUS PRODUCTS IN CRITICAL APPLICATIONS, CUSTOMER AGREES, BY SUCH USE, TO FULLY INDEMNIFY CIRRUS, ITS OFFICERS, DIRECTORS, EMPLOYEES, DISTRIBUTORS AND OTHER AGENTS FROM ANY AND ALL LIABILITY, INCLUDING ATTORNEYS' FEES AND COSTS, THAT MAY RESULT FROM OR ARISE IN CONNECTION WITH THESE USES.

Cirrus Logic, Cirrus, and the Cirrus Logic logo designs are trademarks of Cirrus Logic, Inc. All other brand and product names in this document may be trademarks or service marks of their respective owners.

1. CHARACTERISTICS AND SPECIFICATIONS

1.1 5 V Electrical Characteristics

V+ = +5 V, ±5%; V- = 0V; VCM = 2.5 V; Unless otherwise noted, T_A = 25° C (See Note 1).

Parameter		Min	Typ	Max	Unit
Input Offset Voltage (Note 2)	•	-	±10	±20	μV
Average Input Offset Drift (Note 2)	•	-	±0.01	±0.05	μV/°C
Input Bias Current	•	-	±170	±250	pA
	•	-	-	±1.5	nA
Input Offset Current	•	-	±340	±500	pA
	•	-	-	±3.0	nA
Input Noise Voltage Density					
R _S = 100 Ω, f ₀ = 1 Hz		-	22	-	nV/√Hz
R _S = 100 Ω, f ₀ = 1 kHz		-	22	-	nV/√Hz
Input Noise Voltage		-	460	-	nV _{p-p}
Input Noise Current Density		-	100	-	fA/√Hz
Input Noise Current		-	1.9	-	pA _{p-p}
Input Voltage Range (Note 2)	•	V-	-	V+	V
Common Mode Rejection Ratio (dc)	•	105	120	-	dB
Power Supply Rejection Ratio	•	100	120	-	dB
Large Signal Voltage Gain		-	145	-	dB
(Note 3) R _L = 2 kΩ to V+/2	•	112	135	-	dB
Output Voltage Swing					
R _L = 2 kΩ to V+/2	•	(V+ - 200)	-	(V- + 200)	mV
(Note 4) R _L = 100 kΩ to V+/2	•	(V+ - 20)	-	(V- + 20)	mV
Slew Rate		-	0.25	-	V/μs
Overload Recovery Time		-	40	-	μs
Supply Current	•	-	1.0	1.25	mA
Oscillator Frequency		-	125	-	kHz
Input Capacitance					
Differential		-	1.5	-	pF
Common Mode		-	10	-	pF

- Notes: 1. Symbol “•” denotes specification applies over -40 to +125 ° C.
2. This parameter is guaranteed by design and/or laboratory characterization.
3. Guaranteed within the output limits of (V+ - 0.2 V) to (V- + 0.2 V).
4. Specifies the worst case drive voltage relative to the supply rail under stated load conditions.

1.2 3 V Electrical Characteristics

V+ = +3 V, ±10%; V- = 0V; VCM = 1.5 V; Unless otherwise noted, T_A = 25° C (See Note 5).

Parameter		Min	Typ	Max	Unit
Input Offset Voltage (Note 6)	•	-	±10	±20	μV
Average Input Offset Drift (Note 6)	•	-	±0.01	±0.05	μV/°C
Input Bias Current	•	-	±110	±150	pA
	•	-	-	±1.0	nA
Input Offset Current	•	-	±220	±300	pA
	•	-	-	±2.0	nA
Input Noise Voltage Density		-	22	-	nV/√Hz
R _S = 100 Ω, f ₀ = 1 Hz		-	22	-	nV/√Hz
R _S = 100 Ω, f ₀ = 1 kHz		-	-	-	-
Input Noise Voltage		-	460	-	nV _{p-p}
Input Noise Current Density		-	100	-	fA/√Hz
f ₀ = 1 Hz		-	-	-	-
Input Noise Current		-	1.9	-	pA _{p-p}
0.1 to 10 Hz		-	-	-	-
Input Voltage Range (Note 6)	•	V-	-	V+	V
Common Mode Rejection Ratio (dc)	•	105	120	-	dB
Power Supply Rejection Ratio	•	100	120	-	dB
Large Signal Voltage Gain		-	145	-	dB
(Note 7) R _L = 2 kΩ to V+/2	•	112	135	-	dB
Output Voltage Swing		(V+ - 200)	-	(V- + 200)	mV
(Note 8) R _L = 2 kΩ to V+/2	•	(V+ - 20)	-	(V- + 20)	mV
R _L = 100 kΩ to V+/2		-	-	-	-
Slew Rate		-	0.25	-	V/μs
R _L = 2 k, 100 pF		-	-	-	-
Overload Recovery Time		-	40	-	μs
Supply Current	•	-	1.0	1.25	mA
Oscillator Frequency		-	125	-	kHz
Input Capacitance		-	1.5	-	pF
Differential		-	10	-	pF
Common Mode		-	-	-	-

Notes: 5. Symbol “•” denotes specification applies over -40 to +125 ° C.

6. This parameter is guaranteed by design and laboratory characterization.

7. Guaranteed within the output limits of (V+ - 0.2 V) to (V- + 0.2 V).

8. Specifies the worst case drive voltage relative to the supply rail under stated load conditions.

1.3 Absolute Maximum Ratings

Parameter	Min	Typ	Max	Unit
Supply Voltage [(V+) – (V-)]	2.7	-	5.5	V
Input Voltage	(V-) – (0.3)	-	(V+) + (0.3)	V
Storage Temperature Range	-65	-	+150	°C

2. TYPICAL PERFORMANCE PLOTS

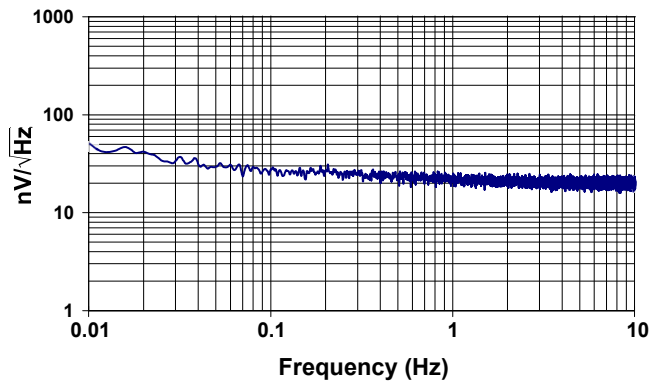


Figure 1. Noise vs. Frequency (Measured)

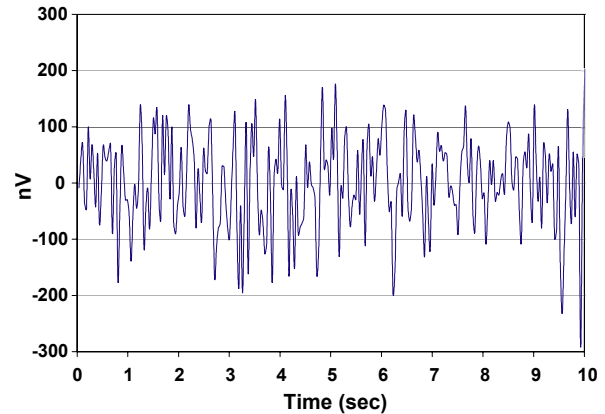


Figure 2. 0.01 Hz to 10 Hz Noise

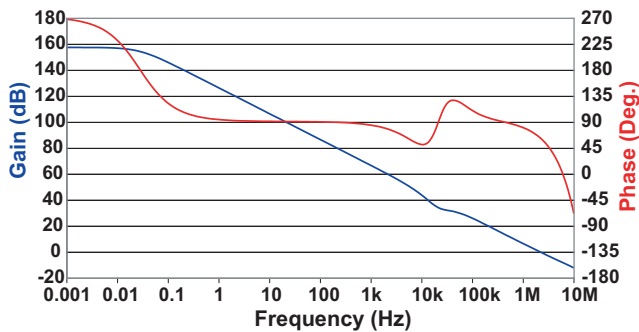


Figure 3. Gain & Phase vs. Frequency (2.7 V)

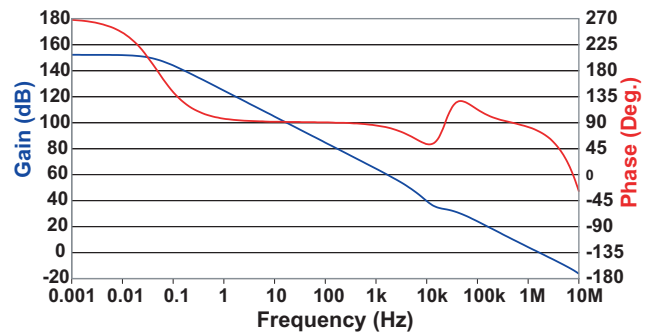


Figure 4. Gain & Phase vs. Frequency (5 V)

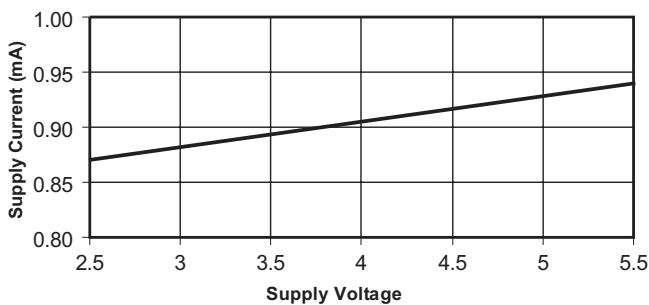


Figure 5. Supply Current vs. Supply Voltage

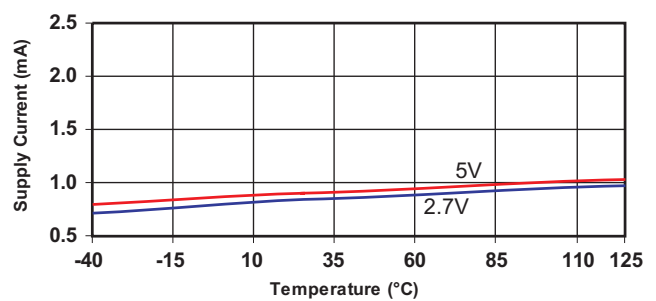


Figure 6. Supply Current vs. Temperature

Typical Performance Plots (Cont.)

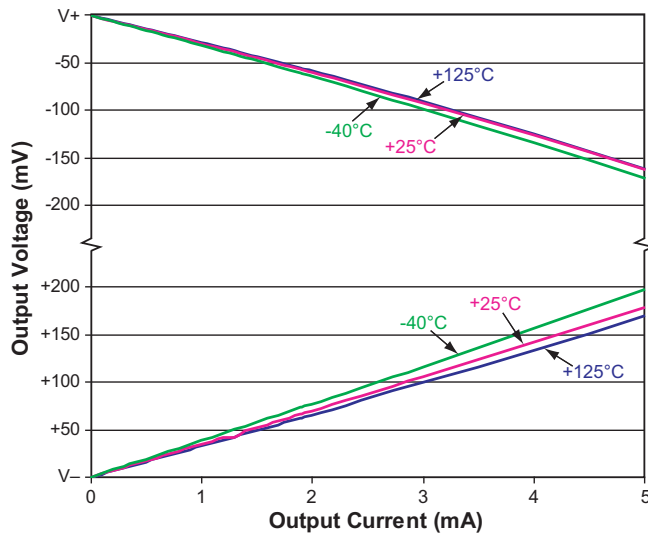


Figure 7. Voltage Swing vs. Output Current (2.7 V)

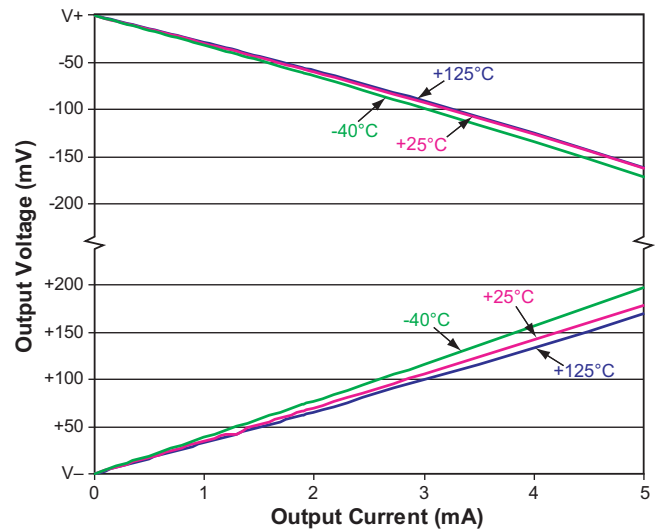
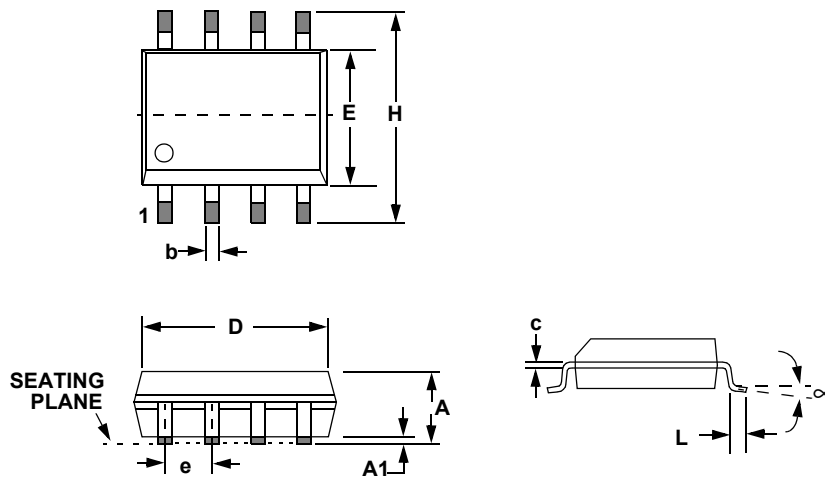


Figure 8. Voltage Swing vs. Output Current (5 V)

3. PACKAGE DRAWINGS

8L SOIC (150 MIL BODY) PACKAGE DRAWING



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.19	0.25
D	0.189	0.197	4.80	5.00
E	0.150	0.157	3.80	4.00
e	0.040	0.060	1.02	1.52
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27
∞	0°	8°	0°	8°

JEDEC # : MS-012

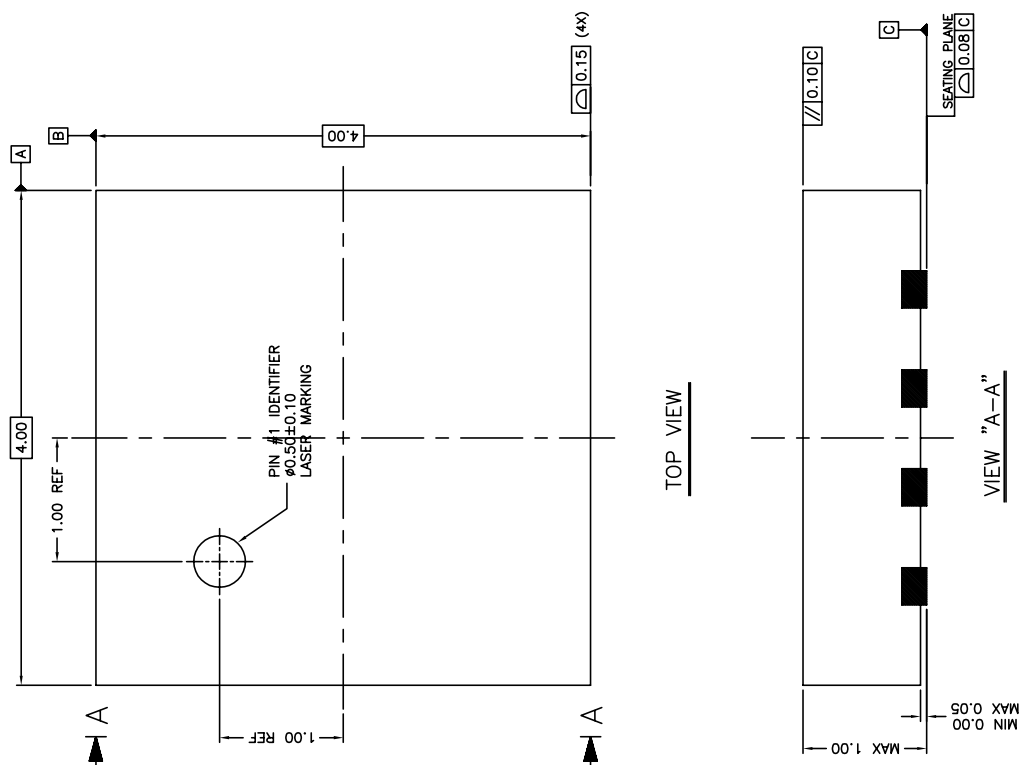
BOTTOM VIEW

Dimensions and features shown in the bottom view:

- Overall width: 3.45
- Overall height: 3.20
- Distance from left edge to first pin: 0.40 ± 0.10
- Distance between pins: 0.80
- Distance from right edge to last pin: 0.75
- Distance from top edge to first pin: 0.275
- Distance between pins: 0.80
- Distance from bottom edge to last pin: 0.35
- Pin #1 CORNER (C 0.25)
- 0.80x3=2.40 REF
- 0.10 (C A B)
- 0.05 (C)
- 0.30

NOTE)

1. CONTROLLING DIMENSIONS ARE IN MM.
2. UNLESS OTHERWISE SPECIFIED TOLERANCE : DECIMAL ± 0.05 ANGULAR $\pm 2'$
3. DIMENSIONING AND TOLERANCE PER ASME Y 14.5M - 1994.
4. DIMENSION LEAD WIDTH APPLIES TO THE PLATED TERMINAL AND IS MEASURED BETWEEN 0.28MM AND 0.33MM FROM THE TERMINAL TIP.



4. ORDERING INFORMATION

Part #	Temperature Range	Package Description
CS3014-FS	-40 °C to +125 °C	8-lead SOIC
CS3014-FSZ	-40 °C to +125 °C	8-lead SOIC, Lead Free
CS3014-FNZ*	-40 °C to +125 °C	8-lead QFN, Lead Free

* Connect thermal die pad to V-.

5. ENVIRONMENTAL, MANUFACTURING, & HANDLING INFORMATION

Model Number	Peak Reflow Temp	MSL Rating*	Max Floor Life
CS3014-FS	240 °C	2	365 Days
CS3014-FSZ	260 °C		
CS3014-FNZ			

* MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.

6. REVISION HISTORY

Revision	Date	Changes
A1	FEB 2007	First public release.
F1	AUG 2007	Updated to "Final" per QPL process.