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12314HK/51513TKIM TC-00002912 No.A2180-1/9

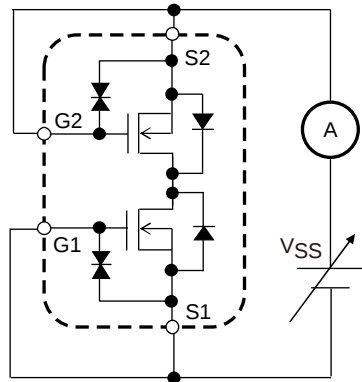
EFC4621R

Electrical Characteristics at $T_a = 25^{\circ}\text{C}$

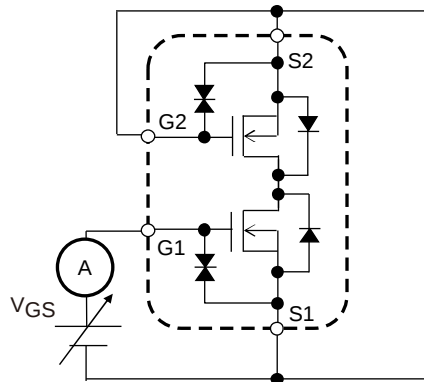
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Source to Source Breakdown Voltage	$V_{(BR)SSS}$	$I_S=1\text{mA}$, $V_{GS}=0\text{V}$ Test Circuit 1	24			V
Zero-Gate Voltage Source Current	I_{SSS}	$V_{SS}=20\text{V}$, $V_{GS}=0\text{V}$ Test Circuit 1			1	μA
Gate to Source Leakage Current	I_{GSS}	$V_{GS}=\pm 8\text{V}$, $V_{SS}=0\text{V}$ Test Circuit 2			± 1	μA
Cutoff Voltage	$V_{GS(off)}$	$V_{SS}=10\text{V}$, $I_S=1\text{mA}$ Test Circuit 3	0.5		1.3	V
Forward Transfer Admittance	$ y_{fs} $	$V_{SS}=10\text{V}$, $I_S=3\text{A}$ Test Circuit 4		7.3		S
Static Source to Source On-State Resistance	$R_{SS(on)1}$	$I_S=3\text{A}$, $V_{GS}=4.5\text{V}$ Test Circuit 5	10.8	15.5	18	$\text{m}\Omega$
	$R_{SS(on)2}$	$I_S=3\text{A}$, $V_{GS}=4.0\text{V}$ Test Circuit 5	11.1	16	19	$\text{m}\Omega$
	$R_{SS(on)3}$	$I_S=3\text{A}$, $V_{GS}=3.7\text{V}$ Test Circuit 5	11.5	16.5	20	$\text{m}\Omega$
	$R_{SS(on)4}$	$I_S=3\text{A}$, $V_{GS}=3.1\text{V}$ Test Circuit 5	12.5	18	23.5	$\text{m}\Omega$
	$R_{SS(on)5}$	$I_S=3\text{A}$, $V_{GS}=2.5\text{V}$ Test Circuit 5	14.9	23	30	$\text{m}\Omega$
Turn-ON Delay Time	$t_d(on)$	$V_{SS}=10\text{V}$, $V_{GS}=4.5\text{V}$, $I_S=3\text{A}$ Test Circuit 7		340		ns
Rise Time	t_r			600		ns
Turn-OFF Delay Time	$t_d(off)$			26000		ns
Fall Time	t_f			28000		ns
Total Gate Charge	Q_g	$V_{SS}=10\text{V}$, $V_{GS}=4.5\text{V}$, $I_S=9\text{A}$ Test Circuit 8		29		nC
Forward Source to Source Voltage	$V_{F(S-S)}$	$I_S=3\text{A}$, $V_{GS}=0\text{V}$ Test Circuit 6		0.77	1.2	V

Test circuits are example of measuring FET1 side

Test Circuit 1
 I_{SS}

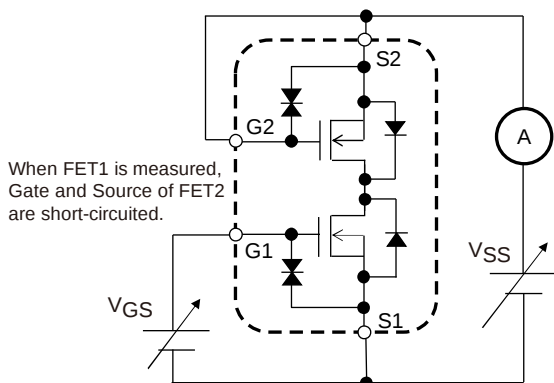


Test Circuit 2
 I_{GSS}

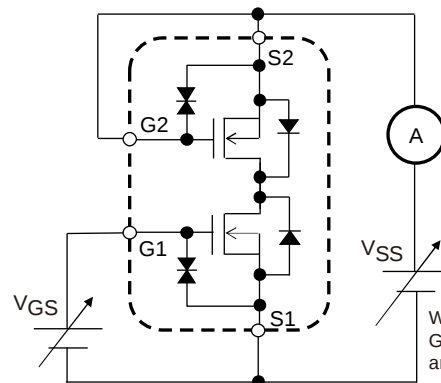


When FET1 is measured, Gate and Source of FET2 are short-circuited.

Test Circuit 3
 $V_{GS(off)}$

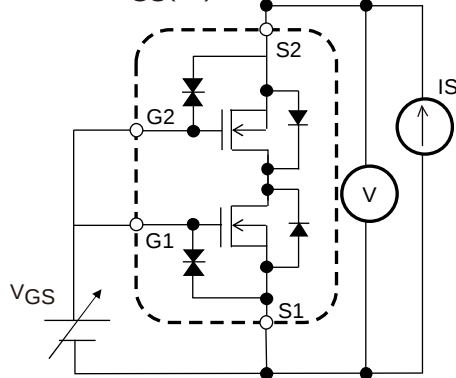


Test Circuit 4
 $|y_{fs}|$

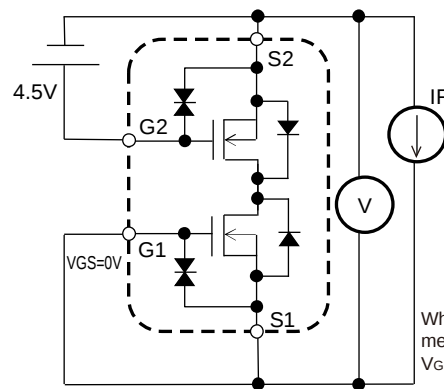


When FET1 is measured, Gate and Source of FET2 are short-circuited.

Test Circuit 5
 $R_{SS(on)}$

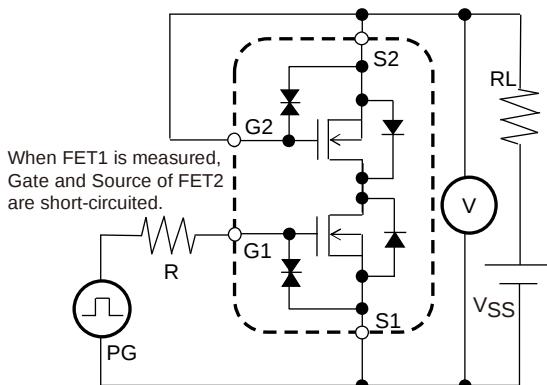


Test Circuit 6
 $V_F(S-S)$

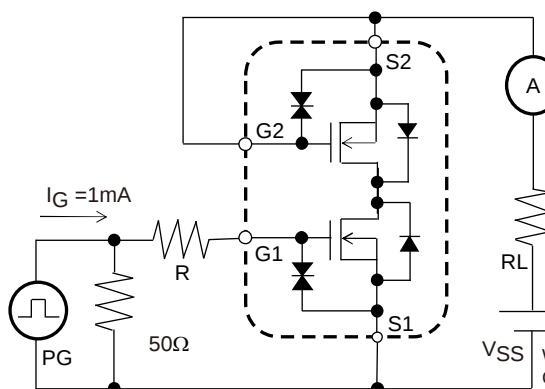


When FET1 is measured, +4.5V is added to V_{GS} of FET2.

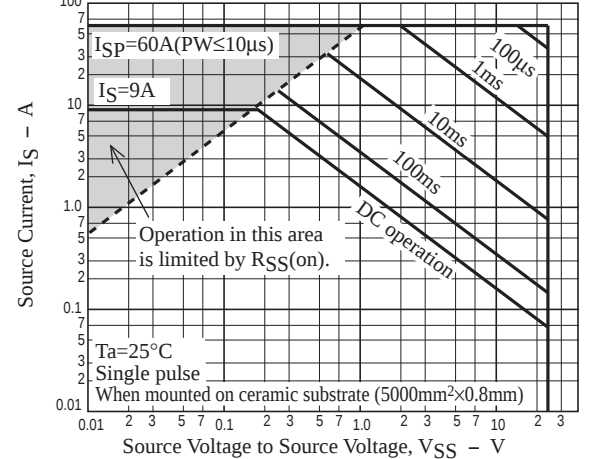
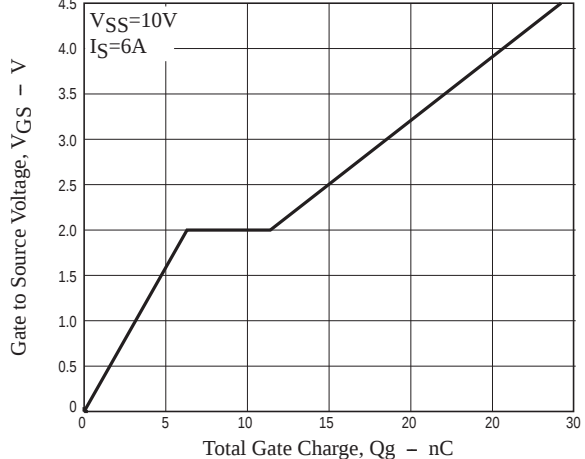
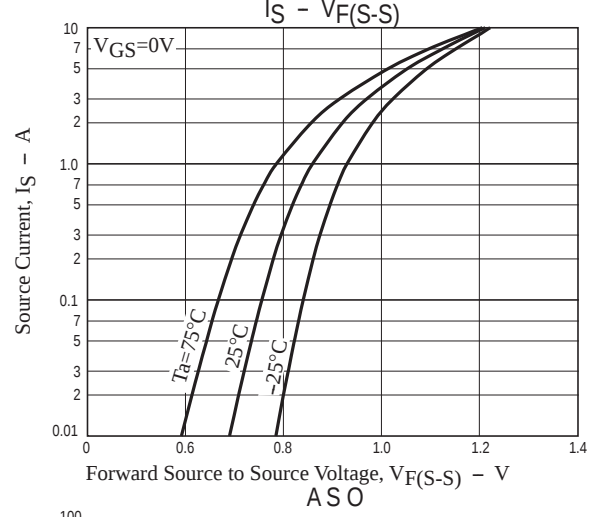
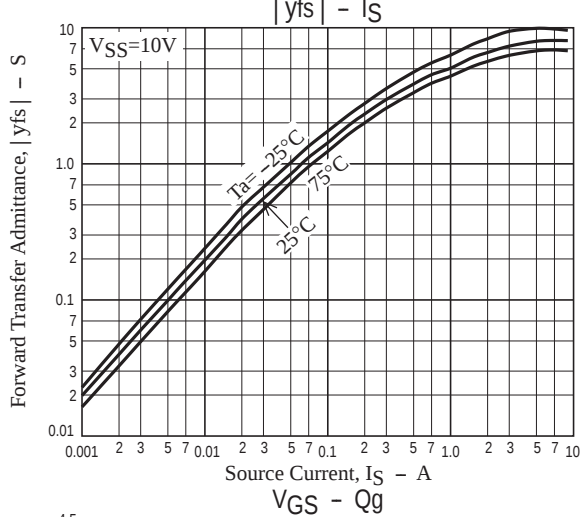
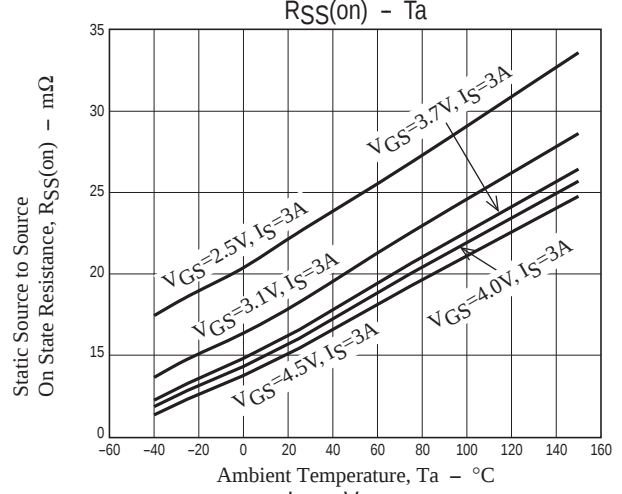
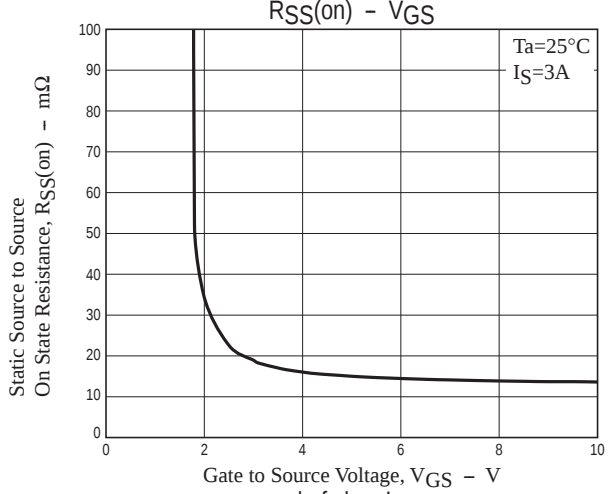
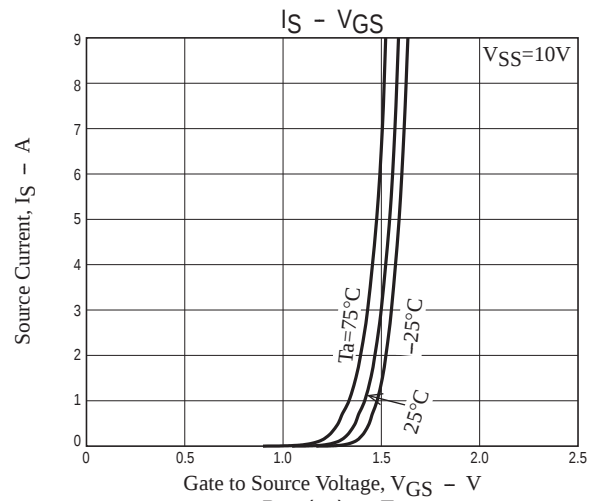
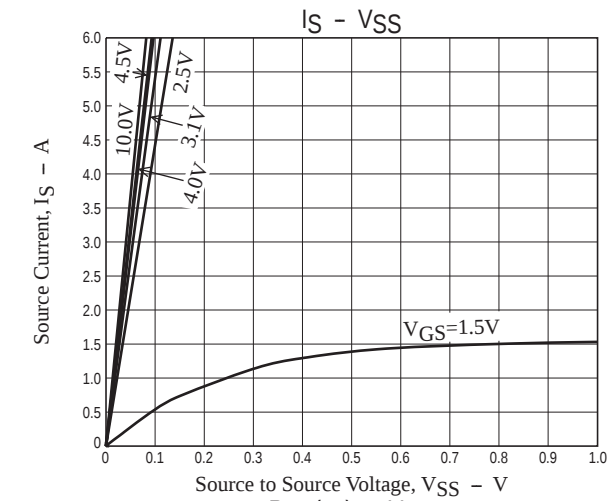
Test Circuit 7
 $t_d(on)$, t_r , $t_d(off)$, t_f

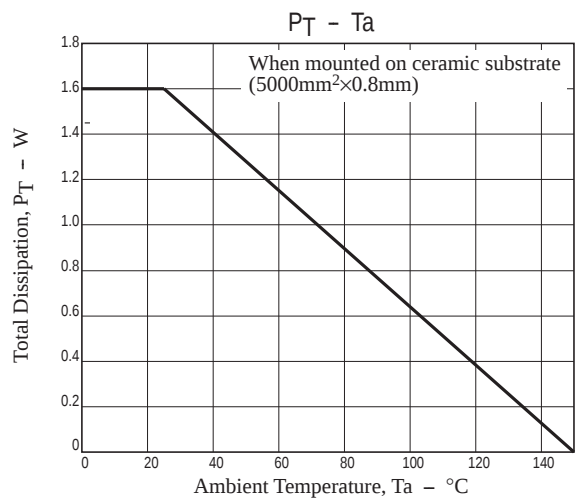


Test Circuit 8
 Q_g

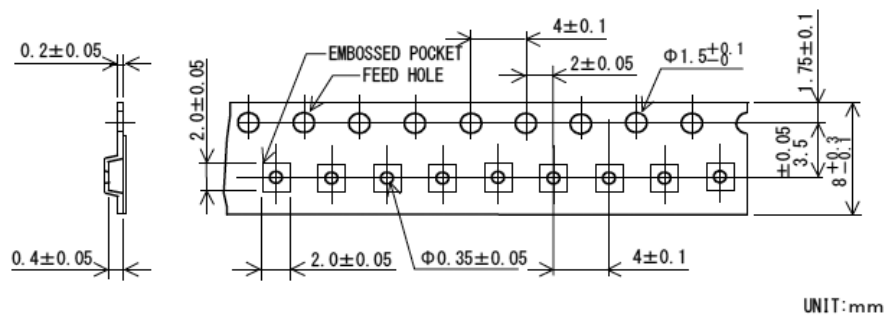


When FET1 is measured, Gate and Source of FET2 are short-circuited.





1- 1 .Carrier Tape Size (unit:mm)



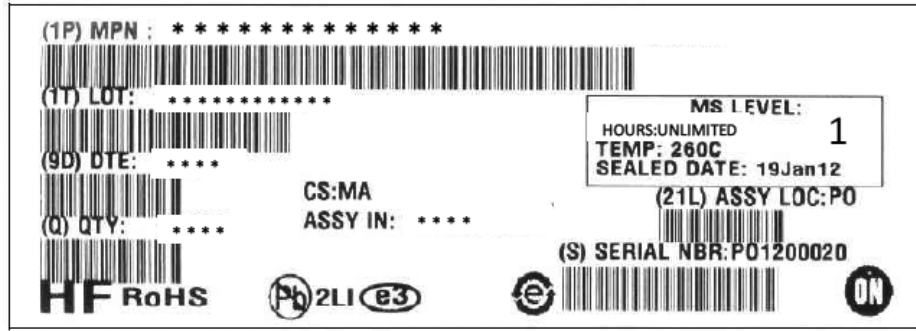
The diagram illustrates the layout of a winding tape. It starts at the 'Winding start' and ends at the 'Winding end'. The tape is divided into sections: a 'No Components' section (Min. 160), a 'Components' section (Min. 100), and a 'Top cover tape' section. The 'Components' section is further divided into 'No Components' (Min. 100) and 'Top cover tape' sections. The 'Direction of unreeling' is indicated by an arrow pointing right. The total length is Min. 400.

EFC4621R

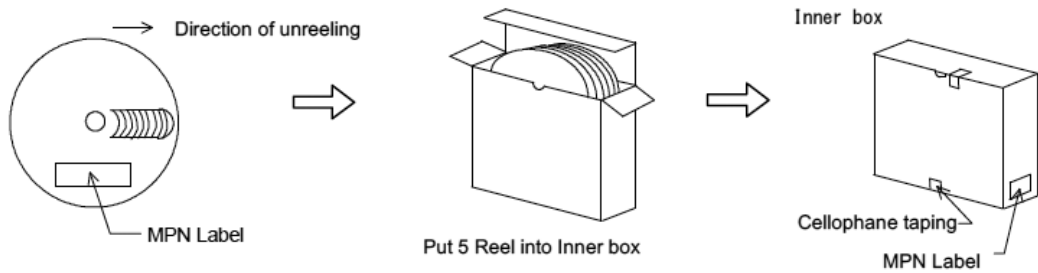
Packing Format

Carrier Tape code	Package code	Maximum Number of devices contained. (pcs.)			Packing Format	
		Reel	Inner box		Inner box BOX(C-1)	
2020X04	EFCP1818-4CE-022	5,000	25,000		5reels contained. Dimensions:mm 183×72×185	

MPN Label



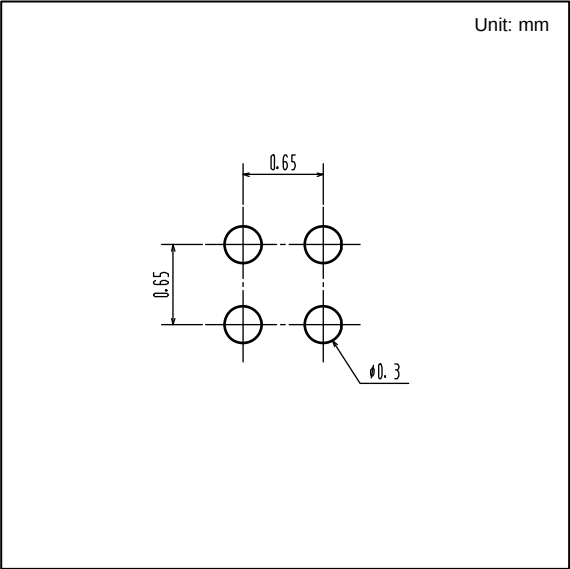
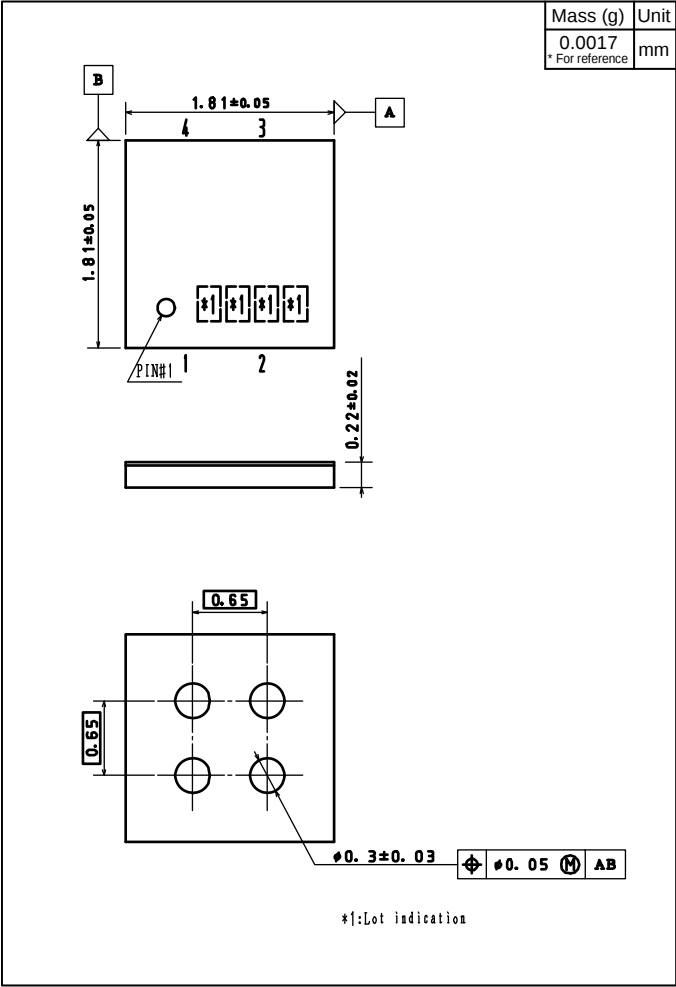
Packing Method



Outline Drawing

EFC4621R-TR

Land Pattern Example



Note on usage : Since the EFC4621R is a MOSFET product, please avoid using this device in the vicinity of highly charged objects.

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