SM5950BM

Asynchronous Sample Rate Converter

OVERVIEW

The SM5950BM is a digital audio signal asynchronous sample rate converter LSI. It supports 16/20/24-bit word-length input/output interface data. It also features a built-in digital deemphasis filter and direct mute functions.

FEATURES

Functions

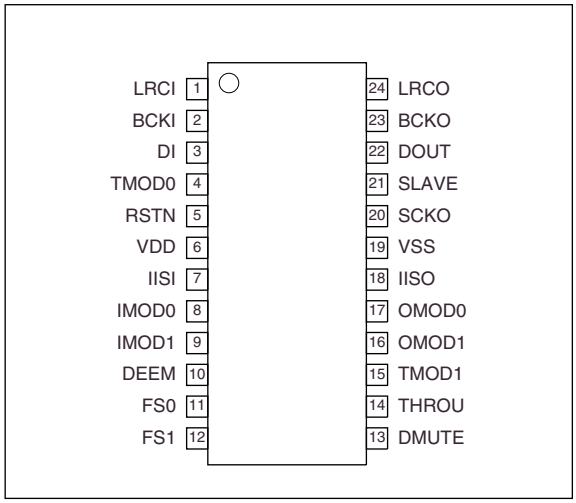
- L/R 2-channel (stereo) processing
- Input sample rate range: 20kHz to 100kHz
- Output sample rate range: 30kHz to 50kHz
- Operating sample rate conversion ratio (fso/fsi)[*1]
  : 0.45 to 2.205 selectable
  [*1]: fsi = input sample rate
  fso = output sample rate
- Asynchronous input and output clock timing
- System clock input
  - Input system clock: 1fsi (LRCI)
  - Output system clock: 512fso (SCKO input)
- Deemphasis filter function
  - IIR-type filter
  - fsi = 44.1kHz, 48kHz, 32kHz compatible
- Direct mute function
- Through mode operation
  - Direct connection from input to output
- Output data clocks (LRCO, BCKO)
  - Slave mode: external inputs
  - Master mode: derived from the output system clock (SCKO)
- Computation round-off processing
  - Normal round-off
- 5V tolerant input pins for direct connection to 5V operation devices
- 3.3V single supply
- Package: 24-pin SSOP

ORDERING INFORMATION

Device	Package
SM5950BM	24-pin SSOP

PINOUT

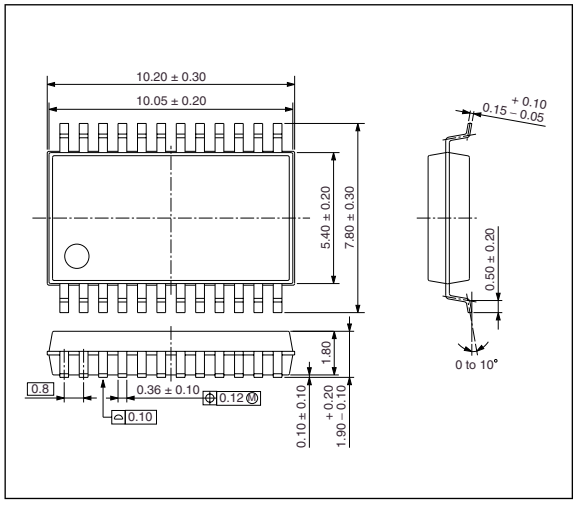
(Top view)



PACKAGE DIMENSIONS

(Unit: mm)

Weight: 0.23g



Note: Dimensions without tolerance are reference values.

FEATURES

Interfaces

- Input data format
  - 2s-complement, MSB-first, L/R alternating serial data
  - IIS/non-IIS formats

Format	IMOD0	IMOD1	IISI
16-bit MSB-first right-justified	L	L	L
20-bit MSB-first right-justified	H	L	L
24-bit MSB-first right-justified	L	H	L
MSB-first left-justified (leading 16 bits valid data)	H	H	L
IIS (leading 16 bits valid data)	H or L	H or L	H

L = Low input level, H = high input level

- Output data format
  - 2s-complement, MSB-first, L/R alternating serial data
  - Bit clock continuous (64fso)

Format	OMOD0	OMOD1	IISO
16-bit MSB-first right-justified	L	L	L
20-bit MSB-first right-justified	H	L	L
24-bit MSB-first right-justified	L	H	L
MSB-first left-justified (16-bit output)	H	H	L
IIS (16-bit output)	H or L	H or L	H

L = Low input level, H = high input level

Structure

- Silicon-gate CMOS process

Applications

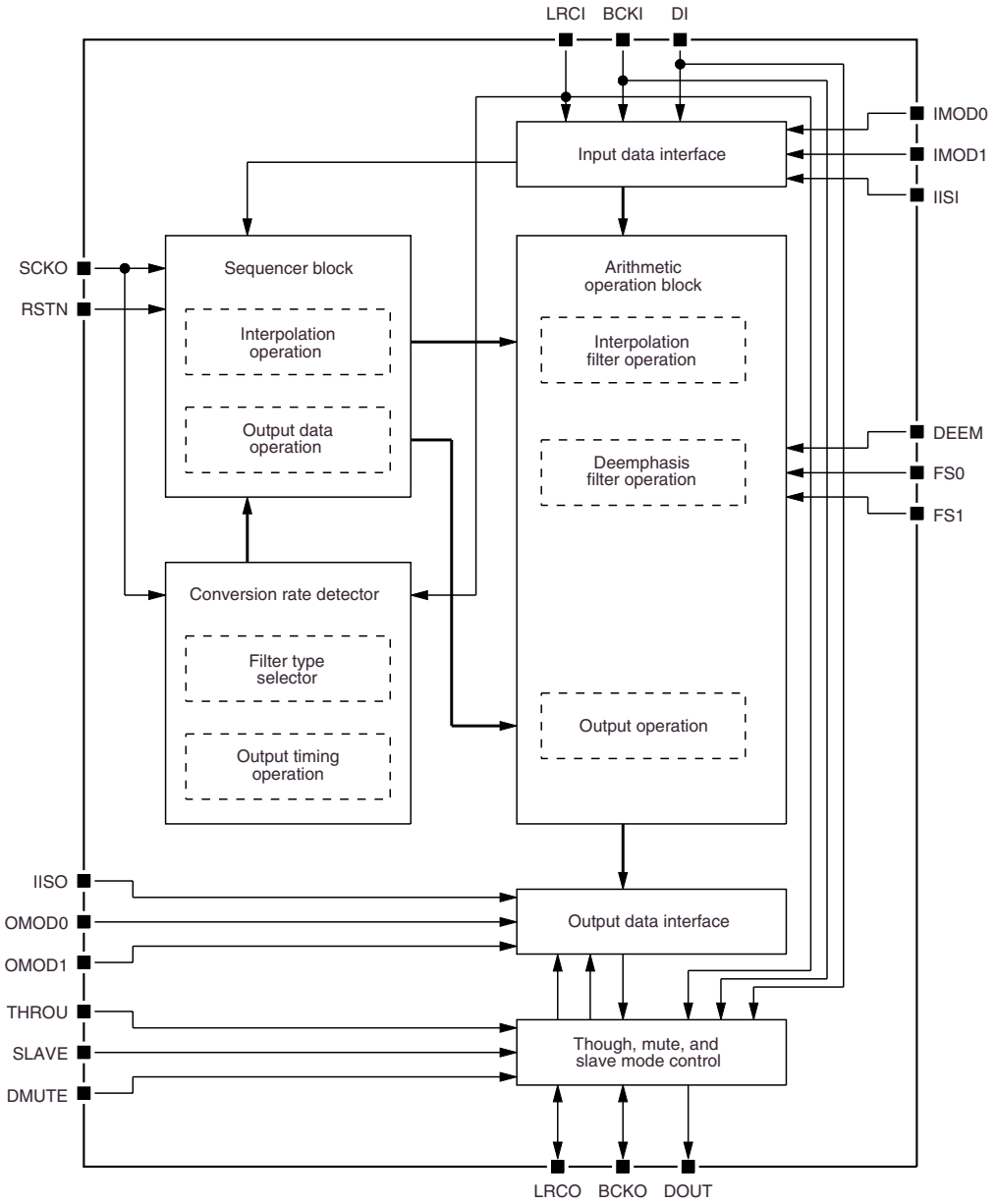
- Digital audio equipment-interface sample rate conversion (AV amplifier, CD-R/RW, DAT, MD, DVC)
- Recording/editing equipment sample rate conversion

Converter Performance

- Internal data word length: 20 bits
- Deemphasis filter characteristics (IIR filter)
  - ± 0.03dB gain deviation from ideal filter characteristic
- Anti-aliasing LPF characteristics (6 types of FIR filter)
  - Output/input sample rate conversion ratio automatic filter select (6 FIR filters)
    1.Up converter LPF
    1.0 to 2.205 times
    2.Down converter LPF I
    about 0.92 times: 48.0kHz to 44.1kHz
    3.Down converter LPF II
    about 0.73 times: 44.1kHz to 32.0kHz
    4.Down converter LPF III
    about 0.67 times: 48.0kHz to 32.0kHz
    5.Down converter LPF IV
    about 0.50 times: 96.0kHz to 48.0kHz
    6.Down converter LPF V
    about 0.45 times: 96.0kHz to 44.1kHz
    - Passband ripple: ± 0.0001dB
    - Stopband attenuation: > 98dB
- Converter insertion quantization noise level
  - Internal calculation (quantization) noise : ≤ – 96dB
  - Output round-off noise:
    - 16-bit output mode : – 98dB
    - 20-bit output mode : – 122dB
    - 24-bit output mode : – 146dB
  - Output S/N ratio (theoretical values)

Output signal word length	S/N ratio		
	16-bit input	20-bit input	24-bit input
16 bits	– 92.5dB	– 94.0dB	– 94.0dB
20 bits	– 93.9dB	– 96.2dB	– 96.2dB
24 bits	– 93.9dB	– 96.2dB	– 96.2dB

BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	I/O	Description	HIGH	LOW
1	LRCI	I	Sample rate clock input (fsi)	–	–
2	BCKI	I	Bit clock input (32fsi to 64fsi)	–	–
3	DI	I	Data input	–	–
4	TMOD0	I	IC test mode select pin (must be LOW for normal operation)	Test	Normal
5	RSTN	I	Reset pin	–	Reset
6	VDD	–	VDD supply (3.3V)	–	–
7	IISI	I	IIS input select pin	–	–
8	IMOD0	I	Input format select pin 0	–	–
9	IMOD1	I	Input format select pin 1	–	–
10	DEEM	I	Deemphasis select pin	ON	OFF
11	FS0	I	Deemphasis frequency select pin 0	–	–
12	FS1	I	Deemphasis frequency select pin 1	–	–
13	DMUTE	I	Direct mute select pin	ON	OFF
14	THROU	I	Through mode select pin	Through	SRC
15	TMOD1	I	IC test mode select pin (must be LOW for normal operation)	Test	Normal
16	OMOD1	I	Output format select pin 1	–	–
17	OMOD0	I	Output format select pin 0	–	–
18	IISO	I	IIS output select pin	–	–
19	VSS	–	GND connection (0V)	–	–
20	SCKO	I	Output system clock input (512fso)	–	–
21	SLAVE	I	Slave select pin	Slave	Master
22	DOUT	O	Data output	–	–
23	BCKO	I/O	Bit clock input/output (64fso)	–	–
24	LRCO	I/O	Sample rate clock input/output (fso)	–	–

SPECIFICATIONS

Absolute Maximum Ratings

V_{SS} = 0V, VDD pin voltage = V_{DD}

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	– 0.3 to 4.6	V
Input voltage range	V_I	– 0.3 to 5.5	V
Output voltage range	V_O	– 0.3 to V_{DD} + 0.3	V
Storage temperature range	T_{stg}	– 55 to 125	°C
Power dissipation	P_W	400	mW

Note: Ratings also apply at supply switch ON and OFF.

Recommended Operating Conditions

V_{SS} = 0V, VDD pin voltage = V_{DD}

Parameter	Symbol	Rating			Unit
		min	typ	max	
Supply voltage	V_{DD}	3.0	3.3	3.6	V
Operating temperature	T_{opr}	– 40	25	85	°C

DC Electrical Characteristics

V_{SS} = 0V, V_{DD} = 3.0 to 3.6V, Ta = –40 to 85°C

Parameter	Pin	Symbol	Condition	Rating			Unit
				min	typ	max	
Current consumption	VDD	I_{DD}	(*A)	–	22.0	30.0	mA
HIGH-level input voltage	(*1) (*3)	V_{IH}		2.0	–	5.5	V
LOW-level input voltage		V_{IL}		0	–	0.7	V
HIGH-level output voltage	(*2) (*3)	V_{OH}	I_{OH} = –2.0mA	2.4	–	V_{DD}	V
LOW-level output voltage		V_{OL}	I_{OL} = 2.0mA	0	–	0.4	V
Input leakage current	(*1) (*3)	I_{LH}	V_{IN} = V_{DD}	– 1.0	–	1.0	µA
		I_{LL}	V_{IN} = 0V	– 1.0	–	1.0	µA

(*A) All output pins with no load, System Clock frequency: F_{SCKO} = 24.576MHz, Input word clock frequency: F_{LRCI} = 48kHz, Supply voltage: V_{DD} = 3.3V

Pin type

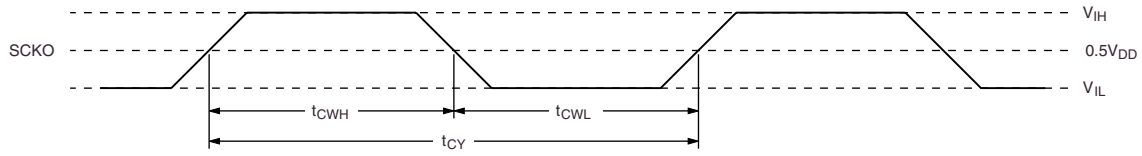
Note	Type	Names
(*1)	Inputs	LRCI, BCKI, DI, TMOD0, RSTN, IISI, IMOD0, IMOD1, DEEM, FS0, FS1, DMUTE, THROU, TMOD1, OMOD1, OMOD0, IISO, SCKO, SLAVE
(*2)	Output	DOUT
(*3)	Inputs/Outputs	BCKO, LRCO

Note. The input and input/output pins are all 5V tolerant. The maximum input voltage that can be applied to these pins are 5.5V. If supply voltage is within over the recommended operating voltage. If the input voltage is between 5.5V and VDD which is smaller than recommended operating voltage, the device doesn't breakdown itself, but it maybe generate reverse current from the input pins to the supply voltage (VDD). Note that input/output pins in input mode have a maximum input voltage of 5.5V, but the maximum voltage when in output mode is VDD level. In output mode, the output voltage must not be set, using external pull-up or other means, to voltages greater than VDD level. It is forbidden to add more voltage than VDD to output mode bidirectional pins.

AC Electrical Characteristics

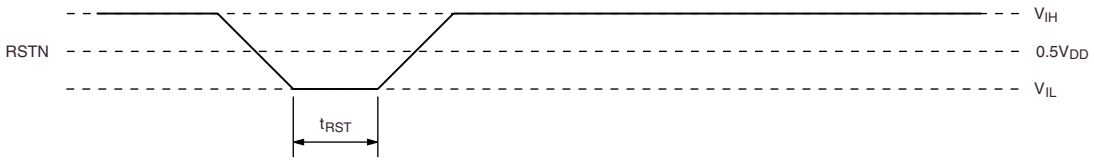
Output system clock (SCKO input)

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Clock pulse cycle time	t_{CY}		39.0	–	65.1	ns
Clock pulsewidth (HIGH level)	t_{CWH}		15.6	–	39.1	ns
Clock pulsewidth (LOW level)	t_{CWL}		15.6	–	39.1	ns
Clock pulse duty			40	–	60	%



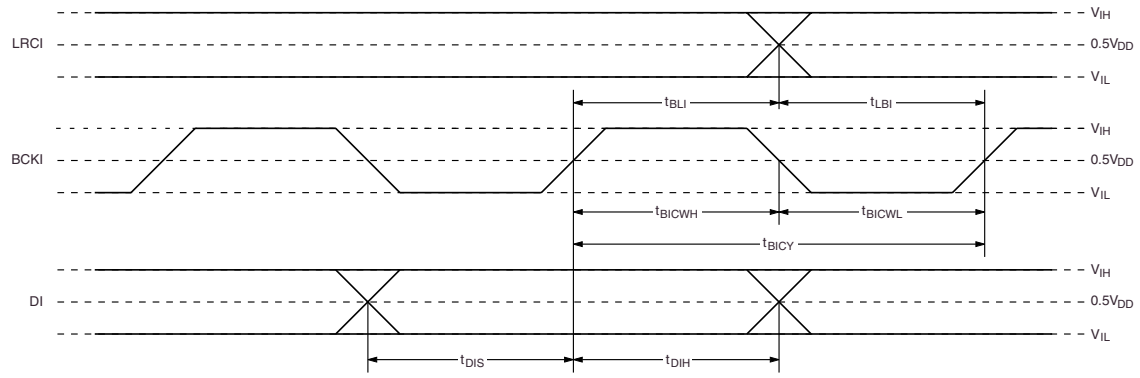
Reset input (RSTN)

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
RSTN pulsewidth	t_{RST}		39	–	–	ns



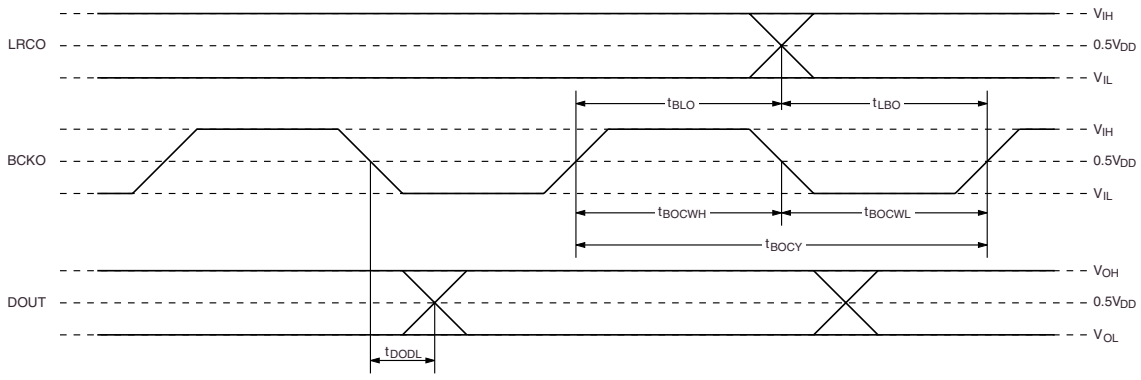
Serial inputs (LRCI, BCKI, DI)

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
LRCI cycle time	t_{LICY}		10	–	50	µs
BCKI pulse cycle time	t_{BICY}		156.25	–	1562.5	ns
BCKI pulsewidth (HIGH level)	t_{BICWH}		60	–	–	ns
BCKI pulsewidth (LOW level)	t_{BICWL}		60	–	–	ns
DI setup time	t_{DIS}		30	–	–	ns
DI hold time	t_{DIH}		30	–	–	ns
Last BCKI rising edge to LRCI edge	t_{BLI}		30	–	–	ns
LRCI edge to first BCKI rising edge	t_{LBI}		30	–	–	ns



Serial outputs (SLAVE = HIGH, LRCO, BCKO inputs, DOUT output)

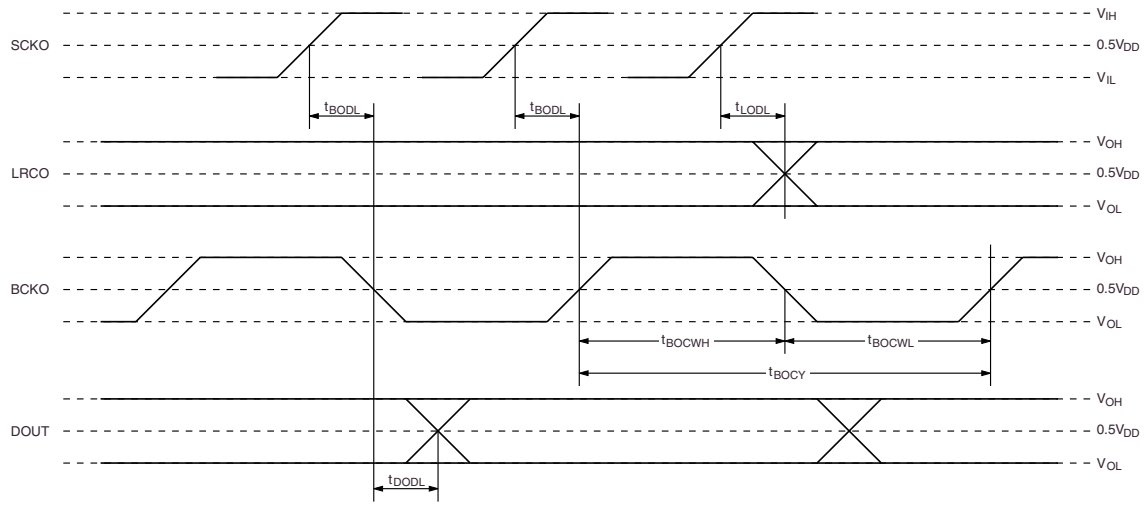
Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
LRCO cycle time	t_{LOCY}		20	–	33.34	µs
BCKO pulse cycle time	t_{BOCY}		312.5	–	520.8	ns
BCKO pulsewidth (HIGH level)	t_{BOCWH}		125	–	–	ns
BCKO pulsewidth (LOW level)	t_{BOCWL}		125	–	–	ns
Last BCKO rising edge to LRCO edge	t_{BLO}		30	–	–	ns
LRCO edge to first BCKO rising edge	t_{LBO}		30	–	–	ns
DOUT output delay	t_{DODL}	C_L = 15pF	–	–	30	ns



Serial outputs (SLAVE = LOW, LRCO, BCKO, DOUT outputs)

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
LRCO cycle time	t_{LOCY}		–	512	–	t_{CY}
LRCO pulsewidth (HIGH level)	t_{LOCWH}		–	256	–	t_{CY}
LRCO pulsewidth (LOW level)	t_{LOCWL}		–	256	–	t_{CY}
BCKO pulse cycle time	t_{BOCY}		–	8	–	t_{CY}
BCKO pulsewidth (HIGH level)	t_{BOCWH}		–	4	–	t_{CY}
BCKO pulsewidth (LOW level)	t_{BOCWL}		–	4	–	t_{CY}
BCKO output delay	t_{BODL}	C_L = 15pF	–	–	30	ns
LRCO output delay	t_{LODL}	C_L = 15pF	–	–	30	ns
DOUT output delay	t_{DODL}	C_L = 15pF	–	–	30	ns

t_{CY} = output system clock (SCKO input) cycle time



FUNCTIONAL DESCRIPTION

Input Interface Settings (IMOD0, IMOD1, IISI)

Input data format

2s-complement, MSB-first, L/R alternating serial data

IMOD0	IMOD1	IISI	Format
L	L	L	16-bit MSB-first right-justified
H	L	L	20-bit MSB-first right-justified
L	H	L	24-bit MSB-first right-justified
H	H	L	MSB-first left-justified (leading 16 bits valid data)
H or L	H or L	H	IIS (leading 16 bits valid data)

Note: L = Low input level, H = high input level

Input timing

The input timing for each input format is shown in figures 4 to 8.

Output System Clock (SCKO)

A clock with frequency 512 times the output sampling frequency (fso) must be input on SCKO. In master mode, the LRCO and BCKO output clocks are derived from the input clock on SCKO. It also functions as the internal computation circuit system clock.

Output Interface Settings (OMOD0, OMOD1, IISO, THROU, SLAVE)

Output data format

2s-complement, MSB-first, L/R alternating serial

OMOD0	OMOD1	IISO	Format
L	L	L	16-bit MSB-first right-justified
H	L	L	20-bit MSB-first right-justified
L	H	L	24-bit MSB-first right-justified
H	H	L	MSB-first left-justified (16-bit output)
H or L	H or L	H	IIS (16-bit output)

Note: L = Low input level, H = high input level

Output mode select

Pin setting		Function		
THROU	SLAVE	Mode	Description	LRCO, BCKO
L	L	Master	LRCO and BCKO are derived form SCKO.	Function as outputs
	H	Slave	LRCO and BCKO are supplied externally.	Function as inputs
H	H or L	Through	LRCO, BCKO, and DOUT are connected directly to LRCI, BCKI, and DI inputs. Note: DMUTE is valid.	Function as outputs

Output timing

The timing for each output format is shown in figures 9 to 13. In slave mode, the input timing of LRCO and BCKO for each output format is shown in figures 9 to 13. In through mode, the LRCI, BCKI, and DI inputs are fed through to the outputs regardless of the output data format settings.

System Reset (RSTN)

The SM5950BM must be reset if any of the following conditions occur during normal operation. A reset pulse is a LOW-level pulse applied to RSTN, although the reset operation actually occurs on the rising edge of the LOW-level pulse.

■ When the power supply is applied

A reset (RSTN = LOW to HIGH) is required when the power supply voltage is applied and after the LRCI, BCKI, SCKO (and LRCO, BCKO if in slave mode) clocks have stabilized.

■ When the LRCI and BCKI clocks are interrupted

This occurs when the sampling frequency is switched, when clocks stop due to a condition in a previous stage, when the LRCI, BCKI clocks are dynamically switched, or when otherwise the clocks are not continuous.
A reset (RSTN = LOW to HIGH) is required after the LRCI, BCKI clocks have stabilized.

■ When the SCKO (and LRCO, BCKO if in slave mode) clocks are interrupted

This occurs when the sampling frequency is switched, when clocks stop due to a condition in a previous stage, when the SCKO, LRCO, BCKO clocks are dynamically switched, or when otherwise the clocks are not continuous.
A reset (RSTN = LOW to HIGH) is required after the SCKO, LRCO, BCKO clocks have stabilized.

A reset pulse is required under these conditions because the conversion ratio calculated based on such non-continuous clocks will result in an incorrect conversion ratio, and hence the output data will have incorrect values.

Output state during reset interval

DOUT is tied LOW during the reset interval (refer to section "Direct Mute" for operation after the reset is released). In master mode, the LRCO and BCKO clocks are also tied LOW.

Direct Mute (DMUTE)

Direct mute ON/OFF

DMUTE	Function
L	Audio data output starts from the next output word.
H	0 data is output from the next output word.

Other mute operations

Direct mute also occurs at system reset.

RSTN	Function
L	0 data is output from the next output word.
H	Computed data output starts after 8 output word cycles.

Sample Rate Conversion

The input/output sample rate conversion ratio is variable over a range 0.45 to 2.205 times frequency. The input sample rate (fsi) range is 20kHz to 100kHz, while the output sample rate (fso) range is 30kHz to 50kHz. Note that the sample rate conversion ratio lower limit means that conversion from fsi = 96kHz to fso = 32kHz is not possible.

Anti-aliasing filter selection

The following 6 filters are provided to function as anti-aliasing filters during sample rate conversion, where the optimum anti-aliasing filter is automatically selected in response to the automatic measurement of the sample conversion ratio between the input sampling frequency (on LRCI) and the output sampling frequency (calculated using SCKO as reference).

Filter mode	fs conversion ratio (fso/fsi)	Selects range	Conversion frequency (example)
1	1.0 to 2.205 times	≥ 0.969697 times	Up conversion
2	0.91875 times	0.864865 to 0.969697 times	48.0 → 44.1
3	0.72562 times	0.711111 to 0.864865 times	44.1 → 32.0
4	0.66667 times	0.627451 to 0.711111 times	48.0 → 32.0
5	0.50000 times	0.492308 to 0.627451 times	96.0 → 48.0
6	0.459375 times	≤ 0.492308 times	96.0 → 44.1

If the selected anti-aliasing filter fs conversion ratio and the actual sample rate conversion ratio do not match, the following phenomena occur.

Conversion condition	Response generated
Actual sample rate conversion ratio is lower than the selected filter conversion ratio.	High-frequency aliasing noise occurs in the audio band.
Actual sample rate conversion ratio is higher than the selected filter conversion ratio.	Primarily cuts high-frequency components in the audio band.

If the fs conversion ratio is not fixed, the conversion will slowly follow the change in ratio, but in the process the possibility exists that noise may occur in the audio data output.

Conversion performance

- Internal data word length: 20 bits
- Gain deviation from deemphasis filter ideal characteristic: ± 0.03dB
- Anti-aliasing filter characteristic
  - Passband ripple: ± 0.0001dB
  - Stopband attenuation: > 98dB
- Conversion insertion quantization noise level
  - Internal computation noise: ≤ – 96dB
  - Output round-off noise: 16-bit output: – 98dB
    20-bit output: – 122dB
    24-bit output: – 146dB

Overall theoretical output S/N ratio

Output signal word length	S/N ratio		
	16-bit input	20-bit input	24-bit input
16 bits	– 92.5dB	– 94.0dB	– 94.0dB
20 bits	– 93.9dB	– 96.2dB	– 96.2dB
24 bits	– 93.9dB	– 96.2dB	– 96.2dB

Anti-aliasing filter characteristics

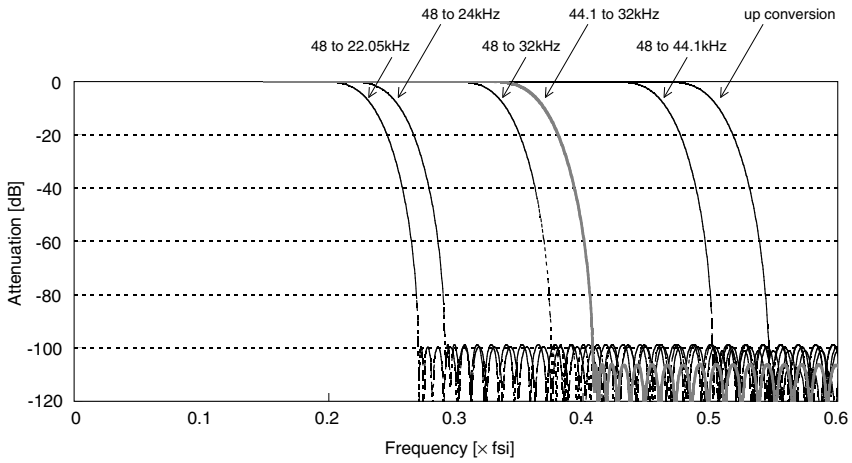


Figure 1. Anti-aliasing filter characteristics

Deemphasis (DEEM)

Basic deemphasis filters are realized using analog circuit configurations. Here, an IIR digital deemphasis filter configuration faithfully reproduces the gain and phase characteristics of an analog deemphasis filter. The filter coefficients are set by pins FS0 and FS1 for 3 input sampling frequencies (fsi) of 44.1kHz, 48.0kHz, and 32.0kHz.

Deemphasis ON/OFF

DEEM	Deemphasis
L	OFF
H	ON

Deemphasis filter coefficient selection

The deemphasis filter is selected by pins FS0 and FS1.

FS0	FS1	fsi
L	L	44.1kHz
H	L	44.1kHz
L	H	48.0kHz
H	H	32.0kHz

Deemphasis filter characteristics

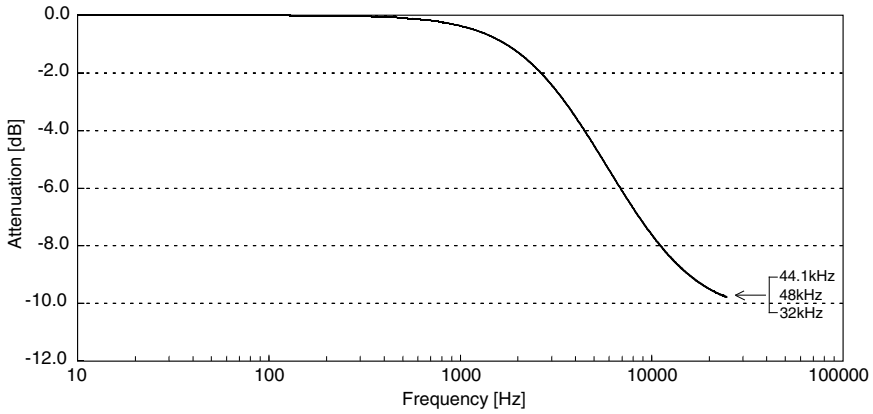


Figure 2. Deemphasis filter frequency characteristics

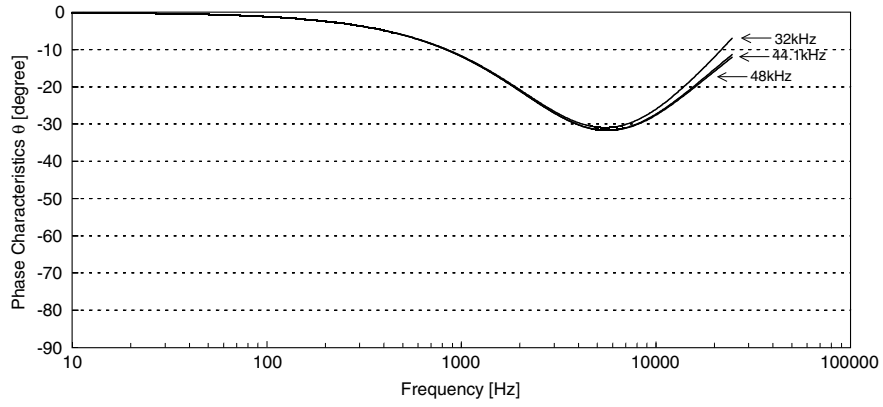


Figure 3. Deemphasis filter phase characteristics

Group Delay Time

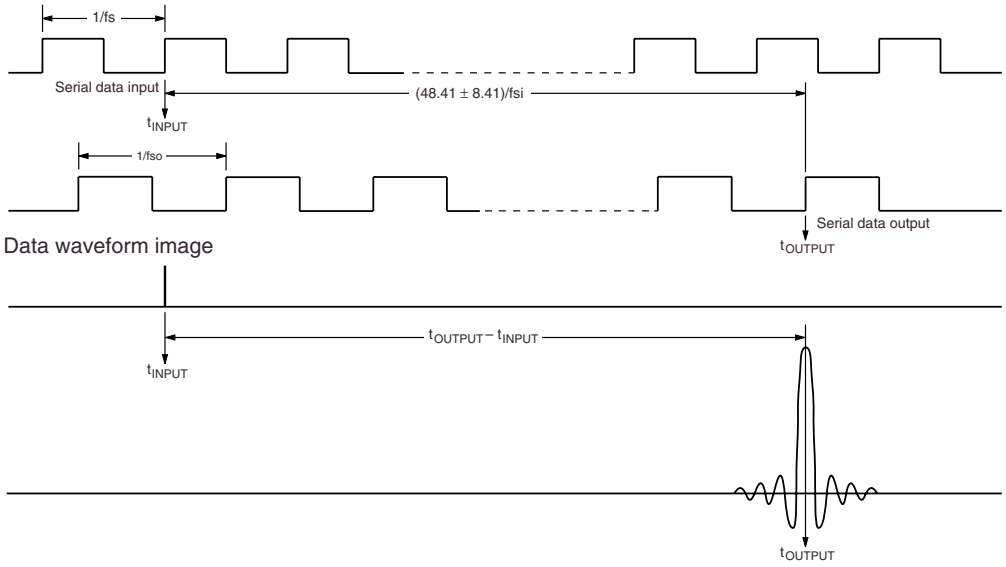
If t_{INPUT} and t_{OUTPUT} are defined as:

t_{INPUT} : Serial input data (fsi rate) read end timing (LRCI clock rising edge)

t_{OUTPUT} : Serial output data (fso rate) output start timing (LRCO clock rising edge)

the group delay is given by:

$t_{OUTPUT} - t_{INPUT} = (48.41 \pm 8.41)/fsi$



Response Time

The conversion rate detector stage requires a certain amount of time to calculate the sample rate conversion ratio with accuracy. The minimum response time, after the SM5950BM input sampling frequency (fsi: LRCI input) and output sampling frequency (fso: derived from SCKO) have stabilized sufficiently, is the time required to determine the sample rate conversion ratio to 16-bit accuracy after reset is cleared, and is given by:

Response time = 16384/fso (371ms at fso = 44.1kHz)

TIMING DIAGRAMS

Input Timing (LRCI, BCKI, DI)

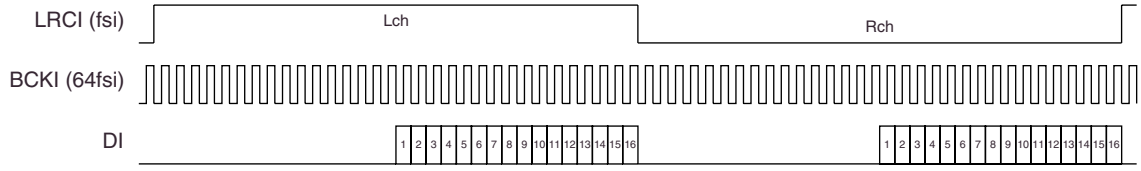


Figure 4. 16-bit MSB-first right-justified (IMOD0 = L, IMOD1 = L, IISI = L), BCKI = 32fsi to 64fsi

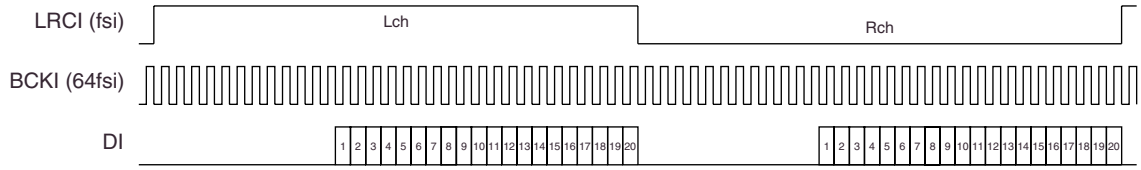


Figure 5. 20-bit MSB-first right-justified (IMOD0 = H, IMOD1 = L, IISI = L), BCKI = 40fsi to 64fsi

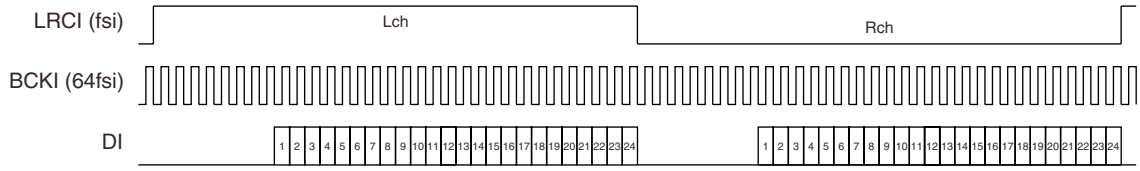


Figure 6. 24-bit MSB-first right-justified (IMOD0 = L, IMOD1 = H, IISI = L), BCKI = 48fsi to 64fsi

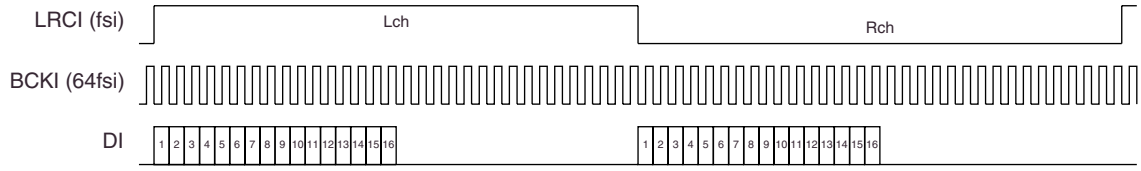


Figure 7. MSB-first left-justified, leading 16 data bits only are valid (IMOD0 = H, IMOD1 = H, IISI = L), BCKI = 32fsi to 64fsi

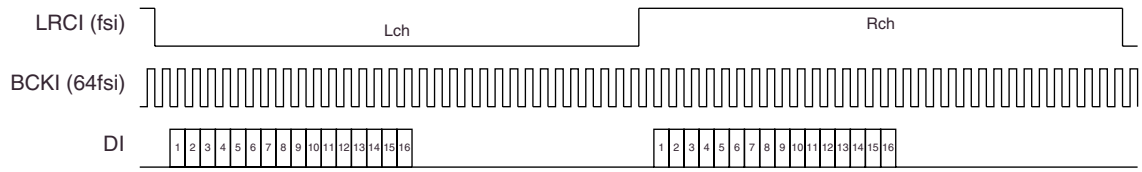


Figure 8. IIS, leading 16 data bits only are valid (IMOD0 = H, IMOD1 = H, IISI = H), BCKI = 64fsi only

Output Timing (LRCO, BCKO, DOUT)

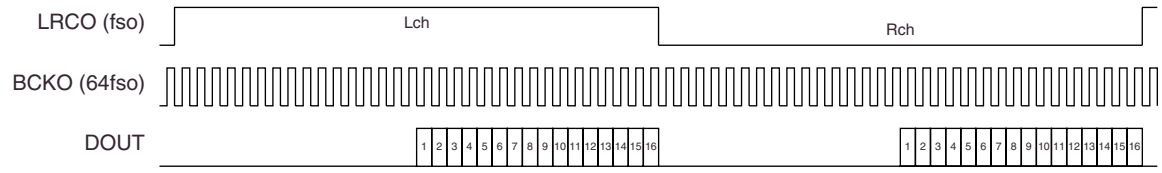


Figure 9. 16-bit MSB-first right-justified (OMOD0 = L, OMOD1 = L, IISO = L), BCKO = 64fso only

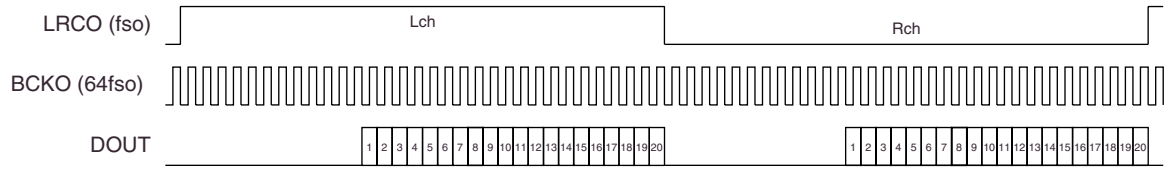


Figure 10. 20-bit MSB-first right-justified (OMOD0 = H, OMOD1 = L, IISO = L), BCKO = 64fso only

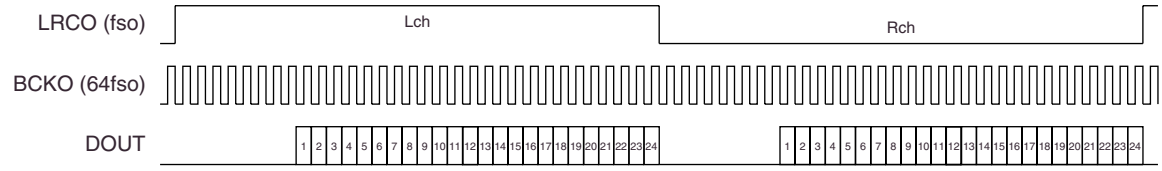


Figure 11. 24-bit MSB-first right-justified (OMOD0 = L, OMOD1 = H, IISO = L), BCKO = 64fso only

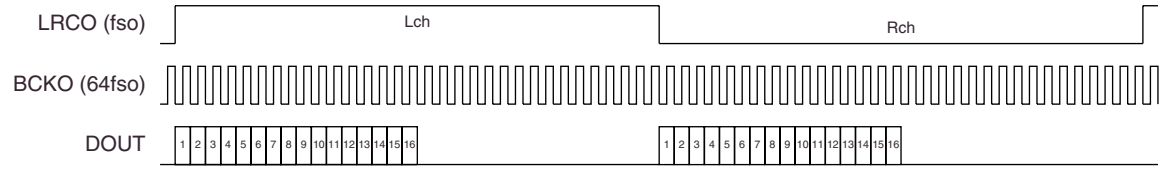


Figure 12. MSB-first left-justified, 16-bit output (OMOD0 = H, OMOD1 = H, IISO = L), BCKO = 64fso only

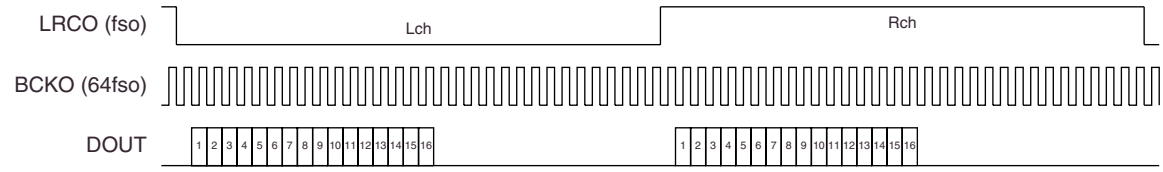
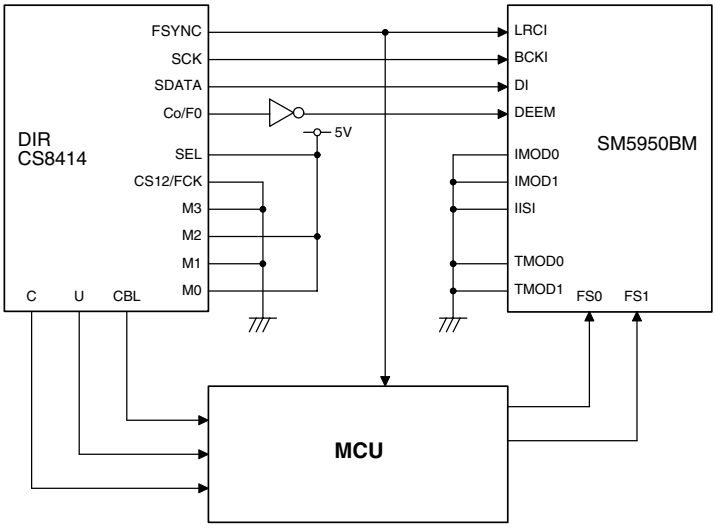


Figure 13. IIS, 16-bit output (OMOD0 = H, OMOD1 = H, IISO = H), BCKO = 64fso only

TYPICAL APPLICATION CIRCUITS

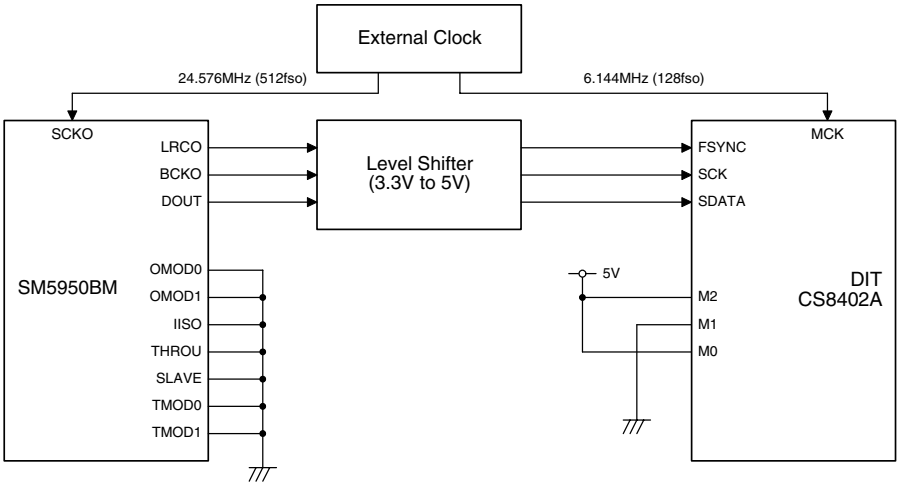
Input Interface Connection Example

Connection with a digital audio interface receiver (DIR:CS8414) example

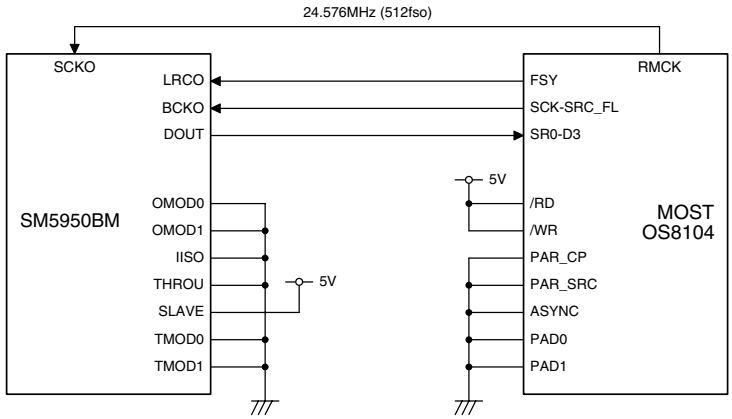


Output Interface Connection Example

Connection to a digital audio interface transceiver (DIT:CS8402A)



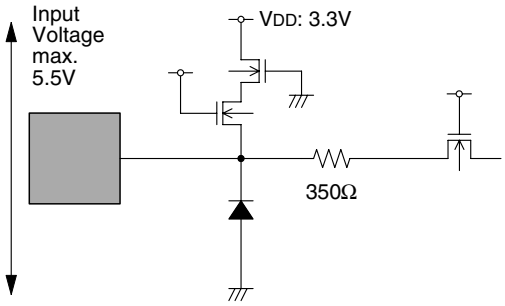
Connection to MOST Interface Transceiver (OS8104)



INPUT/OUTPUT PIN EQUIVALENT CIRCUITS

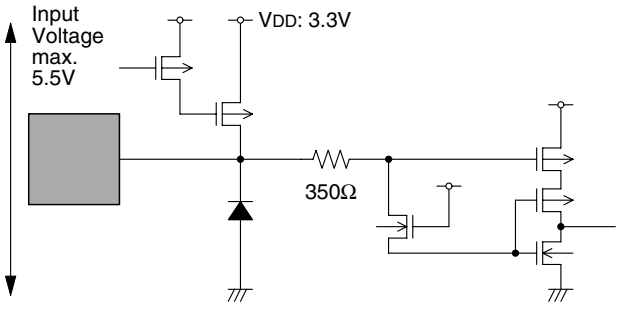
Input Pin Circuit – TYPE1

Pin name (Number): LRCI (1), BCKI (2), DI (3), TMOD0 (4), RSTN (5), IISI (7), IMOD0 (8), IMOD1 (9), DEEM (10), FS0 (11), TMOD1 (15), SCKO (20), SLAVE (21)



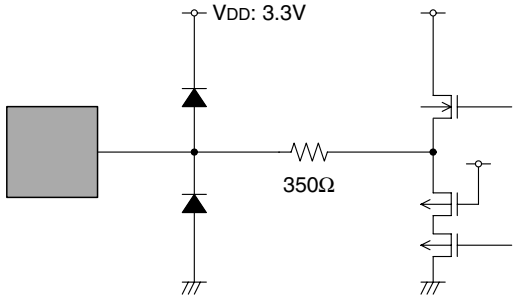
Input Pin Circuit – TYPE2

Pin name (Number): FS1 (12), DMUTE (13), OMOD1 (16), OMOD0 (17), IISO (18)



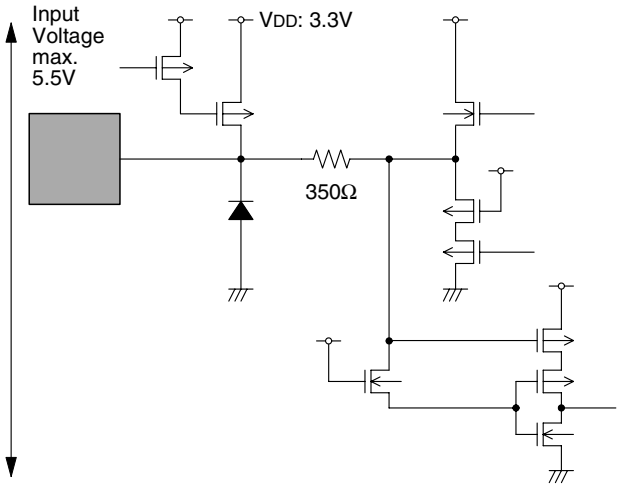
Output Pin Circuit

Pin name (Number): DOUT (22)



Input/Output Pin Circuit

Pin name (Number): BCKO (23), LRCO (24)



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