Product Specification

PE3512

1500 MHz Low Power UltraCMOS™ Divide-by-4 Prescaler

Product Description

The PE3512 is a high-performance static UltraCMOS™ prescaler with a fixed divide ratio of 4. Its operating frequency range is DC to 1500 MHz. The PE3512 operates on a nominal 3 V supply and draws only 8 mA. The input and output interfaces support both AC-coupled, low-Z RF as well as direct connection to low voltage positive logic devices. It is packaged in a small 6-lead SC-70 and is ideal for frequency scaling solutions

The PE3512 is manufactured in Peregrine's patented Ultra Thin Silicon (UTSi©) CMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Features

- DC to 1500 MHz operation
- Fixed divide ratio of 4
- Low-power consumption: 8 mA typical @ 3V
- RF or LV Digital Interface
- Ultra-small package: 6-lead SC-70

Figure 1. Functional Schematic Diagram

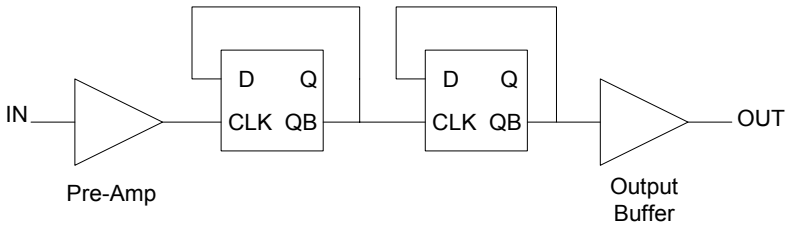


Figure 2. Package Type

6-lead SC70

Table 1. Electrical Specifications ($Z_S = Z_L = 50\ \Omega$)

V_{DD} = 3.0 V, -40° C ≤ T_A ≤ 85° C, unless otherwise specified

Parameter	Conditions	Minimum	Typical	Maximum	Units
Supply Voltage		2.85	3.0	3.15	V
Supply Current			8	12	mA
Input Frequency (F_{in})		DC		1500	MHz
Input Power (P_{in})	DC < Fin ≤ 1000 MHz	-10		+10	dBm
	1000 MHz < Fin ≤ 1500	-3			dBm
Output Power (P_{out})	DC < Fin ≤ 1500 MHz	2			dBm

©2005 Peregrine Semiconductor Corp. All rights reserved.

Table 2. DC Electrical Characteristics (-40° C ≤ T_A ≤ 85° C)

Symbol	Parameter	Condition	Typical	Unit
V_{IH}	High Level Input Voltage	2.7 V ≤ V_{DD} ≤ 3.3 V	2.0	V
V_{IL}	Low Level Input Voltage	2.7 V ≤ V_{DD} ≤ 3.3 V	0.8	V
V_{OH}	High Level Output Voltage	V_{DD} = 2.7 V; I_{OH} = 2.9 mA	2.2	V
V_{OL}	Low Level Output Voltage	V_{DD} = 2.7 V; I_{OL} = 2.6 mA	0.4	V

Table 3. AC Characteristics (-40° C ≤ T_A ≤ 85° C)

Symbol	Parameter	Condition*	Typical	Unit
t_{PHL}	Propagation Delay (High to Low)	50 MHz Pulse Train Input; C_L = 10 pF, R_L = 500 Ω	3.0	ns
t_{PLH}	Propagation Delay (Low to High)	50 MHz Pulse Train Input; C_L = 10 pF, R_L = 500 Ω	3.2	ns
t_r	Output Rise Time (10% to 90%)	50 MHz Pulse Train Input; C_L = 10 pF, R_L = 500 Ω	2.0	ns
t_f	Output Fall Time (90% to 10%)	50 MHz Pulse Train Input; C_L = 10 pF, R_L = 500 Ω	2.0	ns

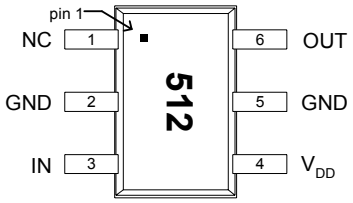
** See figure 5 for AC test circuit*

Table 4. Typical Output Swing (V_{DD} = 2.7 V)

Frequency	Condition	Typical	Unit
50 MHz	200 mVp-p Sinusoidal Input; C_L = 10 pF, R_L = 500 Ω	2.3	Vp-p
500 MHz	200 mVp-p Sinusoidal Input; C_L = 10 pF, R_L = 500 Ω	2.2	Vp-p
1500 MHz	200 mVp-p Sinusoidal Input; C_L = 10 pF, R_L = 500 Ω	1.7	Vp-p

©2005 Peregrine Semiconductor Corp. All rights reserved.

Figure 3. Pin Configuration (Top View)



SC-70

Table 5. Pin Descriptions

Pin No.	Pin Name	Description
1	N/C	No Connect. This pin should be left open.
2	GND	Ground pin. Ground pattern on the board should be as wide as possible to reduce
3	IN	Input signal pin. DC blocking capacitor
4	V_{DD}	Power supply pin. Bypassing is required.
5	GND	Ground pin.
6	OUT	Divided frequency output pin. DC blocking

Table 6. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Supply voltage		4.0	V
Pin	Input Power		13	dBm
T_{ST}	Storage temperature	-65	150	°C
T_{OP}	Operating temperature	-40	85	°C
V_{ESD}	ESD voltage (Human		2000	V

Absolute Maximum Ratings are those values listed in the above table. Exceeding these values may cause permanent device damage. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in Table 6.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Device Functional Considerations

The *PE3512* divides an input signal, up to a frequency of 1500 MHz, by a factor of four thereby producing an output frequency at one-fourth the input frequency. To work properly with low impedance, ground referenced interfaces, the input and output signals (pins 3 & 6) must be AC coupled via an external capacitor, as shown in the test circuit in Figure 4.

The ground pattern on the board should be made as wide as possible to minimize ground impedance. See Figure 9 for a layout example.

©2005 Peregrine Semiconductor Corp. All rights reserved.

Figure 4. Test Circuit Block Diagram

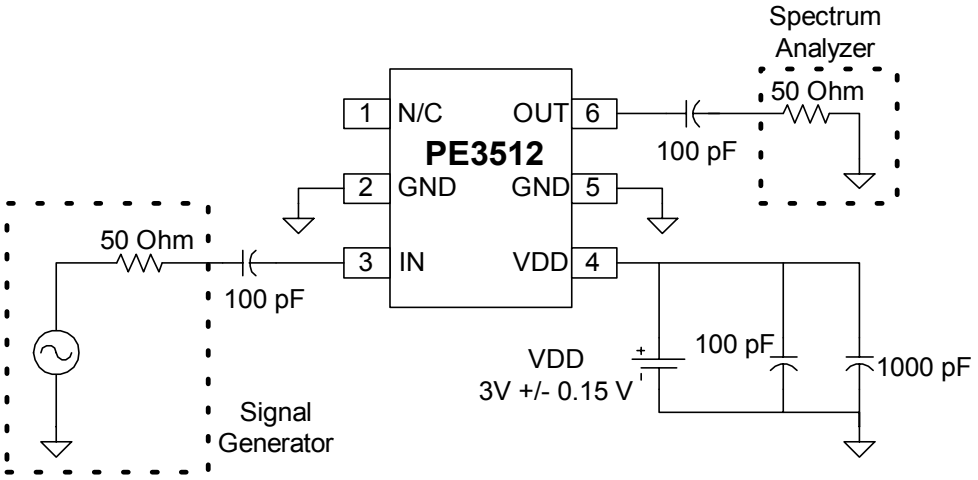
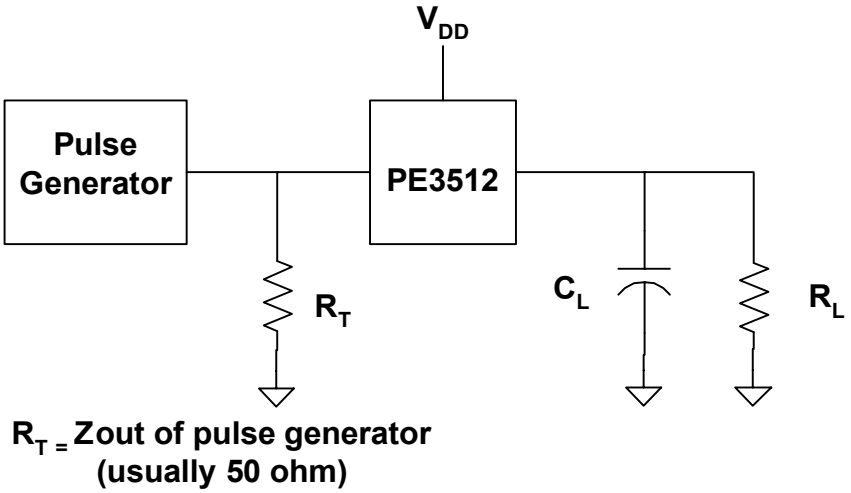


Figure 5. AC Test Circuit



©2005 Peregrine Semiconductor Corp. All rights reserved.

Typical Performance Data: V_{DD} = 3.0 V

Figure 6. Input Sensitivity

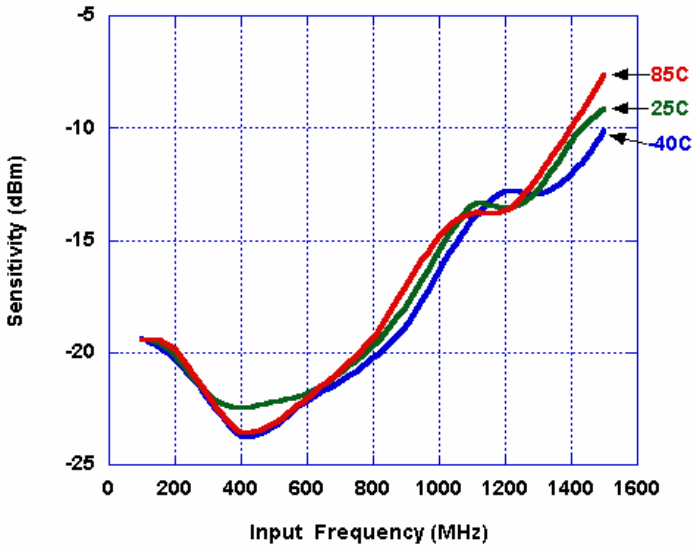


Figure 7. Device Current

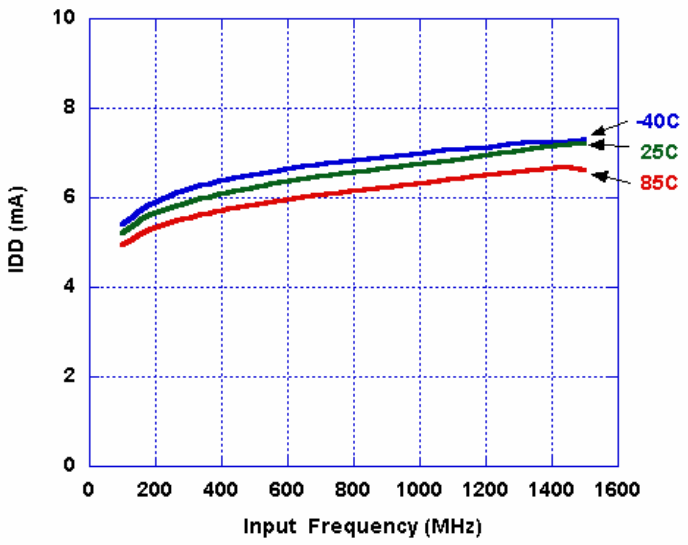
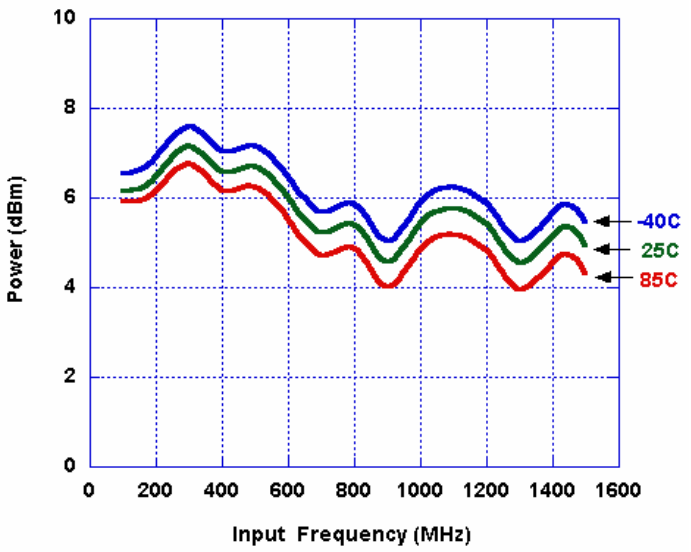


Figure 8. Output Power



©2005 Peregrine Semiconductor Corp. All rights reserved.

Evaluation Kit

Evaluation Kit Operation

The SC-70 Prescaler Evaluation Board was designed to help customers evaluate the *PE3512* divide-by-4 prescaler. On this board, the device input (pin 3) is connected to connector J1 through a 50 Ω transmission line. A series capacitor (C1) provides the necessary DC block for the device input. A value of 100 pF was used for this board layout; other applications may require a different value.

The device output (pin 6) is connected to J3 through a 50 Ω transmission line. A series capacitor (C5) provides the necessary DC block for the device output. This capacitor value must be chosen to have a low impedance at the desired output frequency of the device. A value of 100 pF was chosen for the evaluation board. At both input and output, select a capacitor value that offers low series reactance while ensuring that any parasitic resonances are well above the operating bandwidth.

The board is constructed of a two-layer FR4 material with a total thickness of 0.031". The bottom layer provides ground for the RF transmission lines. The transmission lines were designed using a coplanar waveguide above ground plane model with trace width of 0.030", trace gaps of 0.007", dielectric thickness of 0.028", metal thickness of 0.0014", and ε_r of 4.4. Note that the predominate mode of these transmission lines is coplanar waveguide. Liberal numbers of plated through holes unite the top and bottom ground areas for best performance.

J6 provides DC power to the device via pin 4. Two decoupling capacitors (100 pF, 1000 pF) are included on this trace. It is the customer's responsibility to determine proper supply decoupling for their design application.

Applications Support

If you have a problem with your evaluation kit or if you have applications questions call (858) 731-9400 and ask for applications support. You may also contact us by fax or e-mail:
Fax: (858) 731-9499
E-Mail: help@psemi.com

Figure 9. Evaluation Board Layouts
Peregrine Specification 101/0110

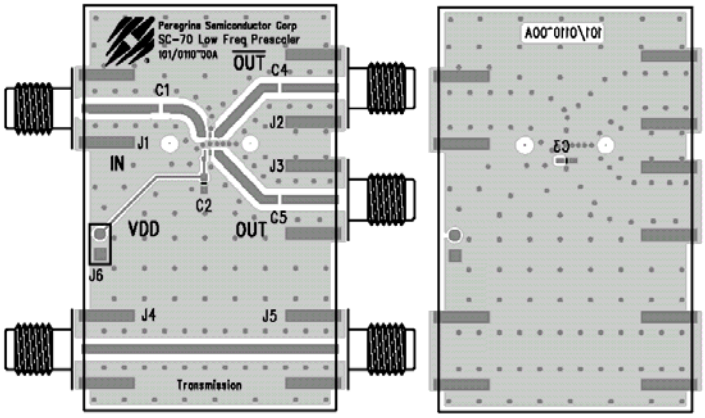
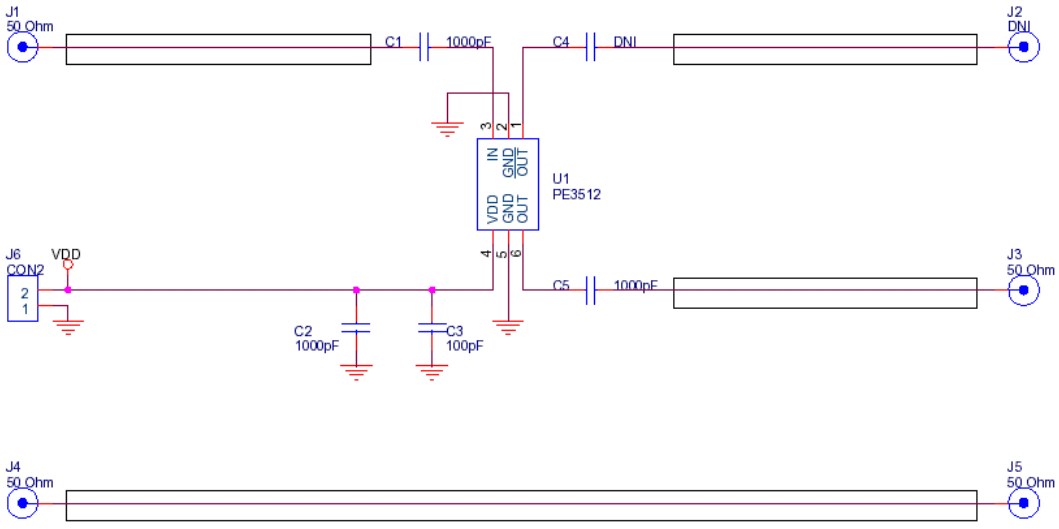


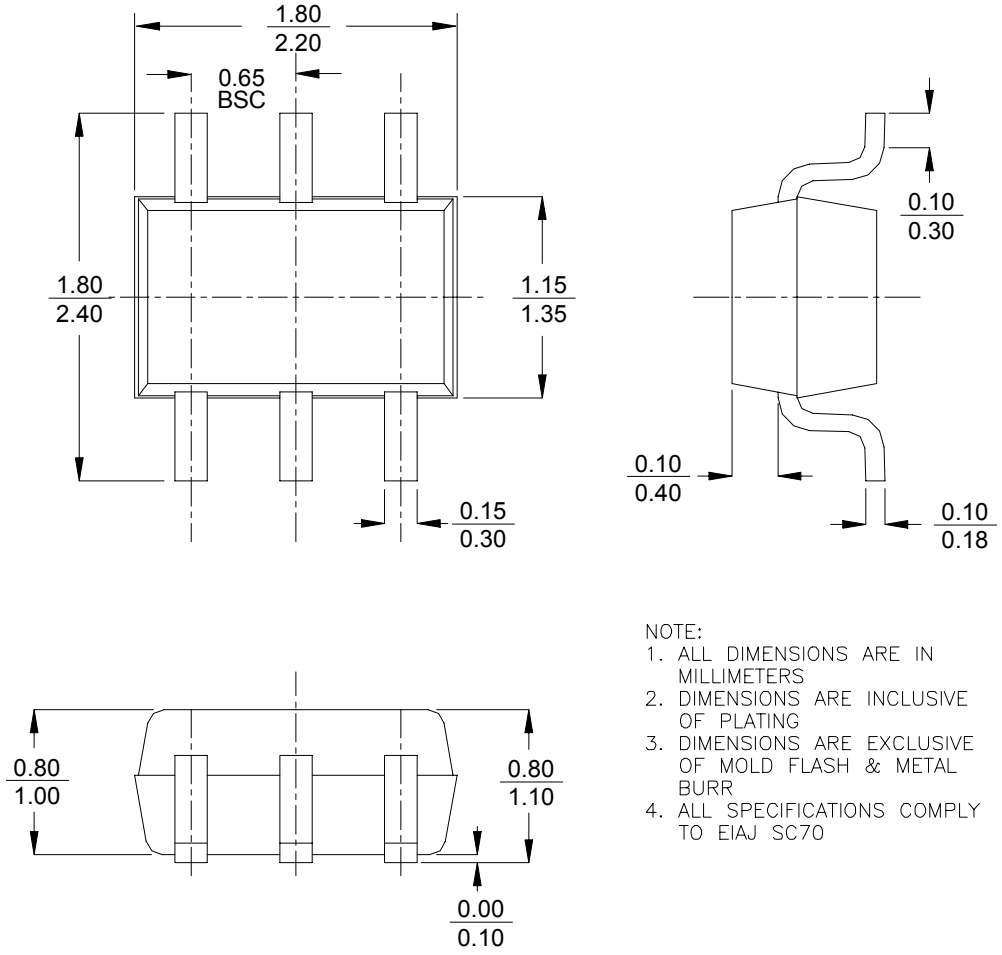
Figure 10. Evaluation Board Schematic
Peregrine Specification 102/0190



©2005 Peregrine Semiconductor Corp. All rights reserved.

Figure 11. Package Drawing

6-lead SC-70



NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS
2. DIMENSIONS ARE INCLUSIVE OF PLATING
3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH & METAL BURR
4. ALL SPECIFICATIONS COMPLY TO EIAJ SC70

Table 7. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
3512-01	512	PE3512-06SC70-7680A	6-lead SC-70	7680 units / Canister
3512-02	512	PE3512-06SC70-3000C	6-lead SC-70	3000 units / T&R
3512-00	PE3512-EK	PE3512-06SC70-EK	Evaluation Kit	1 / Box
3512-51	512	PE3512G-06SC70-7680A	Green 6-lead SC-70	7680 units / Canister
3512-52	512	PE3512G-06SC70-3000C	Green 6-lead SC-70	3000 units / T&R

©2005 Peregrine Semiconductor Corp. All rights reserved.

Sales Offices

The Americas

Peregrine Semiconductor Corp.
9450 Carroll Park Drive
San Diego, CA 92121
Tel 858-731-9400
Fax 858-731-9499

Europe

Peregrine Semiconductor Europe
Commercial Products:
Bâtiment Maine
13-15 rue des Quatre Vents
F- 92380 Garches, France
Tel: +33-1-47-41-91-73
Fax : +33-1-47-41-91-73
Space and Defense Products:
180 Rue Jean de Guiramand
13852 Aix-En-Provence cedex 3, France
Tel: +33(0) 4 4239 3361
Fax: +33(0) 4 4239 7227

North Asia Pacific

Peregrine Semiconductor K.K.
5A-5, 5F Imperial Tower
1-1-1 Uchisaiwaicho, Chiyoda-ku
Tokyo 100-0011 Japan
Tel: +81-3-3502-5211
Fax: +81-3-3502-5213

South Asia Pacific

Peregrine Semiconductor
28G, Times Square,
No. 500 Zhangyang Road,
Shanghai, 200122, P.R. China
Tel: +86-21-5836-8276
Fax: +86-21-5836-7652

For a list of representatives in your area, please refer to our Web site at: ***www.psemi.com***

Data Sheet Identification

Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The data sheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a DCN (Document Change Notice).

The information in this data sheet is believed to be reliable. However, Peregrine assumes no liability for the use of this information. Use shall be entirely at the user's own risk.

No patent rights or licenses to any circuits described in this data sheet are implied or granted to any third party.

Peregrine's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the Peregrine product could create a situation in which personal injury or death might occur. Peregrine assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.

The Peregrine name, logo, and UTSi are registered trademarks and UltraCMOS is a trademark of Peregrine Semiconductor Corp.

©2005 Peregrine Semiconductor Corp. All rights reserved.