To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS

MOS FIELD EFFECT TRANSISTOR

μPA1857

N-CHANNEL MOS FIELD EFFECT TRANSISTOR FOR SWITCHING

DESCRIPTION

The μPA1857 features a low on-state resistance and excellent switching characteristics, and is suitable for applications such as power switch of portable machine and so on.

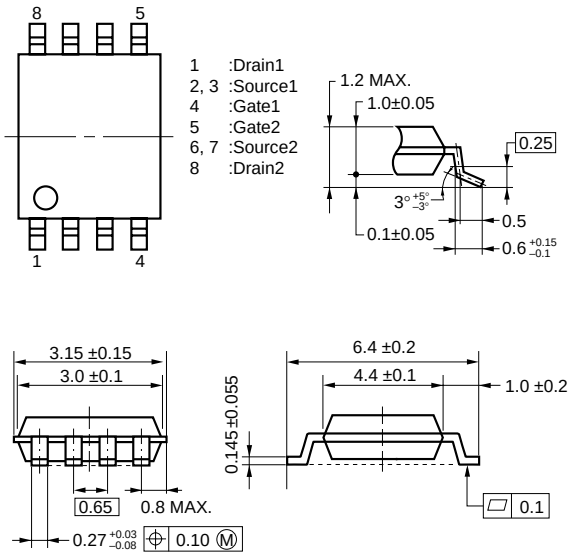
FEATURES

- Low on-state resistance
  $R_{DS(on)1}$ = 67.0 mΩ MAX. (V_{GS} = 10 V, I_D = 2.0 A)
  $R_{DS(on)2}$ = 86.0 mΩ MAX. (V_{GS} = 4.5 V, I_D = 2.0 A)
  $R_{DS(on)3}$ = 95.0 mΩ MAX. (V_{GS} = 4.0 V, I_D = 2.0 A)
- Low C_{iss} C_{iss} = 580 pF TYP.
- Built-in G-S protection diode against ESD

ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA1857GR-9JG	Power TSSOP8

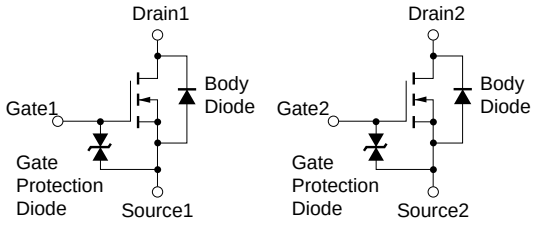
PACKAGE DRAWING (Unit: mm)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	60	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC) (T_A = 25°C)	$I_{D(DC)}$	±3.8	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	±15.2	A
Total Power Dissipation (1unit) Note2	P_{T1}	1.0	W
Total Power Dissipation (2unit) Note2	P_{T2}	1.7	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C
Single Avalanche Current Note3	I_{AS}	3.8	A
Single Avalanche Energy Note3	E_{AS}	33	mJ

EQUIVALENT CIRCUIT



Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. T_A = 25°C Mounted on ceramic substrate of 50 cm^2 x 1.1 mm

3. Starting T_{ch} = 25°C, V_{DD} = 30 V, R_G = 25 Ω, V_{GS} = 20 → 0 V

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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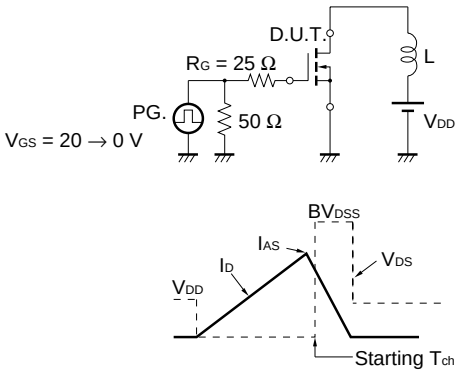
The mark ★ shows major revised points.

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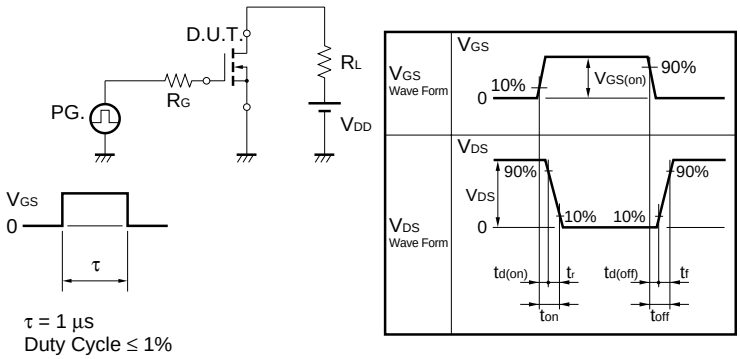
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V			10	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±10	μA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = 10 V, I_D = 2.0 A	2.5	5.4		S
Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 2.0 A		53	67.0	mΩ
	$R_{DS(on)2}$	V_{GS} = 4.5 V, I_D = 2.0 A		64	86.0	mΩ
	$R_{DS(on)3}$	V_{GS} = 4.0 V, I_D = 2.0 A		71	95.0	mΩ
Input Capacitance	C_{iss}	V_{DS} = 10 V		580		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		100		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		50		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 30 V, I_D = 2.0 A		10		ns
Rise Time	t_r	V_{GS} = 10 V		9		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 6 Ω		32		ns
Fall Time	t_f			4		ns
Total Gate Charge	Q_G	V_{DD} = 48 V		12		nC
Gate to Source Charge	Q_{GS}	V_{GS} = 10 V		2		nC
Gate to Drain Charge	Q_{GD}	I_D = 3.8 A		3		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 3.8 A, V_{GS} = 0 V		0.80		V
Reverse Recovery Time	t_{rr}	I_F = 3.8 A, V_{GS} = 0 V		33		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		58		nC

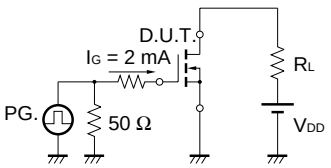
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

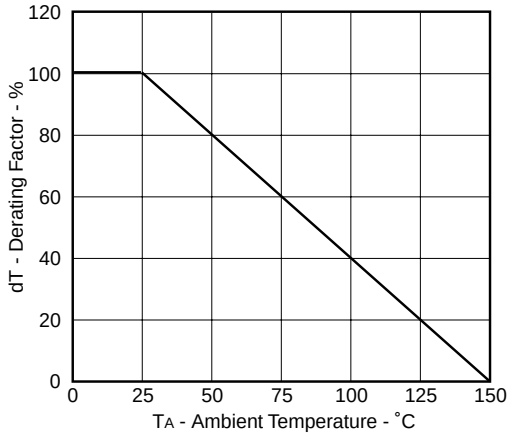


TEST CIRCUIT 3 GATE CHARGE

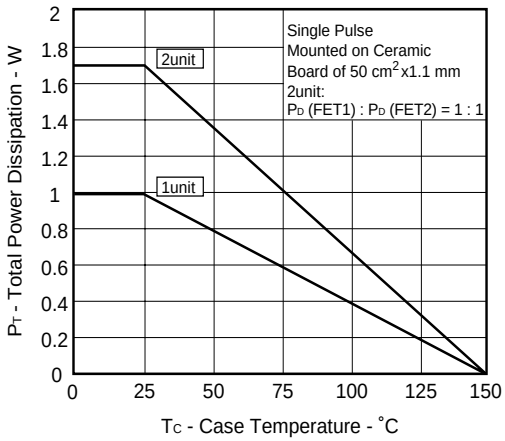


TYPICAL CHARACTERISTICS (T_A = 25°C)

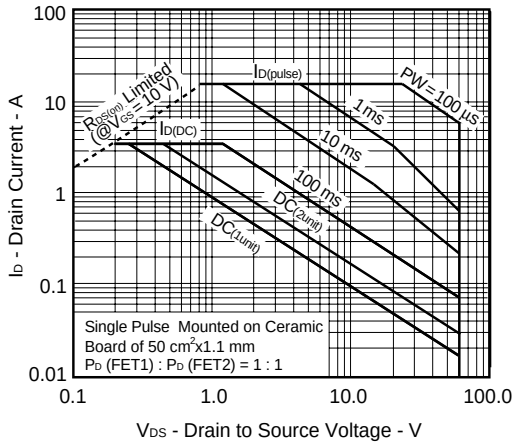
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



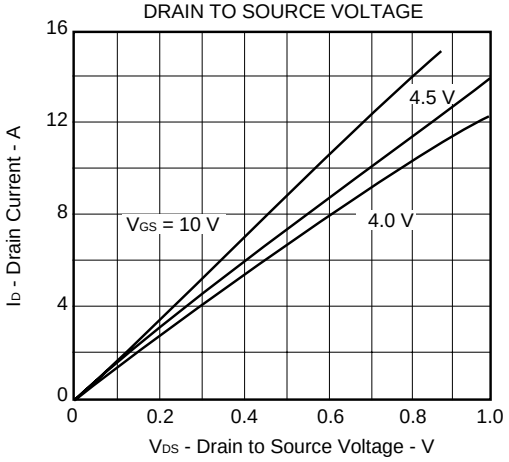
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



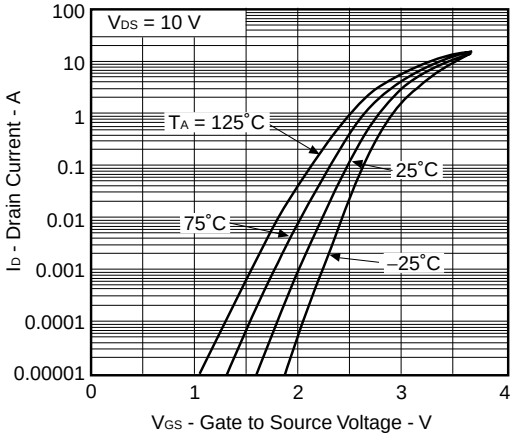
★ FORWARD BIAS SAFE OPERATING AREA



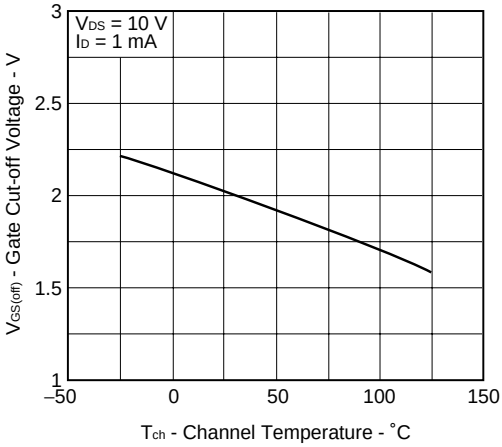
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



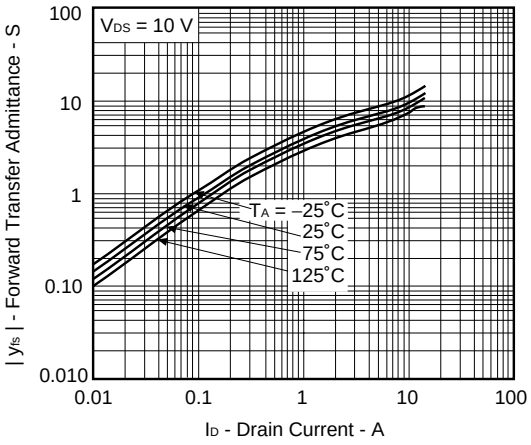
FORWARD TRANSFER CHARACTERISTICS



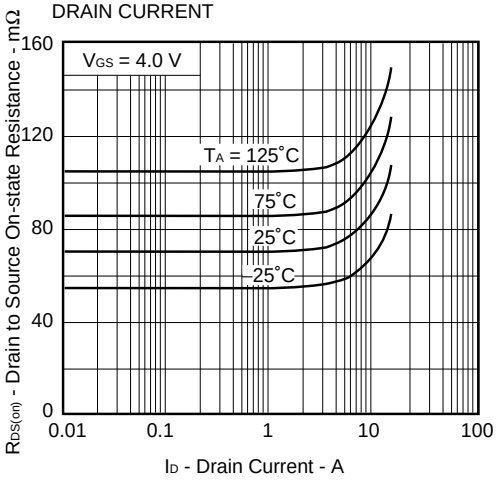
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



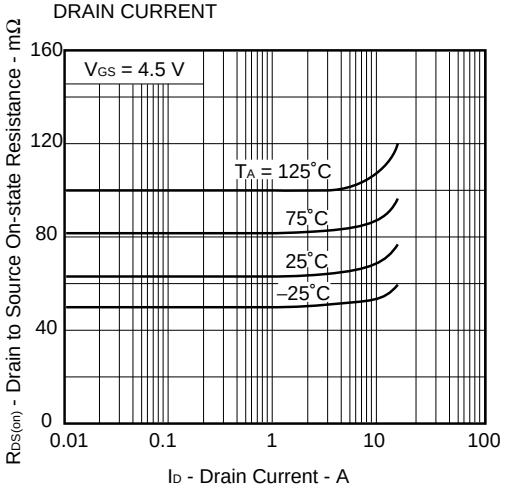
FORWARD TRANSFER ADMITTANCE Vs. DRAIN CURRENT



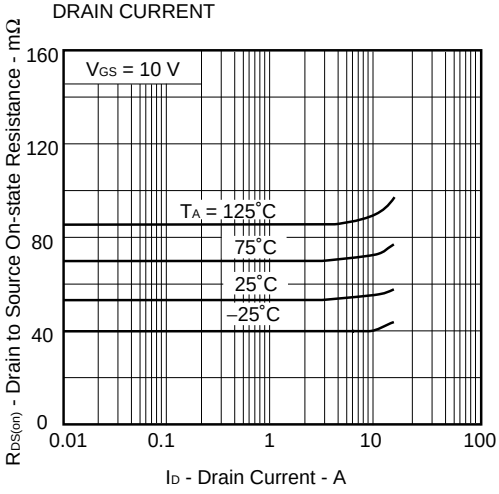
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



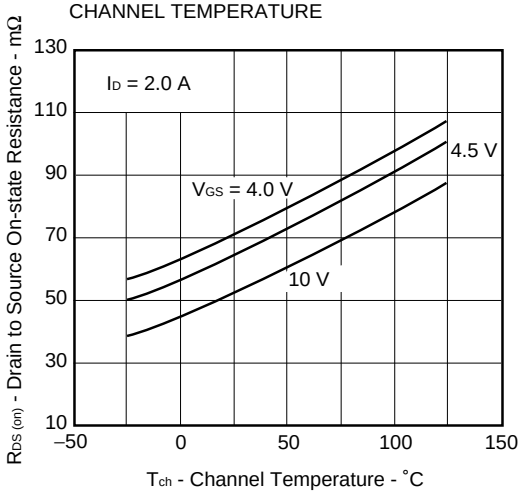
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



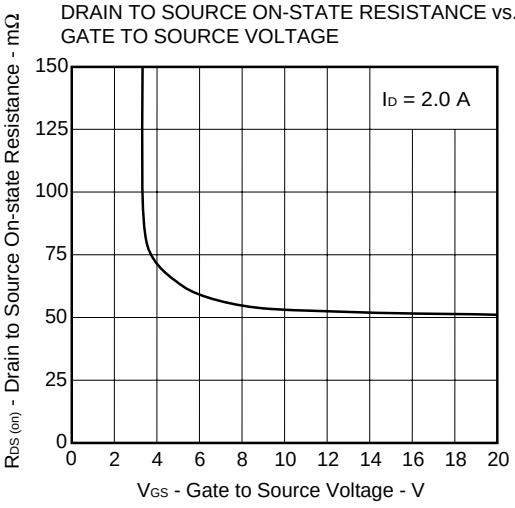
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



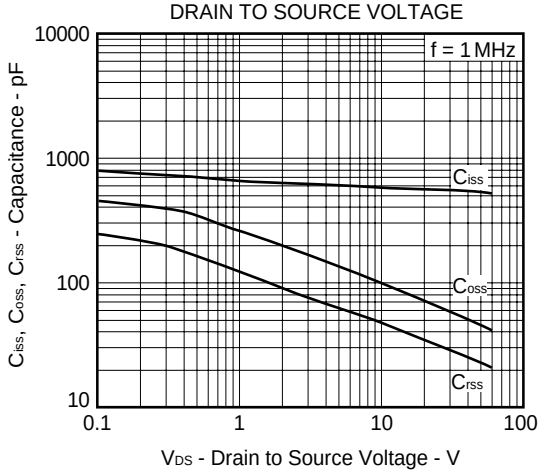
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



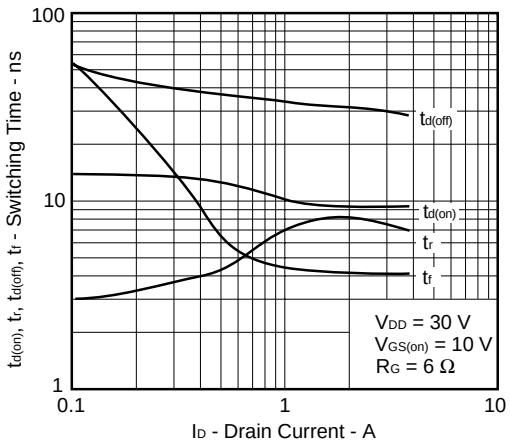
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



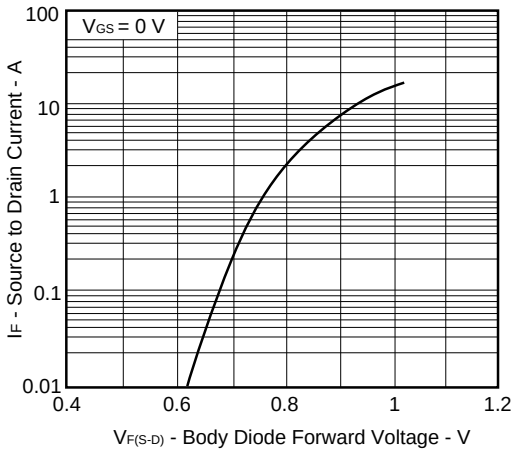
CAPACITANCE vs.
DRAIN TO SOURCE VOLTAGE



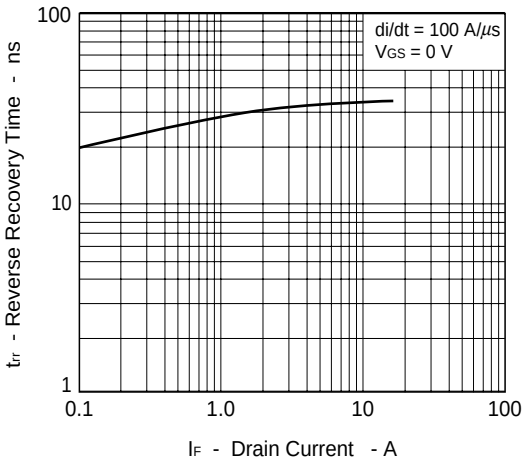
SWITCHING CHARACTERISTICS



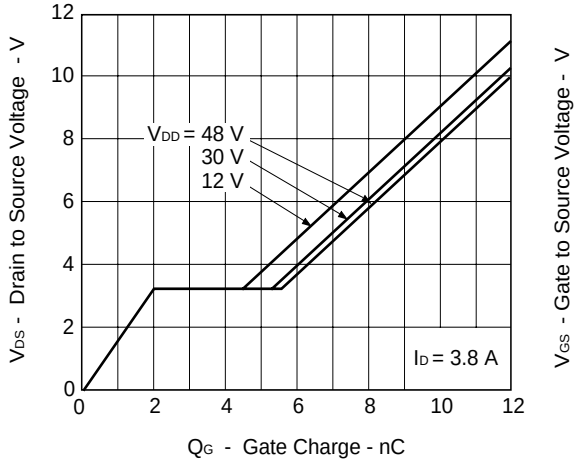
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



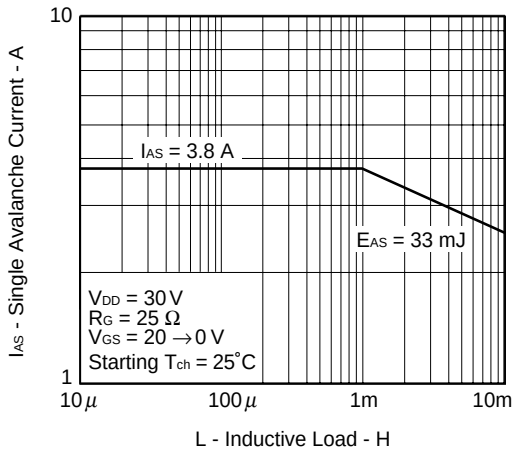
REVERSE RECOVERY TIME vs.
DRAIN CURRENT



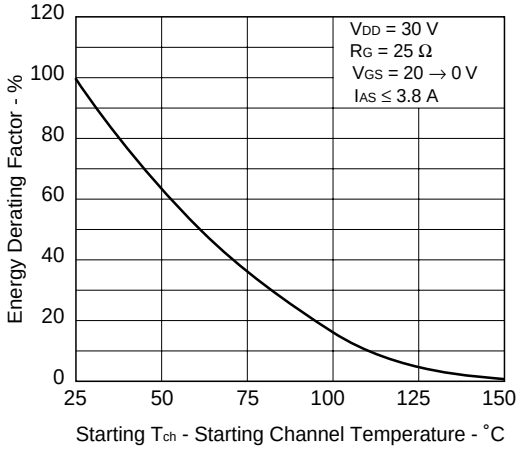
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



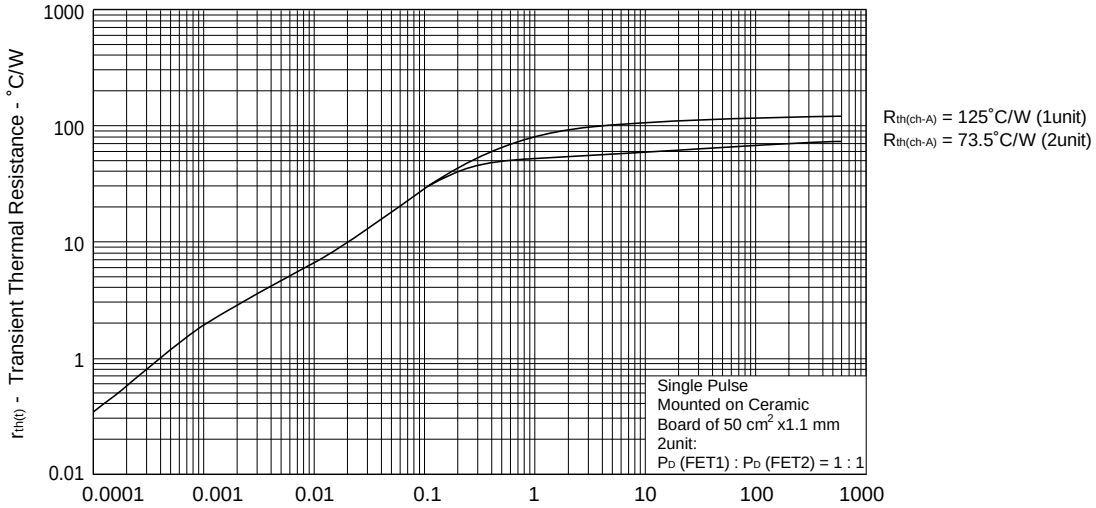
SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY DERATING FACTOR



★ TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



[MEMO]

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