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1. GENERAL DESCRIPTION

The N567HP330 is an advanced 8-ch Melody IC with 8Mbit embedded OTP. It combines with the technology of 8-bit 65C02 core and new 4-bit or 5-bit MDPCM synthesizer to implement sophisticated applications in high level of sound quality.

The N567HP330 provides 32 I/O pins, 384 bytes RAM, IR carrier, and Serial Interface Management (SIM) for various interactive toys or cartridge applications. It contains 6 LED output pins with 64-level control for the application of motor control or LED fading. In addition, N567HP330 provides high quality PWM mode audio output to save power during playback. It also built in internal oscillation to save component cost and control the system frequency in a precise range. Furthermore, N567HP330 provides Watch Dog Timer and Low Voltage Reset to prevent latch-up situation occurring as power bouncing or vibration.

The N567HP330 build in 8Mbit OTP to cover the families of N567G (4-ch), N567K (6-ch) and N567H (8-ch).

2. FEATURES

- Wide range of operating voltage:
  - 8 MHz @ 3.0 volt ~ 5.5 volt
  - 6 MHz @ 2.4 volt ~ 5.5 volt
- Oscillator
  - Internal Oscillator (TRIM)
    - System clock setting: 4096KHz, 6144KHz, and 8192KHz
  - X'tal Oscillator
    - External Crystal: 8MHz~16MHz for system clock 4M~8MHz
- Power management:
  - Stop mode for stopping all IC operations
    - Status changes of the IP0 and BP0~BP2 pins can wake up the chip
- Provides up to 8 inputs and 24 I/O pins
- Audio output: 1 speaker output
  - DAC mode: Typical current output 3mA or 5mA, Resolution 10+3 bits, without Noise Shaping
  - PWM: Direct drive speaker with12-bit resolution. Support Noise Shaping.
- F/W Speech synthesis:
  - Multiple formats
    - New 4-bit MDPCM (NM4), 5-bit MDPCM (MDM), 4-bit MDPCM (MD4), 4-bit ADPCM (APM), 8-bit Log PCM (LP8)
    - Pitch shift ADPCM for voice changer application
  - Dual sample rate in voice synthesis
- F/W Melody synthesis:
  - 8 melody channels that can emulate characteristics of musical instruments
  - Multi-MIDI files simultaneous

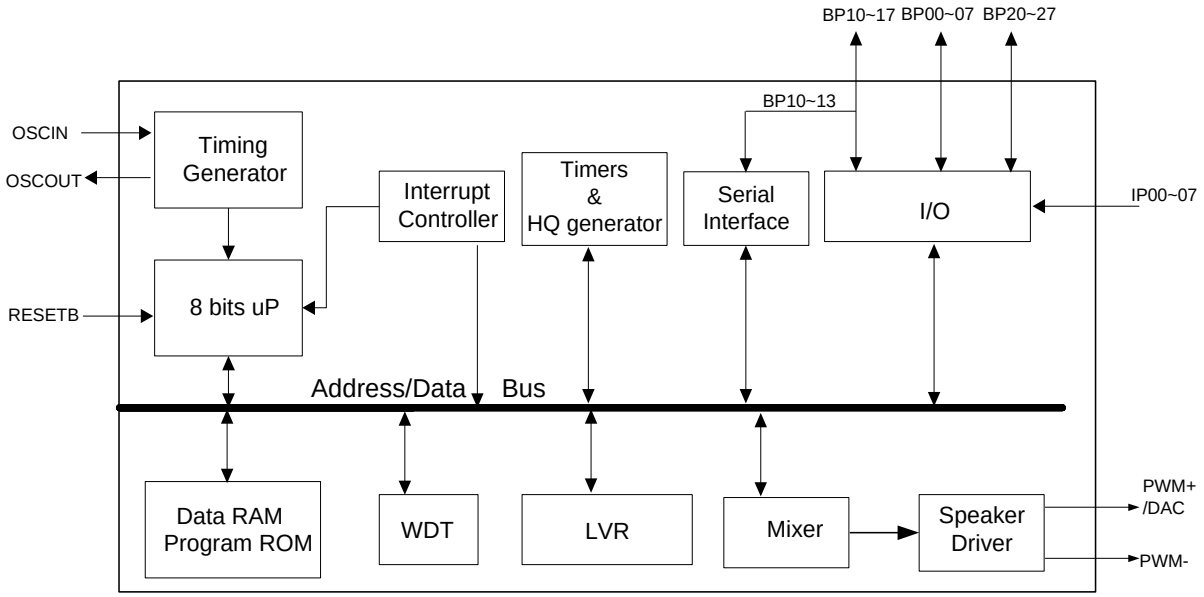
  - Multi-MIDI channels dynamic control
  - More MIDI events are supported for colorful melody playback, such as modulation wheel, pitch-bending, pedal, pitch-shift, and vibrato…etc.
- Speech and melody can be playing at the same time
  - 2 channels speech + 6 channels wavetable melody
  - 1 channel speech + 7 channels wavetable melody
  - 8 channels wavetable melody
- Built-in IR carrier generation circuit to simplify firmware IR application
- Built-in TimerG1 for general purpose applications
- Harmonized synchronization among MIDI, Speech, LED, and Motor
- Build-in 6 LED outputs (3 pairs) with 64-level control of brightness
- Build-in Watch-Dog Timer (WDT) and Low Voltage Reset (LVR)
- Provide Serial Interface Management (SIM) to access the external memory
  - W551Cxxx
  - SPI flash/ROM
- Support ***PowerScript™*** for developing codes in easy way
- Full-fledged development system
  - Source-level ICE debugger (Assembly & ***PowerScript™*** format)
  - ***Ultra_I/O™*** tool for event synchronization mechanism
  - ICE system with USB port
  - User-friendly GUI environment
- Available package form:
  - COB is essential

3. PIN DESCRIPTION

PIN NAME	I/O	FUNCTION
RESETB	In	IC reset input with an internal pull-up resistor, low active.
OSCIN	I	Main-clock oscillation input for X'tal mode. Build-in Rosc by mask option .
OSCOUT	O	Main-clock oscillation output for X'tal mode.
IP00~IP07	In	General input port with pull-high selection. Each input pin can be programmed to generate interrupt request and used to release IC from STOP mode.
BP00~BP07	I/O	General input/output pins. When used as output pin, it can be open–drain or CMOS type and with high sink capability. When set as input pin, there may have a pull-high option and generate interrupt request to release IC from STOP mode. When BP07 is used as output pin, it can be the IR transmission carrier. BP00~BP05 are used as 6 LED outputs with 64-level control (by pair). BP00~BP03 share pins to program OTP
BP10~BP17	I/O	General input/output pins. When used as output pin, it can be open–drain or CMOS type. When used as input pin, there may have a pull-high option and generate interrupt request to release IC from STOP mode. When serial interface management (SIM) is enabled, and set memory type as W551C, BP10~BP12 are used to be an interface with the external memory, W551Cxxx. If set memory to SPI Flash, BP10~BP13 are used to be an interface with the external memory, SPI Flash.
BP20~BP27	I/O	General input/output pins. When used as output pin, it can be open–drain or CMOS type. When used as input pin, there may have a pull-high option and generate interrupt request to release IC from STOP mode.
PWM+/DAC	O	PWM driver positive output or Current type DAC output
PWM-	O	PWM driver negative output
VDD	Power	Positive power supply for uP and peripherals
VSS	Power	Negative power supply for uP and peripherals
VDD_SPK	Power	Positive power supply for speaker driver
VSS_SPK	Power	Negative power supply for speaker driver
VDD_SIM	Power	Positive power supply for Serial Interface Management (SIM) BP10~BP13 For non-SIM application, it should be connected to V_{DD} to keep normal standby current.
V33O	O	For 3 battery (3.3V~5.5V) application, add capacitor 0.1uF to shunt between V33O and GND as power stability for regulator output. For 2 battery (2.4V~3.6V) application, V33O will connect to VDD directly.
VPP	Power	High power to program OTP
V33OSC	I	Power for oscillator. No connect.
TESTB	I	Test pad. No connect.

Note: As program OTP, the BP00 ~ BP03, VDD, VSS, RESETB and VPP pin will be used

4. BLOCK DIAGRAM



5. ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Supply Voltage to Ground Potential	-0.3 to +7.0	V
D.C. Voltage on Any Pin to Ground Potential	-0.3 to V_{DD} +0.3	V
Operating Temperature	0 to +70	°C
Storage Temperature	-55 to +150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

5.2 D.C. Characteristics

(V_{DD}–V_{SS} = 4.5 V, F_M = 8 MHz, Ta = 25°C, No Load unless otherwise specified)

PARAMETER	SYM.	TEST CONDITIONS	SPEC.			UNIT
			Min.	Typ.	Max.	
Operating Voltage	V_{DD}	F_{SYS} = 6 MHz	2.4	-	5.5	V
		F_{SYS} = 8 MHz	3.0	-	5.5	V
Operating Current	I_{OP}	F_{SYS} = 8MHz, normal operation	-	8	12	mA
Standby Current	I_{SB}	STOP mode	-	-	10	μA
Input Low Voltage	V_{IL}	All input pins	V_{SS}	-	0.3 V_{DD}	V
Input High Voltage	V_{IH}	All input pins	0.7 V_{DD}	-	V_{DD}	V
Input Current I/O pins	I_{IN1}	V_{IN} = 0V, pulled-high resistor = 500k ohm	-5	-9	-14	μA
Input Current I/O pins	I_{IN2}	V_{IN} = 0V, pulled-high resistor = 150k ohm	-15	-30	-45	μA
Output Current (BP0)	I_{OL}	V_{DD} = 3V, V_{OUT} = 0.4V	8	12	-	mA
	I_{OH}	V_{DD} = 3V, V_{OUT} = 2.6V	-4	-8	-	mA
Output Current (BP1, BP2)	I_{OL}	V_{DD} = 3V, V_{OUT} = 0.4V	4	6	-	mA
	I_{OH}	V_{DD} = 3V, V_{OUT} = 2.6V	-4	-8	-	mA
DAC Full Scale Current	I_{DAC}	V_{DD} = 4.5V, RL = 100Ω	-2.4 -4.0	-3.0 -5.0	-3.6 -6.0	mA
Output Current PWM+ / PWM-	I_{OL1}	RL= 8 Ohm, [PWM+]---[RL]---[PWM-]	+200	-	-	mA
	I_{OH1}		-200	-	-	mA

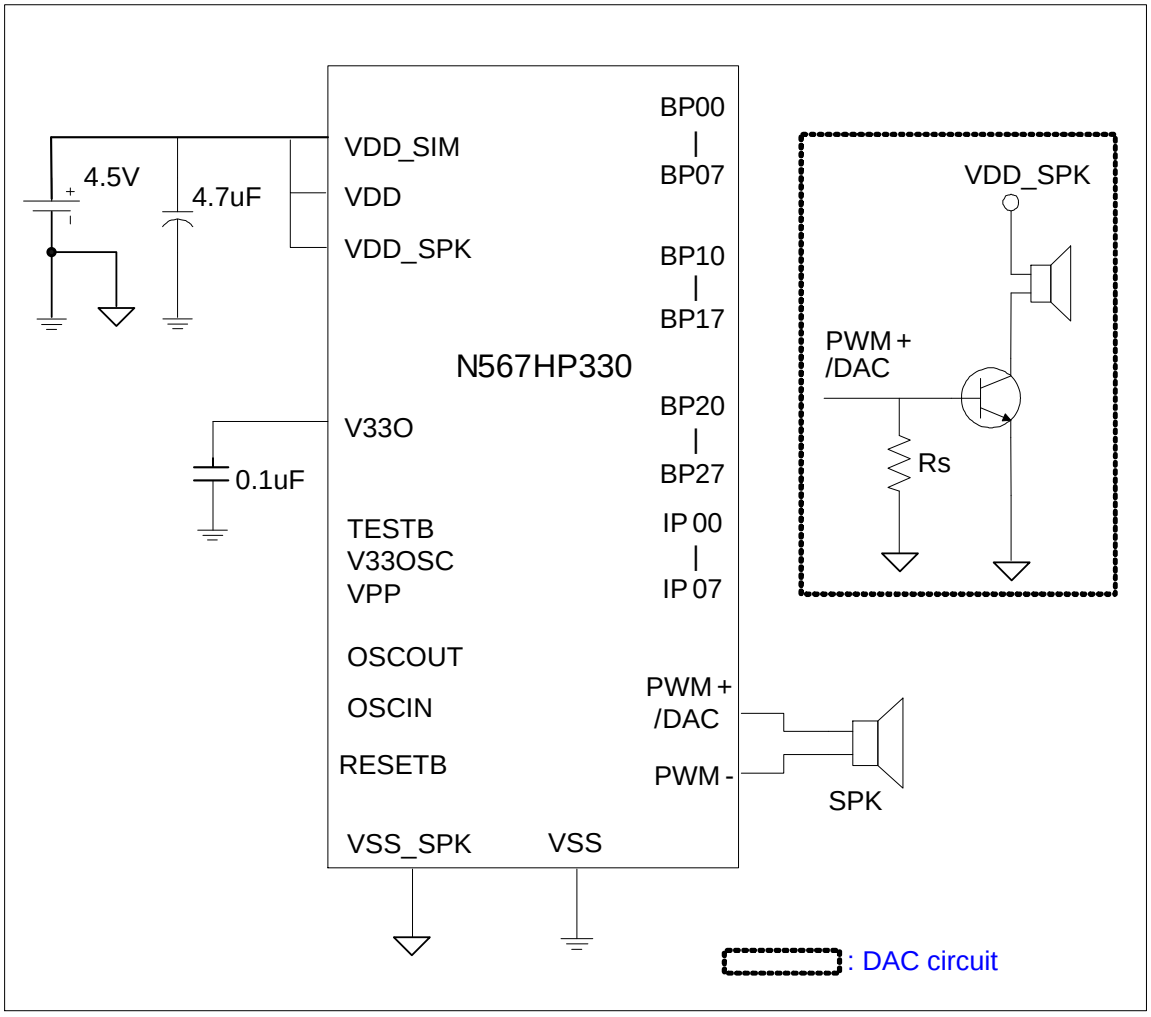
5.3 A.C. Characteristics

(V_{DD}-V_{SS} = 4.5 V, F_M = 8 MHz, Ta = 25°C; No Load unless otherwise specified)

PARAMETER	SYM.	TEST CONDITIONS	SPEC.			UNIT
			Min.	Typ.	Max.	
Main-Clock	F_M	ROSC build-in, @3.0~5.5V	3973	4096	4218	KHz
		ROSC build-in, @3.0~5.5V	5959	6144	6328	
		ROSC build-in, @3.0~5.5V	7946	8192	8437	
Main-Clock	F_M	ROSC build-in, @2.4~3.6V	3973	4096	4218	KHz
		ROSC build-in, @2.4~3.6V	5959	6144	6328	
Main-Clock Wake-up Stable Time	T_{WSM}	2^16 clock cycle	8	-	16	mS

6. TYPICAL APPLICATION CIRCUITS

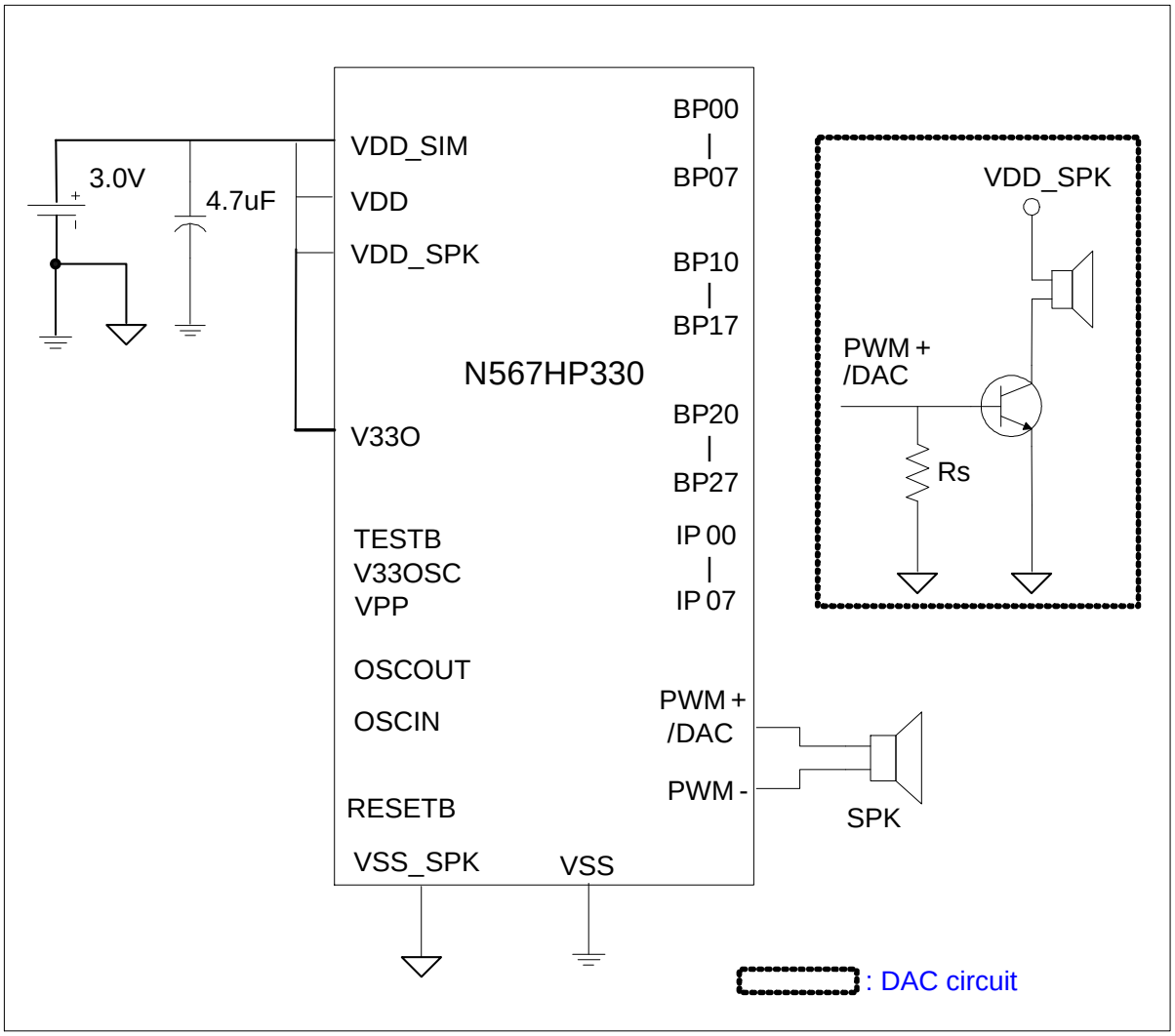
(a) 3-battery Application with Internal Oscillator (TRIM)



Notes:

1. For three batteries application, V33O should shunt a 0.1uF capacitor to GND and can't connect to VDD.
2. Rosc is built in N567H chip internally. User needn't connect Rosc resistor to OSCIN pin.
3. The 4.7uF is necessary for power stability.
4. The Rs value is suggested in 270Ω ~ 1KΩ to limit too large DAC output current flowing into transistor.
5. The VDD_SIM pad must be connected to VDD for non-SIM application.
6. The above application circuits are for reference only. No warranty for mass production.

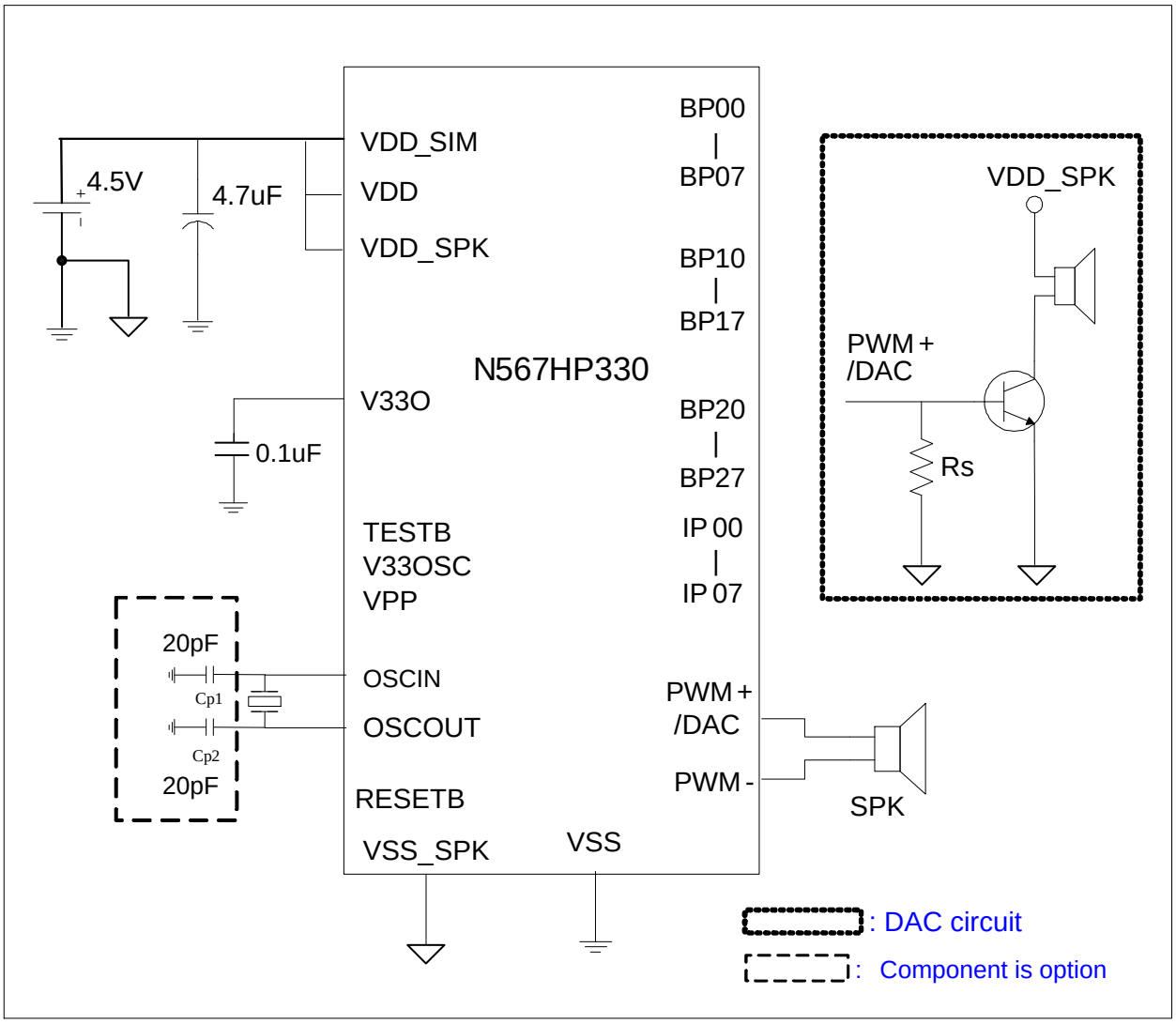
(b) 2-battery Application with Internal Oscillator (TRIM)



Notes:

1. For two batteries application, V33O connect to VDD directly
2. Rosc is built in N567H chip internally. User needn't connect Rosc resistor to OSCIN pin.
3. The 4.7uF is necessary for power stability.
4. The Rs value is suggested in 270Ω ~ 1KΩ to limit too large DAC output current flowing into transistor.
5. The VDD_SIM pad must be connected to VDD for non-SIM application.
6. The above application circuits are for reference only. No warranty for mass production.

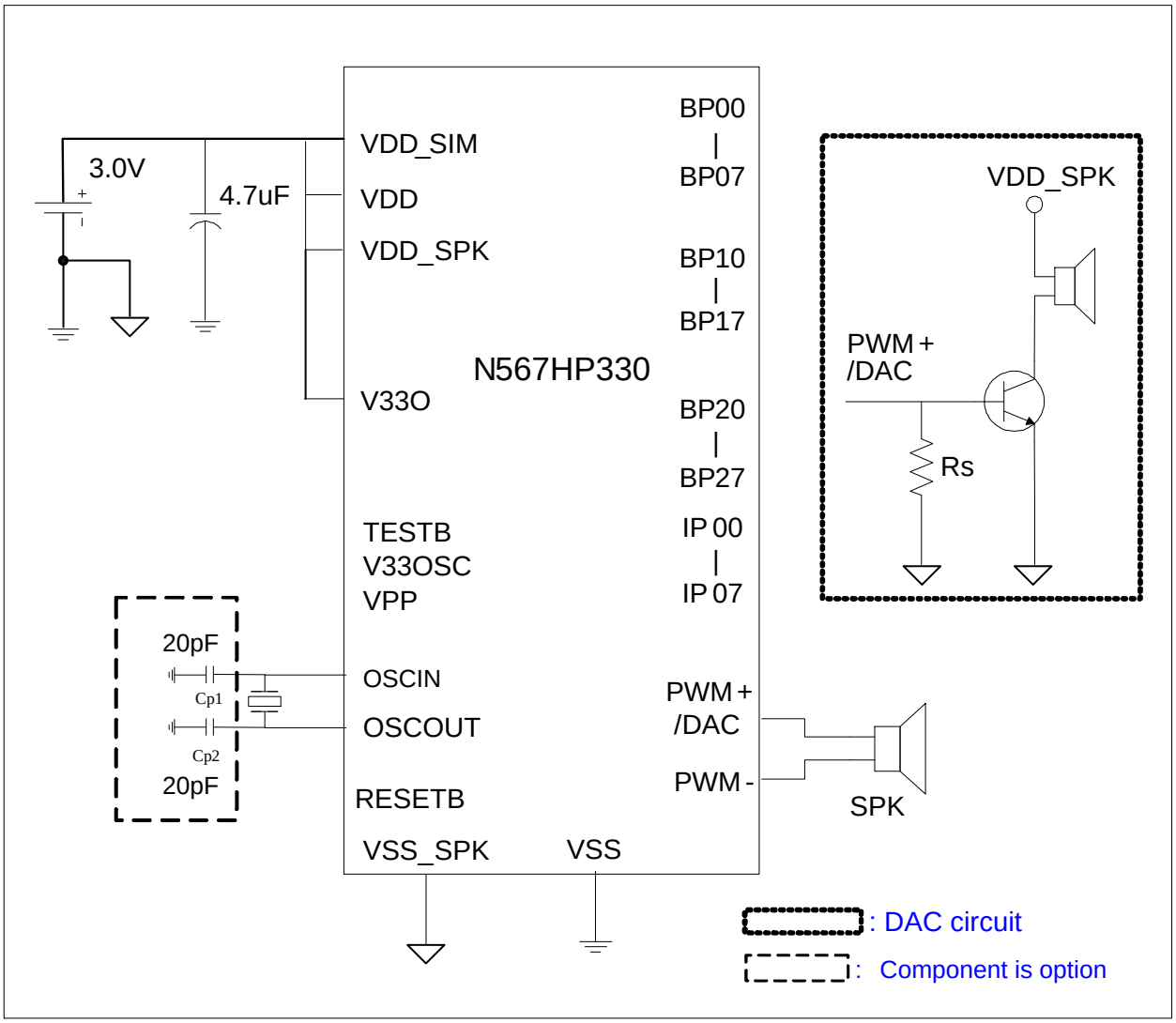
(c) 3-battery Application with Crystal Mode



Notes:

1. The crystal value must be double of system clock (Fsys). For example, as connect X'tal 12MHz, the Fsys will be 6MHz. The crystal had better placed as close to IC in PCB layout for stability concern.
2. The 4.7uF is necessary for power stability.
3. The Rs value is suggested in 270Ω ~ 1KΩ to limit too large DAC output current flowing into transistor.
4. The VDD_SIM pad must be connected to VDD for non-SIM application.
5. The above application circuits are for reference only. No warranty for mass production.
6. For more application circuits, please refer to N567Hxxx design guide.

(d) 2-battery Application with Crystal Mode

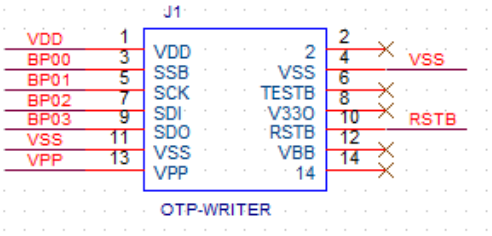


Notes:

1. The crystal value must be double of system clock (Fsys). For example, as connect X'tal 12MHz, the Fsys will be 6MHz. The crystal had better placed as close to IC in PCB layout for stability concern.
2. The 4.7uF is necessary for power stability.
3. The Rs value is suggested in 270Ω ~ 1KΩ to limit too large DAC output current flowing into transistor.
4. The VDD_SIM pad must be connected to VDD for non-SIM application.
5. The above application circuits are for reference only. No warranty for mass production.
6. For more application circuits, please refer to N567Hxxx design guide.

(e) Write interface

1. Writer interface pins are BP00~BP03, RESETB, VPP, VSS and VDD.
2. Detail application circuit, please refer to NHS-N567HP80 V1_0 user's guide A0.



(f) PCB layout guide

1. The IC substrate should be connected to VSS in PCB layout, but VSS_SPK can't connect with IC substrate directly. Both VSS and VSS_SPK tie together in battery negative power.
2. Each VDD, VDD_SIM and VDD_SPK pad must connect to positive power to support stable voltage for individual function work successfully. (Don't let them be floating.)

7. REVISION HISTORY

VERSION	DATE	REASONS FOR CHANGE	PAGE
A0.0	Jul. 2012	Preliminary release	
A1.0	Sep. 2012	Rename to N567HP330	1, 10~13
A2.0	Jan. 2013	Remove VSS_SIM and VDD2 pad description VSS_SIM rename to VSS, connect to VSS directly. VDD2 rename to VDD, connect to VDD directly	4, 8~11

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