National Semiconductor

July 1996

CGS74B303 Octal Divide-by-2 Skew Clock Driver

General Description

These minimum skew clock drivers are designed for high frequency Clock Generation and Support (CGS) applications. These devices are ideal for duty cycle recovery applications with internal frequency divide-by-2 circuitry. The devices guarantee minimum skew across the outputs of a given device. Skew parameters are also provided as a means to measure duty cycle requirements as those found in high speed clocking systems.

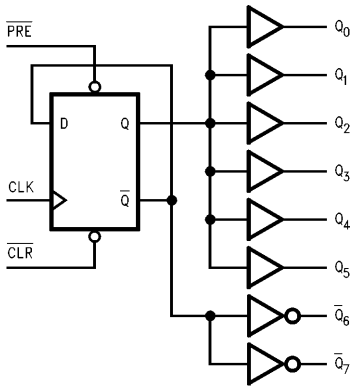
Functional Description

The CGS74B303 contains eight flip-flops designed to have low skew between outputs. The eight outputs (six in-phase with CLK and two out-of-phase) toggle on successive CLK pulses. $\overline{PRE}$ and $\overline{CLR}$ inputs are provided to set Q and $\overline{Q}$ outputs high or low independent of CLK pin.

Features

- Clock Generation and Support (CGS) Devices ideal for high frequency signal generation or clock distribution applications
- Fabricated on National's Advanced Bipolar FAST™ LSI process
- 1 ns pin-to-pin output skew
- Specification for transition skew to meet duty cycle requirements
- Current sourcing 24 mA and current sinking of 48 mA
- Low dynamic power consumption above 20 MHz
- Guaranteed 4 kV ESD protection

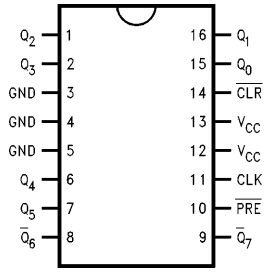
Logic Diagram



TL/F/10966–3

Connection Diagram

Pin Assignment
SOIC (M)



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Pin Description

Pin Names	Description
CLK	Clock Input
Q_0–Q_7	Outputs
$\overline{PRE}$	Preset
$\overline{CLR}$	Clear

Truth Table

Inputs			Outputs	
$\overline{CLR}$	$\overline{PRE}$	CLK	Q_0–Q_5	$\overline{Q}_6$–$\overline{Q}_7$
L	H	X	L	H
H	L	X	H	L
L	L	X	L*	L*
H	H	↑	$\overline{Q}$	Q
H	H	L	Q	$\overline{Q}$

*This state will not persist when $\overline{CLR}$/$\overline{PRE}$ returns to high.

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Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})				7.0V
Input Voltage (V_I)				7.0V
Operating Free Air Temperature				0°C to +70°C
Storage Temperature Range				−65°C to +150°C
Typical θ_{JA}				
Airflow (LFM)	0	225	500	
Jedec SOIC (M) Package	118	96	86	°C/W

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
Input Rise and Fall Times (0.8V to 2.0V)	2 ns max
Free Air Operating Temperature (T_A)	0°C to 70°C

NOTE: *The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the DC and AC Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The Recommended Operating Conditions will define the conditions for actual device operation.*

DC Electrical Characteristics

Over recommended operating conditions unless specified otherwise. All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18$ mA				−1.2	V
V_{IH}	Minimum Input High Level Voltage			2.0			V
V_{IL}	Maximum Input Low Level Voltage					0.8	V
V_{OH}	High Level Output Voltage	$I_{OH} = -2$ mA, $V_{CC} = 4.5V$		$V_{CC} - 2$			V
		$I_{OH} = -24$ mA, $V_{CC} = 4.5V$		2.0			
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$, $I_{OL} = 48$ mA			0.35	0.5	V
I_I	Input Current @ Max Input Voltage	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	m A
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$			−0.1	−0.50	mA
I_O	Output Drive Current	$V_{CC} = 5.5V$, $V_O = 2.25V$		−50		−150	mA
I_{CC}	Supply Current	$V_{CC} = 5.5V$	Outputs High		27	60	mA
			Outputs Low		45	60	mA
C_{IN}	Input Capacitance	$V_{CC} = 5V$			5		pF

AC Electrical Characteristics

Over recommended operating conditions unless specified otherwise. All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	$V_{CC} = 4.5V$ to $5.5V$ $T_A = 0°C$ to $+70°C$ $C_L = 0$ pF–50 pF $R_L = 500\Omega$			Units
		Min	Typ	Max	
f_{MAX}	Maximum Input Frequency (Note 2)	110			MHz
t_{PLH}, t_{PHL}	Propagation Delay CLKn to O_n (Note 2)	4		8.5	ns
t_{PLH}, t_{PHL}	Propagation Delay PRE/CLR	4		11	ns
t_{SU}	Set Up Time before CLK	5			ns
t_W	CLK HI CLK LO CLR/PRE	4 4 4			ns

Extended AC Electrical Characteristics

Over recommended operating conditions unless specified otherwise. All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	$V_{CC} = 4.5V$ to $5.5V$ $T_A = 0°C$ to $+70°C$ $C_L = 0$ pF–50 pF $R_L = 500\Omega$			Units
		Min	Typ	Max	
$t_{OSHL\ Q}$	Maximum Skew Common Edge Output-to-Output Variation (Notes 1, 2)		0.5	1.0	ns
$t_{OSLH\ Q}$	Maximum Skew Common Edge Output-to-Output Variation (Notes 1, 2)		0.5	1.0	ns
$t_{OSHL\ \overline{Q}}$	Maximum Skew Common Edge Output-to-Output Variation (Notes 1, 2)		0.3	0.75	ns
$t_{OSLH\ \overline{Q}}$	Maximum Skew Common Edge Output-to-Output Variation (Notes 1, 2)		0.3	0.75	ns
$t_{OSLH/HL\ Q,\overline{Q}}$	Maximum Skew Common Edge Output-to-Output Variation (Notes 1, 2)		1.0	1.6	ns
$t_{PS\ Q}$	Maximum Skew Pin (Signal) Transition Variation (Notes 1, 2)			1.0	ns
t_{rise}, t_{fall}	Rise/Fall Time (from 0.8V/2.0V to 2.0V/0.8V) 0 pF–30 pF Loads		1.1 0.9	2.0 2.0	ns

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}) or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design.

Note 2: This device is sensitive to noise due to the large transient currents which occur during multiple switching of the eight outptus. V_{CC} by-pass capacitor(s), chip types, must be placed as closely as possible to the V_{CC} pin.

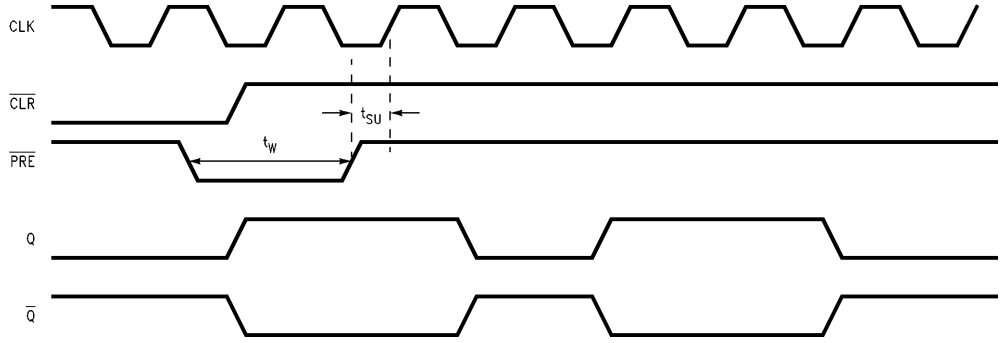
Note 3: Refer to Minimum Skew Parameters Measurement Information Chart for definitions of each skew specification.

Note 4: All input pulses are from 3.5V to 0.3V with rise and fall times of 2.0 ns.

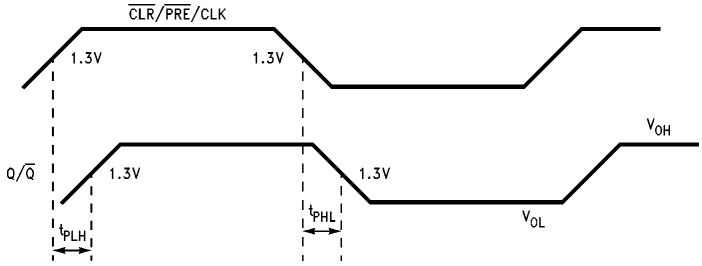
Note 5: Load capacitance includes the test jig.

Timing Diagrams

Minimum Skew Divide-by-2 Clock Drivers

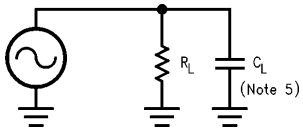


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TL/F/10966–5

Test Circuit

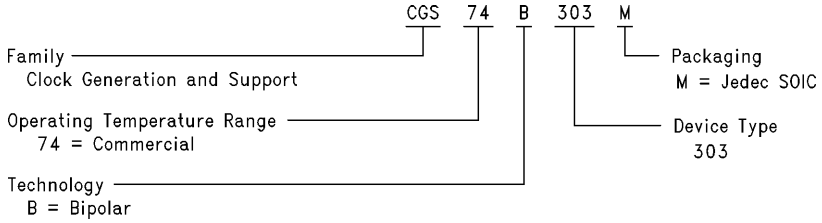


TL/F/10966–6

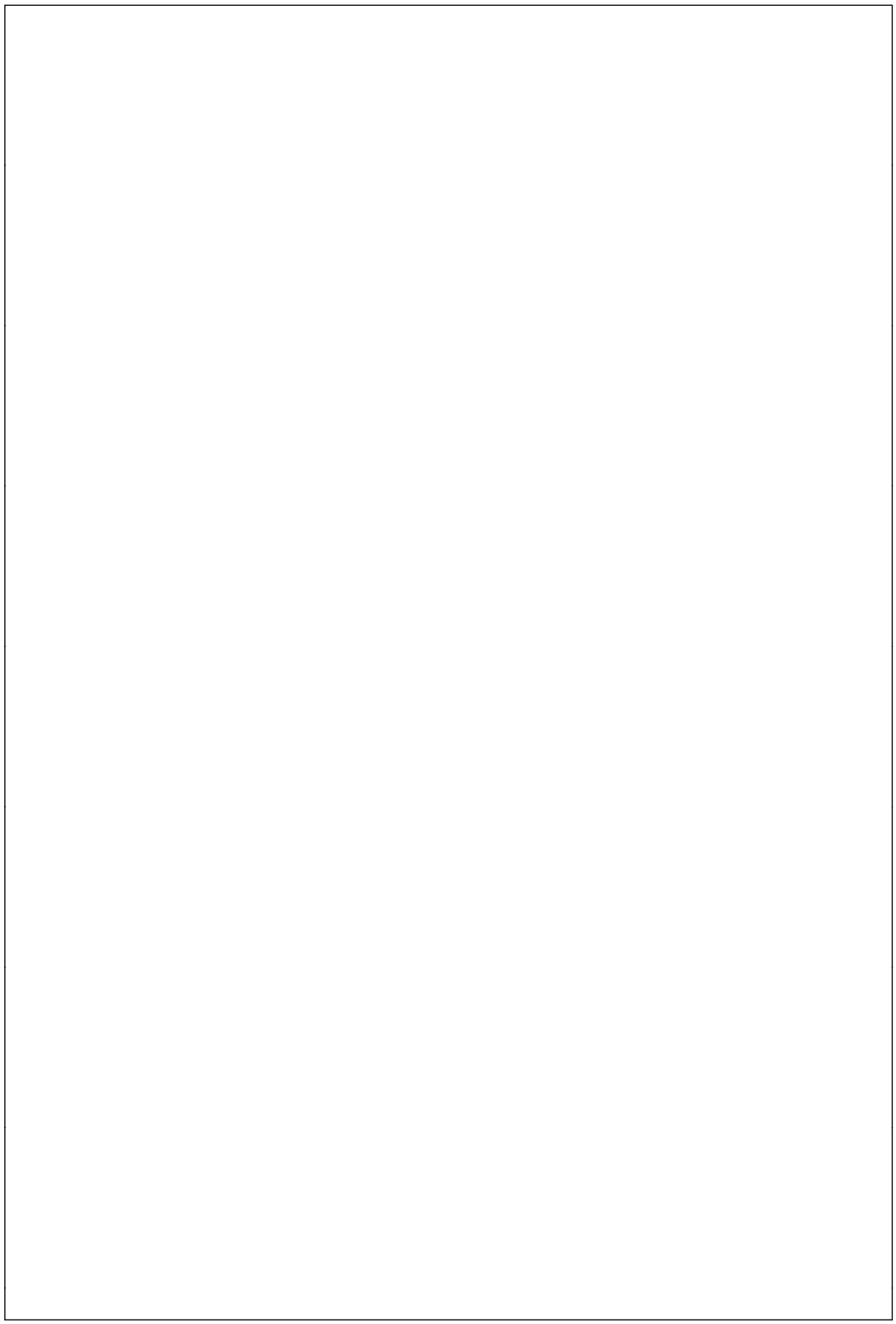
R_L is 500Ω
C_L is 50 pF for all prop delays and skew measurements.
C_L is 30 pF for t_{rise} and t_{fall} measurements.

Ordering Information

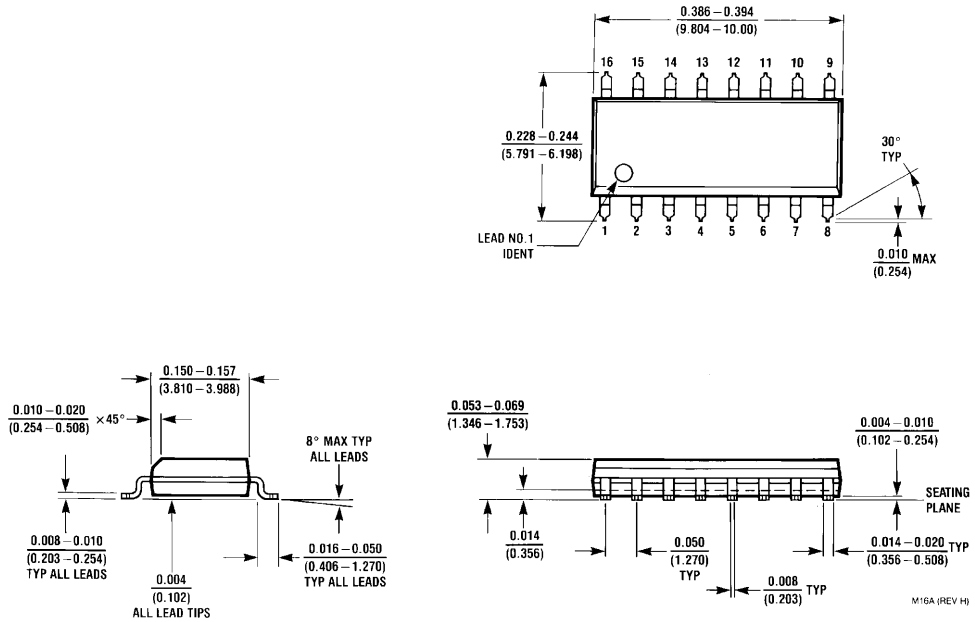
Contact NSC Marketing for specific date of availability



TL/F/10966–7



Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (S)
NS Package Number M16A

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