29 AMP, 75V, 3 PHASE MOSFET BRIDGE WITH INTELLIGENT INTEGRATED GATE DRIVE

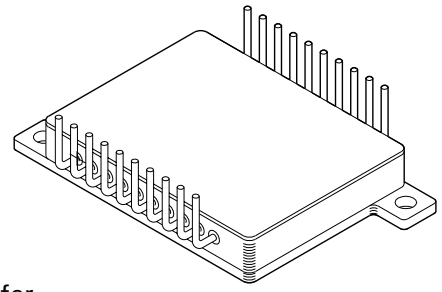
4301

M.S.KENNEDY CORP.
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MIL-PRF-38534 QUALIFIED

FEATURES:

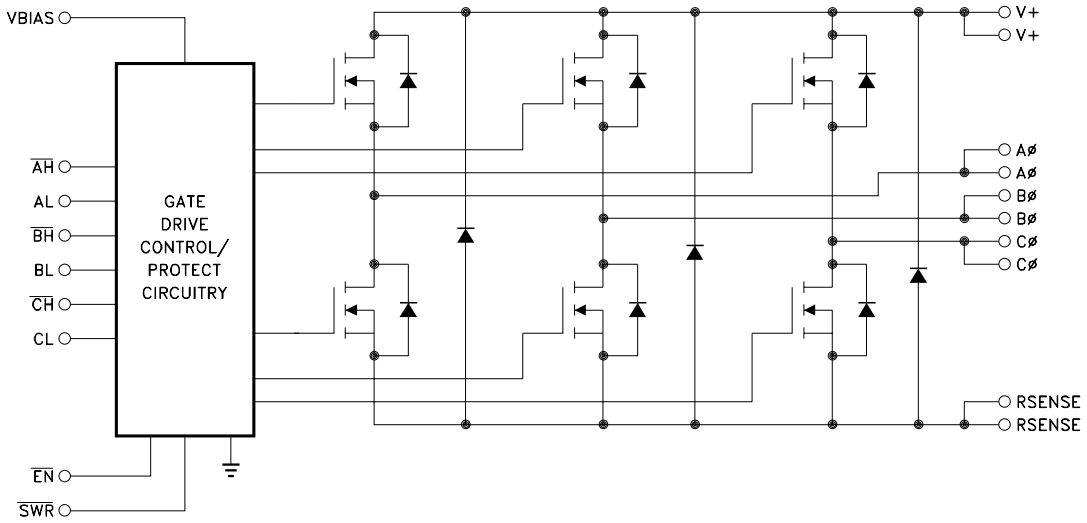
- 75 Volt Motor Supply Voltage
- 29 Amp Output Switch Capability, All N-Channel MOSFET Output Bridge
- 100% Duty Cycle High Side Conduction Capable
- Suitable for PWM Applications from DC to 100KHz
- Shoot-Through/Cross Conduction Protection
- Undervoltage Lockout Protection
- Programmable Dead-Time Control
- Low Active Enable for Bridge Shutdown Control
- Isolated Package Design for High Voltage Isolation Plus Good Thermal Transfer
- Available with Three Lead Bend Options



DESCRIPTION:

The MSK 4301 is a 3 phase MOSFET bridge plus drivers in a convenient isolated hermetic package. The hybrid is capable of 29 amps of output current and 75 volts of DC bus voltage. It has a full line of protection features, including undervoltage lockout protection of the bias voltage, cross conduction control and a user programmable dead-time control for shoot-through elimination. In addition, the bridge may be shut down by using the Enable control. The MSK 4301 provides good thermal conductivity for the MOSFETs due to the electrically isolated package design that allows direct heat sinking of the device without insulators.

EQUIVALENT SCHEMATIC



TYPICAL APPLICATIONS

- 3 Phase Brushless DC
  - Servo Control
  - Fin Actuator Control
  - Gimbal Control
- 3 Phase AC
  - Induction Motor Control
  - HVAC Blower Control

PIN-OUT INFORMATION

1	$\overline{BH}$	20	AØ
2	BL	19	AØ
3	AL	18	V+
4	$\overline{AH}$	17	V+
5	$\overline{SWR}$	16	BØ
6	VBIAS	15	BØ
7	$\overline{EN}$	14	CØ
8	CL	13	CØ
9	$\overline{CH}$	12	RSENSE
10	GND	11	RSENSE

ABSOLUTE MAXIMUM RATINGS

$V+$	High Voltage Supply	75V	
V_{BIAS}	Bias Supply	16V	
V_{IND}	Logic Input Voltages	-0.3V to V_{BIAS} +0.3V	
I_{OUT}	Continuous Output Current	29A	
I_{PK}	Peak Output Current	41A	
θ_{JC}	Thermal Resistance	1°C/W	
T_{ST}	Storage Temperature Range	-65°C to +150°C	
T_{LD}	Lead Temperature Range (10 Seconds)	+300°C	
T_C	Case Operating Temperature		
	(4301H/E)	-55°C to +125°C	
	(4301)	-40°C to +85°C	
T_J	Junction Temperature	+150°C	

ELECTRICAL SPECIFICATIONS

Parameter	Test Conditions	Group A ④ Subgroup	MSK4301H/E ③ Min.	Typ.	Max.	MSK4301 ② Min.	Typ.	Max.	Units
CONTROL SECTION									
V_{BIAS} Quiescent Current	All Inputs Off	1,2,3	-	2.5	8	-	2.5	8	mAmp
V_{BIAS} Operating Current	f = 20KHz, 50% Duty Cycle	1,2,3	-	20	25	-	20	25	mAmp
Undervoltage Threshold (Falling)		1	5.75	6.6	7.5	5.75	6.6	7.5	Volts
Undervoltage Threshold (Rising)		1	6.2	7.1	8.0	6.2	7.1	8.0	Volts
Low Level Input Voltage ①		-	-	-	0.8	-	-	0.8	Volts
High Level Input Voltage ①		-	2.7	-	-	2.7	-	-	Volts
Low Level Input Current ①	V_{IN} = 0V	-	60	100	135	60	100	135	µAmp
High Level Input Current ①	V_{IN} = 5V	-	-1	-	+1	-1	-	+1	µAmp
OUTPUT BRIDGE									
Drain-Source Breakdown Voltage ①	I_D = 25µA, All Inputs Off	-	70	-	-	70	-	-	V
Drain-Source Leakage Current ①	V_{DS} = 70V	-	-	-	25	-	-	25	µAmp
Drain-Source On Resistance (Each FET)	I_D = 29A	1	-	-	0.020	-	-	0.020	Ω
Drain-Source On Resistance ① (Each FET, For Thermal Calculations Only)		-	-	-	0.013	-	-	0.013	Ω
SWITCHING CHARACTERISTICS									
Rise Time ①	$V+$ = 28V, R_L = 1Ω	-	-	120	-	-	120	-	nSec
Fall Time ①	I_D = 29A	-	-	81	-	-	81	-	nSec
Turn-On Prop Delay (Lower)	$\overline{SWR}$ Resistor = ∞	4	-	0.5	2	-	0.5	3	µSec
Turn-Off Prop Delay (Lower)	$\overline{SWR}$ Resistor = ∞	4	-	5	8	-	5	10	µSec
Turn-On Prop Delay (Upper)	$\overline{SWR}$ Resistor = ∞	4	-	5	8	-	5	10	µSec
Turn-Off Prop Delay (Upper)	$\overline{SWR}$ Resistor = ∞	4	-	0.5	2	-	0.5	3	µSec
Dead Time	$\overline{SWR}$ = ∞	4	3.0	5.0	7.0	3.0	5.0	7.0	µSec
Dead Time	$\overline{SWR}$ = 12K	4	0.3	1.0	1.2	0.3	1.0	1.2	µSec
SOURCE-DRAIN DIODE CHARACTERISTICS									
Forward Voltage ①	I_{SD} = 29A	-	-	1.05	1.30	-	1.05	1.30	Volts
Reverse Recovery Time ①	I_{SD} = 29A, di/dt = 100A/µS	-	-	120	-	-	120	-	nSec

NOTES:

① Guaranteed by design but not tested. Typical parameters are representative of actual device performance but are for reference only.
② Industrial grade and "E" suffix devices shall be tested to subgroups 1 and 4 unless otherwise specified.
③ Military grade devices ("H" Suffix) shall be 100% tested to Subgroups 1, 2, 3 and 4.
④ Subgroups 5 and 6 testing available upon request.
⑤ Subgroup 1, 4 $T_A = T_C = +25°C$
2, 5 $T_A = T_C = +125°C$
3, 6 $T_A = T_C = -55°C$

APPLICATION NOTES

MSK 4301 PIN DESCRIPTIONS

AL,BL,CL - Are the lowside logic level digital inputs. These three inputs control the three lowside bridge transistors. If the highside inputs are low, then the lowside inputs will control both the lowside and the highside of the bridge, with deadtime set by the $\overline{SWR}$ resistor. $\overline{EN}$ will override these inputs, forcing all outputs low. These inputs can be driven by logic up to 15V (less than VBIAS). An internal pullup to VBIAS will hold each input high if the pins are not driven.

$\overline{AH}$,$\overline{BH}$,$\overline{CH}$ - Are the highside logic level digital inputs. These three inputs control the three highside bridge transistors. Unless the deadtime is disabled by connecting $\overline{SWR}$ to ground, the lowside input of each phase will override the corresponding highside input. If $\overline{SWR}$ is the lowside input of each phase will override the corresponding highside input. In this condition, tied to ground, deadtime is disabled and the outputs follow the inputs. In this condition, shoot-through must be avoided externally. $\overline{EN}$ will override all inputs, forcing outputs low.

VBIAS - Is the positive supply for the gate drive. This pin should be decoupled to ground with at least a 22μF capacitor in parallel with a 0.1μF ceramic capcitor.

GROUND - Is the return for the VBIAS supply. This pin should be connected to the return of the lowside MOSFETs or the bottom of the sense resistor at the bottom of the bridge. The gate drive current must return through this pin, so trace lengths should be kept to a minimum. All grounds should be returned to the bottom of the bridge or sense resistor in a star fashion. This will eliminate ground loops.

$\overline{SWR}$ - Is the pin for controlling the deadtime between the top and bottom transistors of the bridge. By connecting a pullup resistor between this pin and VBIAS, various deadtimes can be obtained. There is and internal 100KΩ pullup resistor connected internally. By adding additional resistors in externally, reduced deadtimes can be achieved. By connecting this pin directly to ground, all deadtime is eliminated. However, care must be taken to assure that deadtime is being generated by the logic circuitry driving the inputs. Shoot-through can occur (both the top and bottom transistors on at the same time for a given phase, causing a short on the V+ supply to ground) destroying the bridge.

V+ - Is the power connection for the top of the output bridge. These pins must be bypassed by a capacitor to ground of a least 10μF per amp preferrably 100μF per amp of output current mini mum, high quality high frequency bypass capacitance to help suppress switching noise. Connect both pins for proper current sharing.

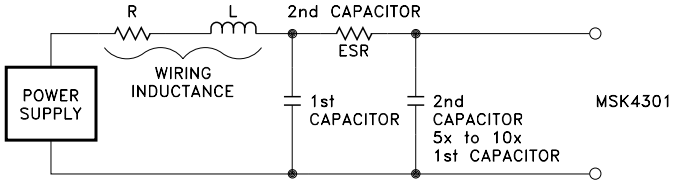
AØ, BØ, CØ - Are the output pins for the three phases of power bridge. Connect both pins for proper current sharing.

$\overline{EN}$ - Is the enabling input for the bridge. This digital input, when pulled low, will enable the bridge, following the inputs from AL, BL, CL and AH, BH, CH inputs. When pulled high, it will override all other inputs and disable the bridge. It is internally pulled high to VBIAS, and can be driven by logic levels up to VBIAS.

RSENSE - Are the connections to the bottom of the bridge. All power flowing through the bridge will flow through this point, and can be sensed by connecting a sense resistor from here to ground. The sense resistor will develop a voltage proportional to the current flowing. Size the value and power rating of the sense resistor according to the voltage necessary. 3 volts is the maximum voltage between this point and ground, or damage to the hybrid will result. Connect both pins for proper current sharing.

BUS VOLTAGE FILTER CAPACITORS

The size and placement of the capacitors for the main voltage bus for the motor will have an effect on the noise filtered throughout the rest of the system. Series RLC tuned circuit is being created by the inductance of the wire (about 30nH per inch), the filter capacitance, and all of the resistances (wire resistance and the capacitor ESR) of the overall power circuit. Voltage spikes from the back EMF if the motor ride on top of the bus voltage. All of this must be taken into account when laying out the system. A first capacitor of high quality and low ESR should be placed as close to the hybrid circuit as possible. Along with that, a capacitor of 5x to 10x the first value should be added (and that second capacitor should have some ESR) and/or a resistor should be added to help with the damping of the voltage spikes. Be careful of the ripple current in all the capacitors. Excessive ripple current, beyond what the capacitor is rated for, will destroy the capacitor.

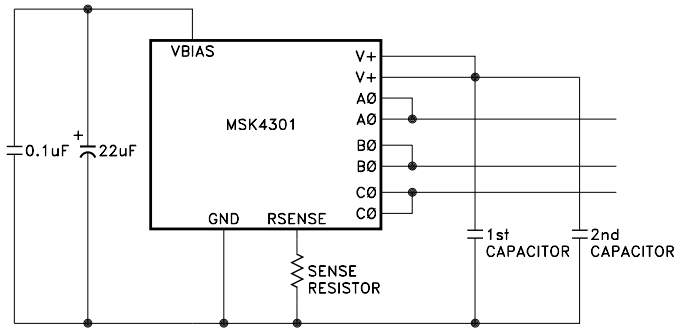


BIAS SUPPLY BYPASS CAPACITORS

It is recommended that at least 22μF of capacitance for bypassing the VBIAS voltage that supplies the drive circuitry for the MSK 4301, along with 0.1μF for helping the high frequency current pulses needed by the gate driver. If an extremely long risetime is exhibited by the turn on of the FETs, the extra high frequency capacitance will help.

GENERAL LAYOUT

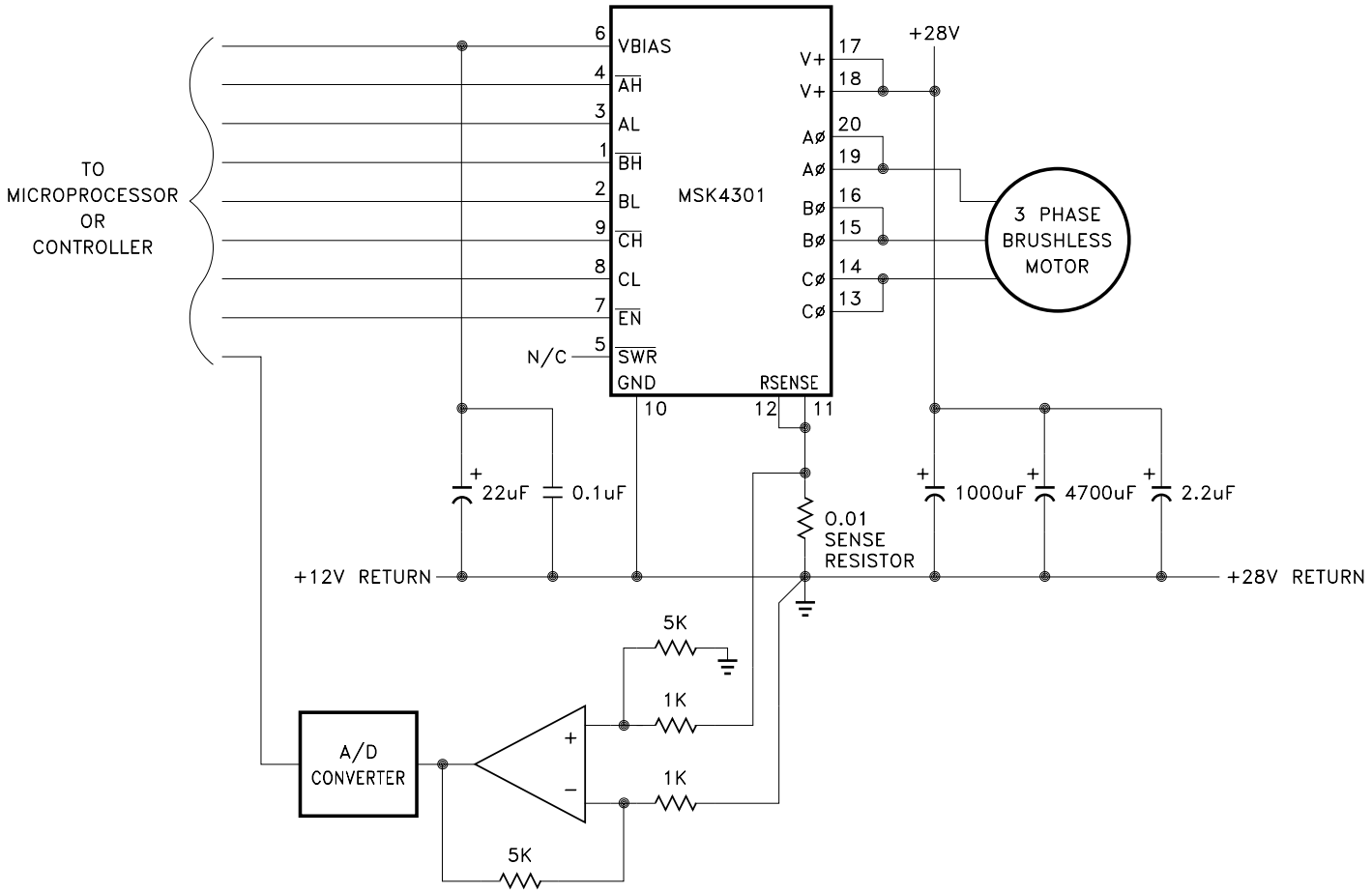
Good high frequency PC layout techniques are a must. Traces wide enough for the current delivered, and placement of the big capacitors close to the MSK 4301 are very important. The path for the RSENSE connection through any sense resistor back to the GND pins must be as short as possible. This path is the gate drive current path for all the FETs on the lower half of each phase. A short, low inductance path will aid in the switching time of those FETs.



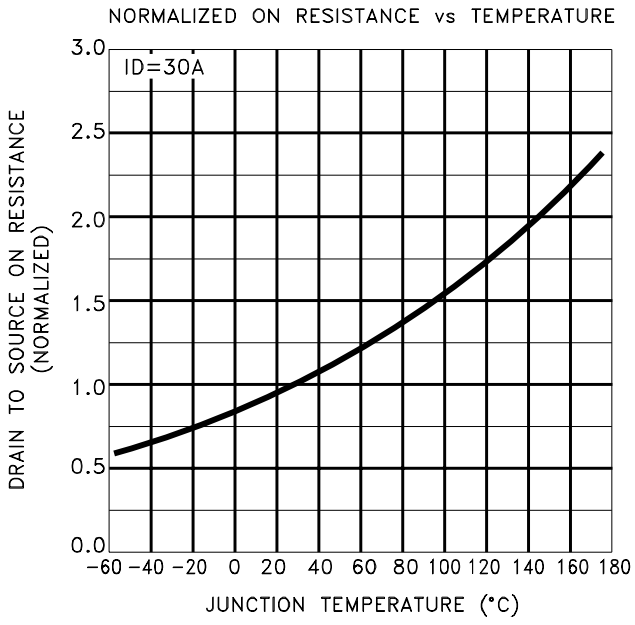
LOW POWER STARTUP

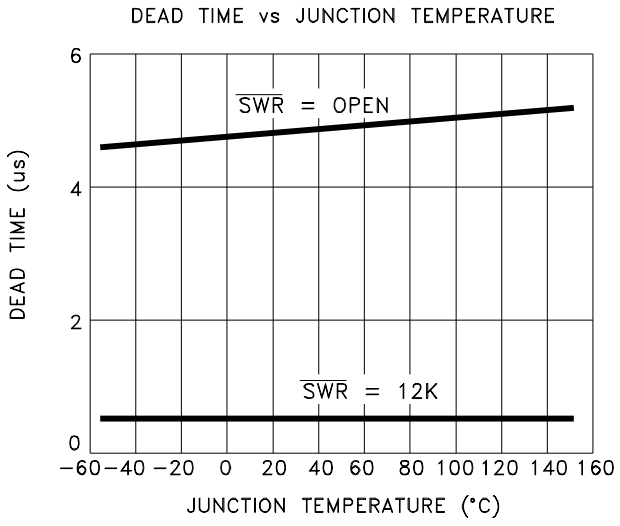
When starting up the circuit utilizing the MSK 4301 for the first time, it is very important to keep certain things in mind. Because of the small size of the bridge, there is no internal short circuit protection and a short circuit will destroy the bridge. Any required short circuit protection must be built outside the bridge. Current and voltage limit the power supply feeding the V+ pins to the bridge, and monitor the current for any signs of short circuiting, or shoot-through currents. If there are large current spikes at the beginning of each switching cycle, there may be shoot through. Try raising the resistor value of the $\overline{SWR}$. This will lengthen the deadtime and stop shoot-through.

TYPICAL APPLICATION SCHEMATIC

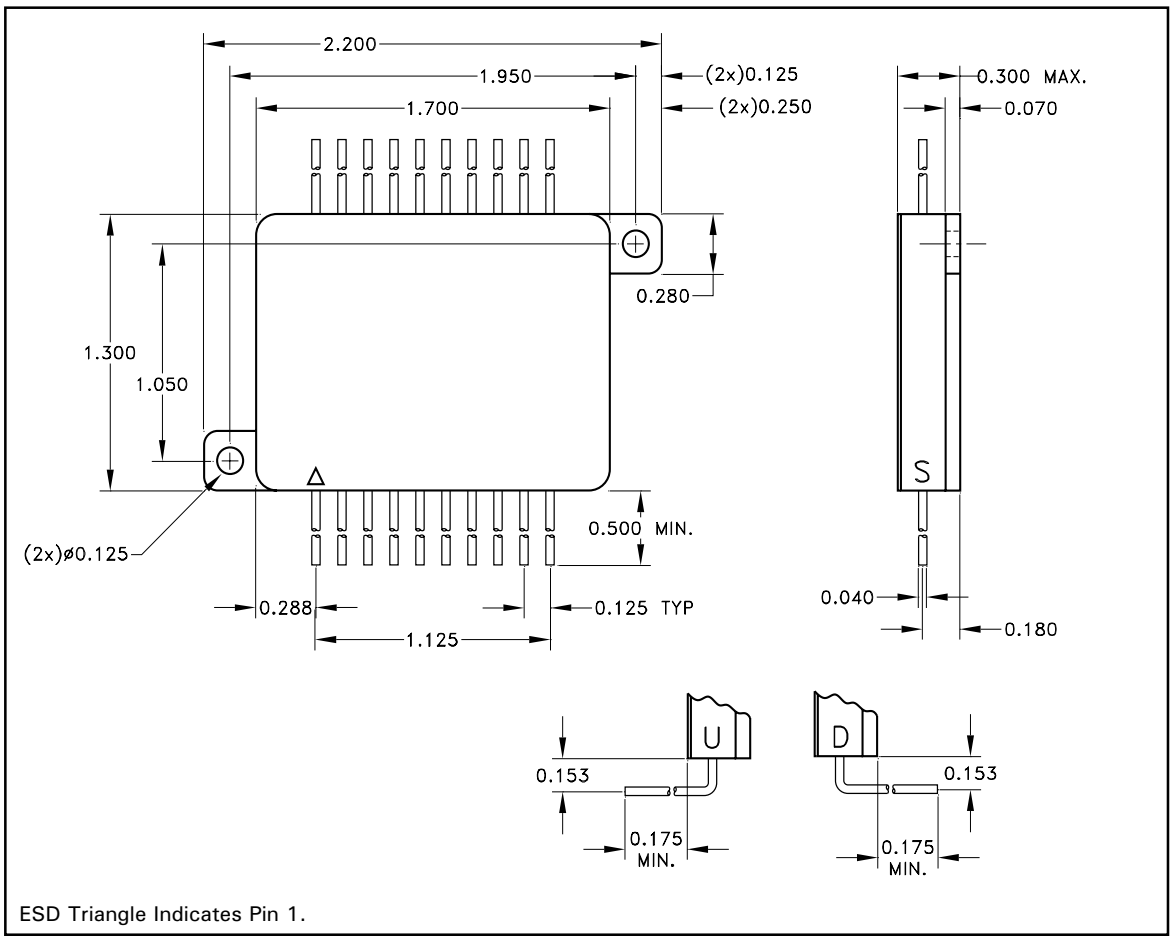


TYPICAL PERFORMANCE CURVES





MECHANICAL SPECIFICATIONS



ESD Triangle Indicates Pin 1.

NOTE: ALL DIMENSIONS ARE ±.010 INCHES UNLESS OTHERWISE LABELED.

ORDERING INFORMATION

MSK4301 H U

LEAD CONFIGURATIONS
S = STRAIGHT; U = BENT UP; D = BENT DOWN

SCREENING
BLANK = INDUSTRIAL; E = EXTENDED RELIABILITY;
H = CLASS H

GENERAL PART NUMBER

The above example is a Military grade hybrid with leads bent up.

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