DATA SHEET

74F723A
Quad 2-to-1 data selector multiplexer (3-State)
74F723-1
Quad 2-to-1 data selector multiplexer with 30Ω equivalent output termination impedance (3-State)
74F725A
Quad 3-to-1 data selector multiplexer (3-State)
74F725-1
Quad 3-to-1 data selector multiplexer with 30Ω equivalent output termination impedance (3-State)

Product specification 1990 Dec 13

IC15 Data Handbook

Philips
Semiconductors

PHILIPS

74F723A Quad 3-to-1 Data Selector Multiplexer (3-State)
74F723-1 Quad 3-to-1 Data Selector Multiplexer with 30Ω Equivalent Output Termination Impedance (3-State)
74F725A Quad 4-to-1 Data Selector Multiplexer
74F725-1 Quad 4-to-1 Data Selector Multiplexer with 30Ω Equivalent Output Termination Impedance

FEATURES for 74F723A/74F723-1

- Consists of four 3-to-1 Multiplexers
- High impedance PNP base inputs for reduced loading (20µA in High and Low states)
- Inverting or non-inverting data path capability by an inverting ($\overline{INV}$) input
- Designed for address multiplexing of dynamic RAM and other applications
- Multiple side pins for V_{CC} and GND to reduce lead inductance (improves speed and noise immunity)
- 3-State outputs sink 64mA (74F723A only)
- 30Ω termination impedance on each output – 74F723-1

FEATURES for 74F725A/74F725-1

- Consists of four 4-to-1 Multiplexers
- High impedance PNP base inputs for reduced loading (20µA in High and Low states)
- Equivalent to two 74F253s without 3-State
- Outputs sink 64mA (74F725A only)
- 30Ω termination impedance on each output – 74F725-1

DESCRIPTION

The 74F723A/74F723-1 consist of four 3-to-1 multiplexers designed for address multiplexing of dynamic RAMs and other multiplexing applications. Select (S0, S1) inputs control which line is to be selected, as defined in the Function Table for 74F723A/74F723-1. When the invering input ($\overline{INV}$) is Low, the input data path is inverted.

To improve speed and noise immunity, V_{CC} and GND side pins are used. The 3-State outputs source 15mA and sink 64mA. The 74F723-1 is the same as 74F723A except that it has a 30Ω temination impedance on each output to reduce line noise and the 3-State outputs sink 5mA.

The 74F725A/74F725-1 consist of four 4-to1 multiplexers designed for general multiplexing purpose. The select (S0, S1) inputs control which line is to be selected, as defined in the Function Table for 74F725A/725-1. The outputs source 15mA and sink 64mA. The 74F725-1 is the same as the 74F725A except that it has a 30Ω termination impedance on each output to reduce line noise and the outputs sink 5mA.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F723A	5.5ns	25mA
74F723-1	7.0ns	26mA
74F725A	5.5ns	20mA
74F725-1	6.5ns	20mA

ORDERING INFORMATION

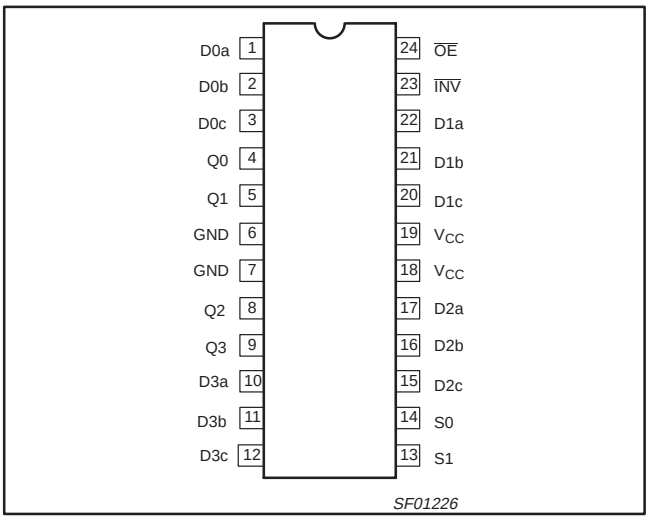
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ± 10% T_{amb} = 0° C to +70°C	PKG DWG #
20-Pin Plastic Slim DIP (300 mil)	N74F723AN, N74F723-1N, N74F725AN, N74F725-1N	SOT222-1
24-Pin Plastic SOL	N74F723AD, N74F723-1D, N74F725AD, N74F725-1D	SOT137-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

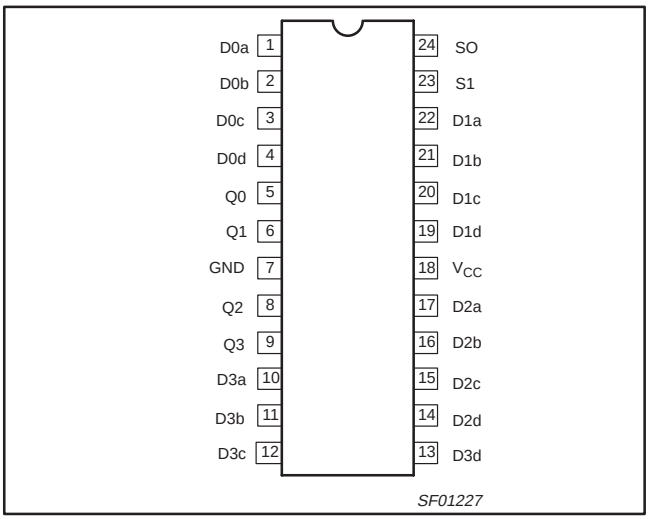
TYPE	PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
74F723A/ 74F723-1	Dna, Dnb, Dnc	Data inputs	1.0/0.066	20µA/40µA
	S0, S1	Select inputs	1.0/0.033	20µA/20µA
	$\overline{OE}$	Output Enable input	1.0/0.033	20µA/20µA
	$\overline{INV}$	Output inverting input	1.0/0.033	20µA/20µA
74F723A	Q0 - Q3	Data outputs for 74F723A	750/106.7	15mA/64mA
74F723-1	Q0 - Q3	Data outputs for 74F723-1	750/8.33	15mA/5mA
74F725A/ 74F725-1	Dna, Dnb, Dnc, Dnd	Data inputs	1.0/0.066	20µA/40µA
	S0, S1	Select inputs	1.0/0.033	20µA/20µA
74F725A	Q0 - Q3	Data outputs	750/106.7	15mA/64mA
74F725-1	Q0 - Q3	Data outputs	750/8.33	15mA/5mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20µA in the High state and 0.6mA in the Low state.

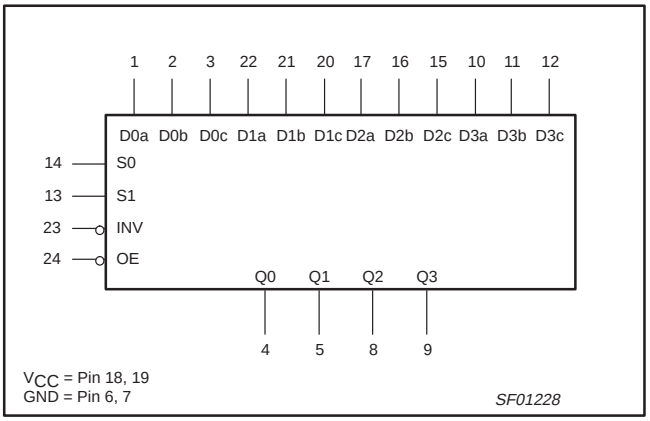
PIN CONFIGURATION – 74F723A/74F723-1



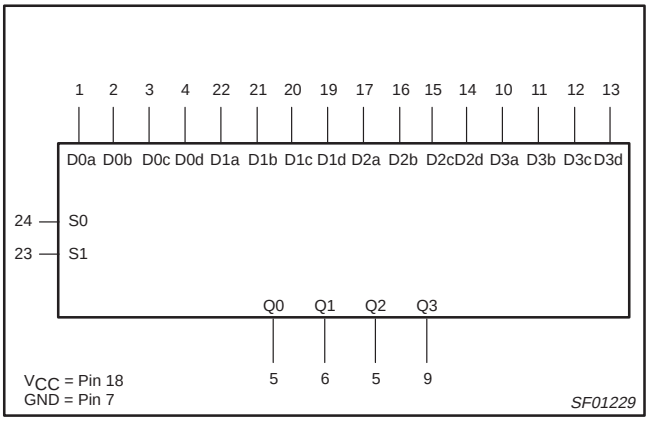
PIN CONFIGURATION – 74F725A/74F725-1



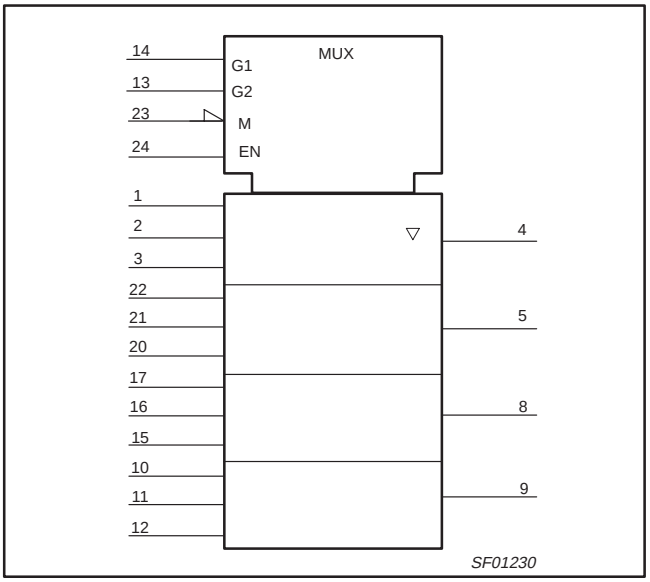
LOGIC SYMBOL – 74F723A/74F723-1



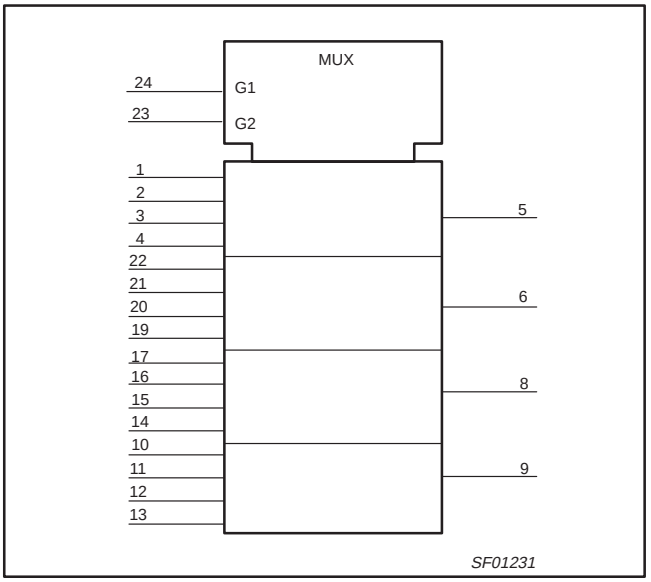
LOGIC SYMBOL – 74F725A/74F725-1



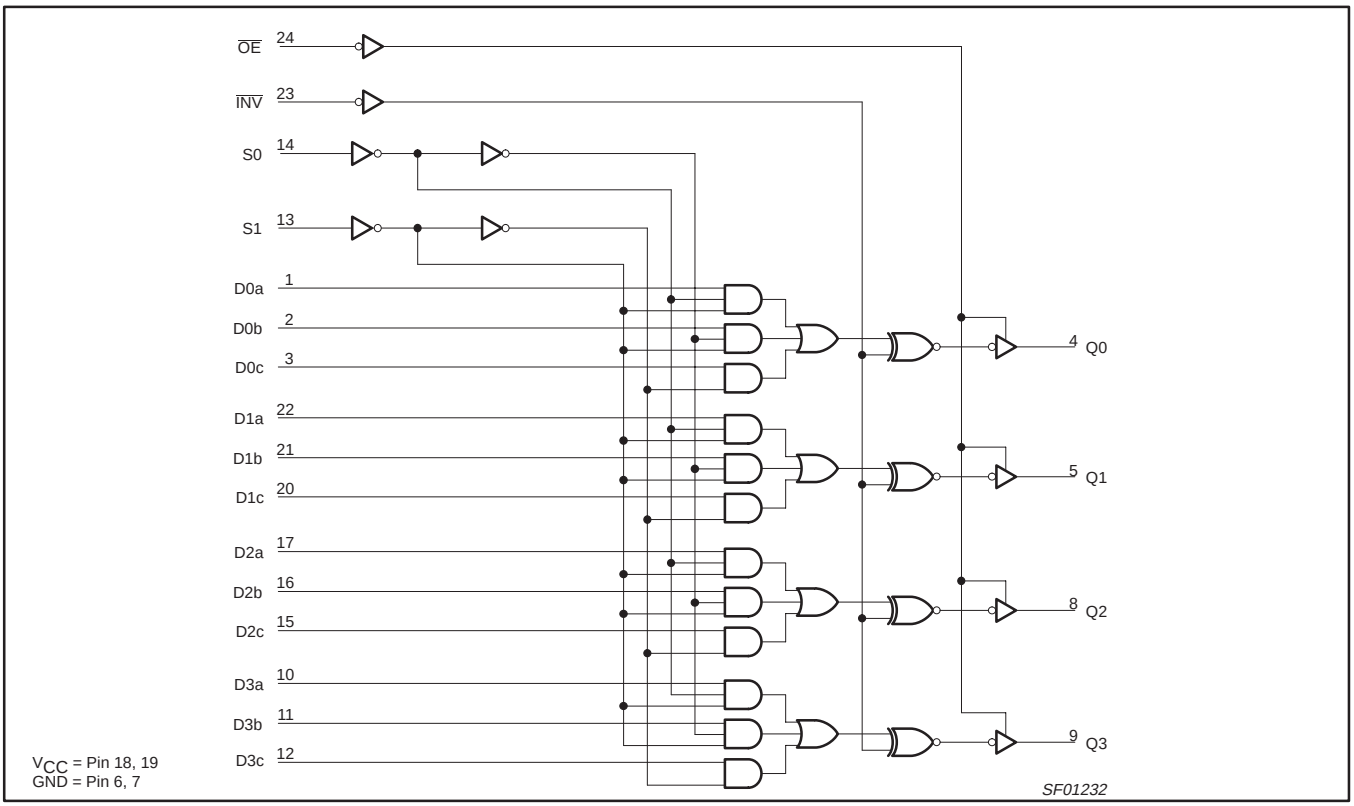
LOGIC SYMBOL (IEEE/IEC) – 74F723A/74F723-1



LOGIC SYMBOL (IEEE/IEC) – 74F725A/74F725-1



LOGIC DIAGRAM – 74F723A/74F723-1

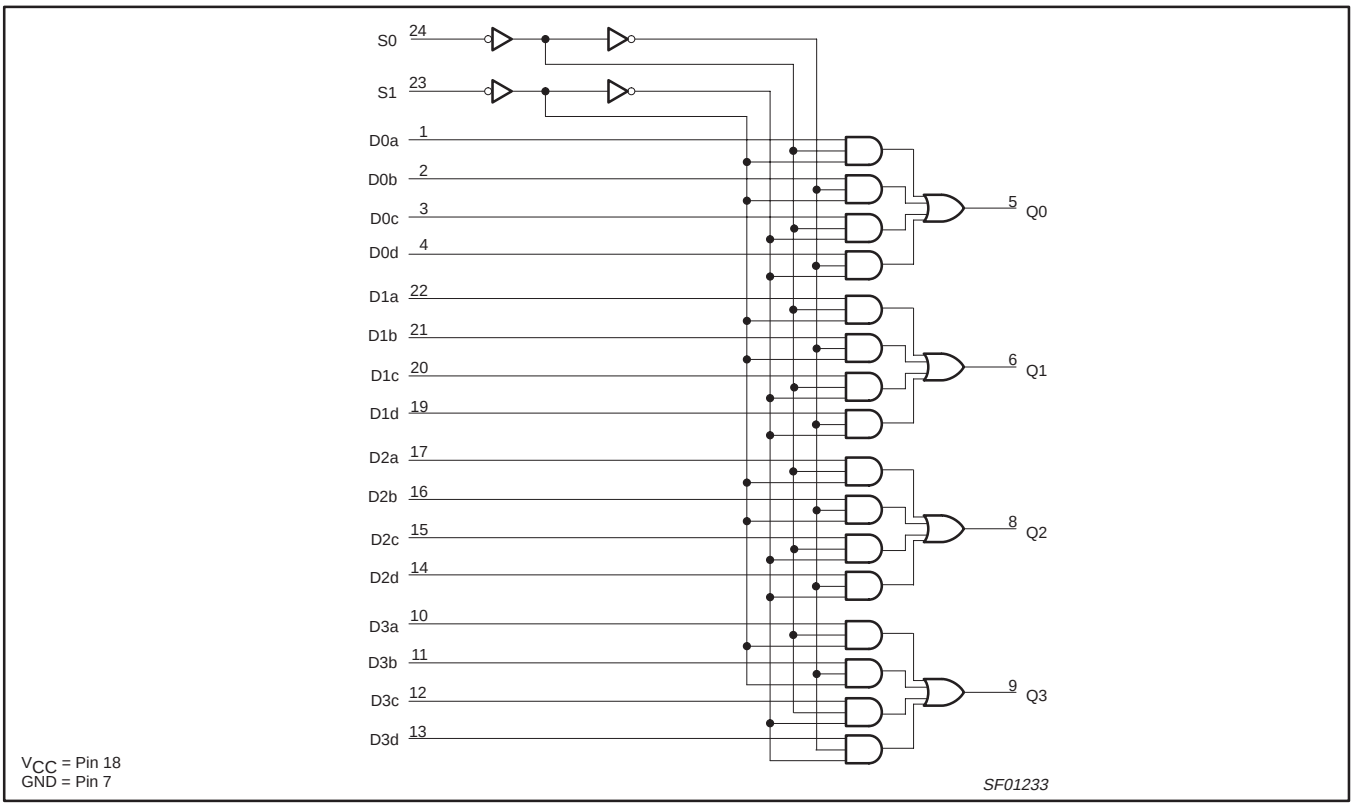


FUNCTION TABLE – 74F723A/74F723-1

INPUTS							OUTPUT
S0	**S1**	**$\overline{INV}$**	**$\overline{OE}$**	**Dna**	**Dnb**	**Dnc**	**Qn**
L	L	L	L	Data a	Data b	Data c	$\overline{\text{Data a}}$
L	L	H	L	Data a	Data b	Data c	Data a
H	L	L	L	Data a	Data b	Data c	$\overline{\text{Data b}}$
H	L	H	L	Data a	Data b	Data c	Data b
X	H	L	L	Data a	Data b	Data c	$\overline{\text{Data c}}$
X	H	H	L	Data a	Data b	Data c	Data c
X	X	X	H	X	X	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

LOGIC DIAGRAM – 74F725A/74F725-1



FUNCTION TABLE – 74F725A/74F725-1

INPUTS						OUTPUT
S0	**S1**	**Dna**	**Dnb**	**Dnc**	**Dnd**	**Qn**
L	L	Data a	Data b	Data c	Data d	Data a
H	L	Data a	Data b	Data c	Data d	Data b
L	H	Data a	Data b	Data c	Data d	Data c
H	H	Data a	Data b	Data c	Data d	Data d

H = High voltage level
L = Low voltage level

ABSOLUTE MAXIMUM RATINGS

Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		–0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	74F723-1, 74F725-1	10	mA
		74F723A, 74F725A	96	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{stg}	Storage temperature		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current				–15	mA
I_{OL}	Low-level output current	74F723-1, 74F725-1			5	mA
		74F723A, 74F725A			64	mA
T_{amb}	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[NO TAG]			LIMITS			UNIT
						MIN	TYP NO TAG	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
				I_{OH} = –15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	74F723-1/ 74F725-1	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 5mA	±10%V_{CC}		0.38	0.50	V
					±5%V_{CC}		0.38	0.50	V
		74F723A/ 74F725A		I_{OL} = MAX	±10%V_{CC}		0.38	0.55	V
					±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	Others	V_{CC} = MAX, V_I = 0.5V					–20	µA
		Dn only						–40	µA
I_{OZH}	Off-state output current High-level voltage applied	74F723A/ 74F723-1 only	V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					–50	µA
I_{OS}	Short-circuit output current[3]	74F723-1/ 74F725-1	V_{CC} = MAX			–60		–150	mA
I_O	Output current[NO TAG]	74F723A/ 74F725A	V_{CC} = MAX, V_O = 2.25V			–60		–150	mA
I_{CC}	Supply current (total)	74F723A	I_{CCH}	V_{CC} = MAX			23	30	mA
			I_{CCL}				29	40	mA
			I_{CCZ}				25	40	mA
		74F723-1	I_{CCH}	V_{CC} = MAX			23	35	mA
			I_{CCL}				29	40	mA
			I_{CCZ}				26	40	mA
		74F725A	I_{CCH}	V_{CC} = MAX			16	25	mA
			I_{CCL}				24	35	mA
		74F725-1	I_{CCH}	V_{CC} = MAX			17	25	mA
			I_{CCL}				25	35	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_O is tested under conditions that produce current approximity one half of the true short-circuit output current (I_{OS}).

AC ELECTRICAL CHARACTERISTICS – 74F723A/74F723-1

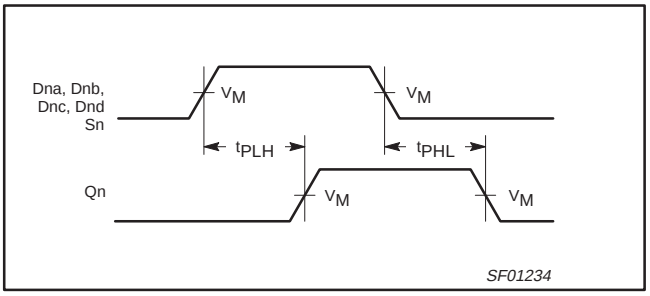
SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_{amb} = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0° C to +70°C, V_{CC} = 5V ± 10%, C_L = 50pF, R_L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb, Dnc to Qn	74F723A	Waveform 1, 2	2.5 2.0	5.0 4.5	8.0 7.0	2.0 2.0	8.5 7.5	ns ns
t_{PLH} t_{PHL}	Propagation delay S0, S1, $\overline{INV}$ to Qn		Waveform 1, 3	6.5 4.0	9.0 7.5	12.5 11.0	4.0 3.5	14.0 12.0	ns ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to Qn		Waveform 4 Waveform 5	2.0 2.5	4.0 4.5	6.5 7.0	2.0 2.0	7.5 7.5	ns ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to Qn		Waveform 4 Waveform 5	2.5 3.0	4.0 5.0	7.0 7.5	2.0 2.5	7.5 8.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb, Dnc to Qn	74F723-1	Waveform 1, 2	2.5 2.5	6.0 5.0	8.5 8.0	2.5 2.0	9.5 8.0	ns ns
t_{PLH} t_{PHL}	Propagation delay S0, S1, $\overline{INV}$ to Qn		Waveform 1, 3	7.0 5.0	10.0 9.0	14.0 12.5	6.0 4.5	16.0 13.5	ns ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to Qn		Waveform 4 Waveform 5	3.0 3.0	4.5 5.0	7.5 7.5	2.5 3.0	8.0 8.0	ns ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to Qn		Waveform 4 Waveform 5	2.5 4.0	4.5 6.0	7.0 8.5	2.0 3.0	8.0 9.5	ns ns

AC ELECTRICAL CHARACTERISTICS – 74F725A/74F725-1

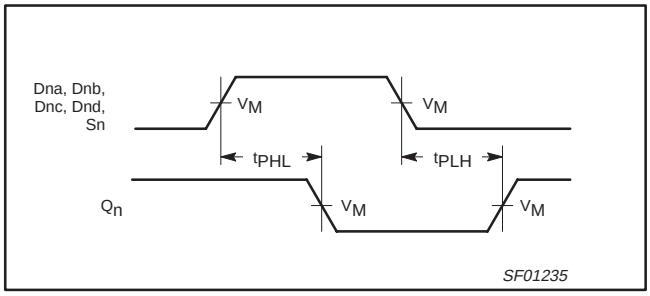
SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_{amb} = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0 to +70°C, V_{CC} = 5V ± 10%, C_L = 50pF, R_L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb, Dnc, Dnd to Qn	74F725A	Waveform 1, 2	2.0 2.0	3.5 3.5	6.5 6.5	2.0 2.0	7.0 6.5	ns ns
t_{PLH} t_{PHL}	Propagation delay S0, S1 to Qn		Waveform 1	6.0 5.0	8.5 7.0	11.5 10.0	5.5 4.5	13.5 10.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb, Dnc, Dnd to Qn	74F725-1	Waveform 1, 2	2.0 2.0	4.0 4.0	7.0 6.5	2.0 2.0	7.5 7.5	ns ns
t_{PLH} t_{PHL}	Propagation delay S0, S1 to Qn		Waveform 1	6.5 5.0	9.0 8.5	12.0 10.5	5.5 5.0	14.0 11.0	ns ns

AC WAVEFORMS

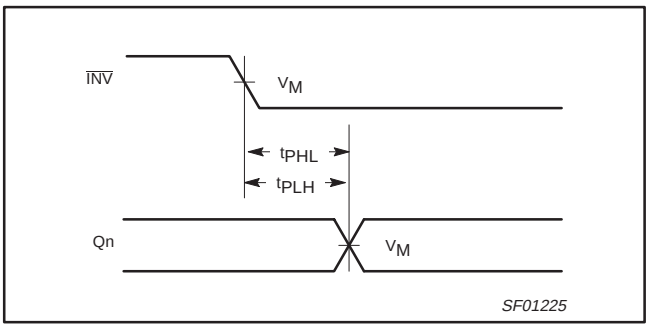
For all waveforms, $V_M = 1.5V$



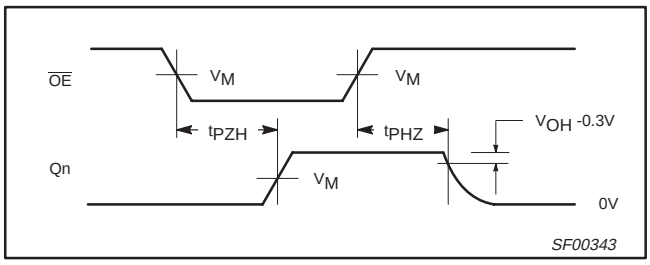
Waveform 1. Propagation Delay for Non-Inverting Output



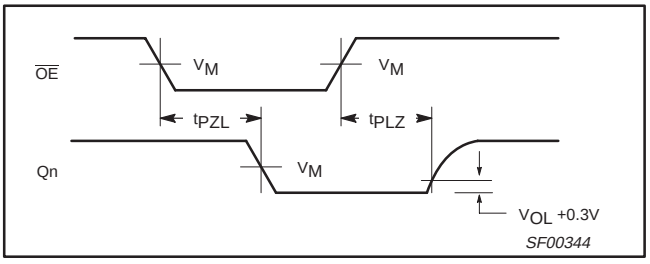
Waveform 2. Propagation Delay for Inverting Output



Waveform 3. Propagation Delay for $\overline{INV}$ to Output

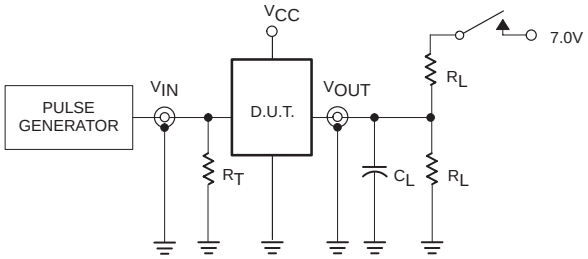


Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level

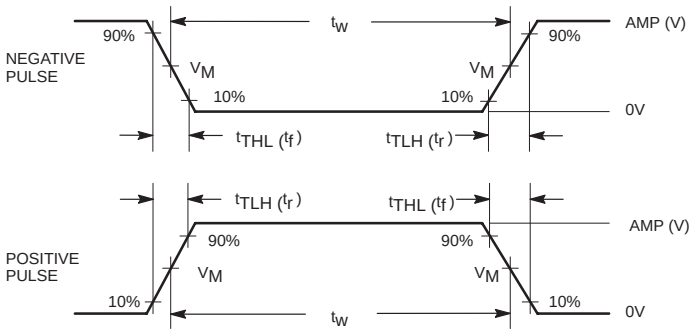


Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

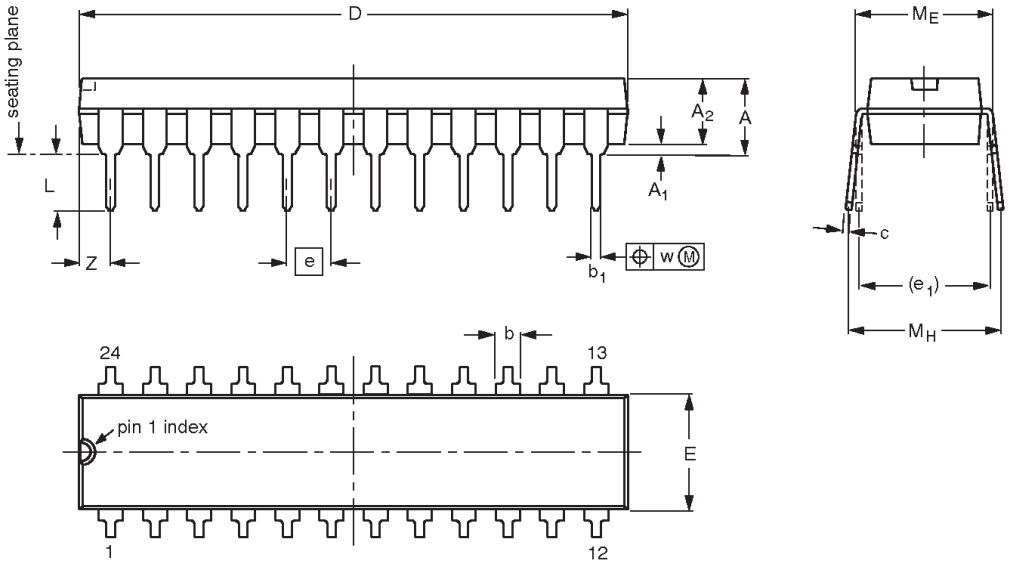
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

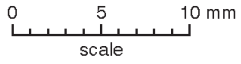
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00777

DIP24: plastic dual in-line package; 24 leads (300 mil) SOT222-1





DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

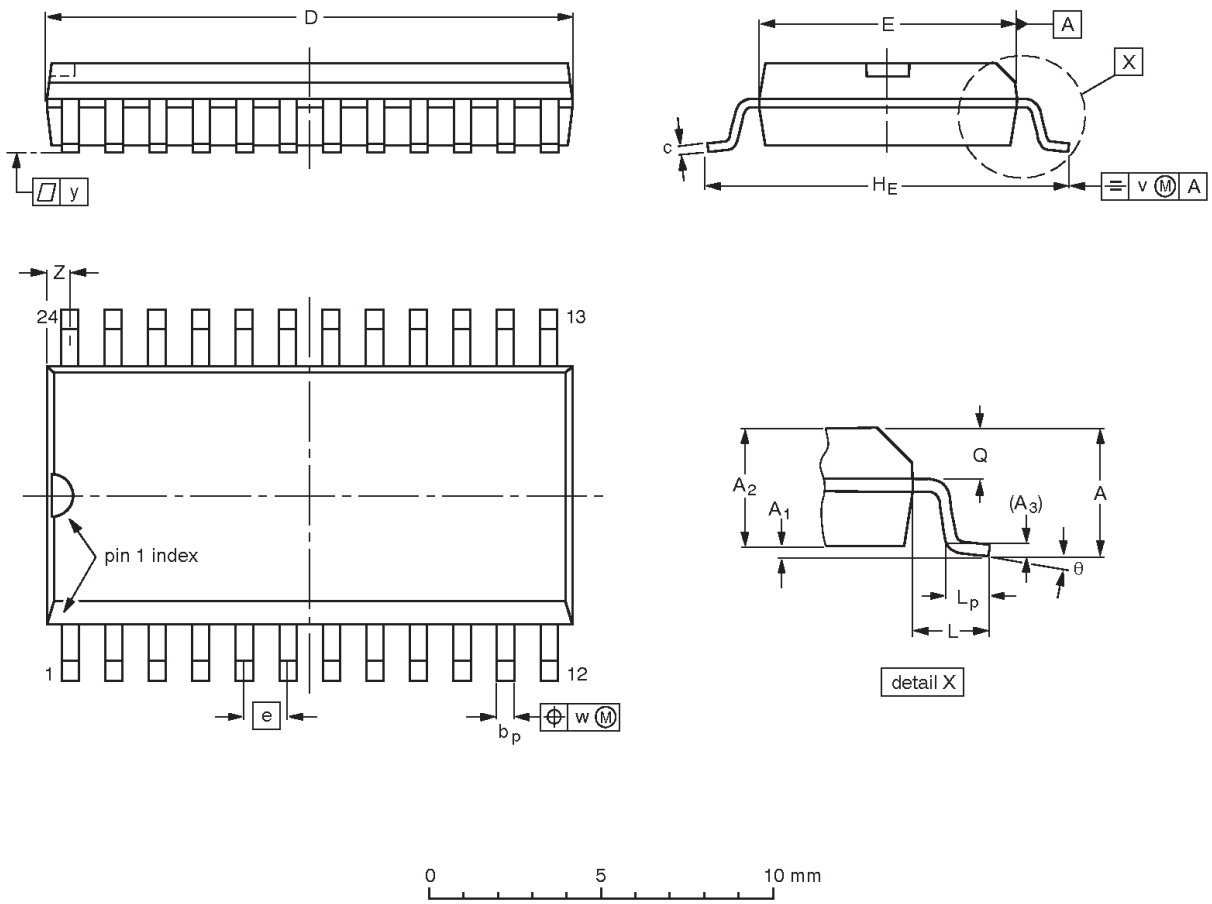
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.70	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.48	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.255	0.100	0.300	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT222-1		MS-001AF				95-03-11

SO24: plastic small outline package; 24 leads; body width 7.5 mm SOT137-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~95-01-24~~ 97-05-22

NOTES

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