# AK4643

## Stereo CODEC with MIC/HP/RCV/SPK-AMP

## GENERAL DESCRIPTION

The AK4643 is a stereo CODEC with a built-in Microphone-Amplifier, Headphone-Amplifier, Receiver-Amplifier and 1.2W output Speaker-Amplifier. The AK4643 features analog mixing circuits and PLL that allows easy interfacing in mobile phone and portable A/V player designs. The AK4643 is available in a 32pin QFN, utilizing less board space than competitive offerings.

## FEATURES

**1. Recording Function**
- **3 Stereo Input Selector**
- **Stereo Mic Input (Full-differential or Single-ended)**
- **Stereo Line Input**
- **MIC Amplifier (+32dB/+26dB/+20dB or 0dB)**
- **Digital ALC (Automatic Level Control)**
  **(+36dB ~ –54dB, 0.375dB Step, Mute)**
- **ADC Performance: S/(N+D): 83dB, DR, S/N: 86dB (MIC-Amp=+20dB)**
  **S/(N+D): 88dB, DR, S/N: 95dB (MIC-Amp=0dB)**
- **Wind-noise Reduction Filter**
- **Stereo Separation Emphasis**
- **Programmable EQ**

**2. Playback Function**
- **Digital De-emphasis Filter (tc=50/15μs, fs=32kHz, 44.1kHz, 48kHz)**
- **Bass Boost**
- **Soft Mute**
- **Digital Volume (+12dB ~ –115.0dB, 0.5dB Step, Mute)**
- **Digital ALC (Automatic Level Control)**
  **(+36dB ~ –54dB, 0.375dB Step, Mute)**
- **Stereo Separation Emphasis**
- **Programmble EQ**
- **Stereo Line Output**
  **- Performance: S/(N+D): 88dB, S/N: 92dB**
- **Mono Receiver-Amp**
  **- BTL Output**
  **- Output Power: 30mW@32Ω (AVDD=3.3V)**
- **Stereo Headphone-Amp**
  **- S/(N+D): 70dB@7.5mW, S/N: 90dB**
  **- Output Power: 70mW@16Ω (HVDD=5V), 62mW@16Ω (HVDD=3.3V)**
  **- Pop Noise Free at Power ON/OFF**
- **Mono Speaker-Amp**
  **- S/(N+D): 50dB@240mW, S/N: 90dB**
  **- BTL Output**
  **- Availbable for both Dynamic and Piezo Speaker**
  **- Output Power: 1.2W@8Ω (HVDD=5V), 400mW@8Ω (HVDD=3.3V)**
  **3.0Vrms@50Ω (HVDD=5V)**
- **Analog Mixing: 3 Stereo Input**

**3. Power Management**

**4. Master Clock:**

**(1) PLL Mode**
- **Frequencies:**
  **11.2896MHz, 12MHz, 12.288MHz, 13.5MHz, 24MHz, 27MHz (MCKI pin)**
  **1fs (LRCK pin)**
  **32fs or 64fs (BICK pin)**

**(2) External Clock Mode**
- **Frequencies: 256fs, 512fs or 1024fs (MCKI pin)**

**5. Output Master Clock Frequencies: 32fs/64fs/128fs/256fs**
**6. Sampling Rate:**
- **PLL Slave Mode (LRCK pin): 7.35kHz ~ 48kHz**
- **PLL Slave Mode (BICK pin): 7.35kHz ~ 48kHz**
- **PLL Slave Mode (MCKI pin):**
  **8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz**
- **PLL Master Mode:**
  **8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz**
- **EXT Master/Slave Mode:**
  **7.35kHz ~ 48kHz (256fs), 7.35kHz ~ 26kHz (512fs), 7.35kHz ~ 13kHz (1024fs)**

**7. μP I/F: 3-wire Serial, $I^2C$ Bus (Ver 1.0, 400kHz High Speed Mode)**
**8. Master/Slave mode**
**9. Audio Interface Format: MSB First, 2's complement**
- **ADC : 16bit MSB justified, $I^2S$, DSP Mode**
- **DAC : 16bit MSB justified, 16bit LSB justified, 16-24bit $I^2S$, DSP Mode**

**10. Ta = –30 ~ 85°C (SPK-Amp=OFF)**
**–30 ~ 70°C (SPK-Amp=ON)**
**11. Power Supply:**
- **AVDD, DVDD: 2.6 ~ 3.6V (typ. 3.3V)**
- **HVDD: 2.6 ~ 5.25V (typ. 3.3V/5.0V)**

**12. Package: 32pin QFN (5mm x 5mm, 0.5mm pitch)**
**13. Pin/Register Compatible with AK4642EN**

## ■ Block Diagram

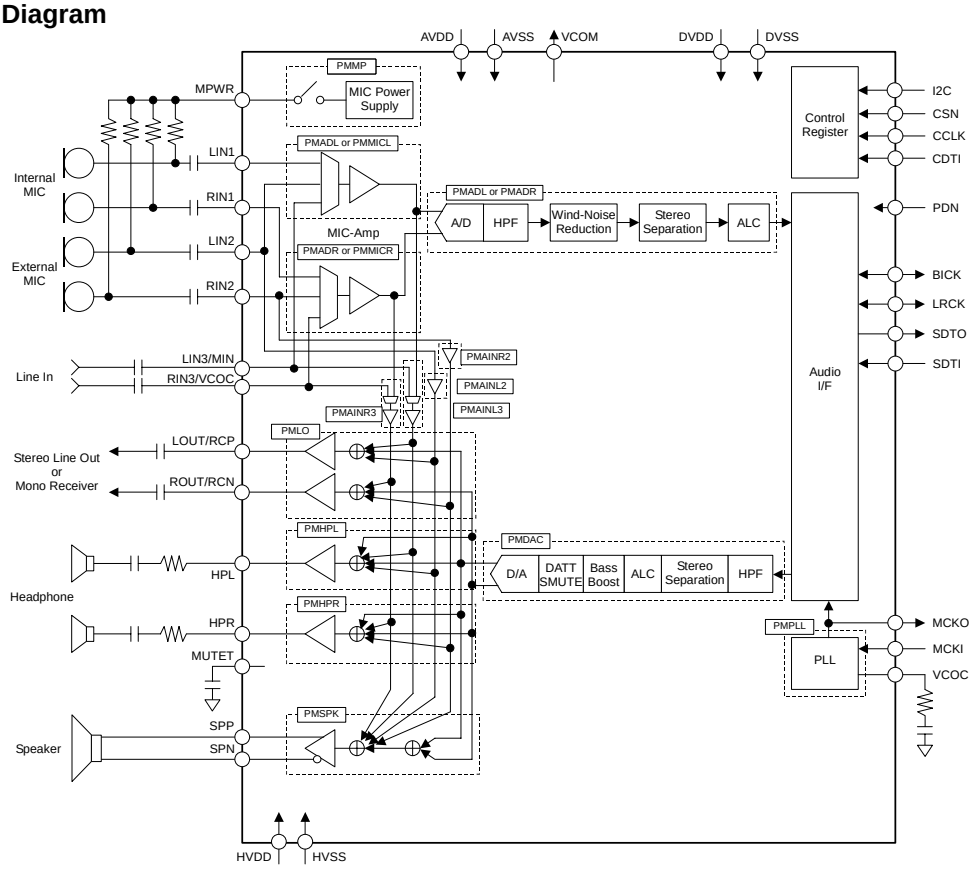
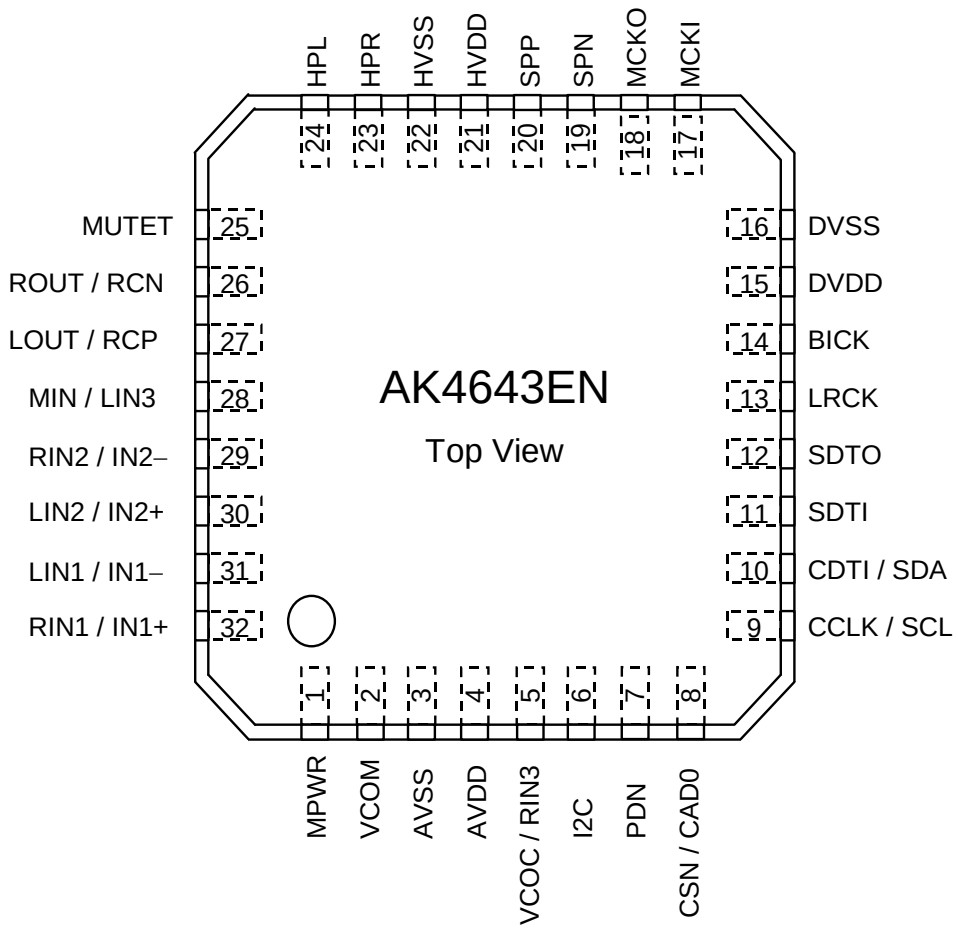



Figure 1. Block Diagram

## ■ Ordering Guide

| | | |
|---|---|---|
| AK4643EN | –30 ~ +85°C | 32pin QFN (0.5mm pitch) |
| AKD4643 | Evaluation board for AK4643 | |

## ■ Pin Layout




## ■ Compatibility with AK4642EN

### 1. Function

| Function | AK4642EN | AK4643 |
|---|---|---|
| SPK-Amp Max Output Power | 400mW@3.3V | 1.2W@5V |
| HP-Amp Max Output Power | 62mW@3.3V | 70mW@5V |
| Receiver-Amp | No | Yes |
| Analog Mixing for Playback | 1 Mono | 3 Stereo |
| Input Selector for Recording | 2 Stereo | 3 Stereo |
| Mono Recording Mode | No | Yes |
| ALC Recovery Waiting Period | 128/fs ~ 1024/fs | 128/fs ~ 16384/fs |
| ALC Fast Recovery Speed | 4 times | 4, 8 or 16 times |
| DSP Format | No | Yes |
| EXT Master Mode | No | Yes |
| DAC Group Delay | 22/fs | 25/fs |

## 2. Pin

| Pin# | AK4642EN | AK4643 |
|---|---|---|
| 5 | VCOC | VCOC/RIN3 |
| 26 | ROUT | ROUT/RCN |
| 27 | LOUT | LOUT/RCP |
| 28 | MIN | MIN/LIN3 |

## 3. Register

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 00H | Power Management 1 | 0 | PMVCM | PMMIN | PMSPK | PMLO | PMDAC | 0 | PMADL |
| 01H | Power Management 2 | 0 | HPMTN | PMHPL | PMHPR | M/S | 0 | MCKO | PMPLL |
| 02H | Signal Select 1 | SPPSN | MINS | DACS | DACL | 0 | PMMP | 0 | MGAIN0 |
| 03H | Signal Select 2 | LOVL | LOPS | MGAIN1 | SPKG1 | SPKG0 | MINL | 0 | 0 |
| 04H | Mode Control 1 | PLL3 | PLL2 | PLL1 | PLL0 | BCKO | 0 | DIF1 | DIF0 |
| 05H | Mode Control 2 | PS1 | PS0 | FS3 | MSBS | BCKP | FS2 | FS1 | FS0 |
| 06H | Timer Select | DVTM | WTM2 | ZTM1 | ZTM0 | WTM1 | WTM0 | RFST1 | RFST0 |
| 07H | ALC Mode Control 1 | 0 | 0 | ALC | ZELMN | LMAT1 | LMAT0 | RGAIN0 | LMTH0 |
| 08H | ALC Mode Control 2 | REF7 | REF6 | REF5 | REF4 | REF3 | REF2 | REF1 | REF0 |
| 09H | Lch Input Volume Control | IVL7 | IVL6 | IVL5 | IVL4 | IVL3 | IVL2 | IVL1 | IVL0 |
| 0AH | Lch Digital Volume Control | DVL7 | DVL6 | DVL5 | DVL4 | DVL3 | DVL2 | DVL1 | DVL0 |
| 0BH | ALC Mode Control 3 | RGAIN1 | LMTH1 | 0 | 0 | 0 | 0 | VBAT | 0 |
| 0CH | Rch Input Volume Control | IVR7 | IVR6 | IVR5 | IVR4 | IVR3 | IVR2 | IVR1 | IVR0 |
| 0DH | Rch Digital Volume Control | DVR7 | DVR6 | DVR5 | DVR4 | DVR3 | DVR2 | DVR1 | DVR0 |
| 0EH | Mode Control 3 | 0 | LOOP | SMUTE | DVOLC | BST1 | BST0 | DEM1 | DEM0 |
| 0FH | Mode Control 4 | 0 | 0 | 0 | 0 | IVOLC | HPM | MINH | DACH |
| 10H | Power Management 3 | INR1 | INL1 | HPG | MDIF2 | MDIF1 | INR0 | INL0 | PMADR |
| 11H | Digital Filter Select | GN1 | GN0 | 0 | FIL1 | EQ | FIL3 | 0 | 0 |
| 12H | FIL3 Co-efficient 0 | F3A7 | F3A6 | F3A5 | F3A4 | F3A3 | F3A2 | F3A1 | F3A0 |
| 13H | FIL3 Co-efficient 1 | F3AS | 0 | F3A13 | F3A12 | F3A11 | F3A10 | F3A9 | F3A8 |
| 14H | FIL3 Co-efficient 2 | F3B7 | F3B6 | F3B5 | F3B4 | F3B3 | F3B2 | F3B1 | F3B0 |
| 15H | FIL3 Co-efficient 3 | 0 | 0 | F3B13 | F3B12 | F3B11 | F3B10 | F3B9 | F3B8 |
| 16H | EQ Co-efficient 0 | EQA7 | EQA6 | EQA5 | EQA4 | EQA3 | EQA2 | EQA1 | EQA0 |
| 17H | EQ Co-efficient 1 | EQA15 | EQA14 | EQA13 | EQA12 | EQA11 | EQA10 | EQA9 | EQA8 |
| 18H | EQ Co-efficient 2 | EQB7 | EQB6 | EQB5 | EQB4 | EQB3 | EQB2 | EQB1 | EQB0 |
| 19H | EQ Co-efficient 3 | 0 | 0 | EQB13 | EQB12 | EQB11 | EQB10 | EQB9 | EQB8 |
| 1AH | EQ Co-efficient 4 | EQC7 | EQC6 | EQC5 | EQC4 | EQC3 | EQC2 | EQC1 | EQC0 |
| 1BH | EQ Co-efficient 5 | EQC15 | EQC14 | EQC13 | EQC12 | EQC11 | EQC10 | EQC9 | EQC8 |
| 1CH | FIL1 Co-efficient 0 | F1A7 | F1A6 | F1A5 | F1A4 | F1A3 | F1A2 | F1A1 | F1A0 |
| 1DH | FIL1 Co-efficient 1 | F1AS | 0 | F1A13 | F1A12 | F1A11 | F1A10 | F1A9 | F1A8 |
| 1EH | FIL1 Co-efficient 2 | F1B7 | F1B6 | F1B5 | F1B4 | F1B3 | F1B2 | F1B1 | F1B0 |
| 1FH | FIL1 Co-efficient 3 | 0 | 0 | F1B13 | F1B12 | F1B11 | F1B10 | F1B9 | F1B8 |
| 20H | Power Management 4 | 0 | 0 | PMAINR3 | PMAINL3 | PMAINR2 | PMAINL2 | PMMICR | PMMICL |
| 21H | Mode Control 5 | 0 | 0 | MICR3 | MICL3 | 0 | MIX | AIN3 | RCV |
| 22H | Lineout Mixing Select | 0 | 0 | 0 | 0 | RINR3 | LINL3 | RINR2 | LINL2 |
| 23H | HP Mixing Select | 0 | 0 | 0 | 0 | RINH3 | LINH3 | RINH2 | LINH2 |
| 24H | SPK Mixing Select | 0 | 0 | 0 | 0 | RINS3 | LINS3 | RINS2 | LINS2 |

These bits are added in the AK4643.

## PIN/FUNCTION

| No. | Pin Name | I/O | Function |
|---|---|---|---|
| 1 | MPWR | O | MIC Power Supply Pin |
| 2 | VCOM | O | Common Voltage Output Pin, 0.45 x AVDD<br>Bias voltage of ADC inputs and DAC outputs. |
| 3 | AVSS | - | Analog Ground Pin |
| 4 | AVDD | - | Analog Power Supply Pin |
| 5 | VCOC | O | Output Pin for Loop Filter of PLL Circuit (AIN3 bit = "0": PLL is available.)<br>This pin should be connected to AVSS with one resistor and capacitor in series. |
| | RIN3 | I | Rch Analog Input 3 Pin (AIN3 bit = "1": PLL is not available.) |
| 6 | I2C | I | Control Mode Select Pin<br>"H": $I^2C$ Bus, "L": 3-wire Serial |
| 7 | PDN | I | Power-Down Mode Pin<br>"H": Power-up, "L": Power-down, reset and initializes the control register. |
| 8 | CSN | I | Chip Select Pin (I2C pin = "L": 3-wire Serial Mode) |
| | CAD0 | I | Chip Address 1 Select Pin (I2C pin = "H": $I^2C$ Bus Mode) |
| 9 | CCLK | I | Control Data Clock Pin (I2C pin = "L": 3-wire Serial Mode) |
| | SCL | I | Control Data Clock Pin (I2C pin = "H": $I^2C$ Bus Mode) |
| 10 | CDTI | I | Control Data Input Pin (I2C pin = "L": 3-wire Serial Mode) |
| | SDA | I/O | Control Data Input Pin (I2C pin = "H": $I^2C$ Bus Mode) |
| 11 | SDTI | I | Audio Serial Data Input Pin |
| 12 | SDTO | O | Audio Serial Data Output Pin |
| 13 | LRCK | I/O | Input / Output Channel Clock Pin |
| 14 | BICK | I/O | Audio Serial Data Clock Pin |
| 15 | DVDD | - | Digital Power Supply Pin |
| 16 | DVSS | - | Digital Ground Pin |
| 17 | MCKI | I | External Master Clock Input Pin |
| 18 | MCKO | O | Master Clock Output Pin |
| 19 | SPN | O | Speaker Amp Negative Output Pin |
| 20 | SPP | O | Speaker Amp Positive Output Pin |
| 21 | HVDD | - | Headphone & Speaker Amp Power Supply Pin |
| 22 | HVSS | - | Headphone & Speaker Amp Ground Pin |
| 23 | HPR | O | Rch Headphone-Amp Output Pin |
| 24 | HPL | O | Lch Headphone-Amp Output Pin |
| 25 | MUTET | O | Mute Time Constant Control Pin<br>Connected to HVSS pin with a capacitor for mute time constant. |
| 26 | ROUT | O | Rch Stereo Line Output Pin (RCV bit = "0": Single-ended Stereo Output) |
| | RCN | O | Receiver-Amp Negative Output Pin (RCV bit = "1": BTL output) |
| 27 | LOUT | O | Lch Stereo Line Output Pin (RCV bit = "0": Single-ended Stereo Output) |
| | RCP | O | Receiver-Amp Positive Output Pin (RCV bit = "1": BTL output) |
| 28 | MIN | I | Mono Signal Input Pin (AIN3 bit = "0": PLL is available.) |
| | LIN3 | I | Lch Analog Input 3 Pin (AIN3 bit = "1: PLL is not available") |
| 29 | RIN2 | I | Rch Analog Input 2 Pin (MDIF2 bit = "0": Single-ended Input) |
| | IN2− | I | Microphone Negative Input 2 Pin (MDIF2 bit = "1": Full-differential Input) |
| 30 | LIN2 | I | Lch Analog Input 2 Pin (MDIF2 bit = "0": Single-ended Input) |
| | IN2+ | I | Microphone Positive Input 2 Pin (MDIF2 bit = "1": Full-differential Input) |
| 31 | LIN1 | I | Lch Analog Input 1 Pin (MDIF1 bit = "0": Single-ended Input) |
| | IN1− | I | Microphone Negative Input 1 Pin (MDIF1 bit = "1": Full-differential Input) |
| 32 | RIN1 | I | Rch Analog Input 1 Pin (MDIF1 bit = "0": Single-ended Input) |
| | IN1+ | I | Microphone Positive Input 1 Pin (MDIF1 bit = "1": Full-differential Input) |

Note 1. All input pins except analog input pins (MIN/LIN3, LIN1, RIN1, LIN2, RIN2, RIN3) should not be left floating.
Note 2. AVDD or AVSS voltage should be input to I2C pin.

## ■ Handling of Unused Pin

The unused I/O pins should be processed appropriately as below.

| Classification | Pin Name | Setting |
|---|---|---|
| Analog | MPWR, VCOC/RIN3, SPN, SPP, HPR, HPL, MUTET, ROUT/RCN, LOUT/RCP, MIN/LIN3, RIN2/IN2–, LIN2/IN2+, LIN1/IN1–, RIN1/IN1+ | These pins should be open. |
| Digital | MCKO | This pin should be open. |
| | MCKI | This pin should be connected to DVSS. |

## ABSOLUTE MAXIMUM RATINGS

(AVSS, DVSS, HVSS=0V; Note 3)

| Parameter | | Symbol | min | max | Units |
|---|---|---|---|---|---|
| Power Supplies: | Analog | AVDD | –0.3 | 6.0 | V |
| | Digital | DVDD | –0.3 | 6.0 | V |
| | Headphone-Amp / Speaker-Amp | HVDD | –0.3 | 6.0 | V |
| | \|AVSS – DVSS\| (Note 4) | ΔGND1 | - | 0.3 | V |
| | \|AVSS – HVSS\| (Note 4) | ΔGND2 | - | 0.3 | V |
| Input Current, Any Pin Except Supplies | | IIN | - | ±10 | mA |
| Analog Input Voltage (Note 5) | | VINA | –0.3 | AVDD+0.3 | V |
| Digital Input Voltage (Note 6) | | VIND | –0.3 | DVDD+0.3 | V |
| Ambient Temperature (powered applied) | | Ta | –30 | 85 | °C |
| Storage Temperature | | Tstg | –65 | 150 | °C |
| Maximum Power Dissipation (Note 7) | Ta=85°C (Note 8) | Pd1 | - | 750 | mW |
| | Ta=70°C (Note 9) | Pd2 | - | 1000 | mW |

Note 3. All voltages with respect to ground.
Note 4. AVSS, DVSS and HVSS must be connected to the same analog ground plane.
Note 5. I2C, MIN/LIN3, RIN3, RIN2/IN2–, LIN2/IN2+, LIN1/IN1–, RIN1/IN1+ pins
Note 6. PDN, CSN/CAD0, CCLK/SCL, CDTI/SDA, SDTI, LRCK, BICK, MCKI pins
Pull-up resistors at SDA and SCL pins should be connected to (DVDD+0.3)V or less voltage.
Note 7. In case that the exposed pad is connected to the ground and PCB wiring density is 100%. If the exposed pad is open, Pd1=400mW(max: Speaker-Amp is not available.) and Pd2=550mW(max: Speaker-Amp is available at HVDD=2.6~3.6V.). This power is the AK4643 internal dissipation that does not include power of externally connected speaker and headphone.
Note 8. Speaker-Amp is available at HVDD=2.6~3.6V.
Note 9. Speaker-Amp is available at HVDD=2.6~5.25V.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

## RECOMMENDED OPERATING CONDITIONS

(AVSS, DVSS, HVSS=0V; Note 3)

| Parameter | | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|---|
| Power Supplies (Note 10) | Analog | AVDD | 2.6 | 3.3 | 3.6 | V |
| | Digital | DVDD | 2.6 | 3.3 | 3.6 | V |
| | HP / SPK-Amp | HVDD | 2.6 | 3.3 / 5.0 | 5.25 | V |
| | Difference | AVDD–DVDD | –0.3 | 0 | +0.3 | V |

Note 3. All voltages with respect to ground.

Note 10. The power-up sequence between AVDD, DVDD and HVDD is not critical. When only AVDD or HVDD is powered OFF, the power supply current of DVDD at power-down mode may be increased. DVDD should not be powered OFF while AVDD or HVDD is powered ON.

* AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

## ANALOG CHARACTERISTICS

(Ta=25°C; AVDD, DVDD, HVDD=3.3V; AVSS=DVSS=HVSS=0V; fs=44.1kHz, BICK=64fs;
Signal Frequency=1kHz; 16bit Data; Measurement frequency=20Hz ~ 20kHz; unless otherwise specified)

| Parameter | | min | typ | max | Units |
|---|---|---|---|---|---|
| **MIC Amplifier:** LIN1/RIN1/LIN2/RIN2 pins & LIN3/RIN3 pins (AIN3 bit = "1"); MDIF1=MDIF2 bits = "0" (Single-ended inputs) | | | | | |
| Input Resistance | MGAIN1-0 bits = "00" | 40 | 60 | 80 | kΩ |
| | MGAIN1-0 bits = "01", "10"or "11" | 20 | 30 | 40 | kΩ |
| Gain | MGAIN1-0 bits = "00" | - | 0 | - | dB |
| | MGAIN1-0 bits = "01" | - | +20 | - | dB |
| | MGAIN1-0 bits = "10" | - | +26 | - | dB |
| | MGAIN1-0 bits = "11" | - | +32 | - | dB |
| **MIC Amplifier:** IN1+/IN1–/IN2+/IN2– pins; MDIF1 = MDIF2 bits = "1" (Full-differential input) | | | | | |
| Maximum Input Voltage (Note 11) | | | | | |
| | MGAIN1-0 bits = "01" | - | - | 0.228 | Vpp |
| | MGAIN1-0 bits = "10" | - | - | 0.114 | Vpp |
| | MGAIN1-0 bits = "11" | - | - | 0.057 | Vpp |
| **MIC Power Supply:** MPWR pin | | | | | |
| Output Voltage (Note 12) | | 2.22 | 2.47 | 2.72 | V |
| Load Resistance | | 0.5 | - | - | kΩ |
| Load Capacitance | | - | - | 30 | pF |

Note 11. The voltage difference between IN1/2+ and IN1/2– pins. AC coupling capacitor should be inserted in series at each input pin. Full-differential mic input is not available at MGAIN1-0 bits = "00". Maximum input voltage of IN1+, IN1–, IN2+ and IN2– pins is proportional to AVDD voltage, respectively.
Vin = 0.069 x AVDD (max)@MGAIN1-0 bits = "01", 0.035 x AVDD (max)@MGAIN1-0 bits = "10", 0.017 x AVDD (max)@MGAIN1-0 bits = "11".
When the signal larger than above value is input to IN1+, IN1–, IN2+ or IN2– pin, ADC does not operate normally.

Note 12. Output voltage is proportional to AVDD voltage. Vout = 0.75 x AVDD (typ)

| Parameter | | | min | typ | max | Units |
|---|---|---|---|---|---|---|
| **ADC Analog Input Characteristics:** LIN1/RIN1/LIN2/RIN2 pins & LIN3/RIN3 pins (AIN3 bit = "1") → ADC → IVOL, IVOL=0dB, ALC=OFF | | | | | | |
| Resolution | | | - | - | 16 | Bits |
| Input Voltage (Note 13) | | (Note 14) | 0.168 | 0.198 | 0.228 | Vpp |
| | | (Note 15) | 1.68 | 1.98 | 2.28 | Vpp |
| S/(N+D) (–1dBFS) | (Note 14, LIN1/RIN1/LIN2/RIN2) | | 71 | 83 | - | dBFS |
| | (Note 14, LIN3/RIN3) | | - | 83 | - | dBFS |
| | (Note 15, LIN1/RIN1/LIN2/RIN2) | | - | 88 | - | dBFS |
| | (Note 15, LIN3/RIN3) | | - | 72 | - | dBFS |
| D-Range (–60dBFS, A-weighted) | | (Note 14) | 76 | 86 | - | dB |
| | | (Note 15) | - | 95 | - | dB |
| S/N (A-weighted) | | (Note 14) | 76 | 86 | - | dB |
| | | (Note 15) | - | 95 | - | dB |
| Interchannel Isolation | | (Note 14) | 75 | 90 | - | dB |
| | | (Note 15) | - | 100 | - | dB |
| Interchannel Gain Mismatch | | (Note 14) | - | 0.1 | 0.8 | dB |
| | | (Note 15) | - | 0.1 | 0.8 | dB |
| **DAC Characteristics:** | | | | | | |
| Resolution | | | - | - | 16 | Bits |
| **Stereo Line Output Characteristics:** DAC → LOUT/ROUT pins, ALC=OFF, IVOL=0dB, DVOL=0dB, LOVL bit = "0", RCV bit = "0", $R_L$=10kΩ | | | | | | |
| Output Voltage (Note 16) | | LOVL bit = "0" | 1.78 | 1.98 | 2.18 | Vpp |
| | | LOVL bit = "1" | 2.25 | 2.50 | 2.75 | Vpp |
| S/(N+D) (–3dBFS) | | | 78 | 88 | - | dBFS |
| S/N (A-weighted) | | | 82 | 92 | - | dB |
| Interchannel Isolation | | | | | | |
| | PMAINL2/R2/L3/R3 bits = "1" | | 80 | 100 | - | dB |
| | PMAINL2/R2/L3/R3 bits = "0" | | - | 100 | - | dB |
| Interchannel Gain Mismatch | | | - | 0.1 | 0.5 | dB |
| Load Resistance | | | 10 | - | - | kΩ |
| Load Capacitance | | | - | - | 30 | pF |
| **Mono Receiver Output Characteristics:** DAC → RCP/RCN pins, ALC=OFF, IVOL=0dB, DVOL=0dB, LOVL bit = "0", RCV bit = "1", $R_L$=32Ω, BTL | | | | | | |
| Output Voltage (Note 17) | | | | | | |
| LOVL bit = "0", –6dBFS, $R_L$=32Ω (Po=15mW) | | | 1.57 | 1.96 | 2.35 | Vpp |
| LOVL bit = "0", –3dBFS, $R_L$=32Ω (Po=30mW) | | | - | 2.77 | - | Vpp |
| LOVL bit = "1", –8dBFS, $R_L$=32Ω (Po=15mW) | | | 1.57 | 1.96 | 2.35 | Vpp |
| LOVL bit = "1", –5dBFS, $R_L$=32Ω (Po=30mW) | | | - | 2.77 | - | Vpp |
| S/(N+D) | | | | | | |
| LOVL bit = "0", –6dBFS, $R_L$=32Ω (Po=15mW) | | | 40 | 60 | - | dB |
| LOVL bit = "0", –3dBFS, $R_L$=32Ω (Po=30mW) | | | - | 60 | - | dB |
| S/N (A-weighted) | | | 85 | 95 | - | dBFS |
| Load Resistance | | | 32 | - | - | Ω |
| Load Capacitance | | | - | - | 30 | pF |

Note 13. Input voltage is proportional to AVDD voltage. Vin = 0.06 x AVDD (typ)@MGAIN1-0 bits = "01" (+20dB), Vin = 0.6 x AVDD(typ)@MGAIN1-0 bits = "00" (0dB)

Note 14. MGAIN1-0 bits = "01" (+20dB)

Note 15. MGAIN1-0 bits = "00" (0dB)

Note 16. Output voltage is proportional to AVDD voltage. Vout = 0.6 x AVDD (typ)@LOVL bit = "0".

Note 17. Output voltage is proportional to AVDD voltage. Vout = (RCP) – (RCN) = 0.59 x AVDD (typ)@LOVL bit = "0", –6dBFS.

| Parameter | | | min | typ | max | Units |
|---|---|---|---|---|---|---|
| **Headphone-Amp Characteristics:** DAC → HPL/HPR pins, ALC=OFF, IVOL=0dB, DVOL=0dB, VBAT bit = "0"; unless otherwise specified. | | | | | | |
| Output Voltage (Note 18) | | | | | | |
| HPG bit = "0", 0dBFS, HVDD=3.3V, $R_L$=22.8Ω | | | 1.58 | 1.98 | 2.38 | Vpp |
| HPG bit = "1", 0dBFS, HVDD=5V, $R_L$=100Ω | | | 2.40 | 3.00 | 3.60 | Vpp |
| HPG bit = "1", 0dBFS, HVDD=3.3V, $R_L$=16Ω (Po=62mW) | | | - | 1.0 | - | Vrms |
| HPG bit = "1", 0dBFS, HVDD=5V, $R_L$=16Ω (Po=70mW) | | | - | 1.06 | - | Vrms |
| S/(N+D) | | | | | | |
| HPG bit = "0", –3dBFS, HVDD=3.3V, $R_L$=22.8Ω | | | 60 | 70 | - | dBFS |
| HPG bit = "1", –3dBFS, HVDD=5V, $R_L$=100Ω | | | - | 80 | - | dBFS |
| HPG bit = "1", 0dBFS, HVDD=3.3V, $R_L$=16Ω (Po=62mW) | | | - | 20 | - | dBFS |
| HPG bit = "1", 0dBFS, HVDD=5V, $R_L$=16Ω (Po=70mW) | | | - | 70 | - | dBFS |
| S/N (A-weighted) | | (Note 19) | 80 | 90 | - | dB |
| | | (Note 20) | - | 90 | - | dB |
| Interchannel Isolation | | | | | | |
| | (Note 19), PMAINL2/R2/L3/R3 bits = "1" | | 65 | 75 | - | dB |
| | (Note 19), PMAINL2/R2/L3/R3 bits = "0" | | - | 75 | - | dB |
| | (Note 20) | | - | 80 | - | dB |
| Interchannel Gain Mismatch | | (Note 19) | - | 0.1 | 0.8 | dB |
| | | (Note 20) | - | 0.1 | 0.8 | dB |
| Load Resistance | | | 16 | - | - | Ω |
| Load Capacitance | C1 in Figure 2 | | - | - | 30 | pF |
| | C2 in Figure 2 | | - | - | 300 | pF |

Note 18. Output voltage is proportional to AVDD voltage.
Vout = 0.6 x AVDD(typ)@HPG bit = "0", 0.91 x AVDD(typ)@HPG bit = "1".
Note 19. HPG bit = "0", HVDD=3.3V, $R_L$=22.8Ω.
Note 20. HPG bit = "1", HVDD=5V, $R_L$=100Ω.

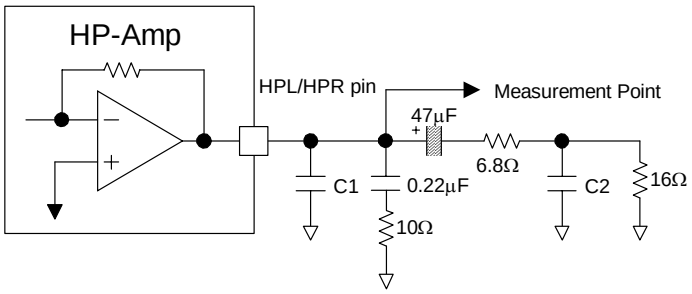



Figure 2. Headphone-Amp output circuit

| Parameter | | | min | typ | max | Units |
|---|---|---|---|---|---|---|
| **Speaker-Amp Characteristics:** DAC → SPP/SPN pins, ALC=OFF, IVOL=0dB, DVOL=0dB, $R_L$=8Ω, BTL, HVDD=3.3V; unless otherwise specified. | | | | | | |
| Output Voltage (Note 21) | | | | | | |
| | SPKG1-0 bits = "00", –0.5dBFS (Po=150mW) | | - | 3.11 | - | Vpp |
| | SPKG1-0 bits = "01", –0.5dBFS (Po=240mW) | | 3.13 | 3.92 | 4.71 | Vpp |
| | HVDD=5V, SPKG1-0 bits = "11", 0dBFS (Po=1W) | | - | 2.83 | - | Vrms |
| | Line Input → SPP/SPN pins, HVDD=5V, SPKG1-0 bits = "11", –1.5dBV Input (Po=1.2W) | | - | 3.1 | - | Vrms |
| S/(N+D) | | | | | | |
| | SPKG1-0 bits = "00", –0.5dBFS (Po=150mW) | | - | 60 | - | dB |
| | SPKG1-0 bits = "01", –0.5dBFS (Po=240mW) | | 20 | 50 | - | dB |
| | HVDD=5V, SPKG1-0 bits = "11", 0dBFS (Po=1W) | | - | 30 | - | dB |
| | Line Input → SPP/SPN pins, HVDD=5V, SPKG1-0 bits = "11", –1.5dBV Input (Po=1.2W) | | - | 20 | - | dB |
| S/N (A-weighted) | | | 80 | 90 | - | dB |
| Load Resistance | | | 8 | - | - | Ω |
| Load Capacitance | | | - | - | 30 | pF |
| **Speaker-Amp Characteristics:** DAC → SPP/SPN pins, ALC=OFF, IVOL=0dB, DVOL=0dB, $C_L$=3μF, $R_{series}$=10Ω x 2, BTL, HVDD=5.0V; unless otherwise specified. | | | | | | |
| Output Voltage (Note 21) | SPKG1-0 bits = "10", 0dBFS | | - | 6.75 | - | Vpp |
| | SPKG1-0 bits = "11", 0dBFS | | 6.80 | 8.50 | 10.20 | Vpp |
| S/(N+D) (Note 22) | SPKG1-0 bits = "10", 0dBFS | | - | 60 | - | dB |
| | SPKG1-0 bits = "11", 0dBFS | | 40 | 50 | - | dB |
| S/N (A-weighted) | | | 80 | 90 | - | dB |
| Load Resistance (Note 23) | | | 50 | - | - | Ω |
| Load Capacitance (Note 23) | | | - | - | 3 | μF |
| **Mono Input:** MIN pin (AIN3 bit = "0"; External Input Resistance=20kΩ) | | | | | | |
| Maximum Input Voltage (Note 24) | | | - | 1.98 | - | Vpp |
| Gain (Note 25) | | | | | | |
| | MIN → LOUT/ROUT | LOVL bit = "0" | –4.5 | 0 | +4.5 | dB |
| | | LOVL bit = "1" | - | +2 | - | dB |
| | MIN → HPL/HPR | HPG bit = "0" | –24.5 | –20 | –15.5 | dB |
| | | HPG bit = "1" | - | –16.4 | - | dB |
| | MIN → SPP/SPN | | | | | |
| | | ALC bit = "0", SPKG1-0 bits = "00" | –0.07 | +4.43 | +8.93 | dB |
| | | ALC bit = "0", SPKG1-0 bits = "01" | - | +6.43 | - | dB |
| | | ALC bit = "0", SPKG1-0 bits = "10" | - | +10.65 | - | dB |
| | | ALC bit = "0", SPKG1-0 bits = "11" | - | +12.65 | - | dB |
| | | ALC bit = "1", SPKG1-0 bits = "00" | - | +6.43 | - | dB |
| | | ALC bit = "1", SPKG1-0 bits = "01" | - | +8.43 | - | dB |
| | | ALC bit = "1", SPKG1-0 bits = "10" | - | +12.65 | - | dB |
| | | ALC bit = "1", SPKG1-0 bits = "11" | - | +14.65 | - | dB |

Note 21. Output voltage is proportional to AVDD voltage.
Vout = 0.94 x AVDD(typ)@SPKG1-0 bits = "00", 1.19 x AVDD(typ)@SPKG1-0 bits = "01", 2.05 x AVDD(typ)@SPKG1-0 bits = "10", 2.58 x AVDD(typ)@SPKG1-0 bits = "11" at Full-differential output.

Note 22. In case of measuring at SPP and SPN pins.

Note 23. Load impedance is total impedance of series resistance ($R_{series}$) and piezo speaker impedance at 1kHz in Figure 61. Load capacitance is capacitance of piezo speaker. When piezo speaker is used, 10Ω or more series resistors should be connected at both SPP and SPN pins, respectively.

Note 24. Maximum voltage is in proportion to both AVDD and external input resistance (Rin). Vin = 0.6 x AVDD x Rin / 20kΩ (typ).

Note 25. The gain is in inverse proportion to external input resistance.

| Parameter | | | min | typ | max | Units |
|---|---|---|---|---|---|---|
| **Stereo Input:** LIN2/RIN2 pins; LIN3/RIN3 pins (AIN3 bit = "1") | | | | | | |
| Maximum Input Voltage (Note 26) | | | - | 1.98 | - | Vpp |
| Gain | | | | | | |
| LIN/RIN → LOUT/ROUT | | LOVL bit = "0" | –4.5 | 0 | +4.5 | dB |
| | | LOVL bit = "1" | - | +2 | - | dB |
| LIN/RIN → HPL/HPR | | HPG bit = "0" | –4.5 | 0 | +4.5 | dB |
| | | HPG bit = "1" | - | +3.6 | - | dB |
| LIN/RIN → SPP/SPN | | | | | | |
| | ALC bit = "0", SPKG1-0 bits = "00" | | –6.09 | –1.59 | +2.91 | dB |
| | ALC bit = "0", SPKG1-0 bits = "01" | | - | +0.41 | - | dB |
| | ALC bit = "0", SPKG1-0 bits = "10" | | - | +4.63 | - | dB |
| | ALC bit = "0", SPKG1-0 bits = "11" | | - | +6.63 | - | dB |
| | ALC bit = "1", SPKG1-0 bits = "00" | | - | +0.41 | - | dB |
| | ALC bit = "1", SPKG1-0 bits = "01" | | - | +2.41 | - | dB |
| | ALC bit = "1", SPKG1-0 bits = "10" | | - | +6.63 | - | dB |
| | ALC bit = "1", SPKG1-0 bits = "11" | | - | +8.63 | - | dB |
| **Power Supplies:** | | | | | | |
| Power-Up (PDN pin = "H") | | | | | | |
| All Circuit Power-up: | | | | | | |
| | AVDD+DVDD (Note 27) | | - | 16 | 24 | mA |
| | HVDD: HP-Amp Normal Operation No Output (Note 28) | | - | 5 | 8 | mA |
| | HVDD: SPK-Amp Normal Operation No Output (Note 29) | | - | 11 | 30 | mA |
| Power-Down (PDN pin = "L") (Note 30) | | | | | | |
| | AVDD+DVDD+HVDD | | - | 10 | 100 | μA |

Note 26. Output voltage is proportional to AVDD voltage. Vout = 0.6 x AVDD (typ).

Note 27. PLL Master Mode (MCKI=12.288MHz) and PMADL = PMADR = PMDAC = PMLO = PMHPL = PMHPR = PMSPK = PMVCM = PMPLL = MCKO = PMMIN = PMMP = M/S bits = "1". MPWR pin outputs 0mA. AVDD=12mA(typ), DVDD=4mA(typ).
EXT Slave Mode (PMPLL = M/S = MCKO bits = "0"): AVDD=11mA(typ), DVDD=3mA(typ).

Note 28. PMADL = PMADR = PMDAC = PMLO = PMHPL = PMHPR = PMVCM = PMPLL = PMMIN bits = "1" and PMSPK bit = "0".

Note 29. PMADL = PMADR = PMDAC = PMLO = PMSPK = PMVCM = PMPLL = PMMIN bits = "1" and PMHPL = PMHPR bits = "0".

Note 30. All digital input pins are fixed to DVDD or DVSS.

## ■ Power Consumption for each operation mode

Condtions: Ta=25°C; AVDD=DVDD=HVDD=3.3V; AVSS=DVSS=HVSS=0V; fs=44.1kHz, External Slave Mode,
BICK=64fs; 1kHz, 0dBFS input; Headphone & Speaker = No output

| Mode | Power Management Bit | | | | | | | | | | | | | | | AVDD [mA] | DVDD [mA] | HVDD [mA] | Total Power [mW] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 00H | | | | | | 01H | | 10H | 20H | | | | | | | | | |
| | PMVCM | PMMIN | PMSPK | PMLO | PMDAC | PMADL | PMHPL | PMHPR | PMADR | PMMICL | PMMICR | PMAINL2 | PMAINR2 | PMAINL3 | PMAINR3 | | | | |
| All Power-down | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| DAC → Lineout | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 5.4 | 1.8 | 0.2 | 24.4 |
| DAC → HP | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 3.7 | 1.8 | 5 | 34.7 |
| DAC → SPK | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 3.7 | 1.8 | 11 | 54.5 |
| LIN2/RIN2 → HP | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1.9 | 0 | 5 | 22.8 |
| LIN2/RIN2 → SPK | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1.9 | 0 | 11 | 42.6 |
| MIN → RCV | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 3.1 | 0 | 0.2 | 10.9 |
| LIN2/RIN2 → ADC | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 5.6 | 1.6 | 0.2 | 24.4 |
| LIN1 (Mono) → ADC | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 3.4 | 1.5 | 0.2 | 16.8 |
| LIN2/RIN2 → ADC & DAC → HP | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 8.1 | 2.8 | 5 | 52.5 |

Table 1. Power Consumption for each operation mode (typ)

## FILTER CHARACTERISTICS

(Ta=25°C; AVDD, DVDD=2.6 ~ 3.6V; HVDD=2.6 ~ 5.25V; fs=44.1kHz; DEM=OFF; FIL1=FIL3=EQ=OFF)

| Parameter | | | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|---|---|
| **ADC Digital Filter (Decimation LPF):** | | | | | | | |
| Passband (Note 31) | | ±0.16dB | PB | 0 | - | 17.3 | kHz |
| | | −0.66dB | | - | 19.4 | - | kHz |
| | | −1.1dB | | - | 19.9 | - | kHz |
| | | −6.9dB | | - | 22.1 | - | kHz |
| Stopband | | | SB | 26.1 | - | - | kHz |
| Passband Ripple | | | PR | - | - | ±0.1 | dB |
| Stopband Attenuation | | | SA | 73 | - | - | dB |
| Group Delay (Note 32) | | | GD | - | 19 | - | 1/fs |
| Group Delay Distortion | | | ΔGD | - | 0 | - | μs |
| **ADC Digital Filter (HPF):** (Note 33) | | | | | | | |
| Frequency Response (Note 31) | | −3.0dB | FR | - | 0.9 | - | Hz |
| | | −0.5dB | | - | 2.7 | - | Hz |
| | | −0.1dB | | - | 6.0 | - | Hz |
| **DAC Digital Filter (LPF):** | | | | | | | |
| Passband (Note 31) | | ±0.1dB | PB | 0 | - | 19.6 | kHz |
| | | −0.7dB | | - | 20.0 | - | kHz |
| | | −6.0dB | | - | 22.05 | - | kHz |
| Stopband | | | SB | 25.2 | - | - | kHz |
| Passband Ripple | | | PR | - | - | ±0.01 | dB |
| Stopband Attenuation | | | SA | 59 | - | - | dB |
| Group Delay (Note 32) | | | GD | - | 25 | - | 1/fs |
| **DAC Digital Filter (LPF) + SCF:** | | | | | | | |
| Frequency Response: 0 ~ 20.0kHz | | | FR | - | ±1.0 | - | dB |
| **DAC Digital Filter (HPF):** (Note 33) | | | | | | | |
| Frequency Response (Note 31) | | −3.0dB | FR | - | 0.9 | - | Hz |
| | | −0.5dB | | - | 2.7 | - | Hz |
| | | −0.1dB | | - | 6.0 | - | Hz |
| **BOOST Filter:** (Note 34) | | | | | | | |
| Frequency Response | MIN | 20Hz | FR | - | 5.76 | - | dB |
| | | 100Hz | | - | 2.92 | - | dB |
| | | 1kHz | | - | 0.02 | - | dB |
| | MID | 20Hz | FR | - | 10.80 | - | dB |
| | | 100Hz | | - | 6.84 | - | dB |
| | | 1kHz | | - | 0.13 | - | dB |
| | MAX | 20Hz | FR | - | 16.06 | - | dB |
| | | 100Hz | | - | 10.54 | - | dB |
| | | 1kHz | | - | 0.37 | - | dB |

Note 31. The passband and stopband frequencies scale with fs (system sampling rate).
For example, DAC is PB=0.454*fs (@−0.7dB). Each response refers to that of 1kHz.

Note 32. The calculated delay time caused by digital filtering. This time is from the input of analog signal to setting of the 16-bit data of both channels from the input register to the output register of the ADC. This time includes the group delay of the HPF. For the DAC, this time is from setting the 16-bit data of both channels from the input register to the output of analog signal. Group delay of DAC part is 25/fs(typ) at PMADL=PMADR bits = "0".

Note 33. When PMADL bit = "1" or PMADR bit = "1", the HPF of ADC is enabled but the HPF of DAC is disabled. When PMADL=PMADR bits = "0", PMDAC bit = "1", the HPF of DAC is enabled but the HPF of ADC is disabled.

Note 34. These frequency responses scale with fs. If a high-level and low frequency signal is input, the analog output clips to the full-scale.

## DC CHARACTERISTICS

(Ta=25°C; AVDD, DVDD=2.6 ~ 3.6V; HVDD=2.6 ~ 5.25V)

| Parameter | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|
| High-Level Input Voltage | VIH | 70%DVDD | - | - | V |
| Low-Level Input Voltage | VIL | - | - | 30%DVDD | V |
| High-Level Output Voltage (Iout=−200μA) | VOH | DVDD−0.2 | - | - | V |
| Low-Level Output Voltage | | | | | |
| (Except SDA pin: Iout=200μA) | VOL | - | - | 0.2 | V |
| (SDA pin: Iout=3mA) | VOL | - | - | 0.4 | V |
| Input Leakage Current | Iin | - | - | ±10 | μA |

## SWITCHING CHARACTERISTICS

(Ta=25°C; AVDD, DVDD=2.6 ~ 3.6V; HVDD=2.6 ~ 5.25V; $C_L$=20pF; unless otherwise specified)

| Parameter | | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|---|
| **PLL Master Mode (PLL Reference Clock = MCKI pin)** | | | | | | |
| **MCKI Input Timing** | | | | | | |
| Frequency | | fCLK | 11.2896 | - | 27 | MHz |
| Pulse Width Low | | tCLKL | 0.4/fCLK | - | - | ns |
| Pulse Width High | | tCLKH | 0.4/fCLK | - | - | ns |
| **MCKO Output Timing** | | | | | | |
| Frequency | | fMCK | 0.2352 | - | 12.288 | MHz |
| Duty Cycle | | | | | | |
| Except 256fs at fs=32kHz, 29.4kHz | | dMCK | 40 | 50 | 60 | % |
| 256fs at fs=32kHz, 29.4kHz | | dMCK | - | 33 | - | % |
| **LRCK Output Timing** | | | | | | |
| Frequency | | fs | 7.35 | - | 48 | kHz |
| DSP Mode: Pulse Width High | | tLRCKH | - | tBCK | - | ns |
| Except DSP Mode: Duty Cycle | | Duty | - | 50 | - | % |
| **BICK Output Timing** | | | | | | |
| Period | BCKO bit = “0” | tBCK | - | 1/(32fs) | - | ns |
| | BCKO bit = “1” | tBCK | - | 1/(64fs) | - | ns |
| Duty Cycle | | dBCK | - | 50 | - | % |
| **PLL Slave Mode (PLL Reference Clock = MCKI pin)** | | | | | | |
| **MCKI Input Timing** | | | | | | |
| Frequency | | fCLK | 11.2896 | - | 27 | MHz |
| Pulse Width Low | | tCLKL | 0.4/fCLK | - | - | ns |
| Pulse Width High | | tCLKH | 0.4/fCLK | - | - | ns |
| **MCKO Output Timing** | | | | | | |
| Frequency | | fMCK | 0.2352 | - | 12.288 | MHz |
| Duty Cycle | | | | | | |
| Except 256fs at fs=32kHz, 29.4kHz | | dMCK | 40 | 50 | 60 | % |
| 256fs at fs=32kHz, 29.4kHz | | dMCK | - | 33 | - | % |
| **LRCK Input Timing** | | | | | | |
| Frequency | | fs | 7.35 | - | 48 | kHz |
| DSP Mode: Pulse Width High | | tLRCKH | tBCK−60 | - | 1/fs – tBCK | ns |
| Except DSP Mode: Duty Cycle | | Duty | 45 | - | 55 | % |
| **BICK Input Timing** | | | | | | |
| Period | | tBCK | 1/(64fs) | - | 1/(32fs) | ns |
| Pulse Width Low | | tBCKL | 0.4 x tBCK | - | - | ns |
| Pulse Width High | | tBCKH | 0.4 x tBCK | - | - | ns |

| Parameter | | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|---|
| **PLL Slave Mode (PLL Reference Clock = LRCK pin)** | | | | | | |
| **LRCK Input Timing** | | | | | | |
| Frequency | | fs | 7.35 | - | 48 | kHz |
| DSP Mode: Pulse Width High | | tLRCKH | tBCK−60 | - | 1/fs − tBCK | ns |
| Except DSP Mode: Duty Cycle | | Duty | 45 | - | 55 | % |
| **BICK Input Timing** | | | | | | |
| Period | | tBCK | 1/(64fs) | - | 1/(32fs) | ns |
| Pulse Width Low | | tBCKL | 130 | - | - | ns |
| Pulse Width High | | tBCKH | 130 | - | - | ns |
| **PLL Slave Mode (PLL Reference Clock = BICK pin)** | | | | | | |
| **LRCK Input Timing** | | | | | | |
| Frequency | | fs | 7.35 | - | 48 | kHz |
| DSP Mode: Pulse Width High | | tLRCKH | tBCK−60 | - | 1/fs − tBCK | ns |
| Except DSP Mode: Duty Cycle | | Duty | 45 | - | 55 | % |
| **BICK Input Timing** | | | | | | |
| Period | PLL3-0 bits = “0010” | tBCK | - | 1/(32fs) | - | ns |
| | PLL3-0 bits = “0011” | tBCK | - | 1/(64fs) | - | ns |
| Pulse Width Low | | tBCKL | 0.4 x tBCK | - | - | ns |
| Pulse Width High | | tBCKH | 0.4 x tBCK | - | - | ns |
| **External Slave Mode** | | | | | | |
| **MCKI Input Timing** | | | | | | |
| Frequency | 256fs | fCLK | 1.8816 | - | 12.288 | MHz |
| | 512fs | fCLK | 3.7632 | - | 13.312 | MHz |
| | 1024fs | fCLK | 7.5264 | - | 13.312 | MHz |
| Pulse Width Low | | tCLKL | 0.4/fCLK | - | - | ns |
| Pulse Width High | | tCLKH | 0.4/fCLK | - | - | ns |
| **LRCK Input Timing** | | | | | | |
| Frequency | 256fs | fs | 7.35 | - | 48 | kHz |
| | 512fs | fs | 7.35 | - | 26 | kHz |
| | 1024fs | fs | 7.35 | - | 13 | kHz |
| DSP Mode: Pulse Width High | | tLRCKH | tBCK−60 | - | 1/fs − tBCK | ns |
| Except DSP Mode: Duty Cycle | | Duty | 45 | - | 55 | % |
| **BICK Input Timing** | | | | | | |
| Period | | tBCK | 312.5 | - | - | ns |
| Pulse Width Low | | tBCKL | 130 | - | - | ns |
| Pulse Width High | | tBCKH | 130 | - | - | ns |
| **External Master Mode** | | | | | | |
| **MCKI Input Timing** | | | | | | |
| Frequency | 256fs | fCLK | 1.8816 | - | 12.288 | MHz |
| | 512fs | fCLK | 3.7632 | - | 13.312 | MHz |
| | 1024fs | fCLK | 7.5264 | - | 13.312 | MHz |
| Pulse Width Low | | tCLKL | 0.4/fCLK | - | - | ns |
| Pulse Width High | | tCLKH | 0.4/fCLK | - | - | ns |
| **LRCK Output Timing** | | | | | | |
| Frequency | | fs | 7.35 | - | 48 | kHz |
| DSP Mode: Pulse Width High | | tLRCKH | - | tBCK | - | ns |
| Except DSP Mode: Duty Cycle | | Duty | - | 50 | - | % |
| **BICK Output Timing** | | | | | | |
| Period | BCKO bit = “0” | tBCK | - | 1/(32fs) | - | ns |
| | BCKO bit = “1” | tBCK | - | 1/(64fs) | - | ns |
| Duty Cycle | | dBCK | - | 50 | - | % |

| Parameter | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|
| **Audio Interface Timing (DSP Mode)** | | | | | |
| **Master Mode** | | | | | |
| LRCK "↑" to BICK "↑" (Note 35) | tDBF | 0.5 x tBCK – 40 | 0.5 x tBCK | 0.5 x tBCK + 40 | ns |
| LRCK "↑" to BICK "↓" (Note 36) | tDBF | 0.5 x tBCK – 40 | 0.5 x tBCK | 0.5 x tBCK + 40 | ns |
| BICK "↑" to SDTO (BCKP bit = "0") | tBSD | –70 | - | 70 | ns |
| BICK "↓" to SDTO (BCKP bit = "1") | tBSD | –70 | - | 70 | ns |
| SDTI Hold Time | tSDH | 50 | - | - | ns |
| SDTI Setup Time | tSDS | 50 | - | - | ns |
| **Slave Mode** | | | | | |
| LRCK "↑" to BICK "↑" (Note 35) | tLRB | 0.4 x tBCK | - | - | ns |
| LRCK "↑" to BICK "↓" (Note 36) | tLRB | 0.4 x tBCK | - | - | ns |
| BICK "↑" to LRCK "↑" (Note 35) | tBLR | 0.4 x tBCK | - | - | ns |
| BICK "↓" to LRCK "↑" (Note 36) | tBLR | 0.4 x tBCK | - | - | ns |
| BICK "↑" to SDTO (BCKP bit = "0") | tBSD | - | - | 80 | ns |
| BICK "↓" to SDTO (BCKP bit = "1") | tBSD | - | - | 80 | ns |
| SDTI Hold Time | tSDH | 50 | - | - | ns |
| SDTI Setup Time | tSDS | 50 | - | - | ns |
| **Audio Interface Timing (Right/Left justified & $I^2S$)** | | | | | |
| **Master Mode** | | | | | |
| BICK "↓" to LRCK Edge (Note 35) | tMBLR | –40 | - | 40 | ns |
| LRCK Edge to SDTO (MSB) (Except $I^2S$ mode) | tLRD | –70 | - | 70 | ns |
| BICK "↓" to SDTO | tBSD | –70 | - | 70 | ns |
| SDTI Hold Time | tSDH | 50 | - | - | ns |
| SDTI Setup Time | tSDS | 50 | - | - | ns |
| **Slave Mode** | | | | | |
| LRCK Edge to BICK "↑" (Note 36) | tLRB | 50 | - | - | ns |
| BICK "↑" to LRCK Edge (Note 37) | tBLR | 50 | - | - | ns |
| LRCK Edge to SDTO (MSB) (Except $I^2S$ mode) | tLRD | - | - | 80 | ns |
| BICK "↓" to SDTO | tBSD | - | - | 80 | ns |
| SDTI Hold Time | tSDH | 50 | - | - | ns |
| SDTI Setup Time | tSDS | 50 | - | - | ns |

Note 35. MSBS, BCKP bits = "00" or "11".
Note 36. MSBS, BCKP bits = "01" or "10".
Note 37. BICK rising edge must not occur at the same time as LRCK edge.

| Parameter | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|
| **Control Interface Timing (3-wire Serial mode)** | | | | | |
| CCLK Period | tCCK | 200 | - | - | ns |
| CCLK Pulse Width Low | tCCKL | 80 | - | - | ns |
| Pulse Width High | tCCKH | 80 | - | - | ns |
| CDTI Setup Time | tCDS | 40 | - | - | ns |
| CDTI Hold Time | tCDH | 40 | - | - | ns |
| CSN "H" Time | tCSW | 150 | - | - | ns |
| CSN "↓" to CCLK "↑" | tCSS | 50 | - | - | ns |
| CCLK "↑" to CSN "↑" | tCSH | 50 | - | - | ns |
| **Control Interface Timing ($I^2C$ Bus mode):** | | | | | |
| SCL Clock Frequency | fSCL | - | - | 400 | kHz |
| Bus Free Time Between Transmissions | tBUF | 1.3 | - | - | µs |
| Start Condition Hold Time (prior to first clock pulse) | tHD:STA | 0.6 | - | - | µs |
| Clock Low Time | tLOW | 1.3 | - | - | µs |
| Clock High Time | tHIGH | 0.6 | - | - | µs |
| Setup Time for Repeated Start Condition | tSU:STA | 0.6 | - | - | µs |
| SDA Hold Time from SCL Falling (Note 39) | tHD:DAT | 0 | - | - | µs |
| SDA Setup Time from SCL Rising | tSU:DAT | 0.1 | - | - | µs |
| Rise Time of Both SDA and SCL Lines | tR | - | - | 0.3 | µs |
| Fall Time of Both SDA and SCL Lines | tF | - | - | 0.3 | µs |
| Capacitive Load on Bus | Cb | - | - | 400 | pF |
| Pulse Width of Spike Noise Suppressed by Input Filter | tSP | 0 | - | 50 | ns |
| **Power-down & Reset Timing** | | | | | |
| PDN Pulse Width (Note 40) | tPD | 150 | - | - | ns |
| PMADL or PMADR "↑" to SDTO valid (Note 41) | tPDV | - | 1059 | - | 1/fs |

Note 38. $I^2C$ is a registered trademark of Philips Semiconductors.
Note 39. Data must be held long enough to bridge the 300ns-transition time of SCL.
Note 40. The AK4643 can be reset by the PDN pin = "L".
Note 41. This is the count of LRCK "↑" from the PMADL or PMADR bit = "1".

## ■ Timing Diagram

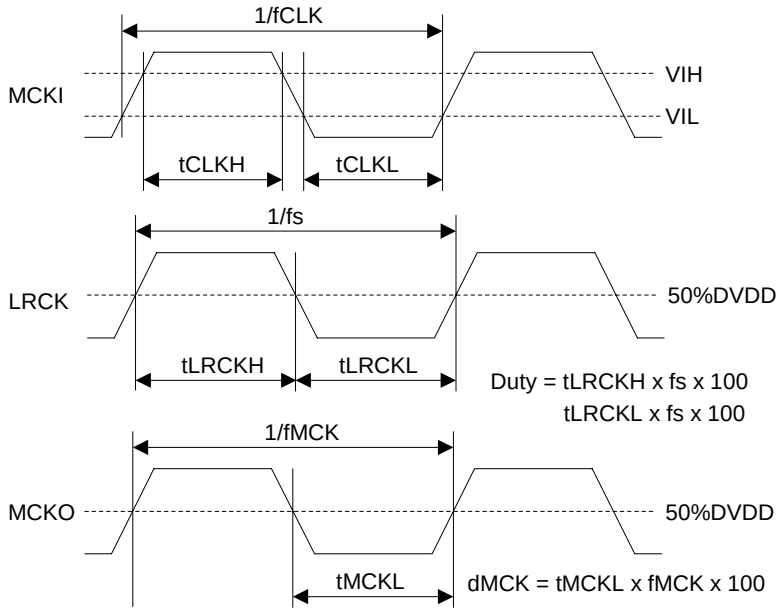



Figure 3. Clock Timing (PLL/EXT Master mode)
Note 42. MCKO is not available at EXT Master mode.

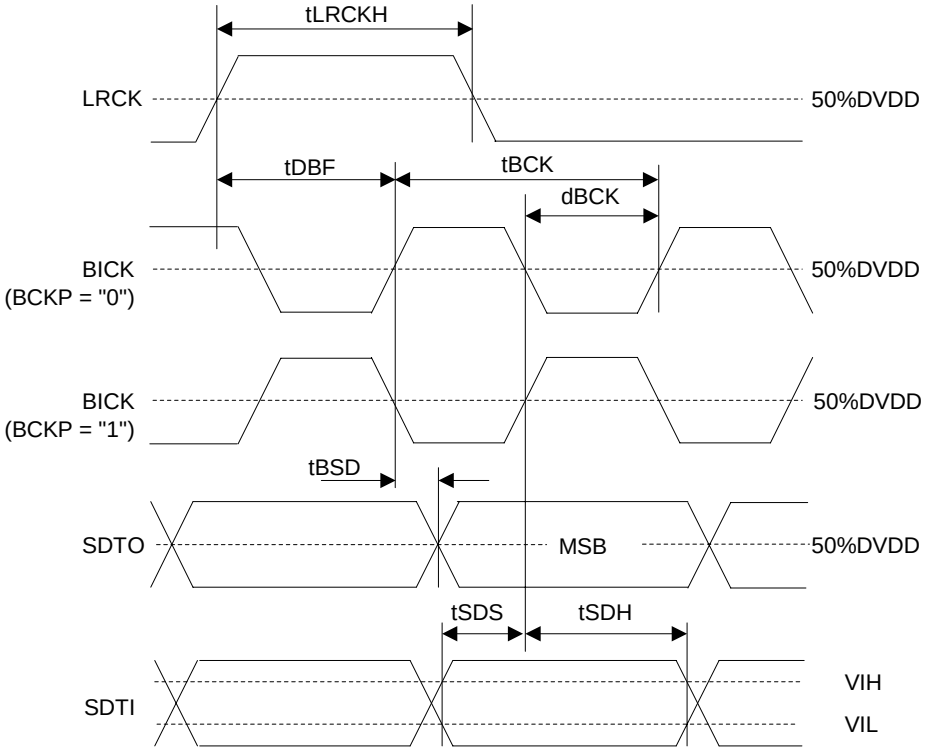



Figure 4. Audio Interface Timing (PLL/EXT Master mode, DSP mode, MSBS = “0”)

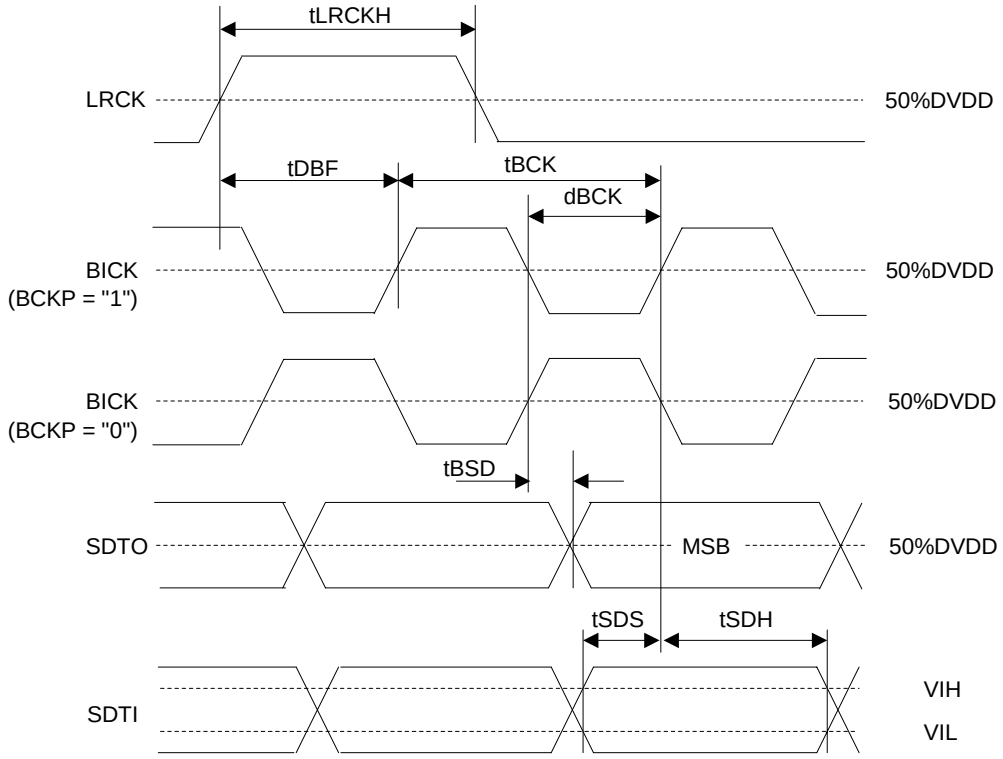



Figure 5. Audio Interface Timing (PLL/EXT Master mode, DSP mode, MSBS = “1”)

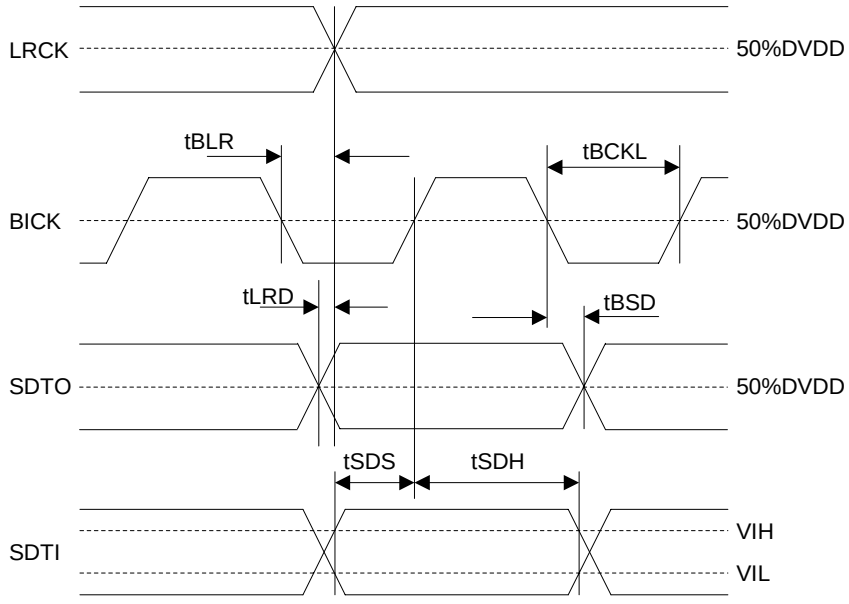



Figure 6. Audio Interface Timing (PLL/EXT Master mode, Except DSP mode)

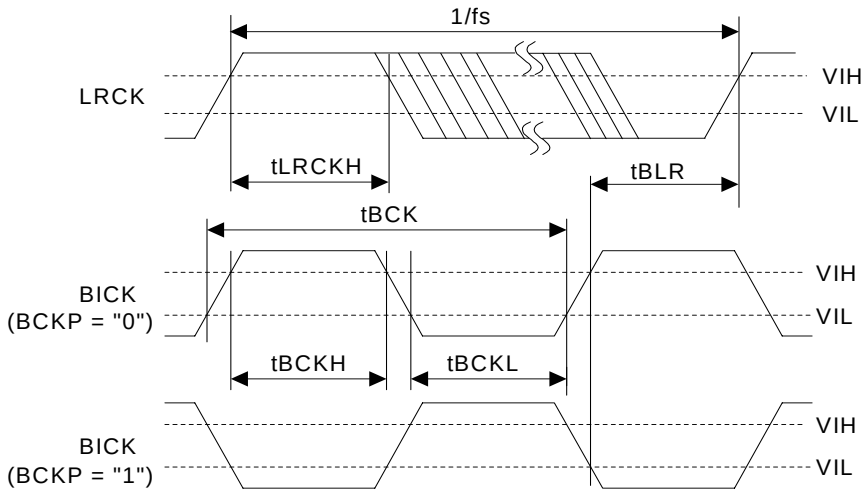



Figure 7. Clock Timing (PLL Slave mode; PLL Reference Clock = LRCK or BICK pin, DSP mode, MSBS = “0”)

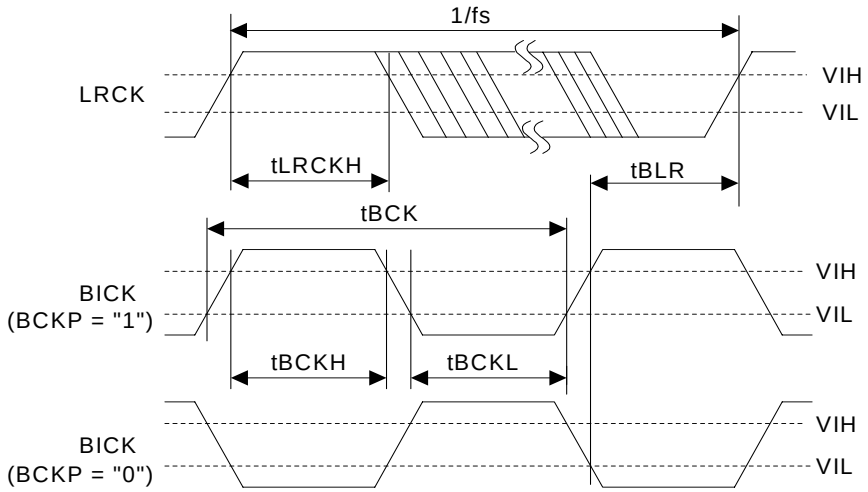



Figure 8. Clock Timing (PLL Slave mode; PLL Reference Clock = LRCK or BICK pin, DSP mode, MSBS = “1”)

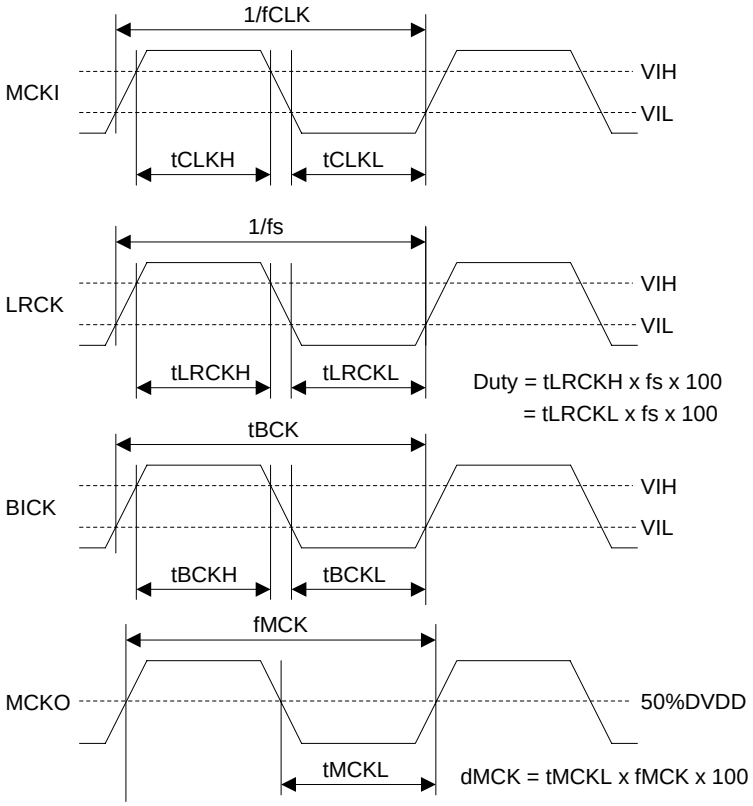



Figure 9. Clock Timing (PLL Slave mode; PLL Reference Clock = MCKI pin, Except DSP mode)

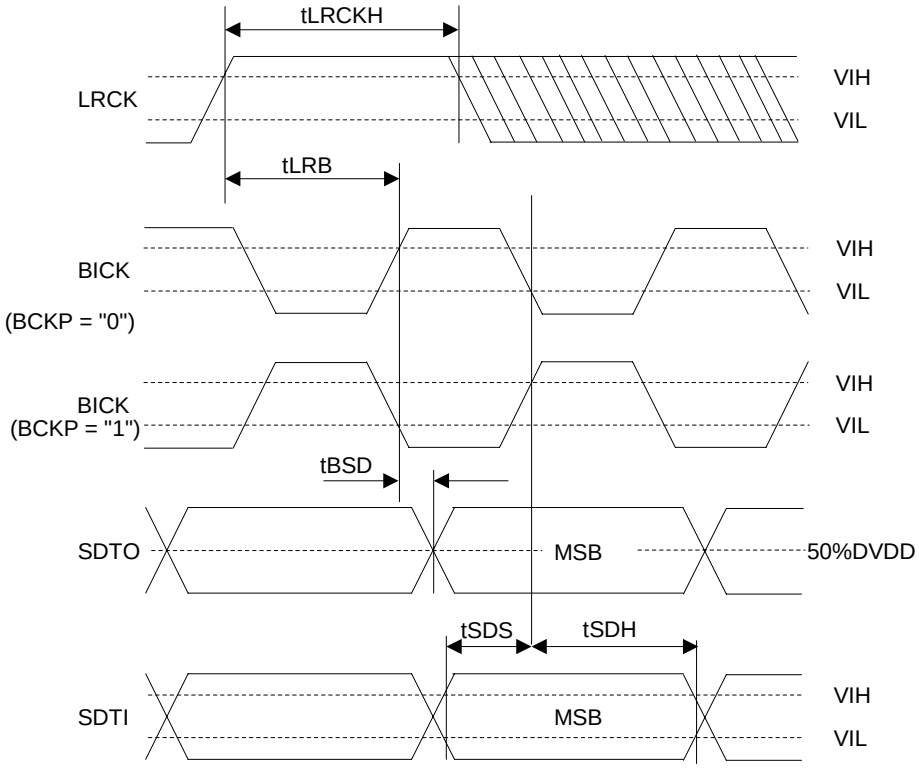



Figure 10. Audio Interface Timing (PLL Slave mode, DSP mode; MSBS = “0”)

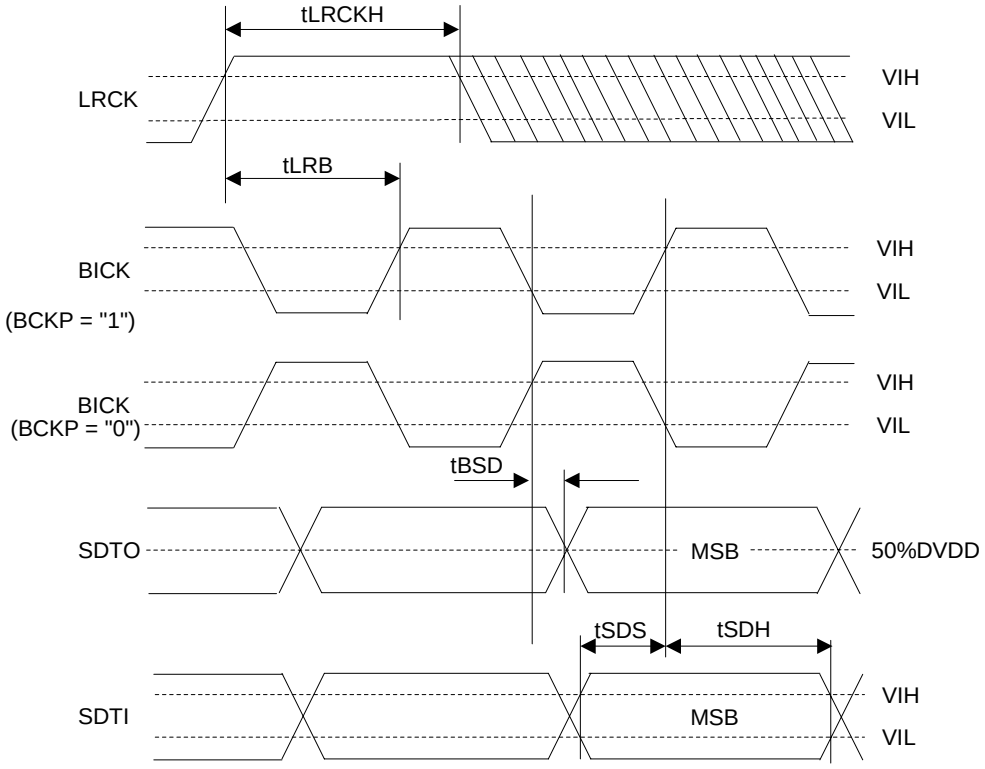



Figure 11. Audio Interface Timing (PLL Slave mode, DSP mode, MSBS = “1”)

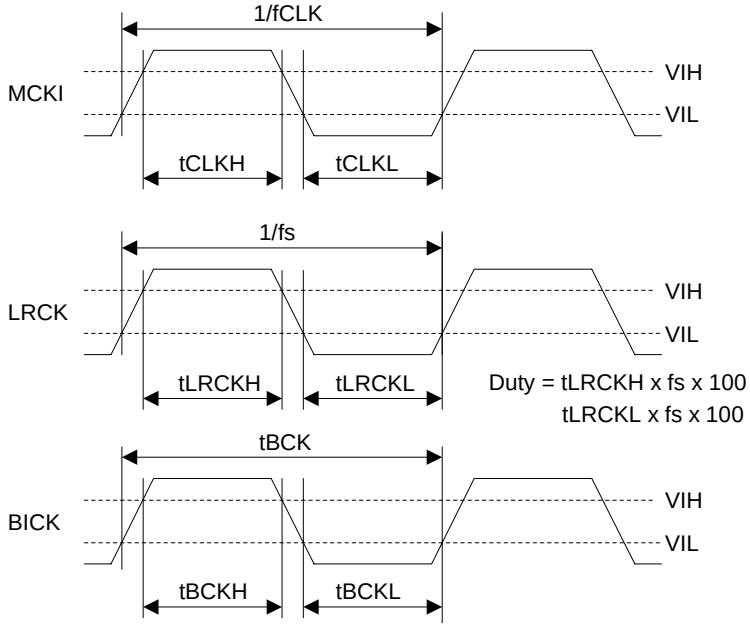



Figure 12. Clock Timing (EXT Slave mode)

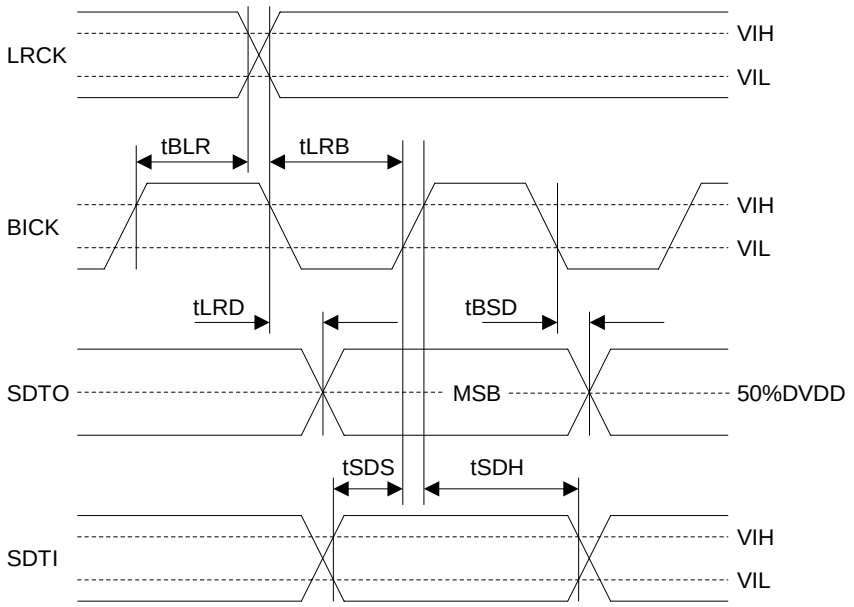



Figure 13. Audio Interface Timing (PLL/EXT Slave mode, Except DSP mode)

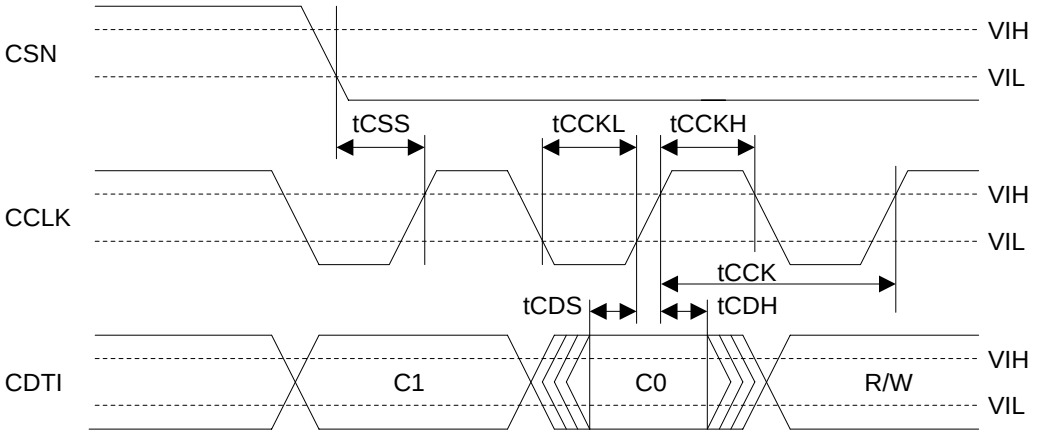



Figure 14. WRITE Command Input Timing

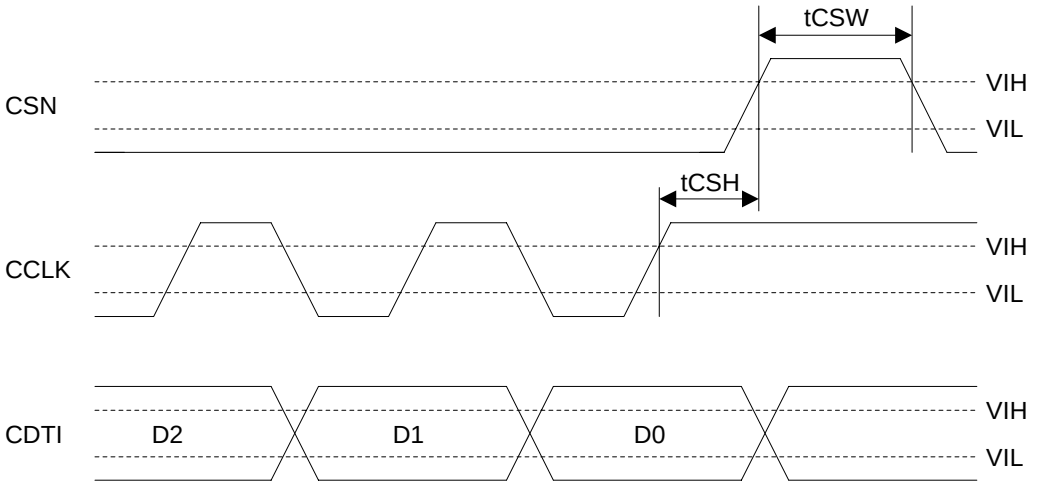



Figure 15. WRITE Data Input Timing

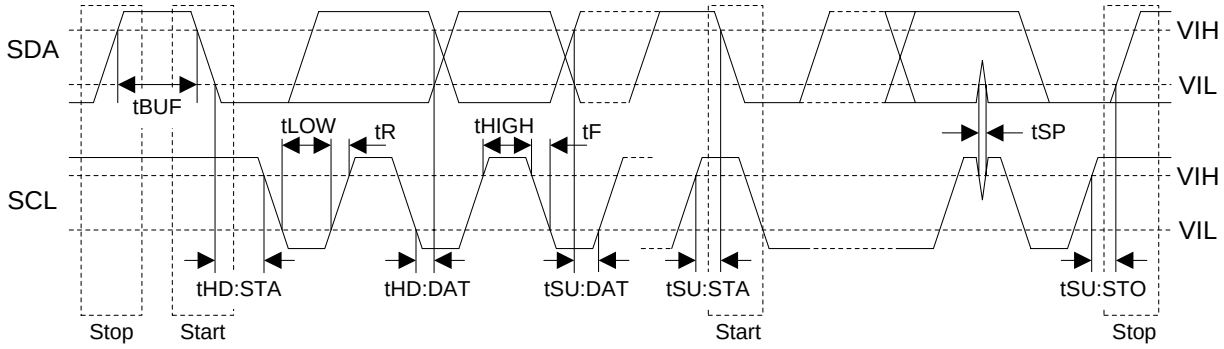



Figure 16. I$^2$C Bus Mode Timing

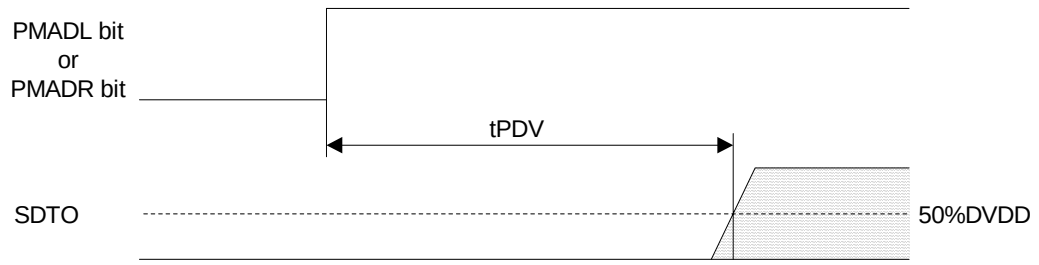



Figure 17. Power Down & Reset Timing 1

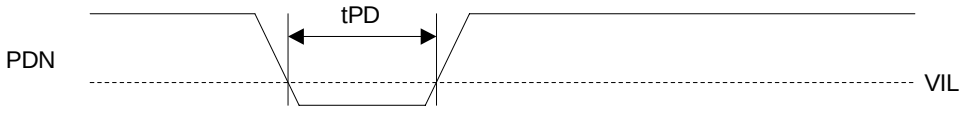



Figure 18. Power Down & Reset Timing 2

## OPERATION OVERVIEW

### ■ System Clock

There are the following four clock modes to interface with external devices (see Table 2 and Table 3).

| Mode | PMPLL bit | M/S bit | PLL3-0 bits | Figure |
|---|---|---|---|---|
| PLL Master Mode (Note 43) | 1 | 1 | See Table 5 | Figure 19 |
| PLL Slave Mode 1<br>(PLL Reference Clock: MCKI pin) | 1 | 0 | See Table 5 | Figure 20 |
| PLL Slave Mode 2<br>(PLL Reference Clock: LRCK or BICK pin) | 1 | 0 | See Table 5 | Figure 21<br>Figure 22 |
| EXT Slave Mode | 0 | 0 | x | Figure 23 |
| EXT Master Mode | 0 | 1 | x | Figure 24 |

Note 43. If M/S bit = "1", PMPLL bit = "0" and MCKO bit = "1" during the setting of PLL Master Mode, the invalid clocks are output from MCKO pin when MCKO bit is "1".

Table 2. Clock Mode Setting (x: Don't care)

| Mode | MCKO bit | MCKO pin | MCKI pin | BICK pin | LRCK pin |
|---|---|---|---|---|---|
| PLL Master Mode | 0 | "L" | Selected by PLL3-0 bits | Output (Selected by BCKO bit) | Output (1fs) |
| | 1 | Selected by PS1-0 bits | | | |
| PLL Slave Mode<br>(PLL Reference Clock: MCKI pin) | 0 | "L" | Selected by PLL3-0 bits | Input (≥ 32fs) | Input (1fs) |
| | 1 | Selected by PS1-0 bits | | | |
| PLL Slave Mode<br>(PLL Reference Clock: LRCK or BICK pin) | 0 | "L" | GND | Input (Selected by PLL3-0 bits) | Input (1fs) |
| EXT Slave Mode | 0 | "L" | Selected by FS1-0 bits | Input (≥ 32fs) | Input (1fs) |
| EXT Master Mode | 0 | "L" | Selected by FS1-0 bits | Output (Selected by BCKO bit) | Output (1fs) |

Table 3. Clock pins state in Clock Mode

### ■ Master Mode/Slave Mode

The M/S bit selects either master or slave mode. M/S bit = "1" selects master mode and "0" selects slave mode. When the AK4643 is power-down mode (PDN pin = "L") and exits reset state, the AK4643 is slave mode. After exiting reset state, the AK4643 goes to master mode by changing M/S bit = "1".

When the AK4643 is used by master mode, LRCK and BICK pins are a floating state until M/S bit becomes "1". LRCK and BICK pins of the AK4643 should be pulled-down or pulled-up by the resistor (about 100kΩ) externally to avoid the floating state.

| M/S bit | Mode | |
|---|---|---|
| 0 | Slave Mode | Default |
| 1 | Master Mode | |

Table 4. Select Master/Slave Mode

## ■ PLL Mode (AIN3 bit = "0", PMPLL bit = "1")

When PMPLL bit is "1", a fully integrated analog phase locked loop (PLL) generates a clock that is selected by the PLL3-0 and FS3-0 bits. The PLL lock time is shown in Table 5, whenever the AK4643 is supplied to a stable clocks after PLL is powered-up (PMPLL bit = "0" → "1") or sampling frequency changes. When AIN3 bit = "1", the PLL is not available.

1) Setting of PLL Mode

| Mode | PLL3 bit | PLL2 bit | PLL1 bit | PLL0 bit | PLL Reference Clock Input Pin | Input Frequency | R and C of VCOC pin | | PLL Lock Time (max) | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | R[Ω] | C[F] | | |
| 0 | 0 | 0 | 0 | 0 | LRCK pin | 1fs | 6.8k | 220n | 160ms | Default |
| 1 | 0 | 0 | 0 | 1 | N/A | - | - | - | - | |
| 2 | 0 | 0 | 1 | 0 | BICK pin | 32fs | 10k | 4.7n | 2ms | |
| | | | | | | | 10k | 10n | 4ms | |
| 3 | 0 | 0 | 1 | 1 | BICK pin | 64fs | 10k | 4.7n | 2ms | |
| | | | | | | | 10k | 10n | 4ms | |
| 4 | 0 | 1 | 0 | 0 | MCKI pin | 11.2896MHz | 10k | 4.7n | 40ms | |
| 5 | 0 | 1 | 0 | 1 | MCKI pin | 12.288MHz | 10k | 4.7n | 40ms | |
| 6 | 0 | 1 | 1 | 0 | MCKI pin | 12MHz | 10k | 4.7n | 40ms | |
| 7 | 0 | 1 | 1 | 1 | MCKI pin | 24MHz | 10k | 4.7n | 40ms | |
| 12 | 1 | 1 | 0 | 0 | MCKI pin | 13.5MHz | 10k | 10n | 40ms | |
| 13 | 1 | 1 | 0 | 1 | MCKI pin | 27MHz | 10k | 10n | 40ms | |
| Others | Others | | | | N/A | | | | | |

Table 5. Setting of PLL Mode (*fs: Sampling Frequency)

2) Setting of sampling frequency in PLL Mode

When PLL reference clock input is MCKI pin, the sampling frequency is selected by FS3-0 bits as defined in Table 6.

| Mode | FS3 bit | FS2 bit | FS1 bit | FS0 bit | Sampling Frequency | |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 8kHz | Default |
| 1 | 0 | 0 | 0 | 1 | 12kHz | |
| 2 | 0 | 0 | 1 | 0 | 16kHz | |
| 3 | 0 | 0 | 1 | 1 | 24kHz | |
| 4 | 0 | 1 | 0 | 0 | 7.35kHz | |
| 5 | 0 | 1 | 0 | 1 | 11.025kHz | |
| 6 | 0 | 1 | 1 | 0 | 14.7kHz | |
| 7 | 0 | 1 | 1 | 1 | 22.05kHz | |
| 10 | 1 | 0 | 1 | 0 | 32kHz | |
| 11 | 1 | 0 | 1 | 1 | 48kHz | |
| 14 | 1 | 1 | 1 | 0 | 29.4kHz | |
| 15 | 1 | 1 | 1 | 1 | 44.1kHz | |
| Others | Others | | | | N/A | |

Table 6. Setting of Sampling Frequency at PMPLL bit = "1" (Reference Clock = MCKI pin)

When PLL reference clock input is LRCK or BICK pin, the sampling frequency is selected by FS3 and FS1-0 bits. (See Table 7) **FS2 bit is "don't care".**

| Mode | FS3 bit | FS2 bit | FS1 bit | FS0 bit | Sampling Frequency Range | |
|---|---|---|---|---|---|---|
| 0 | 0 | Don't care | 0 | 0 | 7.35kHz ≤ fs ≤ 8kHz | Default |
| 1 | 0 | Don't care | 0 | 1 | 8kHz < fs ≤ 12kHz | |
| 2 | 0 | Don't care | 1 | 0 | 12kHz < fs ≤ 16kHz | |
| 3 | 0 | Don't care | 1 | 1 | 16kHz < fs ≤ 24kHz | |
| 6 | 1 | Don't care | 1 | 0 | 24kHz < fs ≤ 32kHz | |
| 7 | 1 | Don't care | 1 | 1 | 32kHz < fs ≤ 48kHz | |
| Others | Others | | | | N/A | |

Table 7. Setting of Sampling Frequency at PMPLL bit = "1" (Reference Clock = LRCK or BICK pin)

## ■ PLL Unlock State

1) PLL Master Mode (AIN3 bit = "0"; PMPLL bit = "1", M/S bit = "1")

In this mode, LRCK and BICK pins go to "L" and irregular frequency clock is output from MCKO pins at MCKO bit is "1" before the PLL goes to lock state after PMPLL bit = "0" → "1". If MCKO bit is "0", MCKO pin goes to "L" (see Table 8).

After the PLL is locked, a first period of LRCK and BICK may be invalid clock, but these clocks return to normal state after a period of 1/fs.

When sampling frequency is changed, BICK and LRCK pins do not output irregular frequency clocks but go to "L" by setting PMPLL bit to "0".

| PLL State | MCKO pin | | BICK pin | LRCK pin |
|---|---|---|---|---|
| | MCKO bit = "0" | MCKO bit = "1" | | |
| After that PMPLL bit "0" → "1" | "L" Output | Invalid | "L" Output | "L" Output |
| PLL Unlock (except above case) | "L" Output | Invalid | Invalid | Invalid |
| PLL Lock | "L" Output | See Table 10 | See Table 11 | 1fs Output |

Table 8. Clock Operation at PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

2) PLL Slave Mode (AIN3 bit = "0", PMPLL bit = "1", M/S bit = "0")

In this mode, an invalid clock is output from MCKO pin before the PLL goes to lock state after PMPLL bit = "0" → "1". After that, the clock selected by Table 10 is output from MCKO pin when PLL is locked. ADC and DAC output invalid data when the PLL is unlocked. For DAC, the output signal should be muted by writing "0" to DACL, DACH and DACS bits.

| PLL State | MCKO pin | |
|---|---|---|
| | MCKO bit = "0" | MCKO bit = "1" |
| After that PMPLL bit "0" → "1" | "L" Output | Invalid |
| PLL Unlock | "L" Output | Invalid |
| PLL Lock | "L" Output | Output |

Table 9. Clock Operation at PLL Slave Mode (PMPLL bit = "0", M/S bit = "0")

### ■ PLL Master Mode (AIN3 bit = “0”, PMPLL bit = “1”, M/S bit = “1”)

When an external clock (11.2896MHz, 12MHz, 12.288MHz, 13.5MHz, 24MHz or 27MHz) is input to MCKI pin, the MCKO, BICK and LRCK clocks are generated by an internal PLL circuit. The MCKO output frequency is selected by PS1-0 bits (see Table 10) and the output is enabled by MCKO bit. The BICK output frequency is selected between 32fs or 64fs, by BCKO bit (see Table 11).

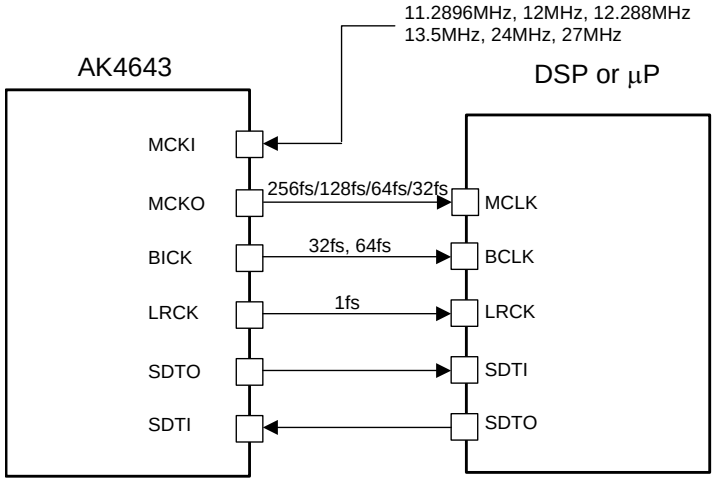



Figure 19. PLL Master Mode

| Mode | PS1 bit | PS0 bit | MCKO pin | |
|---|---|---|---|---|
| 0 | 0 | 0 | 256fs | Default |
| 1 | 0 | 1 | 128fs | |
| 2 | 1 | 0 | 64fs | |
| 3 | 1 | 1 | 32fs | |

Table 10. MCKO Output Frequency (PLL Mode, MCKO bit = “1”)

| BCKO bit | BICK Output Frequency | |
|---|---|---|
| 0 | 32fs | Default |
| 1 | 64fs | |

Table 11. BICK Output Frequency at Master Mode

## ■ PLL Slave Mode (AIN3 bit = “0”, PMPLL bit = “1”, M/S bit = “0”)

A reference clock of PLL is selected among the input clocks to MCKI, BICK or LRCK pin. The required clock to the AK4643 is generated by an internal PLL circuit. Input frequency is selected by PLL3-0 bits (see Table 5).

### a) PLL reference clock: MCKI pin

BICK and LRCK inputs should be synchronized with MCKO output. The phase between MCKO and LRCK dose not matter. MCKO pin outputs the frequency selected by PS1-0 bits (see Table 10) and the output is enabled by MCKO bit. Sampling frequency can be selected by FS3-0 bits (see Table 6).

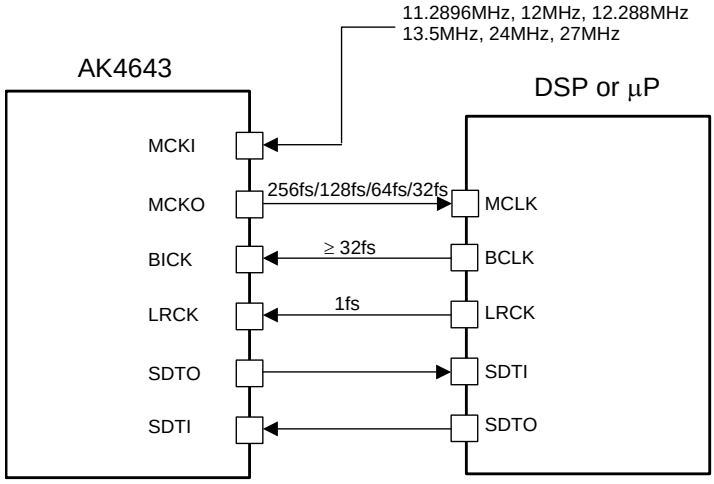



Figure 20. PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)

**b) PLL reference clock: BICK or LRCK pin**

Sampling frequency corresponds to 7.35kHz to 48kHz by changing FS3-0 bits (see Table 7).

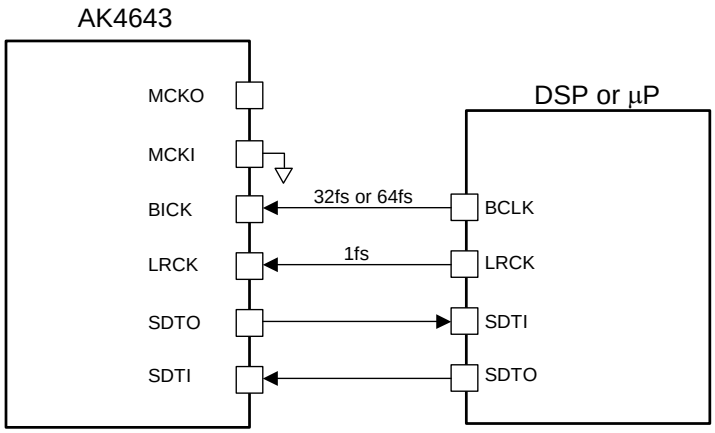



Figure 21. PLL Slave Mode 2 (PLL Reference Clock: BICK pin)

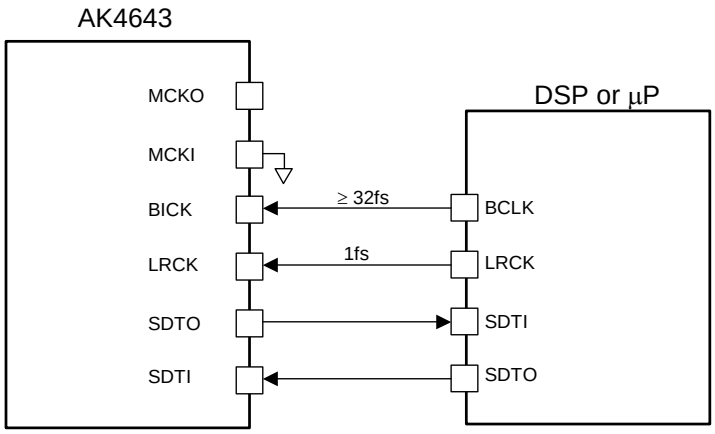



Figure 22. PLL Slave Mode 2 (PLL Reference Clock: LRCK pin)

The external clocks (MCKI, BICK and LRCK) should always be present whenever the ADC or DAC is in operation (PMADL bit = "1", PMADR bit = "1" or PMDAC bit = "1"). If these clocks are not provided, the AK4643 may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If the external clocks are not present, the ADC and DAC should be in the power-down mode (PMADL=PMADR=PMDAC bits = "0").

## ■ EXT Slave Mode (PMPLL bit = “0”, M/S bit = “0”)

When PMPLL bit is “0”, the AK4643 becomes EXT mode. Master clock is input from MCKI pin, the internal PLL circuit is not operated. This mode is compatible with I/F of the normal audio CODEC. The clocks required to operate are MCKI (256fs, 512fs or 1024fs), LRCK (fs) and BICK (≥32fs). The master clock (MCKI) should be synchronized with LRCK. The phase between these clocks does not matter. The input frequency of MCKI is selected by FS1-0 bits (see Table 12).

| Mode | FS3-2 bits | FS1 bit | FS0 bit | MCKI Input Frequency | Sampling Frequency Range | |
|---|---|---|---|---|---|---|
| 0 | Don’t care | 0 | 0 | 256fs | 7.35kHz ~ 48kHz | Default |
| 1 | Don’t care | 0 | 1 | 1024fs | 7.35kHz ~ 13kHz | |
| 2 | Don’t care | 1 | 0 | 256fs | 7.35kHz ~ 48kHz | |
| 3 | Don’t care | 1 | 1 | 512fs | 7.35kHz ~ 26kHz | |

Table 12. MCKI Frequency at EXT Slave Mode (PMPLL bit = “0”, M/S bit = “0”)

The S/N of the DAC at low sampling frequencies is worse than at high sampling frequencies due to out-of-band noise. The out-of-band noise can be improved by using higher frequency of the master clock. The S/N of the DAC output through LOUT/ROUT pins at fs=8kHz is shown in Table 13.

| MCKI | S/N (fs=8kHz, 20kHzLPF + A-weighted) |
|---|---|
| 256fs | 83dB |
| 512fs | 93dB |
| 1024fs | 93dB |

Table 13. Relationship between MCKI and S/N of LOUT/ROUT pins

The external clocks (MCKI, BICK and LRCK) should always be present whenever the ADC or DAC is in operation (PMADL bit = “1”, PMADR bit = “1” or PMDAC bit = “1”). If these clocks are not provided, the AK4643 may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If the external clocks are not present, the ADC and DAC should be in the power-down mode (PMADL=PMADR=PMDAC bits = “0”).

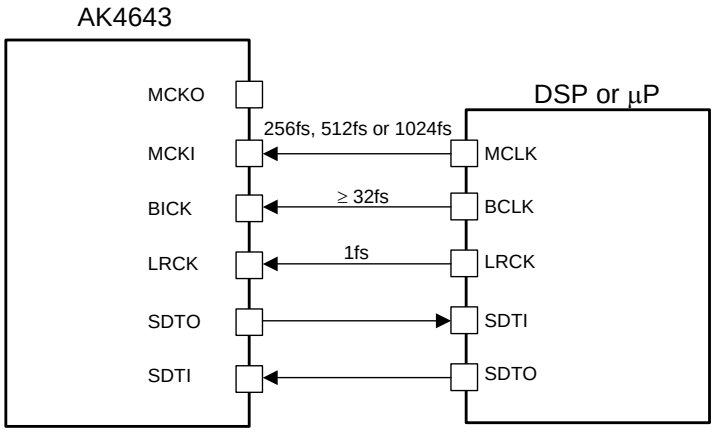



Figure 23. EXT Slave Mode

## ■ EXT Master Mode (PMPLL bit = “0”, M/S bit = “1”)

The AK4643 becomes EXT Master Mode by setting PMPLL bit = “0” and M/S bit = “1”. Master clock is input from MCKI pin, the internal PLL circuit is not operated. The clock required to operate is MCKI (256fs, 512fs or 1024fs). The input frequency of MCKI is selected by FS1-0 bits (see Table 14).

| Mode | FS3-2 bits | FS1 bit | FS0 bit | MCKI Input Frequency | Sampling Frequency Range | |
|---|---|---|---|---|---|---|
| 0 | Don’t care | 0 | 0 | 256fs | 7.35kHz ~ 48kHz | Default |
| 1 | Don’t care | 0 | 1 | 1024fs | 7.35kHz ~ 13kHz | |
| 2 | Don’t care | 1 | 0 | 256fs | 7.35kHz ~ 48kHz | |
| 3 | Don’t care | 1 | 1 | 512fs | 7.35kHz ~ 26kHz | |

Table 14. MCKI Frequency at EXT Master Mode (PMPLL bit = “0”, M/S bit = “1”)

The S/N of the DAC at low sampling frequencies is worse than at high sampling frequencies due to out-of-band noise. The out-of-band noise can be improved by using higher frequency of the master clock. The S/N of the DAC output through LOUT/ROUT pins at fs=8kHz is shown in Table 15.

| MCKI | S/N (fs=8kHz, 20kHzLPF + A-weighted) |
|---|---|
| 256fs | 83dB |
| 512fs | 93dB |
| 1024fs | 93dB |

Table 15. Relationship between MCKI and S/N of LOUT/ROUT pins

MCKI should always be present whenever the ADC or DAC is in operation (PMADL bit = “1”, PMADR bit = “1” or PMDAC bit = “1”). If MCKI is not provided, the AK4643 may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If MCKI is not present, the ADC and DAC should be in the power-down mode (PMADL=PMADR=PMDAC bits = “0”).

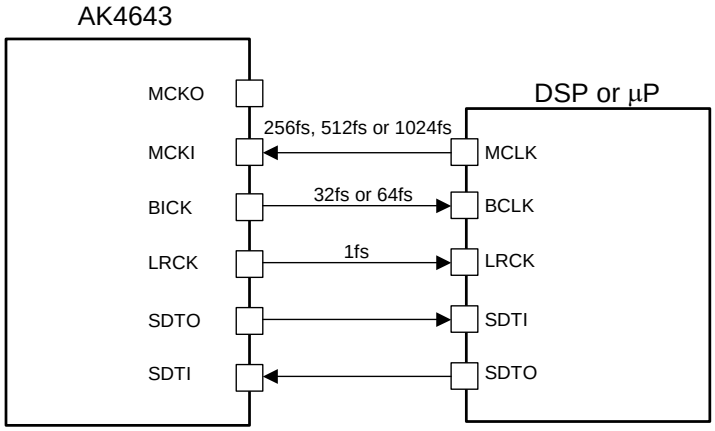



Figure 24. EXT Master Mode

| BCKO bit | BICK Output Frequency | |
|---|---|---|
| 0 | 32fs | Default |
| 1 | 64fs | |

Table 16. BICK Output Frequency at Master Mode

## ■ System Reset

Upon power-up, the AK4643 should be reset by bringing the PDN pin = "L". This ensures that all internal registers reset to their initial values.

The ADC enters an initialization cycle that starts when the PMADL or PMADR bit is changed from "0" to "1" at PMDAC bits is "0". The initialization cycle time is 1059/fs=24ms@fs=44.1kHz. During the initialization cycle, the ADC digital data outputs of both channels are forced to a 2's compliment, "0". The ADC output reflects the analog input signal after the initialization cycle is complete. When PMDAC bit is "1", the ADC does not require an initialization cycle.

The DAC enters an initialization cycle that starts when the PMDAC bit is changed from "0" to "1" at PMADL and PMADR bits are "0". The initialization cycle time is 1059/fs=24ms@fs=44.1kHz. During the initialization cycle, the DAC input digital data of both channels are internally forced to a 2's compliment, "0". The DAC output reflects the digital input data after the initialization cycle is complete. When PMADL or PMADR bit is "1", the DAC does not require an initialization cycle.

## ■ Audio Interface Format

Four types of data formats are available and are selected by setting the DIF1-0 bits (seeTable 17). In all modes, the serial data is MSB first, 2's complement format. Audio interface formats can be used in both master and slave modes. LRCK and BICK are output from the AK4643 in master mode, but must be input to the AK4643 in slave mode.

| Mode | DIF1 bit | DIF0 bit | SDTO (ADC) | SDTI (DAC) | BICK | Figure | |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | DSP Mode | DSP Mode | ≥ 32fs | Table 18 | |
| 1 | 0 | 1 | MSB justified | LSB justified | ≥ 32fs | Figure 29 | |
| 2 | 1 | 0 | MSB justified | MSB justified | ≥ 32fs | Figure 30 | Default |
| 3 | 1 | 1 | $I^2S$ compatible | $I^2S$ compatible | ≥ 32fs | Figure 31 | |

Table 17. Audio Interface Format

In modes 1, 2 and 3, the SDTO is clocked out on the falling edge ("↓") of BICK and the SDTI is latched on the rising edge ("↑").

In Modes 0 (DSP mode), the audio I/F timing is changed by BCKP and MSBS bits (Table 18).

| DIF1 | DIF0 | MSBS | BCKP | Audio Interface Format | Figure | |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | MSB of SDTO is output by the rising edge ("↑") of the first BICK after the rising edge ("↑") of LRCK.<br>MSB of SDTI is latched by the falling edge ("↓") of the BICK just after the output timing of SDTO's MSB. | Figure 25 | Default |
| | | 0 | 1 | MSB of SDTO is output by the falling edge ("↓") of the first BICK after the rising edge ("↑") of LRCK.<br>MSB of SDTI is latched by the rising edge ("↑") of the BICK just after the output timing of SDTO's MSB. | Figure 26 | |
| | | 1 | 0 | MSB of SDTO is output by next rising edge ("↑") of the falling edge ("↓") of the first BICK after the rising edge ("↑") of LRCK.<br>MSB of SDTI is latched by the falling edge ("↓") of the BICK just after the output timing of SDTO's MSB. | Figure 27 | |
| | | 1 | 1 | MSB of SDTO is output by next falling edge ("↓") of the rising edge ("↑") of the first BICK after the rising edge ("↑") of LRCK.<br>MSB of SDTI is latched by the rising edge ("↑") of the BICK just after the output timing of SDTO's MSB. | Figure 28 | |

Table 18. Audio Interface Format in Mode 0

If 16-bit data that ADC outputs is converted to 8-bit data by removing LSB 8-bit, "–1" at 16bit data is converted to "–1" at 8-bit data. And when the DAC playbacks this 8-bit data, "–1" at 8-bit data will be converted to "–256" at 16-bit data and this is a large offset. This offset can be removed by adding the offset of "128" to 16-bit data before converting to 8-bit data.

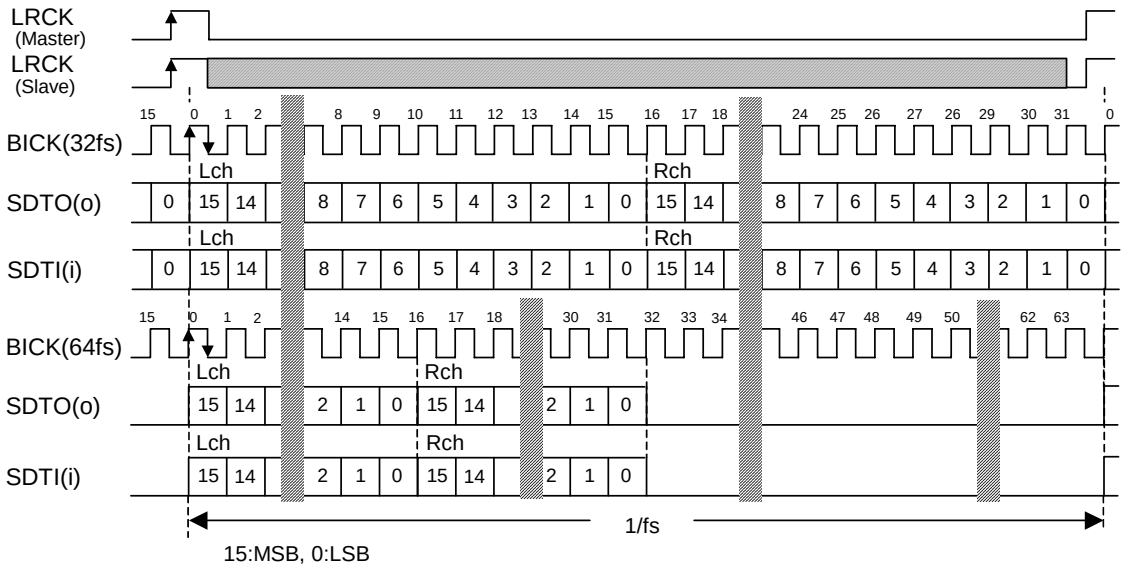



Figure 25. Mode 0 Timing (BCKP = “0”, MSBS = “0”)

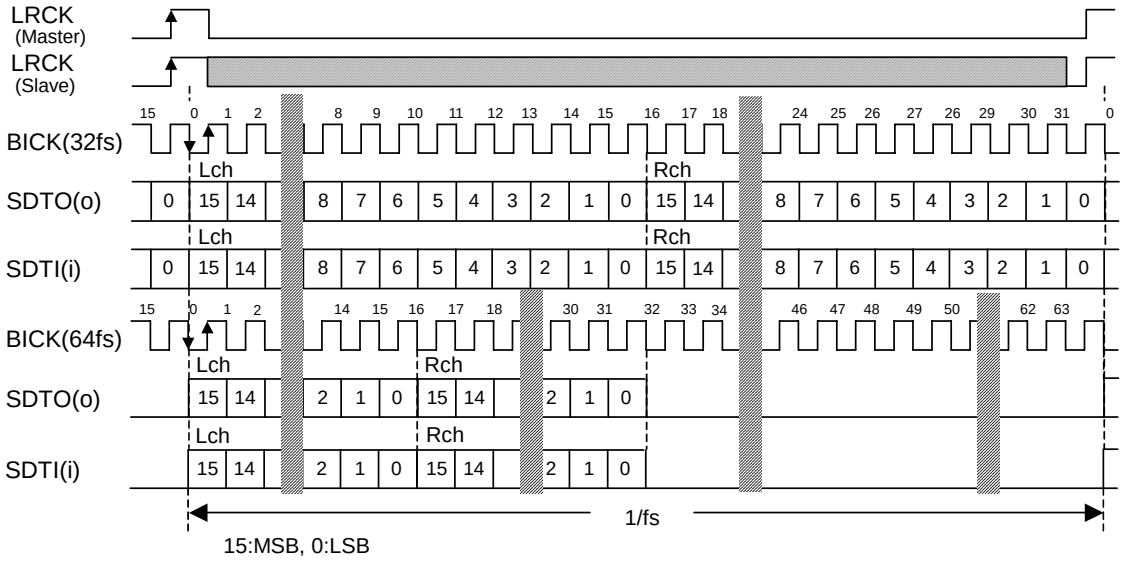



Figure 26. Mode 0 Timing (BCKP = “1”, MSBS = “0”)

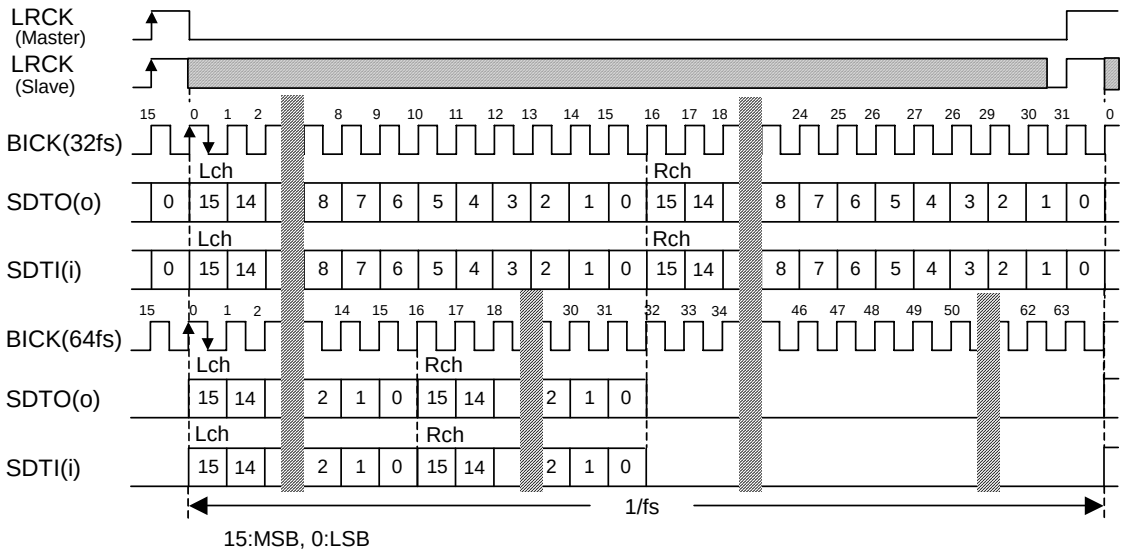



Figure 27. Mode 0 Timing (BCKP = "0", MSBS = "1")

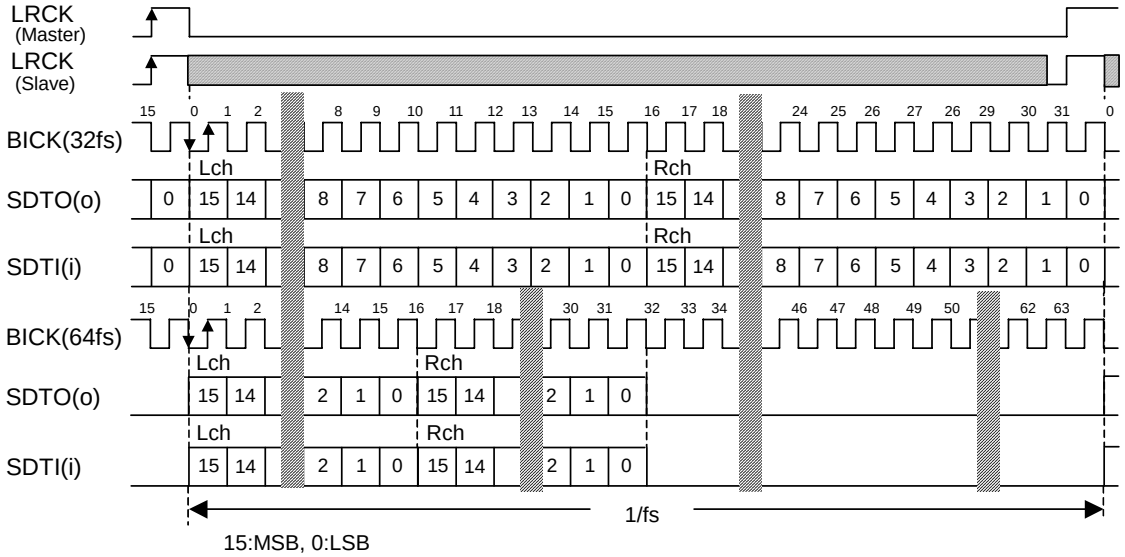



Figure 28. Mode 0 Timing (BCKP = "1", MSBS = "1")

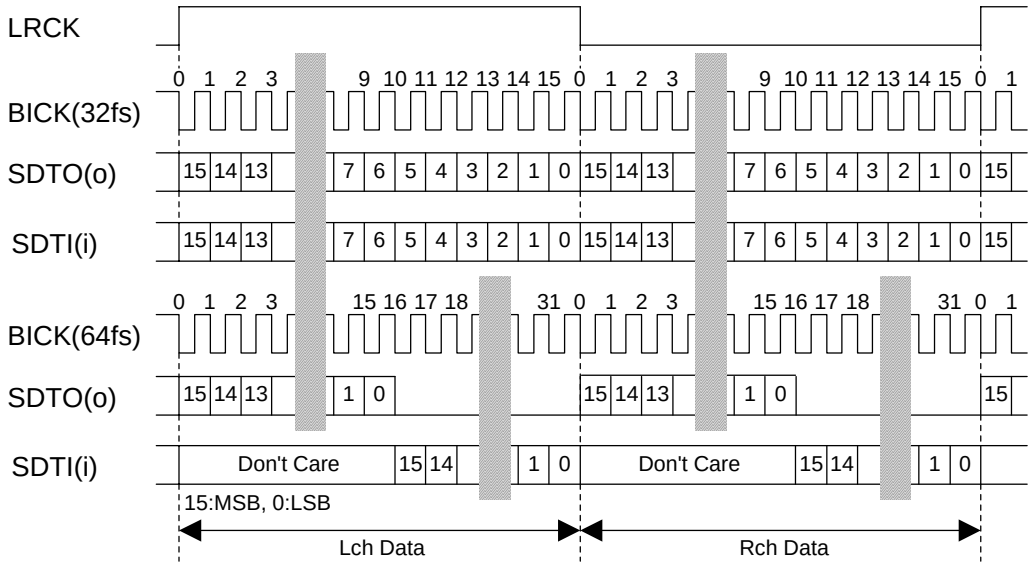



Figure 29. Mode 1 Timing

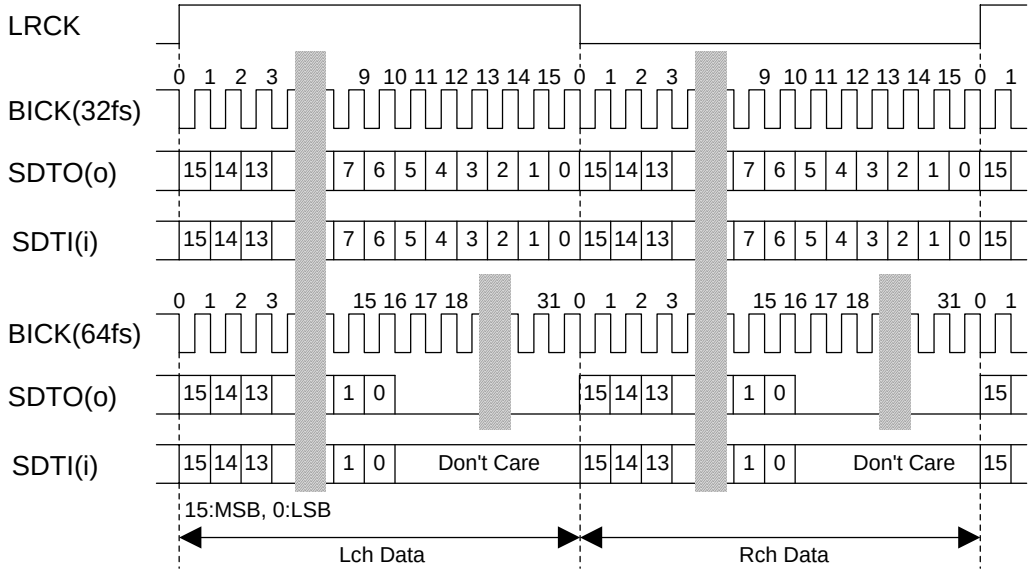



Figure 30. Mode 2 Timing

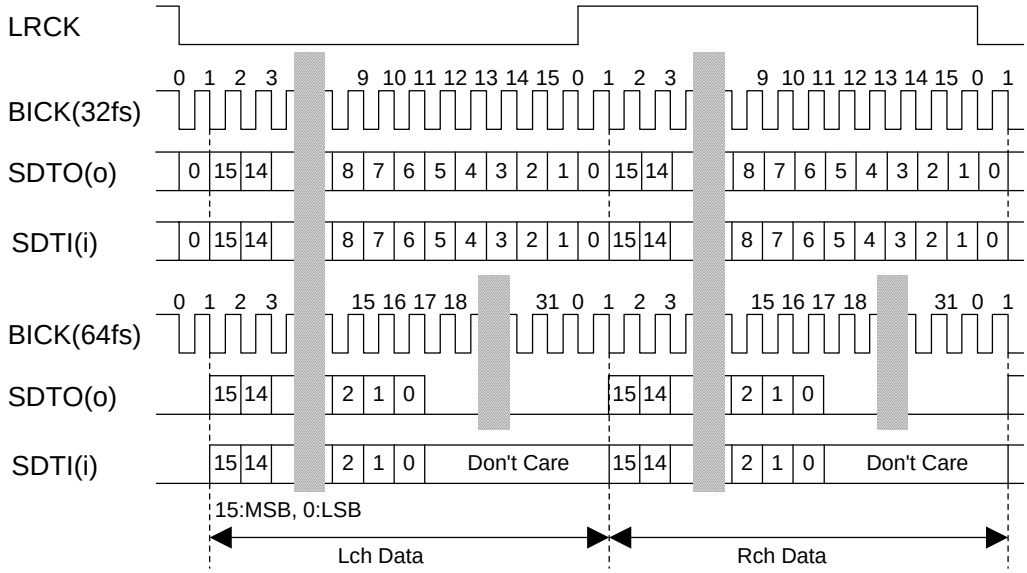



Figure 31. Mode 3 Timing

## ■ Mono/Stereo Mode

PMADL, PMADR and MIX bits set mono/stereo ADC operation. When MIX bit = "1", EQ and FIL3 bits should be set to "0". ALC operation (ALC bit = "1") or digital volume operation (ALC bit = "0") is applied to the data in Table 19.

| PMADL bit | PMADR bit | MIX bit | ADC Lch data | ADC Rch data | |
|---|---|---|---|---|---|
| 0 | 0 | x | All "0" | All "0" | Default |
| 0 | 1 | x | Rch Input Signal | Rch Input Signal | |
| 1 | 0 | x | Lch Input Signal | Lch Input Signal | |
| 1 | 1 | 0 | Lch Input Signal | Rch Input Signal | |
| | | 1 | (L+R)/2 | (L+R)/2 | |

Table 19. Mono/Stereo ADC operation (x: Don't care)

## ■ Digital High Pass Filter

The ADC has a digital high pass filter for DC offset cancellation. The cut-off frequency of the HPF is 0.9Hz (@fs=44.1kHz) and scales with sampling rate (fs). When PMADL bit = "1" or PMADR bit = "1", the HPF of ADC is enabled but the HPF of DAC is disabled. When PMADL=PMADR bits = "0", PMDAC bit = "1", the HPF of DAC is enabled but the HPF of ADC is disabled.

## ■ MIC/LINE Input Selector

The AK4643 has input selector for MIC-Amp. When MDIF1 and MDIF2 bits are "0", INL1-0 and INR1-0 bits select LIN1/LIN2/LIN3 and RIN1/RIN2/RIN3, respectively. When MDIF1 and MDIF2 bits are "1", LIN1, RIN1, LIN2 and RIN2 pins become IN1–, IN1+, IN2+ and IN2– pins respectively. In this case, full-differential input is available (Figure 33). When full-differential input is used, the signal should not be input to the pins marked by "X" in Table 21.

| MDIF1 bit | MDIF2 bit | INL1 bit | INL0 bit | INR1 bit | INR0 bit | Lch | Rch | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | LIN1 | RIN1 | Default |
| 0 | 0 | 0 | 0 | 0 | 1 | LIN1 | RIN2 | |
| 0 | 0 | 0 | 0 | 1 | 0 | LIN1 | RIN3 | |
| 0 | 0 | 0 | 1 | 0 | 0 | LIN2 | RIN1 | |
| 0 | 0 | 0 | 1 | 0 | 1 | LIN2 | RIN2 | |
| 0 | 0 | 0 | 1 | 1 | 0 | LIN2 | RIN3 | |
| 0 | 0 | 1 | 0 | 0 | 0 | LIN3 | RIN1 | |
| 0 | 0 | 1 | 0 | 0 | 1 | LIN3 | RIN2 | |
| 0 | 0 | 1 | 0 | 1 | 0 | LIN3 | RIN3 | |
| 0 | 1 | 0 | 0 | 0 | 0 | LIN1 | IN2+/– | |
| 0 | 1 | 1 | 0 | 0 | 0 | LIN3 | IN2+/– | |
| 1 | 0 | 0 | 0 | 0 | 1 | IN1+/– | RIN2 | |
| 1 | 0 | 0 | 0 | 1 | 0 | IN1+/– | RIN3 | |
| 1 | 1 | 0 | 0 | 0 | 0 | IN1+/– | IN2+/– | |
| Others | | | | | | N/A | N/A | |

Table 20. MIC/Line In Path Select

| Register | | | Pin | | | | | |
|---|---|---|---|---|---|---|---|---|
| AIN3 bit | MDIF1 bit | MDIF2 bit | LIN1 IN1– | RIN1 IN1+ | LIN2 IN2+ | RIN2 IN2– | MIN LIN3 | VCOC RIN3 |
| 0 | 0 | 0 | O | O | O | O | O | - |
| 0 | 0 | 1 | O | X | O | O | O | - |
| 0 | 1 | 0 | O | O | X | O | O | - |
| 0 | 1 | 1 | O | O | O | O | O | - |
| 1 | 0 | 0 | O | O | O | O | O | O |
| 1 | 0 | 1 | O | X | O | O | O | X |
| 1 | 1 | 0 | O | O | X | O | X | O |
| 1 | 1 | 1 | O | O | O | O | X | X |

Table 21. Handling of MIC/Line Input Pins ("-": N/A; "X": Signal should not be input.)

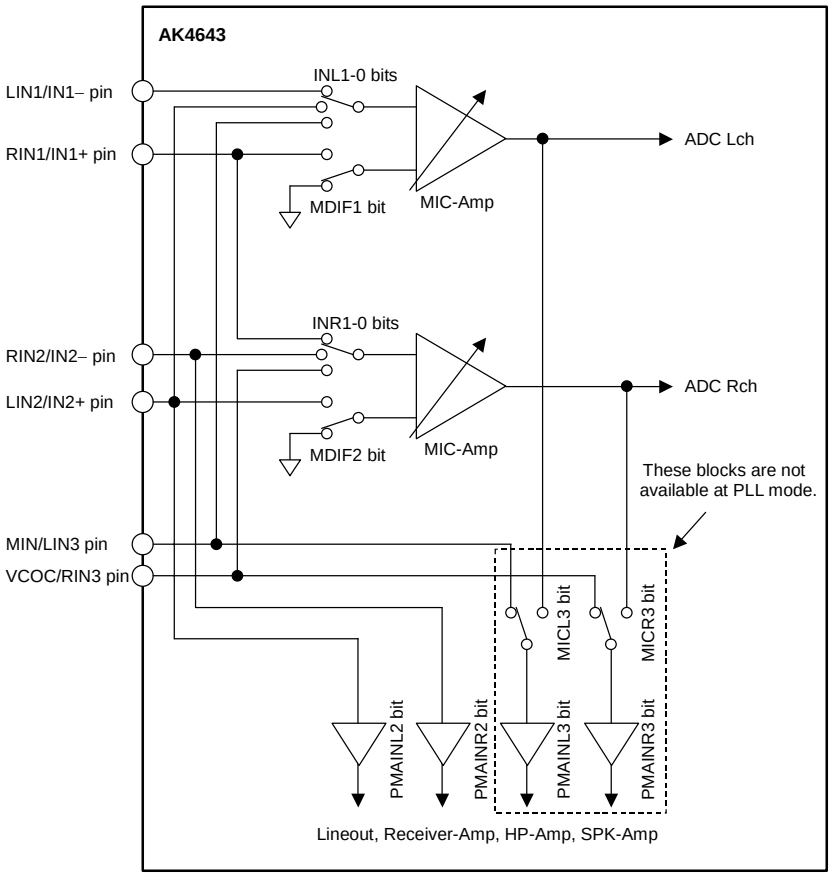



Figure 32. Mic/Line Input Selector

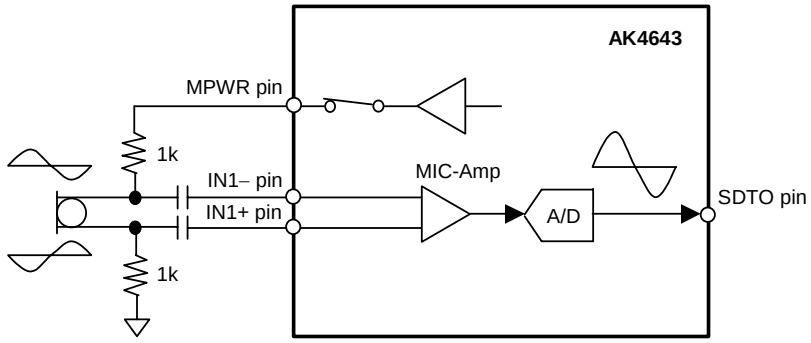



Figure 33. Connection Example for Full-differential Mic Input (MDIF1/2 bits = "1")

### <Input Selector Setting Example>

In case that IN1+/– pins are used as full-differential mic input and LIN2/RIN2 pins are used as stereo line input, it is recommended that the following two modes are set by register setting according to each case.

| MDIF1 bit | MDIF2 bit | INL1 bit | INL0 bit | INR1 bit | INR0 bit | Lch | Rch |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 1 | IN1+/– | RIN2 |
| 0 | 0 | 0 | 1 | 0 | 1 | LIN2 | RIN2 |

Table 22. MIC/Line In Path Select Example

## ■ MIC Gain Amplifier

The AK4643 has a gain amplifier for microphone input. The gain of MIC-Amp is selected by the MGAIN1-0 bits (see Table 23). The typical input impedance is 60kΩ(typ)@MGAIN1-0 bits = "00" or 30kΩ(typ)@MGAIN1-0 bits = "01", "10" or "11".

| MGAIN1 bit | MGAIN0 bit | Input Gain | |
|---|---|---|---|
| 0 | 0 | 0dB | |
| 0 | 1 | +20dB | Default |
| 1 | 0 | +26dB | |
| 1 | 1 | +32dB | |

Table 23. Mic Input Gain

## ■ MIC Power

When PMMP bit = "1", the MPWR pin supplies power for the microphone. This output voltage is typically 0.75 x AVDD and the load resistance is minimum 0.5kΩ. In case of using two sets of stereo mic, the load resistance is minimum 2kΩ for each channel. No capacitor must not be connected directly to MPWR pin (see Figure 34).

| PMMP bit | MPWR pin | |
|---|---|---|
| 0 | Hi-Z | Default |
| 1 | Output | |

Table 24. MIC Power

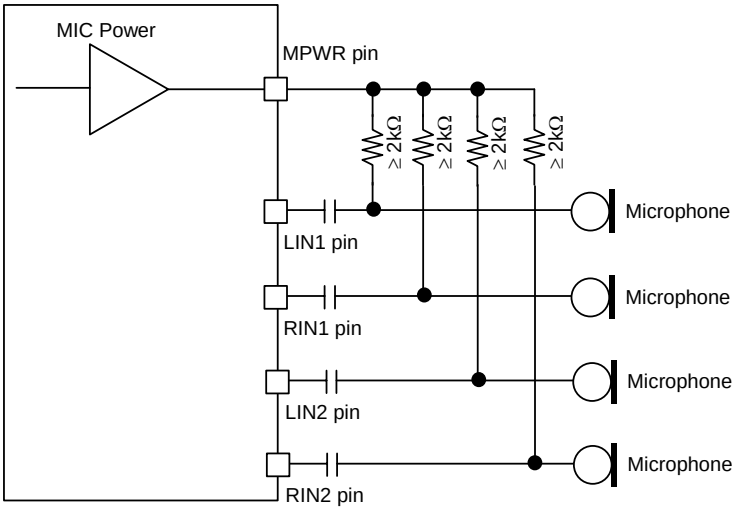



Figure 34. MIC Block Circuit

## ■ Digital EQ/HPF/LPF

The AK4643 performs wind-noise reduction filter, stereo separation emphasis, gain compensation and ALC (Automatic Level Control) by digital domain for A/D converted data (Figure 35). FIL1, FIL3 and EQ blocks are IIR filters of 1st order. The filter coefficient of FIL3, EQ and FIL1 blocks can be set to any value. Refer to the section of "ALC operation" about ALC.

When only DAC is powered-up, digital EQ/HPF/LPF circuit operates at playback path. When only ADC is powered-up or both ADC and DAC are powered-up, digital EQ/HPF/LPF circuit operates at recording path. Even if the path is switched from recording to playback, the register setting of filter coefficient at recording remains. Therefore, FIL3, EQ, FIL1 and GN1-0 bits should be set to "0" if digital EQ/HPF/LPF is not used for playback path.

| PMADL bit, PMADR bit | PMDAC bit | LOOP bit | Status | Digital EQ/HPF/LPF | |
|---|---|---|---|---|---|
| "00" | 0 | x | Power-down | Power-down | Default |
| | 1 | x | Playback | Playback path | |
| "01", "10" or "11" | 0 | x | Recording | Recording path | |
| | 1 | 0 | Recording & Playback | Recording path | |
| | | 1 | Recording Monitor Playback | Recording path | |

Note 44. Stereo separation emphasis circuit is effective only at stereo operation.
Table 25. Digital EQ/HPF/LPF Cirtcuit Setting (x: Don't care)

FIL3 coefficient also sets the attenuation of the stereo separation emphasis.

The combination of GN1-0 bit (Table 26) and EQ coefficient set the compensation gain.

FIL1 and FIL3 blocks become HPF when F1AS and F3AS bits are "0" and become LPF when F1AS and F3AS bits are "1", respectively.

When EQ and FIL1 bits are "0", EQ and FIL1 blocks become "through" (0dB). When FIL3 bit is "0", FIL3 block become "MUTE". When each filter coefficient is changed, each filter should be set to "through" ("MUTE" in case of FIL3).

When MIX bit = "1", only FIL1 is available. In this case, EQ and FIL3 bits should be set to "0".

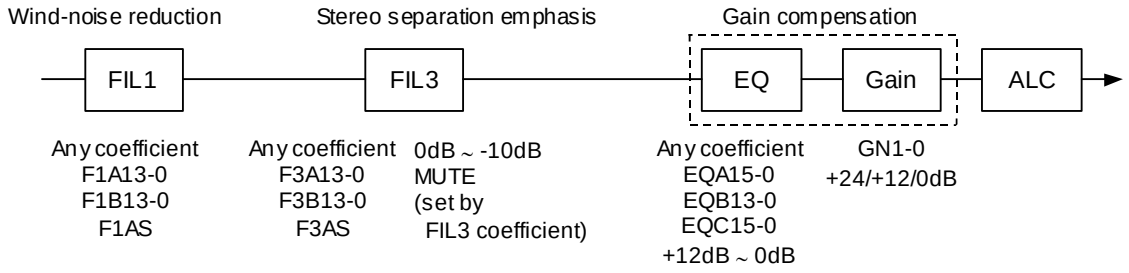



Figure 35. Digital EQ/HPF/LPF

| GN1 | GN0 | Gain | |
|---|---|---|---|
| 0 | 0 | 0dB | Default |
| 0 | 1 | +12dB | |
| 1 | x | +24dB | |

Table 26. Gain select of gain block (x: Don't care)

[Filter Coefficient Setting]

1) When FIL1 and FIL2 are set to “HPF”

fs: Sampling frequency
fc: Cut-off frequency
f: Input signal frequency
K: Filter gain [dB] (Filter gain of should be set to 0dB.)

Register setting
FIL1: F1AS bit = “0”, F1A[13:0] bits =A, F1B[13:0] bits =B
FIL3: F3AS bit = “0”, F3A[13:0] bits =A, F3B[13:0] bits =B
(MSB=F1A13, F1B13, F3A13, F3B13; LSB=F1A0, F1B0, F3A0, F3B0)

$$A = 10^{K/20} \times \frac{1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

| Transfer function | Amplitude | Phase |
|---|---|---|
| $H(z) = A \frac{1 - z^{-1}}{1 + Bz^{-1}}$ | $M(f) = A \sqrt{\frac{2 - 2\cos(2\pi f/fs)}{1 + B^2 + 2B\cos(2\pi f/fs)}}$ | $\theta(f) = \tan^{-1} \frac{(B+1)\sin(2\pi f/fs)}{1 - B + (B-1)\cos(2\pi f/fs)}$ |

2) When FIL1 and FIL2 are set to “LPF”

fs: Sampling frequency
fc: Cut-off frequency
f: Input signal frequency
K: Filter gain [dB] (Filter gain of FIL1 should be set to 0dB.)

Register setting
FIL1: F1AS bit = “1”, F1A[13:0] bits =A, F1B[13:0] bits =B
FIL3: F3AS bit = “1”, F3A[13:0] bits =A, F3B[13:0] bits =B
(MSB=F1A13, F1B13, F3A13, F3B13; LSB=F1A0, F1B0, F3A0, F3B0)

$$A = 10^{K/20} \times \frac{1}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

| Transfer function | Amplitude | Phase |
|---|---|---|
| $H(z) = A \frac{1 + z^{-1}}{1 + Bz^{-1}}$ | $M(f) = A \sqrt{\frac{2 + 2\cos(2\pi f/fs)}{1 + B^2 + 2B\cos(2\pi f/fs)}}$ | $\theta(f) = \tan^{-1} \frac{(B-1)\sin(2\pi f/fs)}{1 + B + (B+1)\cos(2\pi f/fs)}$ |

3) EQ

fs: Sampling frequency
$fc_1$: Pole frequency
$fc_2$: Zero-point frequency
f: Input signal frequency
K: Filter gain [dB] (Maximum +12dB)

Register setting
EQA[15:0] bits =A, EQB[13:0] bits =B, EQC[15:0] bits =C
(MSB=EQA15, EQB13, EQC15; LSB=EQA0, EQB0, EQC0)

$$A = 10^{K/20} \times \frac{1 + 1 / \tan(\pi fc_2/fs)}{1 + 1 / \tan(\pi fc_1/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc_1/fs)}{1 + 1 / \tan(\pi fc_1/fs)}, \quad C = 10^{K/20} \times \frac{1 - 1 / \tan(\pi fc_2/fs)}{1 + 1 / \tan(\pi fc_1/fs)}$$

| Transfer function | Amplitude | Phase |
|---|---|---|
| $H(z) = \frac{A + Cz^{-1}}{1 + Bz^{-1}}$ | $M(f) = \sqrt{\frac{A^2 + C^2 + 2AC\cos(2\pi f/fs)}{1 + B^2 + 2B\cos(2\pi f/fs)}}$ | $\theta(f) = \tan^{-1}\frac{(AB-C)\sin(2\pi f/fs)}{A + BC + (AB+C)\cos(2\pi f/fs)}$ |

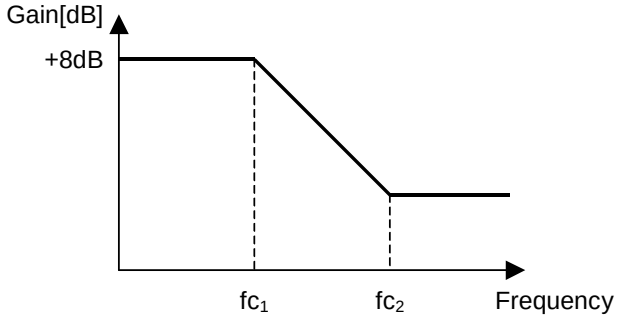
[Translation the filter coefficient calculated by the equations above from real number to binary code (2's complement)]
X = (Real number of filter coefficient calculated by the equations above) x $2^{13}$

X should be rounded to integer, and then should be translated to binary code (2's complement).
MSB of each filter coefficient setting register is sine bit.

[Filter Coefficient Setting Example]

1) FIL1 block
Example: HPF, fs=44.1kHz, fc=100Hz
F1AS bit = "0"
F1A[13:0] bits = 01 1111 1100 0110
F1B[13:0] bits = 10 0000 0111 0100

2) EQ block
Example: fs=44.1kHz, $fc_1$=300Hz, $fc_2$=3000Hz, Gain=+8dB




EQA[15:0] bits = 0000 1001 0110 1110
EQB[13:0] bits = 10 0001 0101 1001
EQC[15:0] bits = 1111 1001 1110 1111

## ■ ALC Operation

The ALC (Automatic Level Control) is done by ALC block when ALC bit is "1". When only DAC is powered-up, ALC circuit operates at playback path. When only ADC is powered-up or both ADC and DAC are powered-up, ALC circuit operates at recording path.

| PMADL bit, PMADR bit | PMDAC bit | LOOP bit | Status | ALC | |
|---|---|---|---|---|---|
| "00" | 0 | x | Power-down | Power-down | Default |
| | 1 | x | Playback | Playback path | |
| "01", "10" or "11" | 0 | x | Recording | Recording path | |
| | 1 | 0 | Recording & Playback | Recording path | |
| | | 1 | Recording Monitor Playback | Recording path | |

Table 27. ALC Setting (x: Don't care)

1. ALC Limiter Operation

During the ALC limiter operation, when either Lch or Rch exceeds the ALC limiter detection level (Table 28), the IVL and IVR values (same value) are attenuated automatically by the amount defined by the ALC limiter ATT step (Table 29).

When ZELMN bit = "0" (zero cross detection is enabled), the IVL and IVR values are changed by ALC limiter operation at the individual zero crossing points of Lch and Rch or at the zero crossing timeout. ZTM1-0 bits set the zero crossing timeout period of both ALC limiter and recovery operation (Table 30).

When ZELMN bit = "1" (zero cross detection is disabled), IVL and IVR values are immediately (period: 1/fs) changed by ALC limiter operation. Attenuation step is fixed to 1 step regardless as the setting of LMAT1-0 bits.

The attenuation operation is done continuously until the input signal level becomes ALC limiter detection level (Table 28) or less. After completing the attenuation operation, unless ALC bit is changed to "0", the operation repeats when the input signal level exceeds LMTH1-0 bits.

| LMTH1 | LMTH0 | ALC Limier Detection Level | ALC Recovery Waiting Counter Reset Level | |
|---|---|---|---|---|
| 0 | 0 | ALC Output ≥ –2.5dBFS | –2.5dBFS > ALC Output ≥ –4.1dBFS | Default |
| 0 | 1 | ALC Output ≥ –4.1dBFS | –4.1dBFS > ALC Output ≥ –6.0dBFS | |
| 1 | 0 | ALC Output ≥ –6.0dBFS | –6.0dBFS > ALC Output ≥ –8.5dBFS | |
| 1 | 1 | ALC Output ≥ –8.5dBFS | –8.5dBFS > ALC Output ≥ –12dBFS | |

Table 28. ALC Limiter Detection Level / Recovery Counter Reset Level

| ZELMN | LMAT1 | LMAT0 | ALC Limiter ATT Step | | |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 step | 0.375dB | Default |
| | 0 | 1 | 2 step | 0.750dB | |
| | 1 | 0 | 4 step | 1.500dB | |
| | 1 | 1 | 8 step | 3.000dB | |
| 1 | x | x | 1step | 0.375dB | |

Table 29. ALC Limiter ATT Step (x: Don't care)

| ZTM1 | ZTM0 | | Zero Crossing Timeout Period | | | |
|---|---|---|---|---|---|---|
| | | | 8kHz | 16kHz | 44.1kHz | |
| 0 | 0 | 128/fs | 16ms | 8ms | 2.9ms | Default |
| 0 | 1 | 256/fs | 32ms | 16ms | 5.8ms | |
| 1 | 0 | 512/fs | 64ms | 32ms | 11.6ms | |
| 1 | 1 | 1024/fs | 128ms | 64ms | 23.2ms | |

Table 30. ALC Zero Crossing Timeout Period

2. ALC Recovery Operation

The ALC recovery operation waits for the WTM2-0 bits (Table 31) to be set after completing the ALC limiter operation. If the input signal does not exceed "ALC recovery waiting counter reset level" (Table 28) during the wait time, the ALC recovery operation is done. The IVL and IVR values are automatically incremented by RGAIN1-0 bits (Table 32) up to the set reference level (Table 33) with zero crossing detection which timeout period is set by ZTM1-0 bits (Table 30). Then the IVL and IVR are set to the same value for both channels. The ALC recovery operation is done at a period set by WTM2-0 bits. When zero cross is detected at both channels during the wait period set by WTM2-0 bits, the ALC recovery operation waits until WTM2-0 period and the next recovery operation is done. If ZTM1-0 is longer than WTM2-0 and no zero crossing occurs, the ALC recovery operation is done at a period set by ZTM1-0 bits.

For example, when the current IVOL value is 30H and RGAIN1-0 bits are set to "01", IVOL is changed to 32H by the auto limiter operation and then the input signal level is gained by 0.75dB (=0.375dB x 2). When the IVOL value exceeds the reference level (REF7-0), the IVOL values are not increased.

When
"ALC recovery waiting counter reset level (LMTH1-0) ≤ Output Signal < ALC limiter detection level (LMTH1-0)" during the ALC recovery operation, the waiting timer of ALC recovery operation is reset. When
"ALC recovery waiting counter reset level (LMTH1-0) > Output Signal",
the waiting timer of ALC recovery operation starts.

The ALC operation corresponds to the impulse noise. When the impulse noise is input, the ALC recovery operation becomes faster than a normal recovery operation (Fast Recovery Operation). When large noise is input to microphone instantaneously, the quality of small level in the large noise can be improved by this fast recovery operation. The speed of fast recovery operation is set by RFST1-0 bits (Table 34).

| WTM2 | WTM1 | WTM0 | | ALC Recovery Operation Waiting Period | | | |
|---|---|---|---|---|---|---|---|
| | | | | 8kHz | 16kHz | 44.1kHz | |
| 0 | 0 | 0 | 128/fs | 16ms | 8ms | 2.9ms | Default |
| 0 | 0 | 1 | 256/fs | 32ms | 16ms | 5.8ms | |
| 0 | 1 | 0 | 512/fs | 64ms | 32ms | 11.6ms | |
| 0 | 1 | 1 | 1024/fs | 128ms | 64ms | 23.2ms | |
| 1 | 0 | 0 | 2048/fs | 256ms | 128ms | 46.4ms | |
| 1 | 0 | 1 | 4096/fs | 512ms | 256ms | 92.9ms | |
| 1 | 1 | 0 | 8192/fs | 1024ms | 512ms | 185.8ms | |
| 1 | 1 | 1 | 16384/fs | 2048ms | 1024ms | 371.5ms | |

Table 31. ALC Recovery Operation Waiting Period

| RGAIN1 | RGAIN0 | GAIN STEP | | |
|---|---|---|---|---|
| 0 | 0 | 1 step | 0.375dB | Default |
| 0 | 1 | 2 step | 0.750dB | |
| 1 | 0 | 3 step | 1.125dB | |
| 1 | 1 | 4 step | 1.500dB | |

Table 32. ALC Recovery GAIN Step

| REF7-0 | GAIN(dB) | Step | |
|---|---|---|---|
| F1H | +36.0 | 0.375dB | |
| F0H | +35.625 | | |
| EFH | +35.25 | | |
| : | : | | |
| E2H | +30.375 | | |
| E1H | +30.0 | | Default |
| E0H | +29.625 | | |
| : | : | | |
| 03H | –53.25 | | |
| 02H | –53.625 | | |
| 01H | –54.0 | | |
| 00H | MUTE | | |

Table 33. Reference Level at ALC Recovery operation

| RFST1 bit | RFST0 bit | Recovery Speed | |
|---|---|---|---|
| 0 | 0 | 4 times | Default |
| 0 | 1 | 8 times | |
| 1 | 0 | 16times | |
| 1 | 1 | N/A | |

Table 34. Fast Recovery Speed Setting

3. Example of ALC Operation

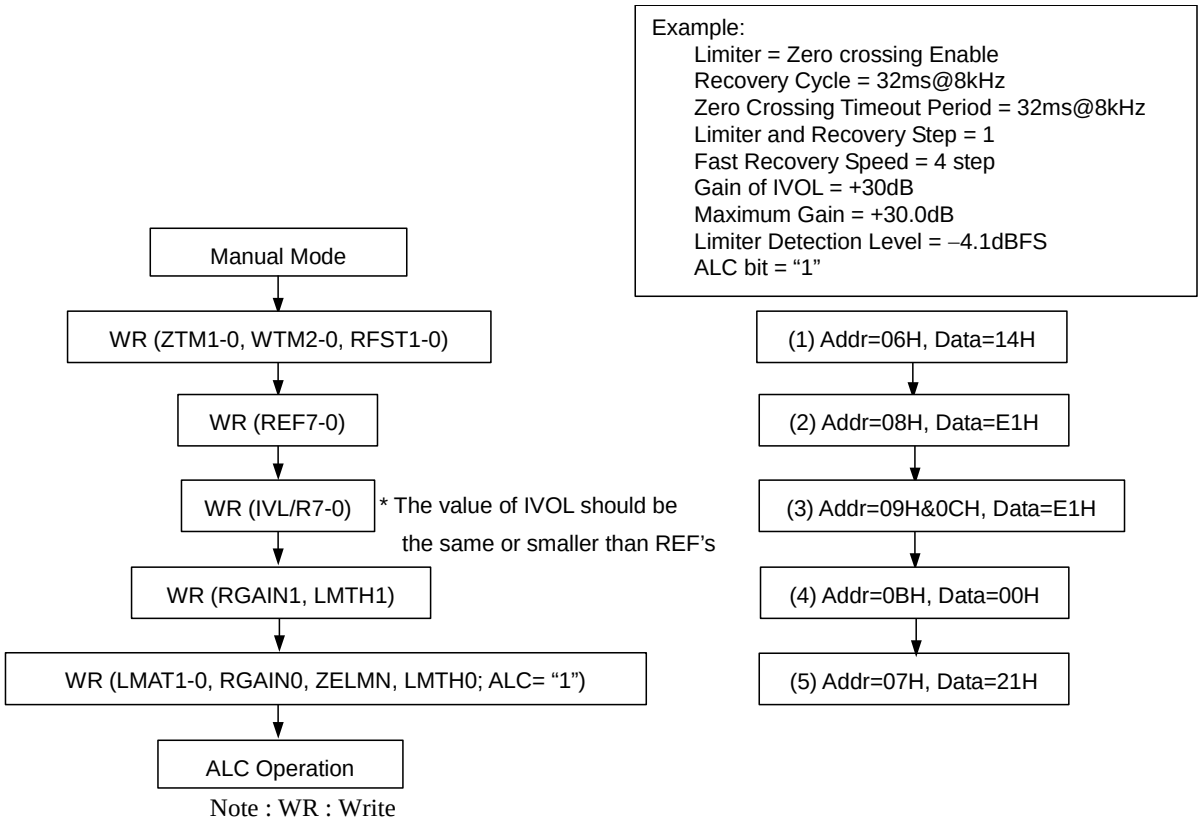
Table 35 shows the examples of the ALC setting for mic recording.

| Register Name | Comment | fs=8kHz | | fs=44.1kHz | |
|---|---|---|---|---|---|
| | | Data | Operation | Data | Operation |
| LMTH1-0 | Limiter detection Level | 01 | –4.1dBFS | 01 | –4.1dBFS |
| ZELMN | Limiter zero crossing detection | 0 | Enable | 0 | Enable |
| ZTM1-0 | Zero crossing timeout period | 01 | 32ms | 11 | 23.2ms |
| WTM2-0 | Recovery waiting period<br>*WTM2-0 bits should be the same or longer data as ZTM1-0 bits. | 001 | 32ms | 011 | 23.2ms |
| REF7-0 | Maximum gain at recovery operation | E1H | +30dB | E1H | +30dB |
| IVL7-0, IVR7-0 | Gain of IVOL | E1H | +30dB | E1H | +30dB |
| LMAT1-0 | Limiter ATT step | 00 | 1 step | 00 | 1 step |
| RGAIN1-0 | Recovery GAIN step | 00 | 1 step | 00 | 1 step |
| RFST1-0 | Fast Recovery Speed | 00 | 4 times | 00 | 4 times |
| ALC | ALC enable | 1 | Enable | 1 | Enable |

Table 35. Example of the ALC setting

The following registers should not be changed during the ALC operation. These bits should be changed after the ALC operation is finished by ALC bit = “0” or PMADL=PMADR bits = “0”.

- **LMTH1-0, LMAT1-0, WTM2-0, ZTM1-0, RGAIN1-0, REF7-0, ZELMN, RFST1-0**




Note : WR : Write

Figure 36. Registers set-up sequence at ALC operation

## ■ Input Digital Volume (Manual Mode)

The input digital volume becomes a manual mode when ALC bit is “0”. This mode is used in the case shown below.

1. After exiting reset state, set-up the registers for the ALC operation (ZTM1-0, LMTH1-0 and etc)
2. When the registers for the ALC operation (Limiter period, Recovery period and etc) are changed. For example; when the change of the sampling frequency.
3. When IVOL is used as a manual volume.

IVL7-0 and IVR7-0 bits set the gain of the volume control (Table 36). The IVOL value is changed at zero crossing or timeout. Zero crossing timeout period is set by ZTM1-0 bits. If IVL7-0 or IVR7-0 bits are written during PMADL=PMADR bits = “0”, IVOL operation starts with the written values at the end of the ADC initialization cycle after PMADL or PMADR bit is changed to “1”.

Even if the path is switched from recording to playback, the register setting of IVOL remains. Therefore, IVL7-0 and IVR7-0 bits should be set to “91H” (0dB).

| IVL7-0<br>IVR7-0 | GAIN (dB) | Step | |
|---|---|---|---|
| F1H | +36.0 | 0.375dB | |
| F0H | +35.625 | | |
| EFH | +35.25 | | |
| : | : | | |
| E2H | +30.375 | | |
| E1H | +30.0 | | Default |
| E0H | +29.625 | | |
| : | : | | |
| 03H | –53.25 | | |
| 02H | –53.625 | | |
| 01H | –54 | | |
| 00H | MUTE | | |

Table 36. Input Digital Volume Setting

When writing to the IVL7-0 and IVR7-0 bits continuouslly, the control register should be written by an interval more than zero crossing timeout. If not, IVL and IVR are not changed since zero crossing counter is reset at every write operation. If the same register value as the previous write operation is written to IVL and IVR, this write operation is ignored and zero crossing counter is not reset. Therefore, IVL and IVR can be written by an interval less than zero crossing timeout.

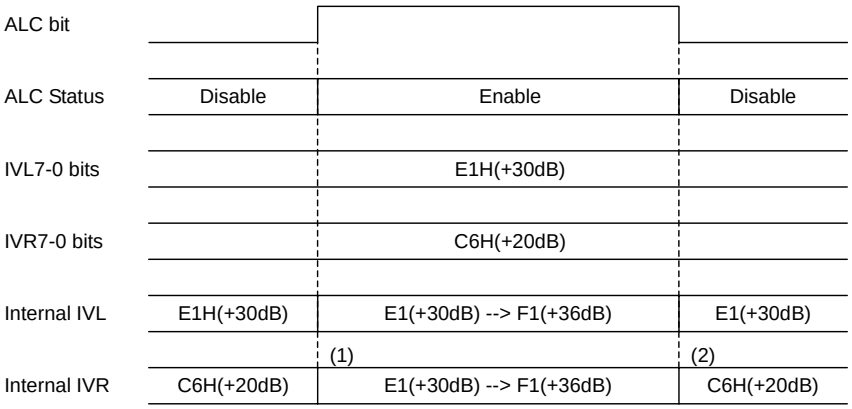



Figure 37. IVOL value during ALC operation

(1) The IVL value becomes the start value if the IVL and IVR are different when the ALC starts. The wait time from ALC bit = "1" to ALC operation start by IVL7-0 bits is at most recovery time (WTM2-0 bits) plus zerocross timeout period (ZTM1-0 bits).
(2) Writing to IVL and IVR registers (09H and 0CH) is ignored during ALC operation. After ALC is disabled, the IVOL changes to the last written data by zero crossing or timeout. When ALC is enabled again, ALC bit should be set to "1" by an interval more than zero crossing timeout period after ALC bit = "0".

## ■ De-emphasis Filter

The AK4643 includes the digital de-emphasis filter (tc = 50/15μs) by IIR filter. Setting the DEM1-0 bits enables the de-emphasis filter (Table 37).

| DEM1 | DEM0 | Mode | |
|---|---|---|---|
| 0 | 0 | 44.1kHz | |
| 0 | 1 | OFF | Default |
| 1 | 0 | 48kHz | |
| 1 | 1 | 32kHz | |

Table 37. De-emphasis Control

## ■ Bass Boost Function

The BST1-0 bits control the amount of low frequency boost applied to the DAC output signal (Table 38). If the BST1-0 bits are set to "01" (MIN Level), use a 47μF capacitor for AC-coupling. If the boosted signal exceeds full scale, the analog output clips to the full scale. Figure 38 shows the boost frequency response at –20dB signal input.

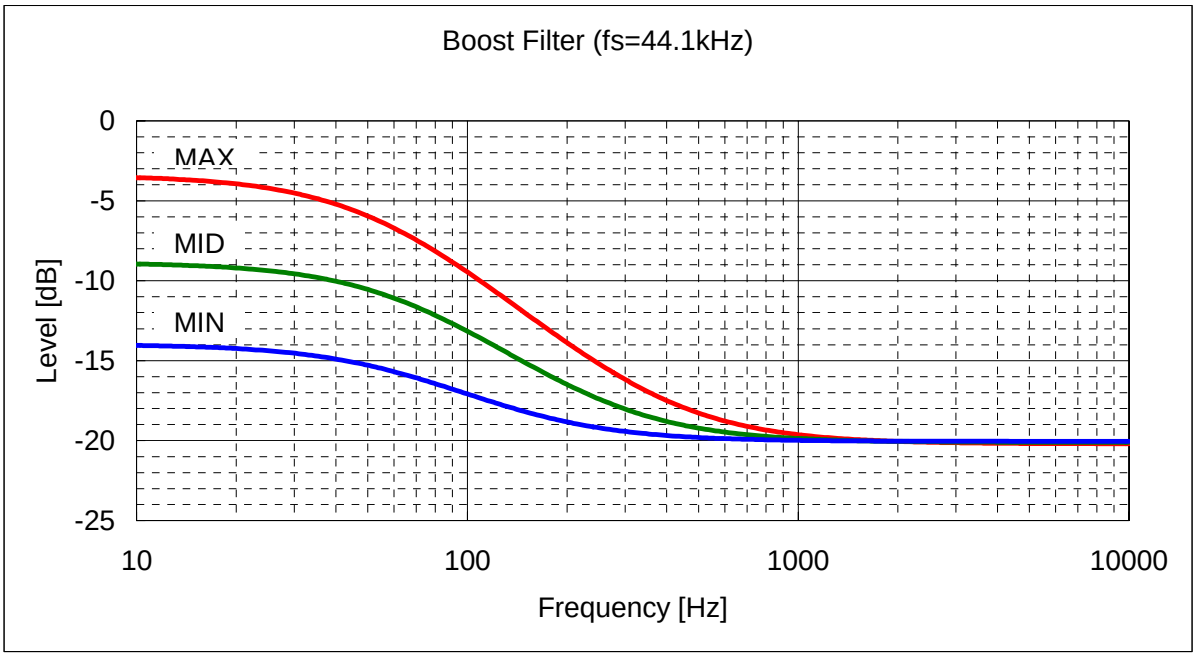



Figure 38. Bass Boost Frequency Response (fs=44.1kHz)

| BST1 | BST0 | Mode | |
|---|---|---|---|
| 0 | 0 | OFF | Default |
| 0 | 1 | MIN | |
| 1 | 0 | MID | |
| 1 | 1 | MAX | |

Table 38. Bass Boost Control

## ■ Digital Output Volume

The AK4643 has a digital output volume (256 levels, 0.5dB step, Mute). The volume can be set by the DVL7-0 and DVR7-0 bits. The volume is included in front of a DAC block. The input data of DAC is changed from +12 to –115dB or MUTE. When the DVOLC bit = "1", the DVL7-0 bits control both Lch and Rch attenuation levels. When the DVOLC bit = "0", the DVL7-0 bits control Lch level and DVR7-0 bits control Rch level. This volume has a soft transition function. The DVTM bit sets the transition time between set values of DVL/R7-0 bits as either 1061/fs or 256/fs (Table 40). When DVTM bit = "0", a soft transition between the set values occurs (1062 levels). It takes 1061/fs (=24ms@fs=44.1kHz) from 00H (+12dB) to FFH (MUTE).

| DVL/R7-0 | Gain | |
|---|---|---|
| 00H | +12.0dB | |
| 01H | +11.5dB | |
| 02H | +11.0dB | |
| : | : | |
| 18H | 0dB | Default |
| : | : | |
| FDH | –114.5dB | |
| FEH | –115.0dB | |
| FFH | MUTE (–∞) | |

Table 39. Digital Volume Code Table

| DVTM bit | Transition time between DVL/R7-0 bits = 00H and FFH | | | |
|---|---|---|---|---|
| | Setting | fs=8kHz | fs=44.1kHz | |
| 0 | 1061/fs | 133ms | 24ms | Default |
| 1 | 256/fs | 32ms | 6ms | |

Table 40. Transition Time Setting of Digital Output Volume

## ■ Soft Mute

Soft mute operation is performed in the digital domain. When the SMUTE bit goes to “1”, the output signal is attenuated by –∞ (“0”) during the cycle set by the DVTM bit. When the SMUTE bit is returned to “0”, the mute is cancelled and the output attenuation gradually changes to the value set by the DVL/R7-0 bits during the cycle set of the DVTM bit. If the soft mute is cancelled within the cycle set by the DVTM bit after starting the operation, the attenuation is discontinued and returned to the value set by the DVL/R7-0 bits. The soft mute is effective for changing the signal source without stopping the signal transmission (Figure 39).

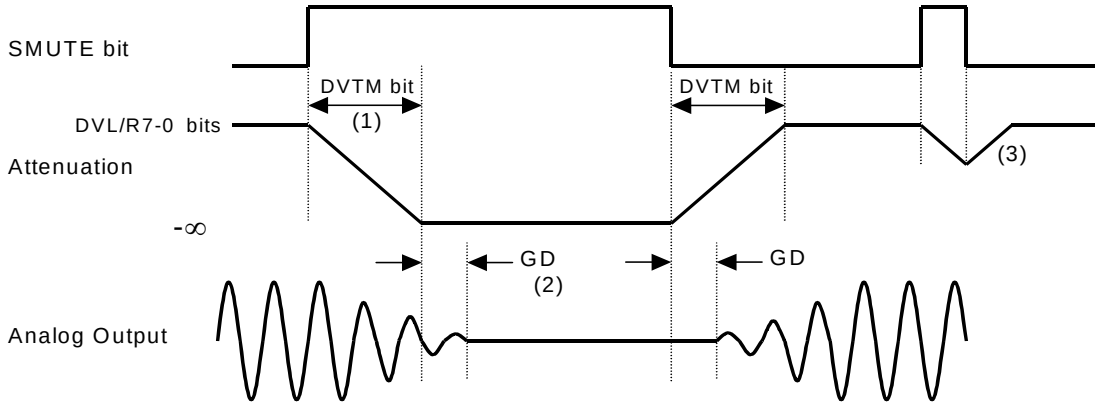



Figure 39. Soft Mute Function

(1) The output signal is attenuated until –∞ (“0”) by the cycle set by the DVTM bit.
(2) Analog output corresponding to digital input has the group delay (GD).
(3) If the soft mute is cancelled within the cycle set by the DVTM bit, the attenuation is discounted and returned to the value set by the DVL/R7-0 bits.

## ■ Analog Mixing: Stereo Input (LIN2/RIN2, AIN3 bit = "1": LIN3/RIN3 pins)

When PMAINL2=PMAINR2 bits = "1", LIN2 and RIN2 pins can be used as stereo line input for analog mixing. When the LINS2 and RINS2 bits are set to "1", the input signal from the LIN2/RIN2 pins is output to Speaker-Amp. When the LINH2 and RINH2 bits are set to "1", the input signal from the LIN2/RIN2 pins is output to Headphone-Amp. When the LINL2/RINR2 bits are set to "1", the input signal from the LIN2/RIN2 pins is output to the stereo line output amplifier.

When the analog mixing is used, A/D converter is also available if PMADL or PMADR bit is "1". In this case, the input resistance of LIN2/RIN2 pins becomes 30kΩ (typ) at MGAIN1-0 bits = "00" and 20kΩ (typ) at MGAIN1-0 bits = "01", "10" or "11", respectively.

When AIN3 bit = "1", MIN and VCOC pins becomes LIN3 and RIN3 pins, respectively. In this case, PLL is not available. When PMAINL3=PMAINR3 bits = "1", LIN3 and RIN3 pins can be used as stereo line input for analog mixing. When PMMICL=PMMICR=MICL3=MICR3 bits = "1", analog mixing source is changed from LIN3/RIN3 input to MIC-Amp output signal. When the LINS3 and RINS3 bits are set to "1", the input signal from the LIN3/RIN3 pins is output to Speaker-Amp. When the LINH3 and RINH3 bits are set to "1", the input signal from the LIN3/RIN3 pins is output to Headphone-Amp. When the LINL3/RINR3 bits are set to "1", the input signal from the LIN3/RIN3 pins is output to the stereo line output amplifier.

When the analog mixing is used, A/D converter is also available if PMADL or PMADR bit is "1". When the analog mixing is used at MICL3=MICR3 bits = "0", the input resistance of LIN3/RIN3 pins becomes 30kΩ (typ) at MGAIN1-0 bits = "00" and 20kΩ (typ) at MGAIN1-0 bits = "01", "10" or "11", respectively. When the analog mixing is used at MICL3=MICR3 bits = "1", the input resistance of LIN3/RIN3 pins becomes 60kΩ (typ) at MGAIN1-0 bits = "00" and 30kΩ (typ) at MGAIN1-0 bits = "01", "10" or "11", respectively.

Table 41, Table 42, Table 43 and Table 44show the typical gain.

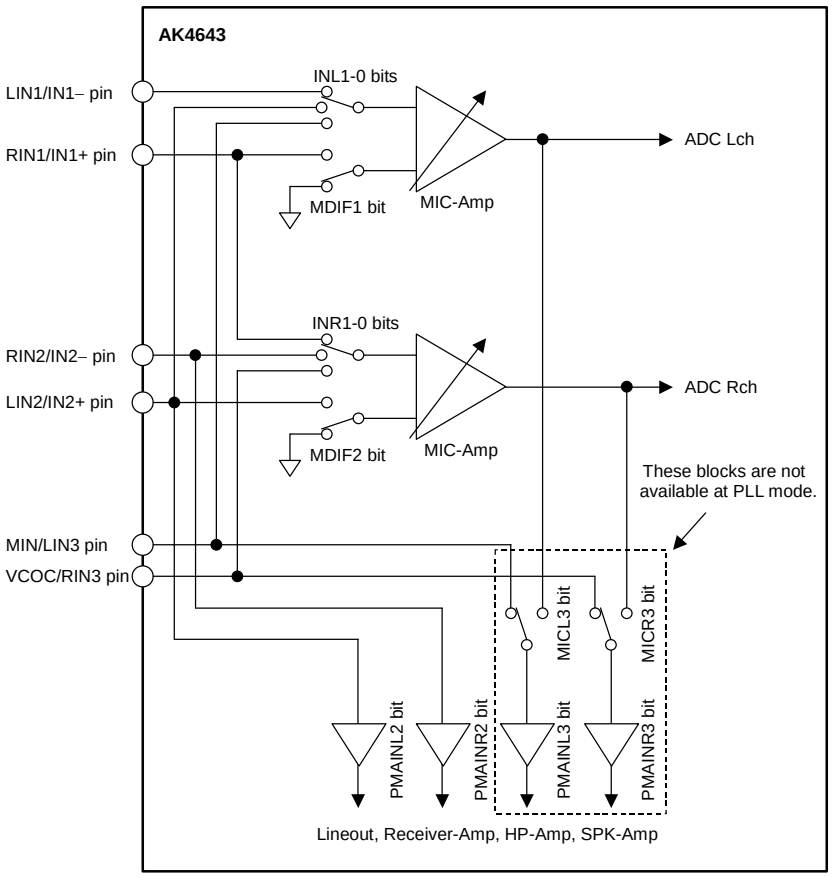



Figure 40. Analog Mixing Circuit

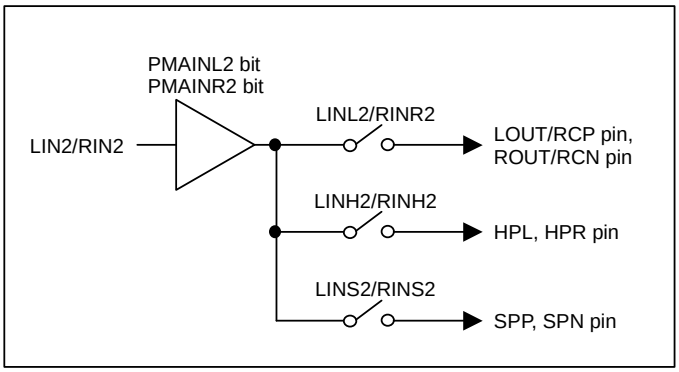



Figure 41. Analog Mixing Circuit (LIN2/RIN2)

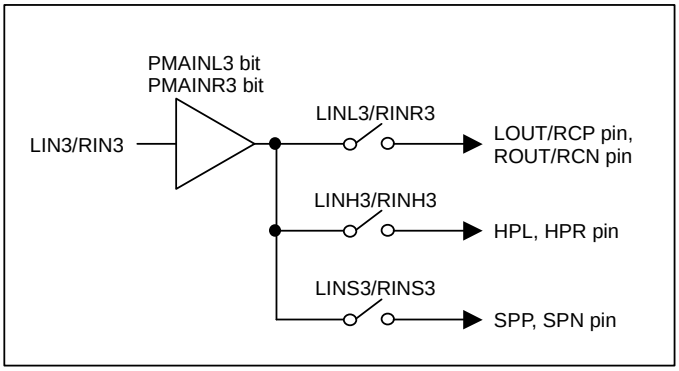



Figure 42. Analog Mixing Circuit (LIN3/RIN3; PLL is not available)

| LOVL bit | LIN2/RIN2/LIN3/RIN3 → LOUT/ROUT | |
|---|---|---|
| 0 | 0dB | Default |
| 1 | +2dB | |

Table 41. LIN2/RIN2/LIN3/RIN3 Input → LOUT/ROUT Output Gain (typ)

| LOVL bit | LIN2/RIN2/LIN3/RIN3 → RCP/RCN | |
|---|---|---|
| 0 | 0dB | Default |
| 1 | +2dB | |

Table 42. LIN2/RIN2/LIN3/RIN3 Input → RCP/RCN Output Gain (typ)

| HPG bit | LIN2/RIN2/LIN3/RIN3 → HPL/HPR | |
|---|---|---|
| 0 | 0dB | Default |
| 1 | +3.6dB | |

Table 43. LIN2/RIN2/LIN3/RIN3 Input → Headphone-Amp Output Gain (typ)

| SPKG1-0 bits | LIN2/RIN2/LIN3/RIN3 → SPP/SPN | | |
|---|---|---|---|
| | ALC bit = "0" | ALC bit = "1" | |
| 00 | –1.59dB | +0.41dB | Default |
| 01 | +0.41dB | +2.41dB | |
| 10 | +4.63dB | +6.63dB | |
| 11 | +6.63dB | +8.63dB | |

Table 44. LIN2/RIN2/LIN3/RIN3 Input → Speaker-Amp Output Gain (typ)

## ■ Analog Mixing: Mono Input (MIN pin)

When AIN3 bit = "0", MIN pin is used as mono input for analog mixing. When the PMMIN bit is set to "1", the mono input is powered-up. When the MINS bit is set to "1", the input signal from the MIN pin is output to Speaker-Amp. When the MINH bit is set to "1", the input signal from the MIN pin is output to Headphone-Amp. When the MINL bit is set to "1", the input signal from the MIN pin is output to the stereo line output amplifier. The external resister Ri adjusts the signal level of MIN input. Table 45, Table 47 and Table 48 show the typical gain example at $R_i$ = 20kΩ. This gain is in inverse proportion to $R_i$.

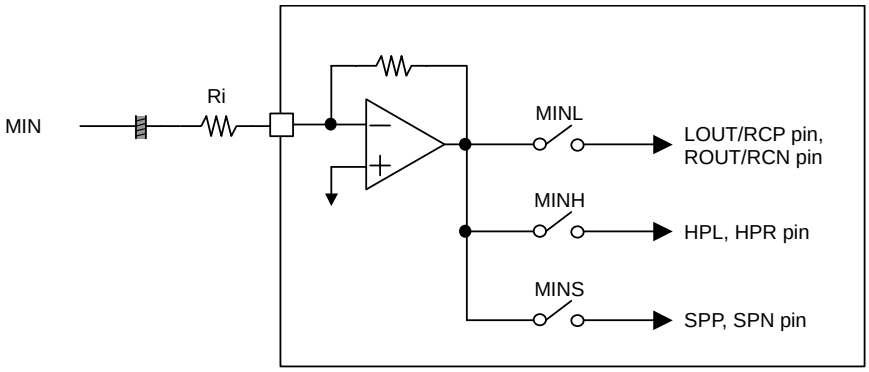



Figure 43 Block Diagram of MIN pin

| LOVL bit | MIN → LOUT/ROUT | |
|---|---|---|
| 0 | 0dB | Default |
| 1 | +2dB | |

Table 45. MIN Input → LOUT/ROUT Output Gain (typ) at $R_i$ = 20kΩ

| LOVL bit | MIN → RCP/RCN | |
|---|---|---|
| 0 | 0dB | Default |
| 1 | +2dB | |

Table 46. MIN Input → RCP/RCN Output Gain (typ) at $R_i$ = 20kΩ

| HPG bit | MIN → HPL/HPR | |
|---|---|---|
| 0 | –20dB | Default |
| 1 | –16.4dB | |

Table 47. MIN Input → Headphone-Amp Output Gain (typ) at $R_i$ = 20kΩ

| SPKG1-0 bits | MIN → SPP/SPN | | |
|---|---|---|---|
| | ALC bit = "0" | ALC bit = "1" | |
| 00 | +4.43dB | +6.43dB | Default |
| 01 | +6.43dB | +8.43dB | |
| 10 | +10.65dB | +12.65dB | |
| 11 | +12.65dB | +14.65dB | |

Table 48. MIN Input → Speaker-Amp Output Gain (typ) at $R_i$ = 20kΩ

## ■ Stereo Line Output (LOUT/ROUT pins)

When DACL bit is "1", Lch/Rch signal of DAC is output from the LOUT/ROUT pins which is single-ended. When DACL bit is "0", output signal is muted and LOUT/ROUT pins output VCOM voltage. The load impedance is 10kΩ (min.). When the PMLO=LOPS bits = "0", the stereo line output enters power-down mode and the output is pulled-down to AVSS by 100kΩ(typ). When the LOPS bit is "1", stereo line output enters power-save mode. Pop noise at power-up/down can be reduced by changing PMLO bit at LOPS bit = "1". In this case, output signal line should be pulled-down to AVSS by 20kΩ after AC coupled as Figure 45. Rise/Fall time is 300ms(max) at C=1μF and AVDD=3.3V. When PMLO=LOPS bits = "1", stereo line output is in normal operation.

LOVL bit set the gain of stereo line output.

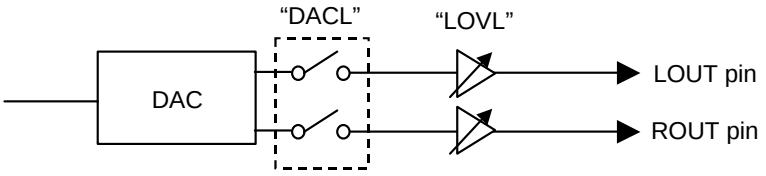



Figure 44. Stereo Line Output

| LOPS | PMLO | Mode | LOUT/ROUT pin | |
|---|---|---|---|---|
| 0 | 0 | Power-down | Pull-down to AVSS | Default |
| | 1 | Normal Operation | Normal Operation | |
| 1 | 0 | Power-save | Fall down to AVSS | |
| | 1 | Power-save | Rise up to VCOM | |

Table 49. Stereo Line Output Mode Select (x: Don't care)

| LOVL | Gain | Output Voltage (typ) | |
|---|---|---|---|
| 0 | 0dB | 0.6 x AVDD | Default |
| 1 | +2dB | 0.757 x AVDD | |

Table 50. Stereo Line Output Volume Setting

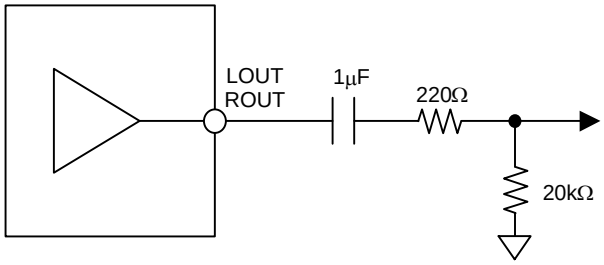



Figure 45. External Circuit for Stereo Line Output (in case of using Pop Reduction Circuit)

**<Stereo Line Output Control Sequence (in case of using Pop Reduction Circuit)>**

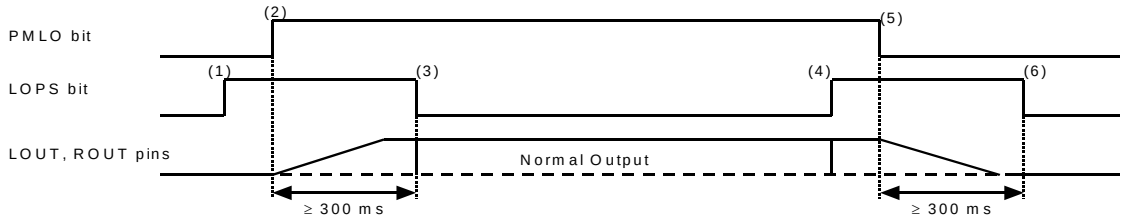



Figure 46. Stereo Line Output Control Sequence (in case of using Pop Reduction Circuit)

(1) Set LOPS bit = “1”. Stereo line output enters the power-save mode.
(2) Set PMLO bit = “1”. Stereo line output exits the power-down mode.
LOUT and ROUT pins rise up to VCOM voltage. Rise time is 200ms (max 300ms) at C=1μF and AVDD=3.3V.
(3) Set LOPS bit = “0” after LOUT and ROUT pins rise up. Stereo line output exits the power-save mode.
Stereo line output is enabled.
(4) Set LOPS bit = “1”. Stereo line output enters power-save mode.
(5) Set PMLO bit = “0”. Stereo line output enters power-down mode.
LOUT and ROUT pins fall down to AVSS. Fall time is 200ms (max 300ms) at C=1μF and AVDD=3.3V.
(6) Set LOPS bit = “0” after LOUT and ROUT pins fall down. Stereo line output exits the power-save mode.

### <Analog Mixing Circuit for Stereo Line Output>

When AIN3 bit = “0”, DACL, MINL, LINL2 and RINR2 bits controls each path switch.
MIN path mixing gain is 0dB(typ)@LOVL bit = “0” when the external input resistance is 20kΩ.
LIN2, RIN2 and DAC pathes mixing gain is 0dB(typ)@LOVL bit = “0”.

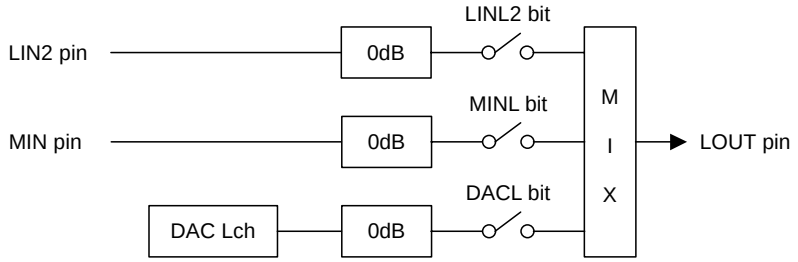



Figure 47. LOUT Mixing Circuit (AIN3 bit = “0”, LOVL bit = “0”)

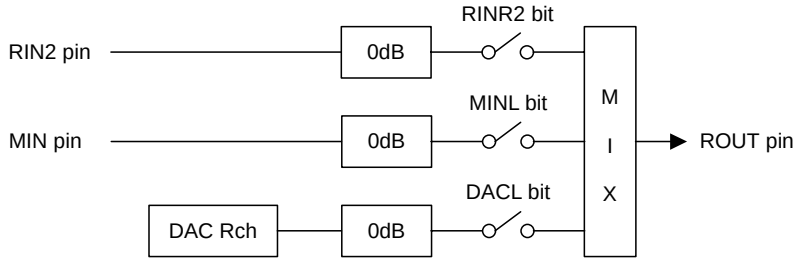



Figure 48. ROUT Mixing Circuit (AIN3 bit = “0”, LOVL bit = “0”)

When AIN3 bit = “1”, DACL, LINL2, RINR2, LINL3, RINR3, MICL3 and MICR3 bits controls each path switch. All pathes mixing gain is 0dB(typ)@LOVL bit = “0”.

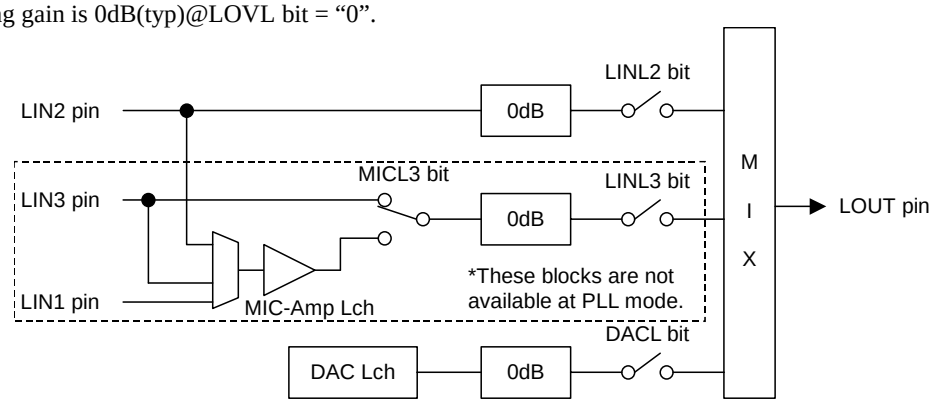



Figure 49. LOUT Mixing Circuit (AIN3 bit = “1”, LOVL bit = “0”)

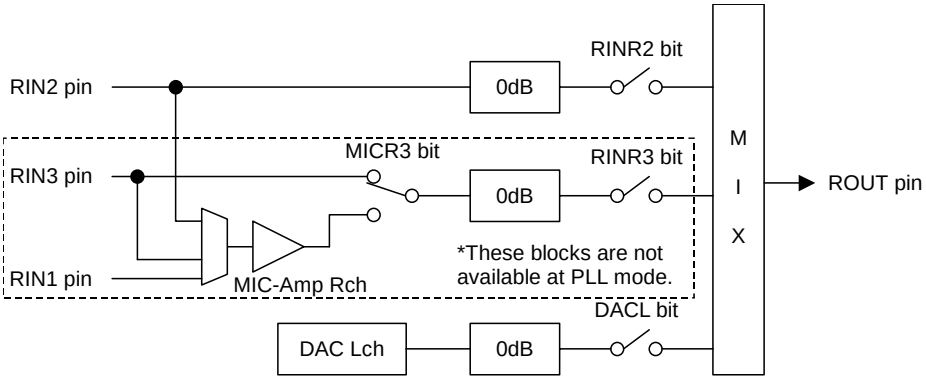



Figure 50. ROUT Mixing Circuit (AIN3 bit = “1”, LOVL bit = “0”)

### ■ Mono Reveiver Output (RCP/RCN pins)

When RCV bit = "1", LOUT/ROUT pins become RCP/RCN pins, respectively. Lch/Rch signal of DAC or LIN2/RIN2/LIN3/RIN3 is output from the RCP/RCN pins which is BTL as (L+R)/2 signal. The load impedance is 32Ω (min). When the PMLO bit = "0", the mono receiver output enters power-down mode and the output is Hi-Z. When the PMLO bit is "1" and LOPS bit is "1", mono receiver output enters power-save mode. Pop noise at power-up/down can be reduced by changing PMLO bit at LOPS bit = "0". When PMLO bit = "1" and LOPS bit = "0", mono receiver output enters in normal operation. LOVL bit set the gain of mono receiver output.

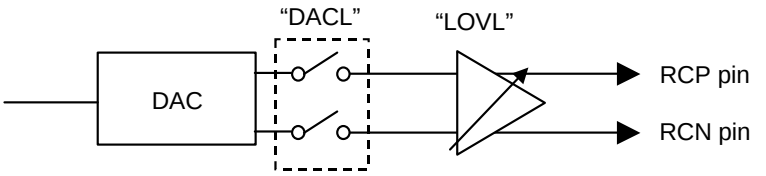



Figure 51. Mono Receiver Output

| LOVL | Gain | Output Voltage (typ) | |
|---|---|---|---|
| 0 | +6dB | 0.59 x AVDD @–6dBFS | Default |
| 1 | +8dB | 0.59 x AVDD @–8dBFS | |

Table 51. Mono Receiver Output Volume Setting

| PMLO | LOPS | Mode | RCP | RCN | |
|---|---|---|---|---|---|
| 0 | x | Power-down | Hi-Z | Hi-Z | |
| 1 | 1 | Power-save | Hi-Z | VCOM/2 | Default |
| | 0 | Normal Operation | Normal Operation | Normal Operation | |

Table 52. Receiver-Amp Mode Setting (x: Don't care)

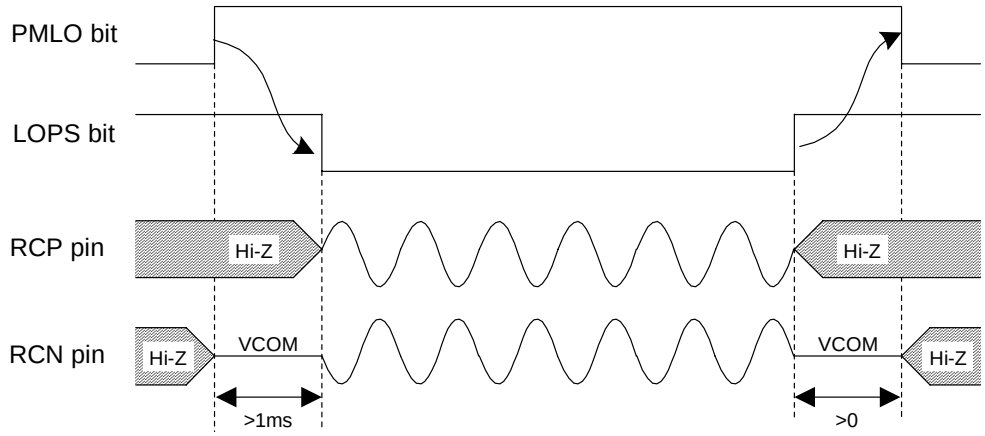



Figure 52. Power-up/Power-down Timing for Receiver-Amp

### <Analog Mixing Circuit for Receiver Output>

When AIN3 bit = “0”, DACL, MINL, LINL2 and RINR2 bits controls each path switch.
MIN path mixing gain is +6dB(typ)@LOVL bit = “0” when the external input resistance is 20kΩ.
LIN2, RIN2 and DAC pathes mixing gain is 0dB(typ)@LOVL bit = “0”.

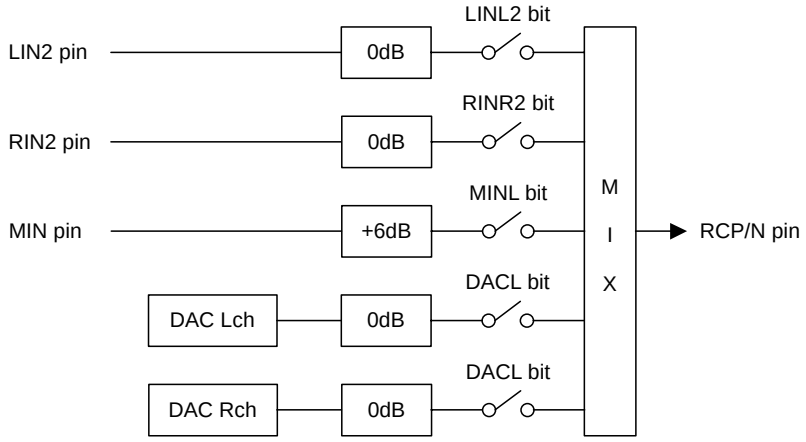



Figure 53. Receiver Mixing Circuit (AIN3 bit = “0”, LOVL bit = “0”)

When AIN3 bit = “1”, DACL, LINL2, RINR2, LINL3, RINR3, MICL3 and MICR3 bits controls each path switch. All pathes mixing gain is 0dB(typ)@LOVL bit = “0”.

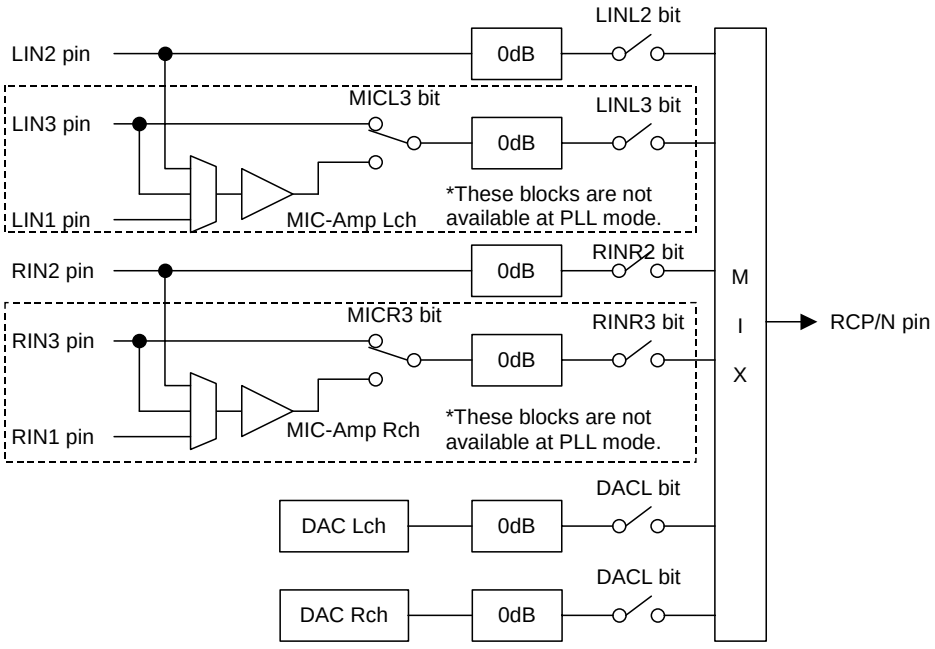



Figure 54. Receiver Mixing Circuit (AIN3 bit = “1”, LOVL bit = “0”)

## ■ Headphone Output

Power supply voltage for the Headphone-Amp is supplied from the HVDD pin and centered on the HVDD/2 voltage at VBAT bit = "0". The load resistance is 16Ω (min). HPG bit selects the output voltage (see Table 53).

| HPG bit | 0 | 1 |
|---|---|---|
| Output Voltage [Vpp] | 0.6 x AVDD | 0.91 x AVDD |

Table 53. Headphone-Amp Output Voltage

When the HPMTN bit is "0", the common voltage of Headphone-Amp falls and the outputs (HPL and HPR pins) go to "L" (HVSS). When the HPMTN bit is "1", the common voltage rises to HVDD/2 at VBAT bit = "0". A capacitor between the MUTET pin and ground reduces pop noise at power-up. Rise/Fall time constant is in proportional to HVDD voltage and the capacitor at MUTET pin.

[Example]: A capacitor between the MUTET pin and ground = 1.0μF, HVDD=3.3V:
Rise/fall time constant: τ = 100ms(typ), 250ms(max)
Time until the common goes to HVSS when HPMTN bit = "1" → "0": 500ms(max)

When PMHPL and PMHPR bits are "0", the Headphone-Amp is powered-down, and the outputs (HPL and HPR pins) go to "L" (HVSS).

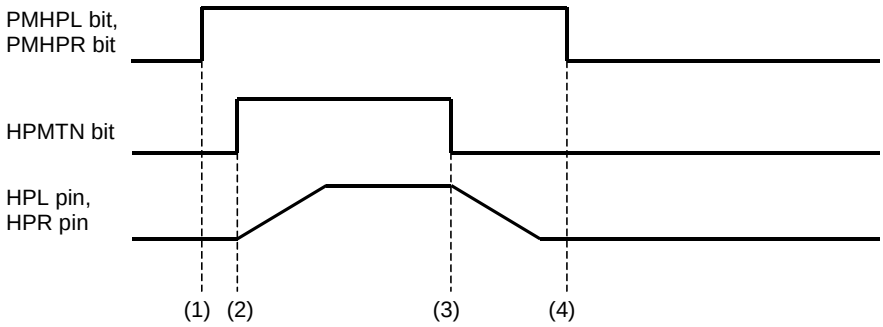



Figure 55. Power-up/Power-down Timing for Headphone-Amp

(1) Headphone-Amp power-up (PMHPL, PMHPR bit = "1"). The outputs are still HVSS.
(2) Headphone-Amp common voltage rises up (HPMTN bit = "1"). Common voltage of Headphone-Amp is rising.
(3) Headphone-Amp common voltage falls down (HPMTN bit = "0"). Common voltage of Headphone-Amp is falling.
(4) Headphone-Amp power-down (PMHPL, PMHPR bit = "0"). The outputs are HVSS. If the power supply is switched off or Headphone-Amp is powered-down before the common voltage goes to HVSS, some POP noise occurs.

When BOOST=OFF, the cut-off frequency (fc) of Headphone-Amp depends on the external resistor and capacitor. This fc can be shifted to lower frequency by using bass boost function. Table 54 shows the cut off frequency and the output power for various resistor/capacitor combinations. The headphone impedance $R_L$ is 16Ω. Output powers are shown at HVDD = 2.7, 3.0 and 3.3V. The output voltage of headphone is 0.6 x AVDD (Vpp).

When an external resistor R is smaller than 12Ω, put an oscillation prevention circuit (0.22μF±20% capacitor and 10Ω±20% resistor) because it has the possibility that Headphone-Amp oscillates.

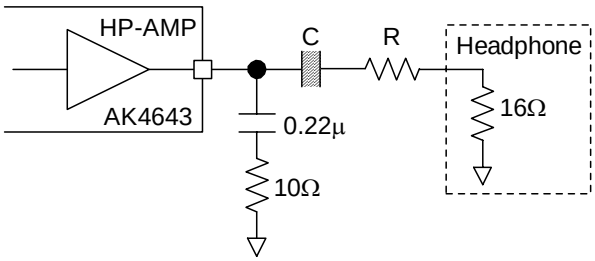



Figure 56. External Circuit Example of Headphone

| HPG bit | R [Ω] | C [μF] | fc [Hz] BOOST =OFF | fc [Hz] BOOST =MIN fs=44.1kHz | Output Power [mW]@0dBFS | | |
|---|---|---|---|---|---|---|---|
| | | | | | HVDD=3.0V AVDD=3.0V | HVDD=3.3V AVDD=3.3V | HVDD=5V AVDD=3.3V |
| 0 | 0 | 220 | 45 | 17 | 25.3 | 30.6 | 30.6 |
| | | 100 | 100 | 43 | | | |
| | 6.8 | 100 | 70 | 28 | 12.5 | 15.1 | 15.1 |
| | | 47 | 149 | 78 | | | |
| | 16 | 100 | 50 | 19 | 6.3 | 7.7 | 7.7 |
| | | 47 | 106 | 47 | | | |
| 1 | 0 | 220 | 45 | 17 | 51 (Note 46) | 62 (Note 46) | 70 |
| | | 100 | 100 | 43 | | | |
| | 100 | 22 | 62 | 25 | 1.1 | 1.3 | 1.3 |
| | | 10 | 137 | 69 | | | |

Table 54. External Circuit Example

Note 45. Output power at 16Ω load.

Note 46. Output signal is clipped.

### <Headphone-Amp PSRR>

When HVDD is directly supplied from the battery in the mobile phone system, RF noise may influences headphone output performance. When VBAT bit is set to "1", HP-Amp PSRR for the noise applied to HVDD is improved. In this case, HP-Amp common voltage is 0.64 x AVDD (typ). When AVDD is 3.3V, common voltage is 2.1V. Therefore, when HVDD voltage becomes lower than 4.2V, the output signal will be clipped easily.

| VBAT bit | 0 | 1 |
|---|---|---|
| Common Voltage [V] | 0.5 x HVDD | 0.64 x AVDD |

Table 55. HP-Amp Common Voltage

### <Analog Mixing Circuit for Headphone Output>

When AIN3 bit = “0”, DACH, MINH, LINH2 and RINH2 bits controls each path switch.
MIN path mixing gain is –20dB(typ)@HPG bit = “0” when the external input resistance is 20kΩ.
LIN2, RIN2 and DAC pathes mixing gain is 0dB(typ)@HPG bit = “0”.

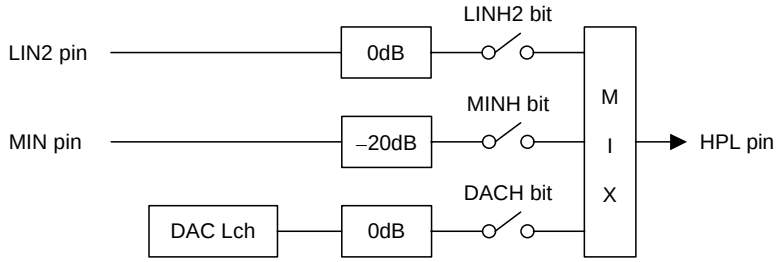



Figure 57. HPL Mixing Circuit (AIN3 bit = “0”, HPG bit = “0”)

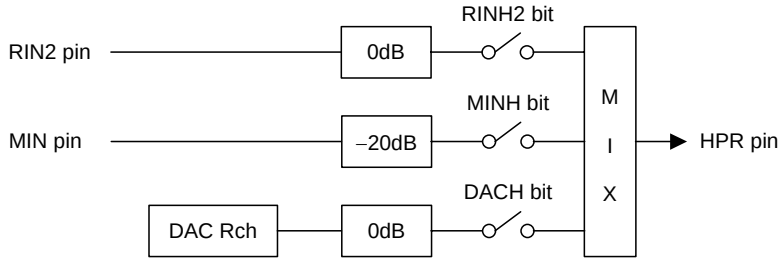



Figure 58. HPR Mixing Circuit (AIN3 bit = “0”, HPG bit = “0”)

When AIN3 bit = “1”, DACH, LINH2, RINH2, LINH3, RINH3, MICL3 and MICR3 bits controls each path switch. All pathes mixing gain is 0dB(typ)@HPG bit = “0”.
,

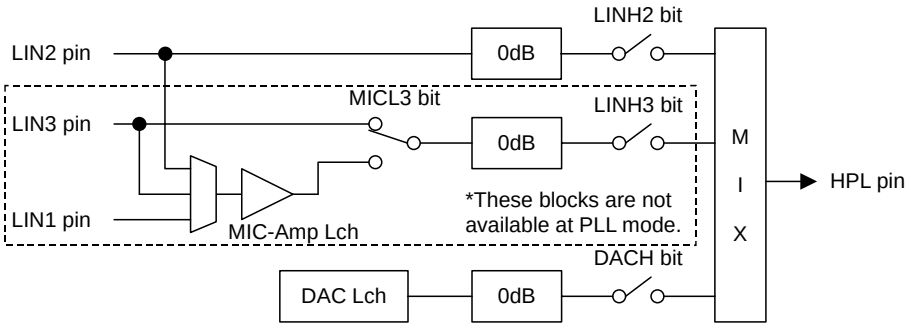



Figure 59. HPL Mixing Circuit (AIN3 bit = “1”, HPG bit = “0”)

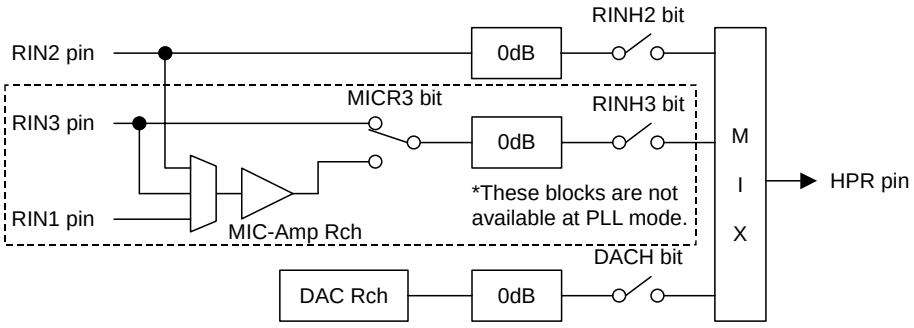



Figure 60. HPR Mixing Circuit (AIN3 bit = “1”, HPG bit = “0”)

## ■ Speaker Output

Power supply for Speaker-Amp (HVDD) is 2.6V to 5.25V.

| Speaker Type | Dynamic Speaker | Piezo (Ceramic) Speaker |
|---|---|---|
| Load Resistance (min) | 8Ω | 50Ω |
| Load Capacitance (max) | 30pF | 3μF |

Note 23. Load impedance is total impedance of series resistance (Rseries) and piezo speaker impedance at 1kHz in Figure 61. Load capacitance is capacitance of piezo speaker. When piezo speaker is used, 10Ω or more series resistors should be connected at both SPP and SPN pins, respectively.

Table 56. Speaker Type and Power Supply Range

The DAC or LIN2/RIN2/LIN3/RIN3 signal is input to the Speaker-amp as [(L+R)/2]. The Speaker-amp is mono and BTL output. The gain is set by SPKG1-0 bits. Output level depends on AVDD voltage and SPKG1-0 bits.

| SPKG1-0 bits | Gain | | |
|---|---|---|---|
| | ALC bit = "0" | ALC bit = "1" | |
| 00 | +4.43dB | +6.43dB | Default |
| 01 | +6.43dB | +8.43dB | |
| 10 | +10.65dB | +12.65dB | |
| 11 | +12.65dB | +14.65dB | |

Table 57. SPK-Amp Gain

| AVDD | HVDD | SPKG1-0 bits | SPK-Amp Output (DAC Input = 0dBFS) | |
|---|---|---|---|---|
| | | | ALC bit = "0" | ALC bit = "1" (LMTH1-0 bits = "00") |
| 3.3V | 3.3V | 00 | 3.30Vpp | 3.11Vpp |
| | | 01 | 4.15Vpp (Note 47) | 3.92Vpp |
| | | 10 | 6.75Vpp (Note 47) | 6.37Vpp (Note 47) |
| | | 11 | 8.50Vpp (Note 47) | 8.02Vpp (Note 47) |
| | 5.0V | 00 | 3.30Vpp | 3.11Vpp |
| | | 01 | 4.15Vpp | 3.92Vpp |
| | | 10 | 6.75Vpp (Note 47) | 6.37Vpp (Note 47) |
| | | 11 | 8.50Vpp (Note 47) | 8.02Vpp (Note 47) |

Note 47. The output level is calculated by assuming that output signal is not clipped. In actual case, output signal may be clipped when DAC outputs 0dBFS signal. DAC output level should be set to lower level by setting digital volume so that Speaker-Amp output level is 4.0Vpp (HVDD=3.3V) or 6.0V (HVDD=5V) or less and output signal is not clipped.

Table 58. SPK-Amp Output Level

### <ALC Operation Example of Speaker Playback>

| Register Name | Comment | fs=44.1kHz | |
|---|---|---|---|
| | | Data | Operation |
| LMTH1-0 | Limiter detection Level | 00 | –2.5dBFS |
| ZELMN | Limiter zero crossing detection | 0 | Enable |
| ZTM1-0 | Zero crossing timeout period | 10 | 11.6ms |
| WTM2-0 | Recovery waiting period<br>*WTM2-0 bits should be the same or longer data as ZTM1-0 bits | 11 | 23.2ms |
| REF7-0 | Maximum gain at recovery operation | C1H | +18dB |
| IVL7-0,<br>IVR7-0 | Gain of IVOL | 91H | 0dB |
| LMAT1-0 | Limiter ATT step | 00 | 1 step |
| RGAIN1-0 | Recovery GAIN step | 00 | 1 step |
| ALC | ALC enable | 1 | Enable |

Table 59. ALC Operation Example of Speaker Playback

### <Caution for using Piezo Speaker>

When a piezo speaker is used, resistances more than 10Ω should be inserted between SPP/SPN pins and speaker in series, respectively, as shown in Figure 61. Zener diodes should be inserted between speaker and GND as shown in Figure 61, in order to protect SPK-Amp of AK4643 from the power that the piezo speaker outputs when the speaker is pressured. Zener diodes of the following zener voltage should be used.

0.92 x HVDD ≤ Zener voltage of zener diodo (ZD in Figure 61) ≤ HVDD+0.3V
Ex) In case of HVDD = 5.0V: 4.6V ≤ ZD ≤ 5.3V
For example, zener diode which zener voltage is 5.1V(Min: 4.97V, Max: 5.24V) can be used.

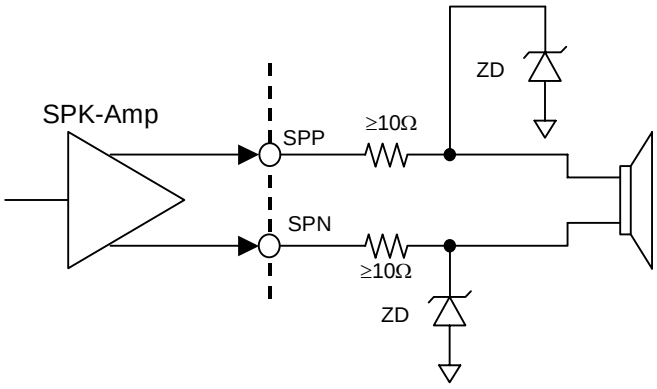



Figure 61. Speaker Output Circuit (Load Capacitance > 30pF)

### <Speaker-Amp Control Sequence>

Speaker-Amp is powered-up/down by PMSPK bit. When PMSPK bit is "0", both SPP and SPN pin are in Hi-Z state. When PMSPK bit is "1" and SPPSN bit is "0", the Speaker-Amp enters power-save mode. In this mode, SPP pin is placed in Hi-Z state and SPN pin goes to HVDD/2 voltage. Power-save mode can reduce the pop noise at power-up and power-down.

| PMSPK | SPPSN | Mode | SPP | SPN | |
|---|---|---|---|---|---|
| 0 | x | Power-down | Hi-Z | Hi-Z | Default |
| 1 | 0 | Power-save | Hi-Z | HVDD/2 | |
| | 1 | Normal Operation | Normal Operation | Normal Operation | |

Table 60. Speaker-Amp Mode Setting (x: Don't care)

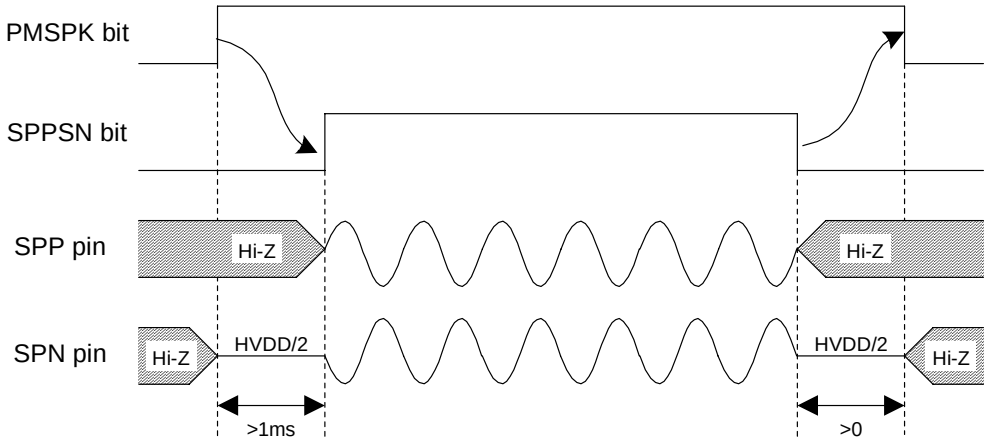



Figure 62. Power-up/Power-down Timing for Speaker-Amp

### <Analog Mixing Circuit for Speaker Output>

When AIN3 bit = “0”, DACS, MINS, LINS2 and RINS2 bits controls each path switch.
MIN path mixing gain is +4.43dB(typ)@SPKG bits = “00” & ALC bit = “0” when the external input resistance is 20kΩ.
LIN2, RIN2 and DAC pathes mixing gain is –1.59dB(typ)@SPKG bits = “00” & ALC bit = “0”.

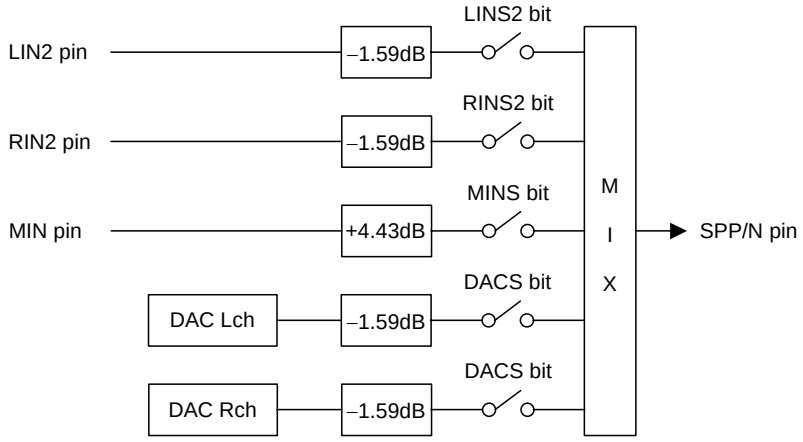



Figure 63. Speaker Mixing Circuit (AIN3 bit = “0”, SPKG1-0 bits = “00”, ALC bit = “0”)

When AIN3 bit = “1”, DACS, LINS2, RINS2, LINS3, RINS3, MICL3 and MICR3 bits controls each path switch. All pathes mixing gain is 0dB(typ)@HPG bit = “0”.

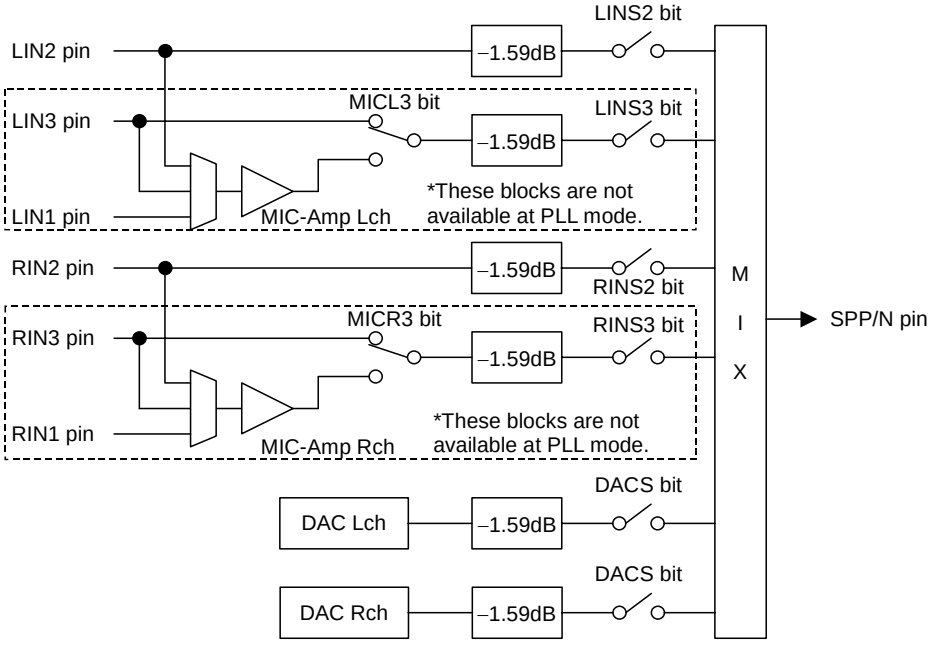
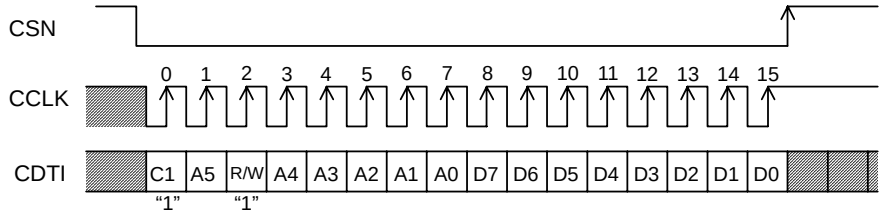



Figure 64. Speaker Mixing Circuit (AIN3 bit = “1”, SPKG bits = “00”, ALC bit = “0”)

## ■ Serial Control Interface

(1) 3-wire Serial Control Mode (I2C pin = “L”)

Internal registers may be written by using the 3-wire µP interface pins (CSN, CCLK and CDTI). The data on this interface consists of a 1-bit Chip address (Fixed to “1”), Read/Write (Fixed to “1”), Register address (MSB first, 6bits) and Control data (MSB first, 8bits). Each bit is clocked in on the rising edge (“↑”) of CCLK. Address and data are latched on the 16th CCLK rising edge (“↑”) after CSN falling edge(“↓”). Clock speed of CCLK is 5MHz (max). The value of internal registers are initialized by PDN pin = “L”.




C1: Chip Address; Fixed to “1”
R/W: READ/WRITE (“1”: WRITE, “0”: READ); Fixed to “1”
A5-A0: Register Address
D7-D0: Control data

Figure 65. Serial Control I/F Timing

(2) I²C-bus Control Mode (I2C pin = "H")

The AK4643 supports the fast-mode I²C-bus (max: 400kHz). Pull-up resistors at SDA and SCL pins should be connected to (DVDD+0.3)V or less voltage.

(2)-1. WRITE Operations

Figure 66 shows the data transfer sequence for the I²C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 72). After the START condition, a slave address is sent. This address is 7 bits long followed by an eighth bit that is a data direction bit (R/W). The most significant six bits of the slave address are fixed as "001001". The next bit is CAD0 (device address bit). This bit identifies the specific device on the bus. The hard-wired input pin (CAD0 pin) sets these device address bits (Figure 67). If the slave address matches that of the AK4643, the AK4643 generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 73). A R/W bit value of "1" indicates that the read operation is to be executed. A "0" indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK4643. The format is MSB first, and those most significant 2-bits are fixed to zeros (Figure 68). The data after the second byte contains control data. The format is MSB first, 8bits (Figure 69). The AK4643 generates an acknowledge after each byte has been received. A data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 72).

The AK4643 can perform more than one byte write operation per sequence. After receipt of the third byte the AK4643 generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal 6-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 24H prior to generating a stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW (Figure 74) except for the START and STOP conditions.

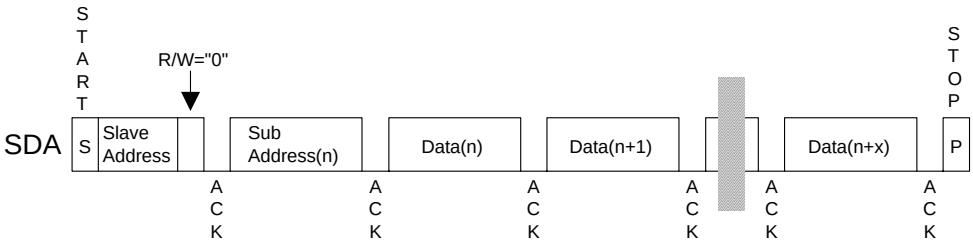



Figure 66. Data Transfer Sequence at the I²C-Bus Mode

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | 1 | CAD0 | R/W |

(Those CAD1/0 should match with CAD1/0 pins)

Figure 67. The First Byte

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | 0 | A5 | A4 | A3 | A2 | A1 | A0 |

Figure 68. The Second Byte

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Figure 69. Byte Structure after the second byte

(2)-2. READ Operations

Set the R/W bit = “1” for the READ operation of the AK4643. After transmission of data, the master can read the next address’s data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet the internal 6-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 24H prior to generating a stop condition, the address counter will “roll over” to 00H and the data of 00H will be read out.

The AK4643 supports two basic read operations: CURRENT ADDRESS READ and RANDOM ADDRESS READ.

(2)-2-1. CURRENT ADDRESS READ

The AK4643 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) were to address n, the next CURRENT READ operation would access data from the address n+1. After receipt of the slave address with R/W bit set to “1”, the AK4643 generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but instead generates a stop condition, the AK4643 ceases transmission.

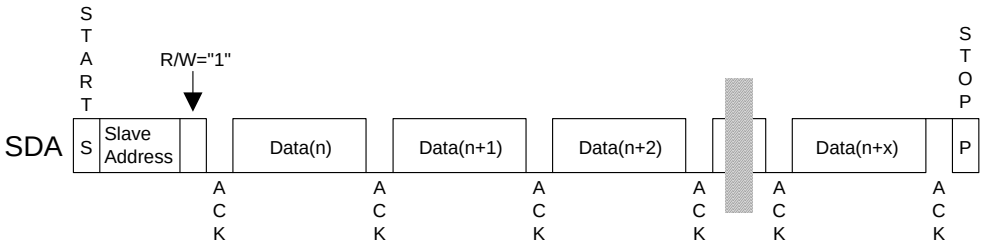



Figure 70. CURRENT ADDRESS READ

(2)-2-2. RANDOM ADDRESS READ

The random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit set to “1”, the master must first perform a “dummy” write operation. The master issues a start request, a slave address (R/W bit = “0”) and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit set to “1”. The AK4643 then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but instead generates a stop condition, the AK4643 ceases transmission.

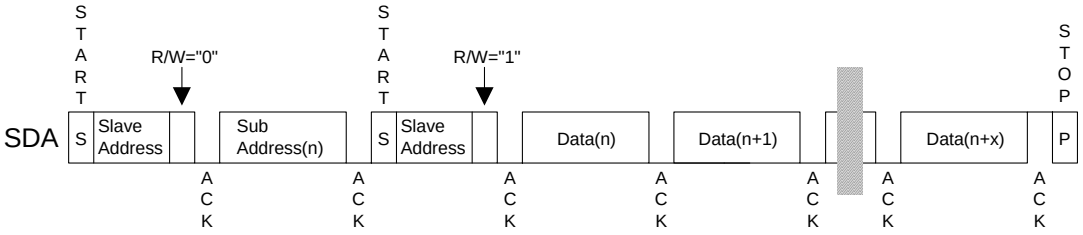



Figure 71. RANDOM ADDRESS READ

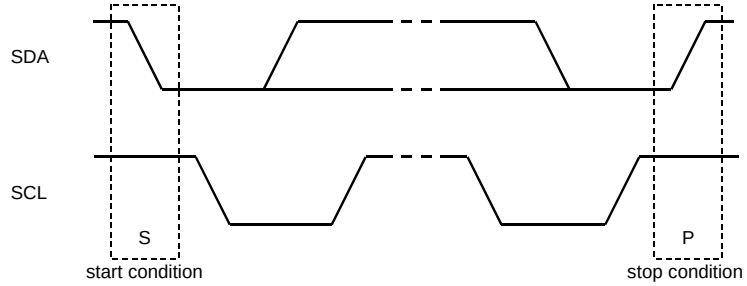



Figure 72. START and STOP Conditions

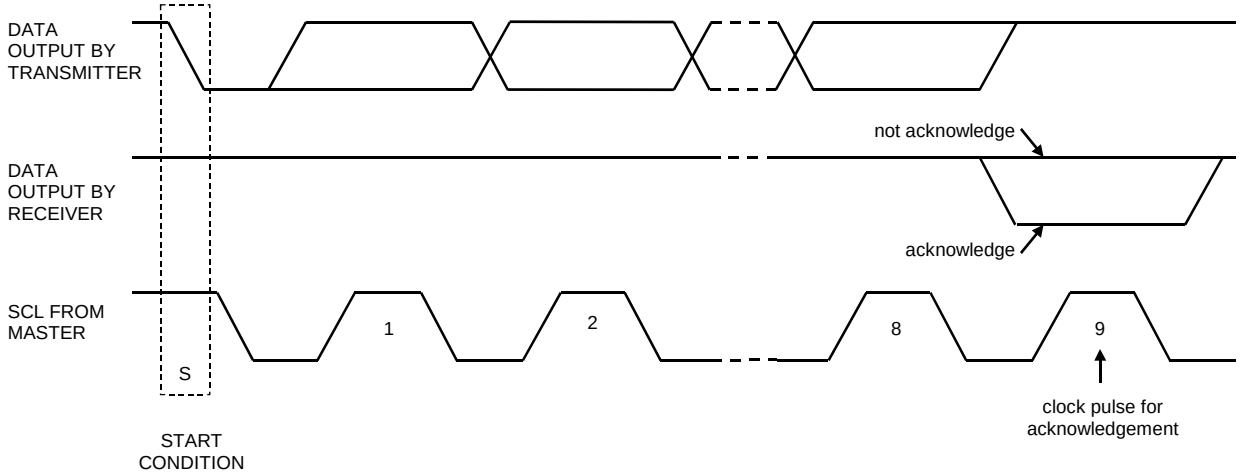



Figure 73. Acknowledge on the $I^2C$-Bus

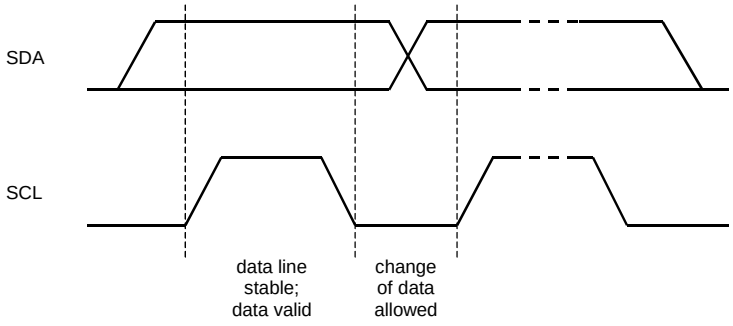



Figure 74. Bit Transfer on the $I^2C$-Bus

## ■ Register Map

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 00H | Power Management 1 | 0 | PMVCM | PMMIN | PMSPK | PMLO | PMDAC | 0 | PMADL |
| 01H | Power Management 2 | 0 | HPMTN | PMHPL | PMHPR | M/S | 0 | MCKO | PMPLL |
| 02H | Signal Select 1 | SPPSN | MINS | DACS | DACL | 0 | PMMP | 0 | MGAIN0 |
| 03H | Signal Select 2 | LOVL | LOPS | MGAIN1 | SPKG1 | SPKG0 | MINL | 0 | 0 |
| 04H | Mode Control 1 | PLL3 | PLL2 | PLL1 | PLL0 | BCKO | 0 | DIF1 | DIF0 |
| 05H | Mode Control 2 | PS1 | PS0 | FS3 | MSBS | BCKP | FS2 | FS1 | FS0 |
| 06H | Timer Select | DVTM | WTM2 | ZTM1 | ZTM0 | WTM1 | WTM0 | RFST1 | RFST0 |
| 07H | ALC Mode Control 1 | 0 | 0 | ALC | ZELMN | LMAT1 | LMAT0 | RGAIN0 | LMTH0 |
| 08H | ALC Mode Control 2 | REF7 | REF6 | REF5 | REF4 | REF3 | REF2 | REF1 | REF0 |
| 09H | Lch Input Volume Control | IVL7 | IVL6 | IVL5 | IVL4 | IVL3 | IVL2 | IVL1 | IVL0 |
| 0AH | Lch Digital Volume Control | DVL7 | DVL6 | DVL5 | DVL4 | DVL3 | DVL2 | DVL1 | DVL0 |
| 0BH | ALC Mode Control 3 | RGAIN1 | LMTH1 | 0 | 0 | 0 | 0 | VBAT | 0 |
| 0CH | Rch Input Volume Control | IVR7 | IVR6 | IVR5 | IVR4 | IVR3 | IVR2 | IVR1 | IVR0 |
| 0DH | Rch Digital Volume Control | DVR7 | DVR6 | DVR5 | DVR4 | DVR3 | DVR2 | DVR1 | DVR0 |
| 0EH | Mode Control 3 | 0 | LOOP | SMUTE | DVOLC | BST1 | BST0 | DEM1 | DEM0 |
| 0FH | Mode Control 4 | 0 | 0 | 0 | 0 | IVOLC | HPM | MINH | DACH |
| 10H | Power Management 3 | INR1 | INL1 | HPG | MDIF2 | MDIF1 | INR0 | INL0 | PMADR |
| 11H | Digital Filter Select | GN1 | GN0 | 0 | FIL1 | EQ | FIL3 | 0 | 0 |
| 12H | FIL3 Co-efficient 0 | F3A7 | F3A6 | F3A5 | F3A4 | F3A3 | F3A2 | F3A1 | F3A0 |
| 13H | FIL3 Co-efficient 1 | F3AS | 0 | F3A13 | F3A12 | F3A11 | F3A10 | F3A9 | F3A8 |
| 14H | FIL3 Co-efficient 2 | F3B7 | F3B6 | F3B5 | F3B4 | F3B3 | F3B2 | F3B1 | F3B0 |
| 15H | FIL3 Co-efficient 3 | 0 | 0 | F3B13 | F3B12 | F3B11 | F3B10 | F3B9 | F3B8 |
| 16H | EQ Co-efficient 0 | EQA7 | EQA6 | EQA5 | EQA4 | EQA3 | EQA2 | EQA1 | EQA0 |
| 17H | EQ Co-efficient 1 | EQA15 | EQA14 | EQA13 | EQA12 | EQA11 | EQA10 | EQA9 | EQA8 |
| 18H | EQ Co-efficient 2 | EQB7 | EQB6 | EQB5 | EQB4 | EQB3 | EQB2 | EQB1 | EQB0 |
| 19H | EQ Co-efficient 3 | 0 | 0 | EQB13 | EQB12 | EQB11 | EQB10 | EQB9 | EQB8 |
| 1AH | EQ Co-efficient 4 | EQC7 | EQC6 | EQC5 | EQC4 | EQC3 | EQC2 | EQC1 | EQC0 |
| 1BH | EQ Co-efficient 5 | EQC15 | EQC14 | EQC13 | EQC12 | EQC11 | EQC10 | EQC9 | EQC8 |
| 1CH | FIL1 Co-efficient 0 | F1A7 | F1A6 | F1A5 | F1A4 | F1A3 | F1A2 | F1A1 | F1A0 |
| 1DH | FIL1 Co-efficient 1 | F1AS | 0 | F1A13 | F1A12 | F1A11 | F1A10 | F1A9 | F1A8 |
| 1EH | FIL1 Co-efficient 2 | F1B7 | F1B6 | F1B5 | F1B4 | F1B3 | F1B2 | F1B1 | F1B0 |
| 1FH | FIL1 Co-efficient 3 | 0 | 0 | F1B13 | F1B12 | F1B11 | F1B10 | F1B9 | F1B8 |
| 20H | Power Management 4 | 0 | 0 | PMAINR3 | PMAINL3 | PMAINR2 | PMAINL2 | PMMICR | PMMICL |
| 21H | Mode Control 5 | 0 | 0 | MICR3 | MICL3 | 0 | MIX | AIN3 | RCV |
| 22H | Lineout Mixing Select | 0 | 0 | 0 | 0 | RINR3 | LINL3 | RINR2 | LINL2 |
| 23H | HP Mixing Select | 0 | 0 | 0 | 0 | RINH3 | LINH3 | RINH2 | LINH2 |
| 24H | SPK Mixing Select | 0 | 0 | 0 | 0 | RINS3 | LINS3 | RINS2 | LINS2 |

Note 48. PDN pin = “L” resets the registers to their default values.
Note 49. Unused bits must contain a “0” value.

## ■ Register Definitions

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 00H | Power Management 1 | 0 | PMVCM | PMMIN | PMSPK | PMLO | PMDAC | 0 | PMADL |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PMADL: MIC-Amp Lch and ADC Lch Power Management
0: Power-down (Default)
1: Power-up
When the PMADL or PMADR bit is changed from "0" to "1", the initialization cycle (1059/fs=24ms @44.1kHz) starts. After initializing, digital data of the ADC is output.

PMDAC: DAC Power Management
0: Power-down (Default)
1: Power-up

PMLO: Stereo Line Out Power Management
0: Power-down (Default)
1: Power-up

PMSPK: Speaker-Amp Power Management
0: Power-down (Default)
1: Power-up

PMMIN: MIN Input Power Management
0: Power-down (Default)
1: Power-up
PMMIN or PMAINL3 bit should be set to "1" for playback.

PMVCM: VCOM Power Management
0: Power-down (Default)
1: Power-up
When any blocks are powered-up, the PMVCM bit must be set to "1". PMVCM bit can be set to "0" only when all power management bits of 00H, 01H, 02H, 10H, 20H and MCKO bits are "0".

Each block can be powered-down respectively by writing "0" in each bit of this address. When the PDN pin is "L", all blocks are powered-down regardless as setting of this address. In this case, register is initialized to the default value.

When all power management bits are "0" in the 00H, 01H, 02H, 10H and 20H addresses and MCKO bit is "0", all blocks are powered-down. The register values remain unchanged.

When neither ADC nor DAC are used, external clocks may not be present. When ADC or DAC is used, external clocks must always be present.

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 01H | Power Management 2 | 0 | HPMTN | PMHPL | PMHPR | M/S | 0 | MCKO | PMPLL |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PMPLL: PLL Power Management
0: EXT Mode and Power-Down (Default)
1: PLL Mode and Power-up

MCKO: Master Clock Output Enable
0: Disable: MCKO pin = “L” (Default)
1: Enable: Output frequency is selected by PS1-0 bits.

M/S: Master / Slave Mode Select
0: Slave Mode (Default)
1: Master Mode

PMHPR: Headphone-Amp Rch Power Management
0: Power-down (Default)
1: Power-up

PMHPL: Headphone-Amp Lch Power Management
0: Power-down (Default)
1: Power-up

HPMTN: Headphone-Amp Mute Control
0: Mute (Default)
1: Normal operation

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 02H | Signal Select 1 | SPPSN | MINS | DACS | DACL | 0 | PMMP | 0 | MGAIN0 |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

MGAIN1-0: MIC-Amp Gain Control (See Table 23)
MGAIN1 bit is D5 bit of 03H.

PMMP: MPWR pin Power Management
0: Power-down: Hi-Z (Default)
1: Power-up

DACL: Switch Control from DAC to Stereo Line Output or Receiver Output
0: OFF (Default)
1: ON
When PMLO bit is “1”, DACL bit is enabled. When PMLO bit is “0”, the LOUT/ROUT pins go to AVSS.

DACS: Switch Control from DAC to Speaker-Amp
0: OFF (Default)
1: ON
When DACS bit is “1”, DAC output signal is input to Speaker-Amp.

MINS: Switch Control from MIN pin to Speaker-Amp
0: OFF (Default)
1: ON
When MINS bit is “1”, mono signal is input to Speaker-Amp.

SPPSN: Speaker-Amp Power-Save Mode
0: Power-Save Mode (Default)
1: Normal Operation
When SPPSN bit is “0”, Speaker-Amp is in power-save mode. In this mode, SPP pin goes to Hi-Z and SPN pin is outputs HVDD/2 voltage. When PMSPK bit = “1”, SPPSN bit is enabled.

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 03H | Signal Select 2 | LOVL | LOPS | MGAIN1 | SPKG1 | SPKG0 | MINL | 0 | 0 |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

MINL: Switch Control from MIN pin to Stereo Line Output or Receiver Output
0: OFF (Default)
1: ON
When PMLO bit is "1", MINL bit is enabled. When PMLO bit is "0", the LOUT/ROUT pins go to AVSS.

SPKG1-0: Speaker-Amp Output Gain Select (See Table 57)

MGAIN1: MIC-Amp Gain Control (See Table 23)

LOPS: Stereo Line Output Power-Save Mode
0: Normal Operation (Default)
1: Power-Save Mode

LOVL: Stereo Line Output / Receiver Output Gain Select (See Table 50, Table 51)
0: 0dB/+6dB (Default)
1: +2dB/+8dB

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 04H | Mode Control 1 | PLL3 | PLL2 | PLL1 | PLL0 | BCKO | 0 | DIF1 | DIF0 |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

DIF1-0: Audio Interface Format (See Table 17)
Default: "10" (Left jutified)

BCKO: BICK Output Frequency Select at Master Mode (See Table 11)

PLL3-0: PLL Reference Clock Select (See Table 5)
Default: "0000"(LRCK pin)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 05H | Mode Control 2 | PS1 | PS0 | FS3 | MSBS | BCKP | FS2 | FS1 | FS0 |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

FS3-0: Sampling Frequency Select (See Table 6 and Table 7.) and MCKI Frequency Select (See Table 12.)
FS3-0 bits select sampling frequency at PLL mode and MCKI frequency at EXT mode.

BCKP: BICK Polarity at DSP Mode (See Table 18)
"0": SDTO is output by the rising edge ("↑") of BICK and SDTI is latched by the falling edge ("↓"). (Default)
"1": SDTO is output by the falling edge ("↓") of BICK and SDTI is latched by the rising edge ("↑").

MSBS: LRCK Polarity at DSP Mode (See Table 18)
"0": The rising edge ("↑") of LRCK is half clock of BICK before the channel change. (Default)
"1": The rising edge ("↑") of LRCK is one clock of BICK before the channel change.

PS1-0: MCKO Output Frequency Select (See Table 10)
Default: "00"(256fs)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 06H | Timer Select | DVTM | WTM2 | ZTM1 | ZTM0 | WTM1 | WTM0 | RFST1 | RFST0 |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

RFST1-0: ALC First recovery Speed (See Table 34)
Default: "00"(4times)

WTM2-0: ALC Recovery Waiting Period (See Table 31.)
Default: "000" (128/fs)

ZTM1-0: ALC Limiter/Recovery Operation Zero Crossing Timeout Period (See Table 30.)
Default: "00" (128/fs)

DVTM: Digital Volume Transition Time Setting (See Table 40.)
0: 1061/fs (Default)
1: 256/fs
This is the transition time between DVL/R7-0 bits = 00H and FFH.

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 07H | ALC Mode Control 1 | 0 | 0 | ALC | ZELMN | LMAT1 | LMAT0 | RGAIN0 | LMTH0 |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LMTH1-0: ALC Limiter Detection Level / Recovery Counter Reset Level (See Table 28.)
Default: "00"
LMTH1 bit is D6 bit of 0BH.

RGAIN1-0: ALC Recovery GAIN Step (See Table 32.)
Default: "00"
RGAIN1 bit is D7 bit of 0BH.

LMAT1-0: ALC Limiter ATT Step (See Table 29.)
Default: "00"

ZELMN: Zero Crossing Detection Enable at ALC Limiter Operation
0: Enable (Default)
1: Disable

ALC: ALC Enable
0: ALC Disable (Default)
1: ALC Enable

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 08H | ALC Mode Control 2 | REF7 | REF6 | REF5 | REF4 | REF3 | REF2 | REF1 | REF0 |
| Default | | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |

REF7-0: Reference Value at ALC Recovery Operation. 0.375dB step, 242 Level (See Table 33.)
Default: "E1H" (+30.0dB)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 09H | Lch Input Volume Control | IVL7 | IVL6 | IVL5 | IVL4 | IVL3 | IVL2 | IVL1 | IVL0 |
| 0CH | Rch Input Volume Control | IVR7 | IVR6 | IVR5 | IVR4 | IVR3 | IVR2 | IVR1 | IVR0 |
| Default | | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |

IVL7-0, IVR7-0: Input Digital Volume; 0.375dB step, 242 Level (See Table 36.)
Default: "E1H" (+30.0dB)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0AH | Lch Digital Volume Control | DVL7 | DVL6 | DVL5 | DVL4 | DVL3 | DVL2 | DVL1 | DVL0 |
| 0DH | Rch Digital Volume Control | DVR7 | DVR6 | DVR5 | DVR4 | DVR3 | DVR2 | DVR1 | DVR0 |
| Default | | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |

DVL7-0, DVR7-0: Output Digital Volume (See Table 39.)
Default: "18H" (0dB)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0BH | ALC Mode Control 3 | RGAIN1 | LMTH1 | 0 | 0 | 0 | 0 | VBAT | 0 |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

VBAT: HP-Amp Common Voltage (See Table 55.)
0: 0.5 x HVDD (Default)
1: 0.64 x AVDD

LMTH1: ALC Limiter Detection Level / Recovery Counter Reset Level (See Table 28.)

RGAIN1: ALC Recovery GAIN Step (See Table 32.)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0EH | Mode Control 3 | 0 | LOOP | SMUTE | DVOLC | BST1 | BST0 | DEM1 | DEM0 |
| Default | | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |

DEM1-0: De-emphasis Frequency Select (See Table 37)
Default: "01" (OFF)

BST1-0: Bass Boost Function Select (See Table 38)
Default: "00" (OFF)

DVOLC: Output Digital Volume Control Mode Select
0: Independent
1: Dependent (Default)
When DVOLC bit = "1", DVL7-0 bits control both Lch and Rch volume level, while register values of DVL7-0 bits are not written to DVR7-0 bits. When DVOLC bit = "0", DVL7-0 bits control Lch level and DVR7-0 bits control Rch level, respectively.

SMUTE: Soft Mute Control
0: Normal Operation (Default)
1: DAC outputs soft-muted

LOOP: Digital Loopback Mode
0: SDTI → DAC (Default)
1: SDTO → DAC

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0FH | Mode Control 4 | 0 | 0 | 0 | 0 | IVOLC | HPM | MINH | DACH |
| Default | | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

DACH: Switch Control from DAC to Headphone-Amp
0: OFF (Default)
1: ON

MINH: Switch Control from MIN pin to Headphone-Amp
0: OFF (Default)
1: ON

HPM: Headphone-Amp Mono Output Select
0: Stereo (Default)
1: Mono
When the HPM bit = "1", DAC output signal is output to Lch and Rch of the Headphone-Amp as (L+R)/2.

IVOLC: Input Digital Volume Control Mode Select
0: Independent
1: Dependent (Default)
When IVOLC bit = "1", IVL7-0 bits control both Lch and Rch volume level, while register values of IVL7-0 bits are not written to IVR7-0 bits. When IVOLC bit = "0", IVL7-0 bits control Lch level and IVR7-0 bits control Rch level, respectively.

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 10H | Power Management 3 | INR1 | INL1 | HPG | MDIF2 | MDIF1 | INR0 | INL0 | PMADR |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PMADR: MIC-Amp Lch and ADC Rch Power Management
0: Power-down (Default)
1: Power-up

INL1-0: ADC Lch Input Source Select
Default: 00 (LIN1 pin)

INR1-0: ADC Rch Input Source Select
Default: 00 (RIN1 pin)

MDIF1: Single-ended / Full-differential Input Select 1
0: Single-ended input (LIN1/RIN1 pins: Default)
1: Full-differential input (IN1+/IN1– pins)
MDIF1 bit selects the input type of pins #32 and #31.

MDIF2: Single-ended / Full-differential Input Select 2
0: Single-ended input (LIN2/RIN2 pins: Default)
1: Full-differential input (IN2+/IN2– pins)
MDIF2 bit selects the input type of pins #30 and #29.

HPG: Headphone-Amp Gain Select (See Table 53.)
0: 0dB (Default)
1: +3.6dB

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 11H | Digital Filter Select | GN1 | GN0 | 0 | FIL1 | EQ | FIL3 | 0 | 0 |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

GN1-0: Gain Select at GAIN block (See Table 26.)
Default: "00"

FIL3: FIL3 (Stereo Separation Emphasis Filter) Coefficient Setting Enable
0: Disable (Default)
1: Enable
When FIL3 bit is "1", the settings of F3A13-0 and F3B13-0 bits are enabled. When FIL3 bit is "0", FIL3 block is OFF (MUTE).

EQ: EQ (Gain Compensation Filter) Coefficient Setting Enable
0: Disable (Default)
1: Enable
When EQ bit is "1", the settings of EQA15-0, EQB13-0 and EQC15-0 bits are enabled. When EQ bit is "0", EQ block is through (0dB).

FIL1: FIL1 (Wind-noise Reduction Filter) Coefficient Setting Enable
0: Disable (Default)
1: Enable
When FIL1 bit is "1", the settings of F1A13-0 and F1B13-0 bits are enabled. When FIL1 bit is "0", FIL1 block is through (0dB).

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 12H | FIL3 Co-efficient 0 | F3A7 | F3A6 | F3A5 | F3A4 | F3A3 | F3A2 | F3A1 | F3A0 |
| 13H | FIL3 Co-efficient 1 | F3AS | 0 | F3A13 | F3A12 | F3A11 | F3A10 | F3A9 | F3A8 |
| 14H | FIL3 Co-efficient 2 | F3B7 | F3B6 | F3B5 | F3B4 | F3B3 | F3B2 | F3B1 | F3B0 |
| 15H | FIL3 Co-efficient 3 | 0 | 0 | F3B13 | F3B12 | F3B11 | F3B10 | F3B9 | F3B8 |
| 16H | EQ Co-efficient 0 | EQA7 | EQA6 | EQA5 | EQA4 | EQA3 | EQA2 | EQA1 | EQA0 |
| 17H | EQ Co-efficient 1 | EQA15 | EQA14 | EQA13 | EQA12 | EQA11 | EQA10 | EQA9 | EQA8 |
| 18H | EQ Co-efficient 2 | EQB7 | EQB6 | EQB5 | EQB4 | EQB3 | EQB2 | EQB1 | EQB0 |
| 19H | EQ Co-efficient 3 | 0 | 0 | EQB13 | EQB12 | EQB11 | EQB10 | EQB9 | EQB8 |
| 1AH | EQ Co-efficient 4 | EQC7 | EQC6 | EQC5 | EQC4 | EQC3 | EQC2 | EQC1 | EQC0 |
| 1BH | EQ Co-efficient 5 | EQC15 | EQC14 | EQC13 | EQC12 | EQC11 | EQC10 | EQC9 | EQC8 |
| 1CH | FIL1 Co-efficient 0 | F1A7 | F1A6 | F1A5 | F1A4 | F1A3 | F1A2 | F1A1 | F1A0 |
| 1DH | FIL1 Co-efficient 1 | F1AS | 0 | F1A13 | F1A12 | F1A11 | F1A10 | F1A9 | F1A8 |
| 1EH | FIL1 Co-efficient 2 | F1B7 | F1B6 | F1B5 | F1B4 | F1B3 | F1B2 | F1B1 | F1B0 |
| 1FH | FIL1 Co-efficient 3 | 0 | 0 | F1B13 | F1B12 | F1B11 | F1B10 | F1B9 | F1B8 |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

F3A13-0, F3B13-0: FIL3 (Stereo Separation Emphasis Filter) Coefficient (14bit x 2)
Default: “0000H”

F3AS: FIL3 (Stereo Separation Emphasis Filter) Select
0: HPF (Default)
1: LPF

EQA15-0, EQB13-0, EQC15-C0: EQ (Gain Compensation Filter) Coefficient (14bit x 2 + 16bit x 1)
Default: “0000H”

F1A13-0, F1B13-B0: FIL1 (Wind-noise Reduction Filter) Coefficient (14bit x 2)
Default: “0000H”

F1AS: FIL1 (Wind-noise Reduction Filter) Select
0: HPF (Default)
1: LPF

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 20H | Power Management 4 | 0 | 0 | PMAINR3 | PMAINL3 | PMAINR2 | PMAINL2 | PMMICR | PMMICL |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PMMICL: MIC-Amp Lch Power Management
0: Power down (Default)
1: Power up

PMMICR: MIC-Amp Rch Power Management
0: Power down (Default)
1: Power up

PMAINL2: LIN2 Mixing Circuit Power Management
0: Power down (Default)
1: Power up

PMAINR2: RIN2 Mixing Circuit Power Management
0: Power down (Default)
1: Power up

PMAINL3: LIN3 Mixing Circuit Power Management
0: Power down (Default)
1: Power up
PMMIN or PMAINL3 bit should be set to “1” for playback.

PMAINR3: RIN3 Mixing Circuit Power Management
0: Power down (Default)
1: Power up

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 21H | Mode Control 5 | 0 | 0 | MICR3 | MICL3 | 0 | MIX | AIN3 | RCV |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

RCV: Receiver Select
0: Stereo Line Output (LOUT/ROUT pins) (Default)
1: Mono Receiver Output (RCP/RCN pins)

AIN3: Analog Mixing Select
0: Mono Input (MIN pin) (Default)
1: Stereo Input (LIN3/RIN3 pins): PLL is not available.

MIX: Mono Recording
0: Stereo (Default)
1: Mono: (L+R)/2

MICL3: Switch Control from MIC-Amp Lch to Analog Output
0: LIN3 input signal is selected. (Default)
1: MIC-Amp Lch output signal is selected.

MICR3: Switch Control from MIC-Amp Rch to Analog Output
0: RIN3 input signal is selected. (Default)
1: MIC-Amp Rch output signal is selected.

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 22H | Lineout Mixing Select | 0 | 0 | 0 | 0 | RINR3 | LINL3 | RINR2 | LINL2 |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LINL2: Switch Control from LIN2 pin to Stereo Line Output (without MIC-Amp)
0: OFF (Default)
1: ON

RINR2: Switch Control from RIN2 pin to Stereo Line Output (without MIC-Amp)
0: OFF (Default)
1: ON

LINL3: Switch Control from LIN3 pin (or MIC-Amp Lch) to Stereo Line Output
0: OFF (Default)
1: ON

RINR3: Switch Control from RIN3 pin (or MIC-Amp Rch) to Stereo Line Output
0: OFF (Default)
1: ON

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 23H | HP Mixing Select | 0 | 0 | 0 | 0 | RINH3 | LINH3 | RINH2 | LINH2 |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LINH2: Switch Control from LIN2 pin to Headphone Output (without MIC-Amp)
0: OFF (Default)
1: ON

RINH2: Switch Control from RIN2 pin to Headphone Output (without MIC-Amp)
0: OFF (Default)
1: ON

LINH3: Switch Control from LIN3 pin (or MIC-Amp Lch) to Headphone Output
0: OFF (Default)
1: ON

RINH3: Switch Control from RIN3 pin (or MIC-Amp Rch) to Headphone Output
0: OFF (Default)
1: ON

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 24H | SPK Mixing Select | 0 | 0 | 0 | 0 | RINS3 | LINS3 | RINS2 | LINS2 |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LINS2: Switch Control from LIN2 pin to Speaker Output (without MIC-Amp)
0: OFF (Default)
1: ON

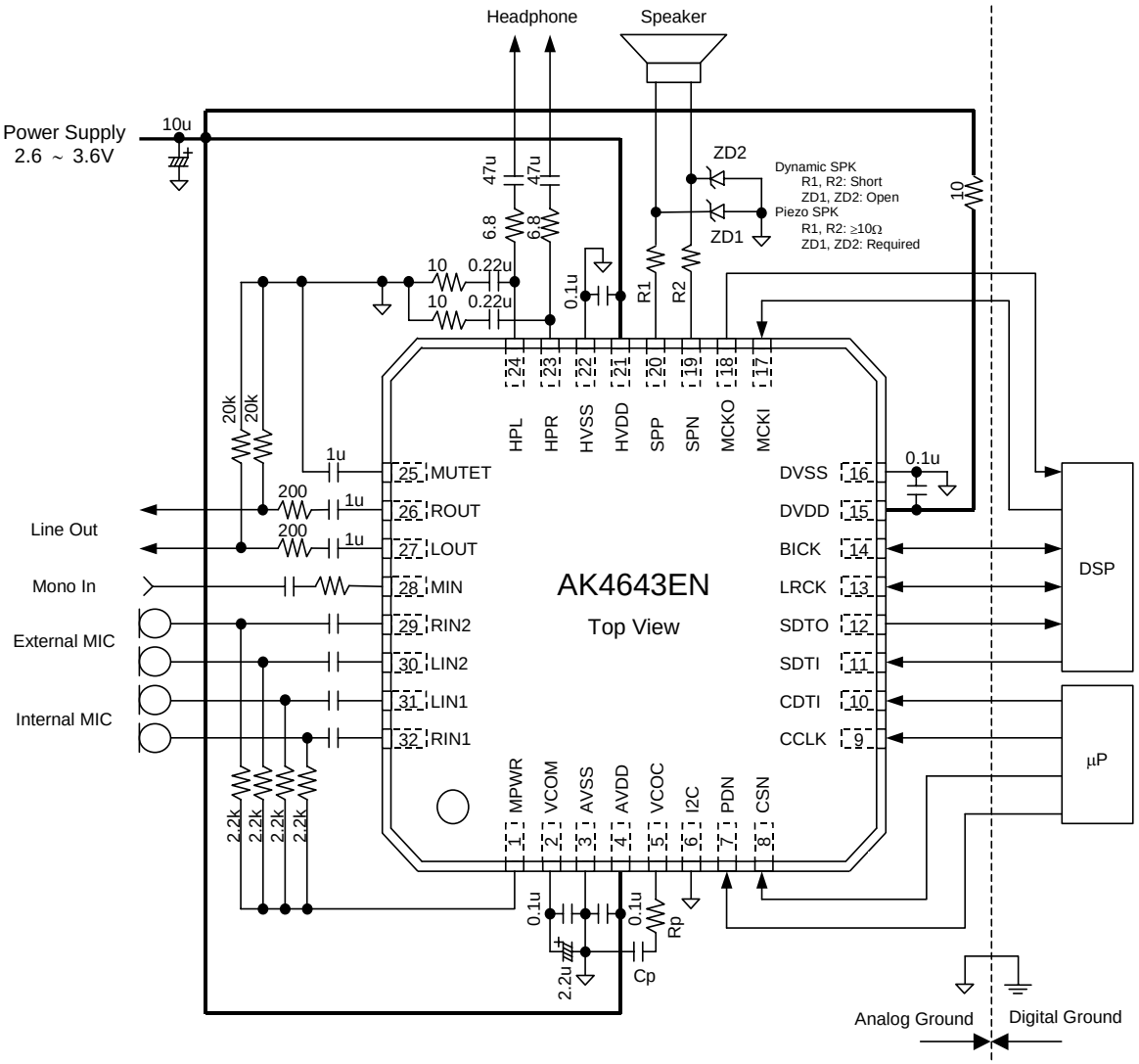
RINS2: Switch Control from RIN2 pin to Speaker Output (without MIC-Amp)
0: OFF (Default)
1: ON

LINS3: Switch Control from LIN3 pin (or MIC-Amp Lch) to Speaker Output
0: OFF (Default)
1: ON

RINS3: Switch Control from RIN3 pin (or MIC-Amp Rch) to Speaker Output
0: OFF (Default)
1: ON

## SYSTEM DESIGN

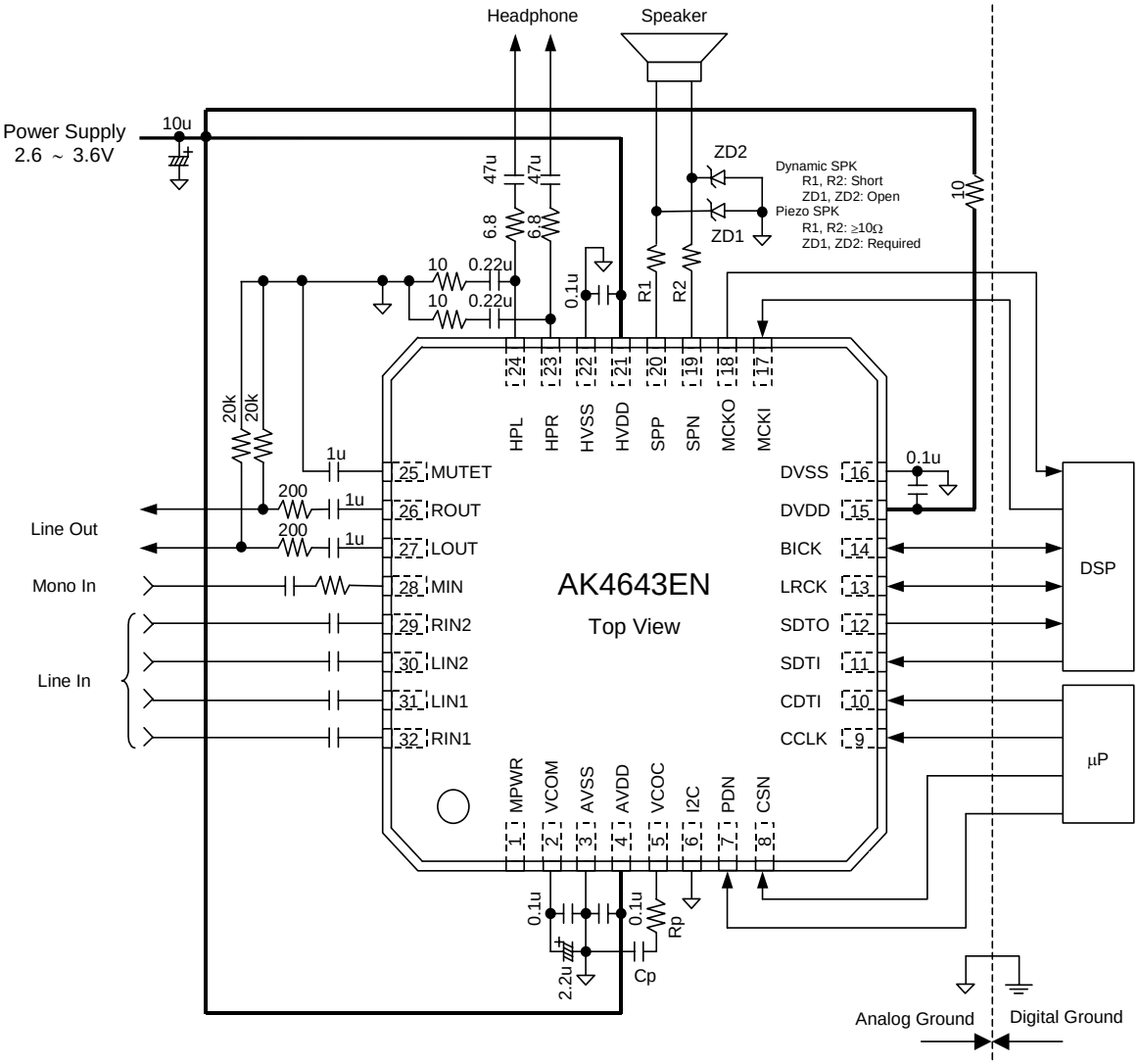
Figure 75, Figure 76 and Figure 77 shows the system connection diagram for the AK4643. An evaluation board [AKD4643] is available which demonstrates the optimum layout, power supply arrangements and measurement results.




Notes:

- AVSS, DVSS and HVSS of the AK4643 should be distributed separately from the ground of external controllers.
- All digital input pins should not be left floating.
- When the AK4643 is EXT mode (PMPLL bit = "0"), a resistor and capacitor of VCOC pin is not needed.
- When the AK4643 is PLL mode (PMPLL bit = "1"), a resistor and capacitor of VCOC pin is shown in Table 5.
- When piezo speaker is used, 2.6 ~ 5.25V power should be supplied to HVDD and 10Ω or more series resistors should be connected to both SPP and SPN pins, respectively.
- When the AK4643 is used at master mode, LRCK and BICK pins are floating before M/S bit is changed to "1". Therefore, 100kΩ around pull-up resistor should be connected to LRCK and BICK pins of the AK4643.

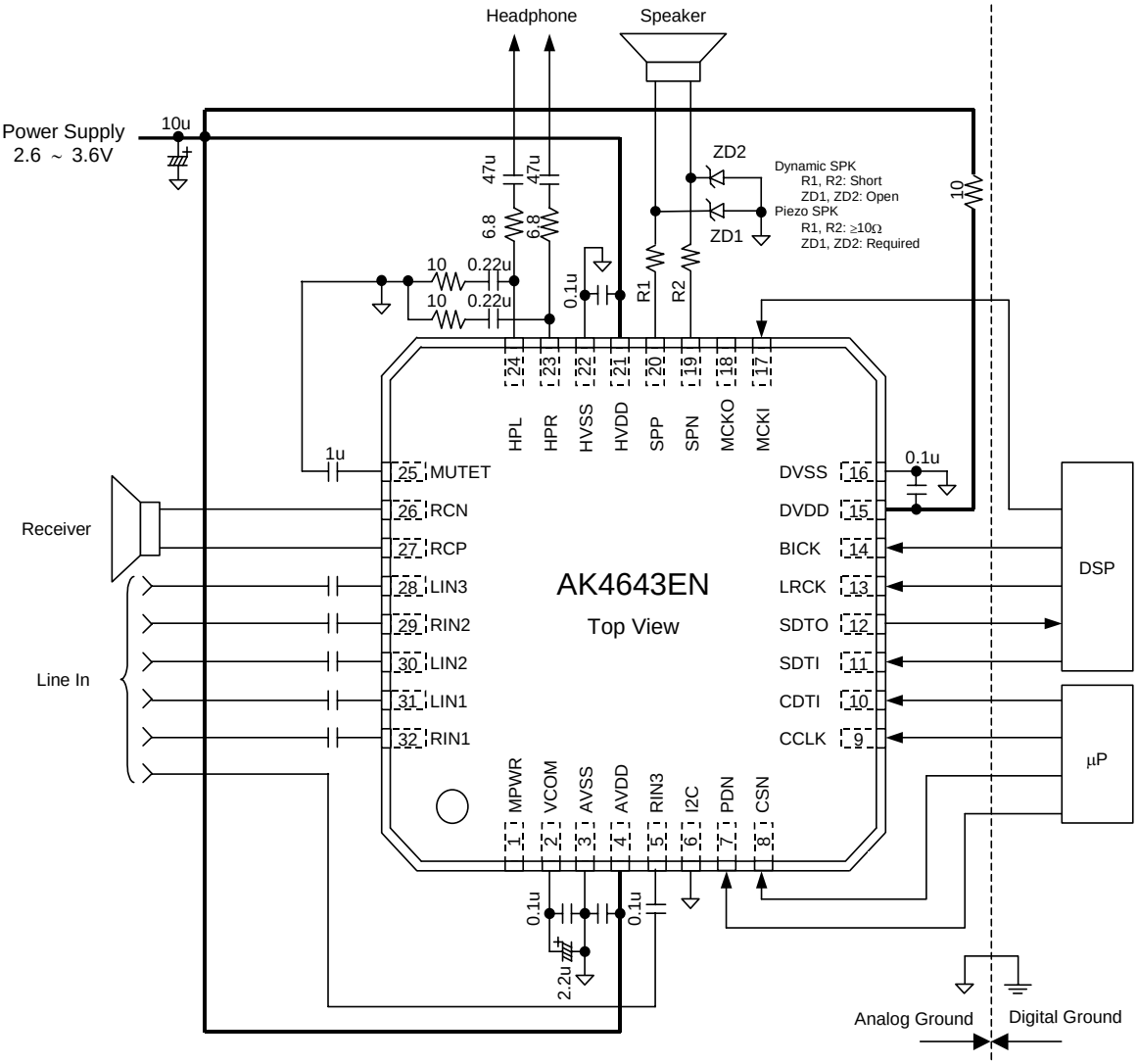
Figure 75. Typical Connection Diagram (AIN3 bit = "0", MIC Input)




Notes:

- AVSS, DVSS and HVSS of the AK4643 should be distributed separately from the ground of external controllers.
- All digital input pins should not be left floating.
- When the AK4643 is EXT mode (PMPLL bit = "0"), a resistor and capacitor of VCOC pin is not needed.
- When the AK4643 is PLL mode (PMPLL bit = "1"), a resistor and capacitor of VCOC pin is shown in Table 5.
- When piezo speaker is used, 2.6 ~ 5.25V power should be supplied to HVDD and 10Ω or more series resistors should be connected to both SPP and SPN pins, respectively.
- When the AK4643 is used at master mode, LRCK and BICK pins are floating before M/S bit is changed to "1". Therefore, 100kΩ around pull-up resistor should be connected to LRCK and BICK pins of the AK4643.

Figure 76. Typical Connection Diagram (AIN3 bit = "0", Line Input)




Notes:

- AVSS, DVSS and HVSS of the AK4643 should be distributed separately from the ground of external controllers.
- All digital input pins should not be left floating.
- When AIN3 bit = "1", PLL is not available.
- When piezo speaker is used, 2.6 ~ 5.25V power should be supplied to HVDD and 10Ω or more series resistors should be connected to both SPP and SPN pins, respectively.

Figure 77. Typical Connection Diagram (AIN3 bit = "1": PLL is not available, RCV bit = "1", Line Input)

## 1. Grounding and Power Supply Decoupling

The AK4643 requires careful attention to power supply and grounding arrangements. AVDD, DVDD and HVDD are usually supplied from the system's analog supply. If AVDD, DVDD and HVDD are supplied separately, the power-up sequence is not critical. AVSS, DVSS and HVSS of the AK4643 should be connected to the analog ground plane. System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4643 as possible, with the small value ceramic capacitor being the nearest.

## 2. Voltage Reference

VCOM is a signal ground of this chip. A 2.2μF electrolytic capacitor in parallel with a 0.1μF ceramic capacitor attached to the VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from the VCOM pin. All signals, especially clocks, should be kept away from the VCOM pin in order to avoid unwanted coupling into the AK4643.

## 3. Analog Inputs

The Mic, Line and MIN inputs are single-ended. The input signal range scales with nominally at 0.06 x AVDD Vpp(typ) @MGAIN1-0 bits = "01", 0.03 x AVDD Vpp(typ) @MGAIN1-0 bits = "10", 0.015 x AVDD Vpp(typ) @MGAIN1-0 bits = "11" or 0.6 x AVDD Vpp(typ) @MGAIN1-0 bits = "00" for the Mic/Line input and 0.6 x AVDD Vpp (typ) for the MIN input, centered around the internal common voltage (0.45 x AVDD). Usually the input signal is AC coupled using a capacitor. The cut-off frequency is fc = (1/2πRC). The AK4643 can accept input voltages from AVSS to AVDD.

## 4. Analog Outputs

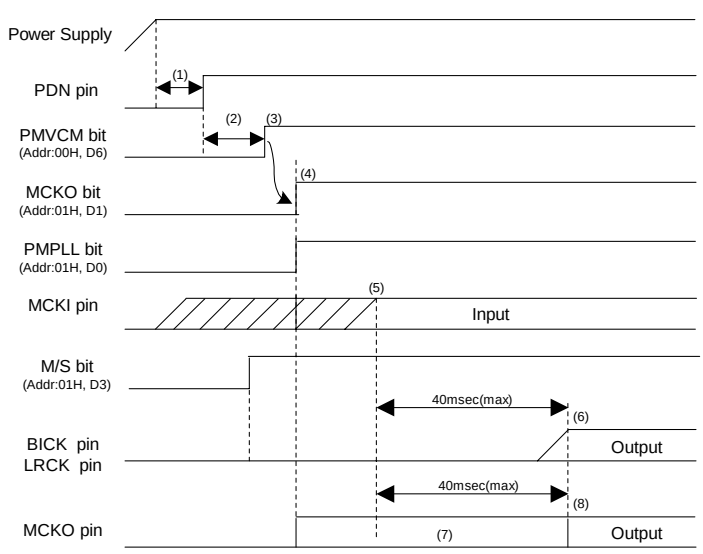
The input data format for the DAC is 2's complement. The output voltage is a positive full scale for 7FFFH(@16bit) and a negative full scale for 8000H(@16bit). Stereo Line Output and Receiver Output are centered at 0.45 x AVDD. The Headphone-Amp and Speaker-Amp outputs are centered at HVDD/2.

## CONTROL SEQUENCE

### ■ Clock Set up

When ADC or DAC is powered-up, the clocks must be supplied.

1. PLL Master Mode.



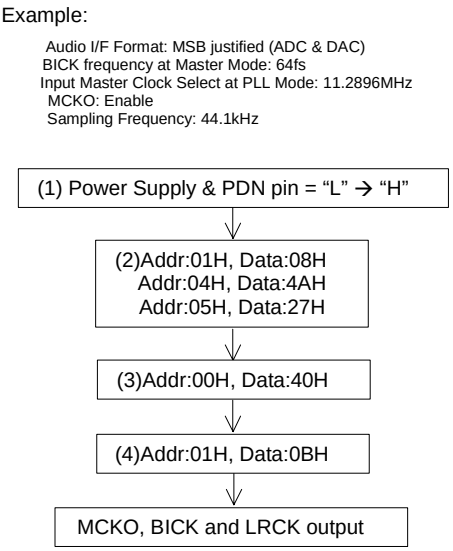




Figure 78. Clock Set Up Sequence (1)

<Example>

(1) After Power Up, PDN pin = "L" → "H"
"L" time of 150ns or more is needed to reset the AK4643.
(2) DIF1-0, PLL3-0, FS3-0, BCKO and M/S bits should be set during this period.
(3) Power UpVCOM: PMVCM bit = "0" → "1"
VCOM should first be powered-up before the other block operates.
(4) In case of using MCKO output: MCKO bit = "1"
In case of not using MCKO output: MCKO bit = "0"
(5) PLL lock time is 40ms(max) after PMPLL bit changes from "0" to "1" and MCKI is supplied from an external source.
(6) The AK4643 starts to output the LRCK and BICK clocks after the PLL becomes stable. Then normal operation starts.
(7) The invalid frequency is output from MCKO pin during this period if MCKO bit = "1".
(8) The normal clock is output from MCKO pin after the PLL is locked if MCKO bit = "1".

2. PLL Slave Mode (LRCK or BICK pin)

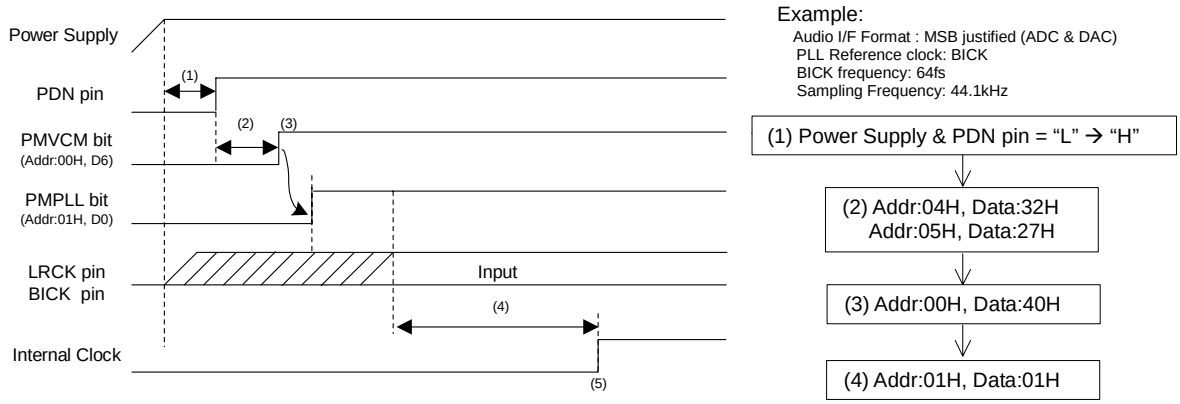



Figure 79. Clock Set Up Sequence (2)

<Example>

(1) After Power Up: PDN pin "L" → "H"
"L" time of 150ns or more is needed to reset the AK4643.

(2) DIF1-0, FS3-0 and PLL3-0 bits should be set during this period.

(3) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM should first be powered up before the other block operates.

(4) PLL starts after the PMPLL bit changes from "0" to "1" and PLL reference clock (LRCK or BICK pin) is supplied. PLL lock time is 160ms(max) when LRCK is a PLL reference clock. And PLL lock time is 2ms(max) when BICK is a PLL reference clock.

(5) Normal operation stats after that the PLL is locked.

3. PLL Slave Mode (MCKI pin)

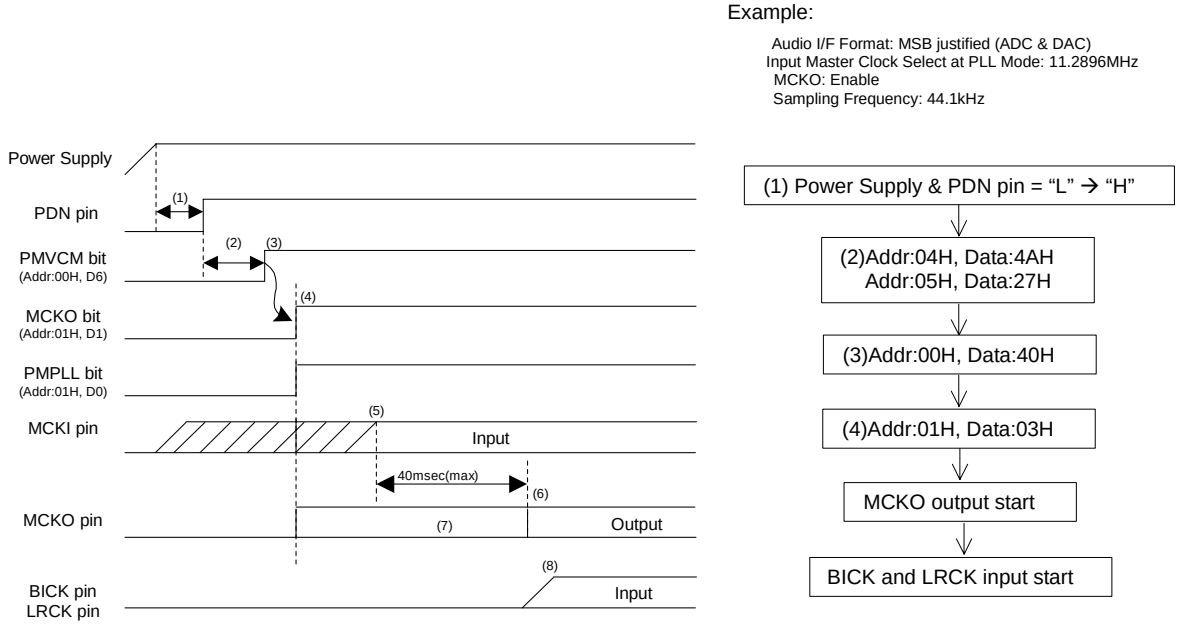



Figure 80. Clock Set Up Sequence (3)

<Example>

(1) After Power Up: PDN pin "L" → "H"
"L" time of 150ns or more is needed to reset the AK4643.
(2) DIF1-0, PLL3-0 and FS3-0 bits should be set during this period.
(3) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM should first be powered up before the other block operates.
(4) Enable MCKO output: MCKO bit = "1"
(5) PLL starts after that the PMPLL bit changes from "0" to "1" and PLL reference clock (MCKI pin) is supplied. PLL lock time is 40ms(max).
(6) The normal clock is output from MCKO after PLL is locked.
(7) The invalid frequency is output from MCKO during this period.
(8) BICK and LRCK clocks should be synchronized with MCKO clock.

4. EXT Slave Mode

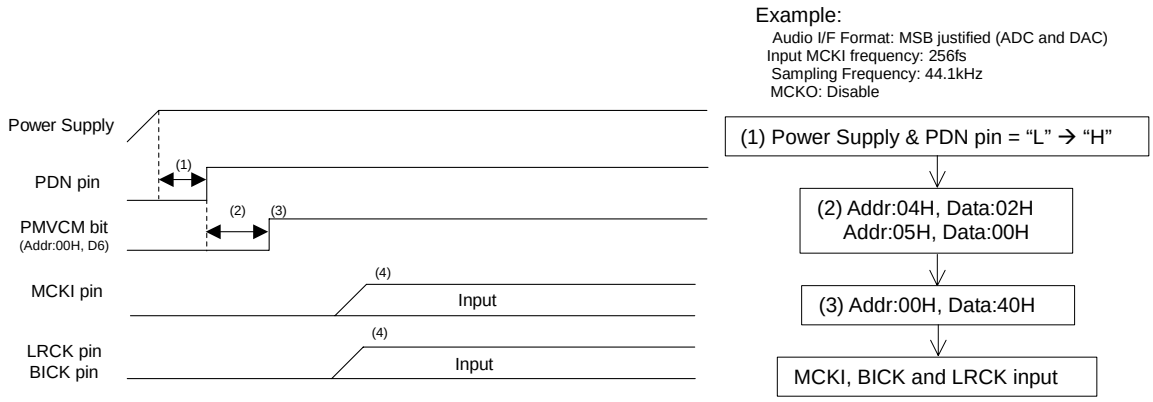



Figure 81. Clock Set Up Sequence (4)

<Example>

(1) After Power Up: PDN pin "L" → "H"
"L" time of 150ns or more is needed to reset the AK4643.
(2) DIF1-0 and FS1-0 bits should be set during this period.
(3) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM should first be powered up before the other block operates.
(4) Normal operation starts after the MCKI, LRCK and BICK are supplied.

5. EXT Master Mode

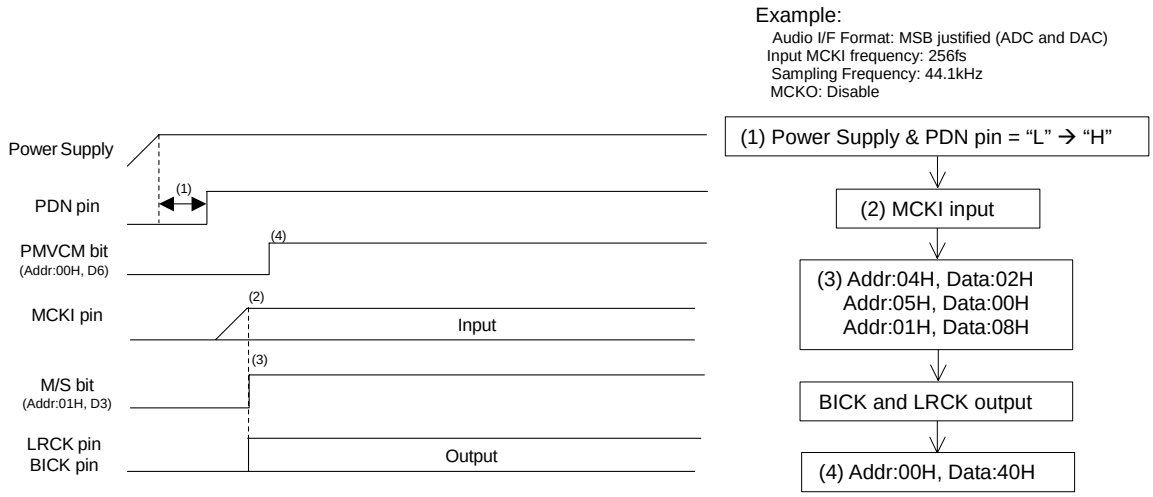



Figure 82. Clock Set Up Sequence (5)

<Example>

(1) After Power Up: PDN pin "L" → "H"
"L" time of 150ns or more is needed to reset the AK4643.
(2) MCKI should be input.
(3) After DIF1-0 and FS1-0 bits are set, M/S bit should be set to "1". Then LRCK and BICK are output.
(4) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM should first be powered up before the other block operates.

## ■ MIC Input Recording (Stereo)

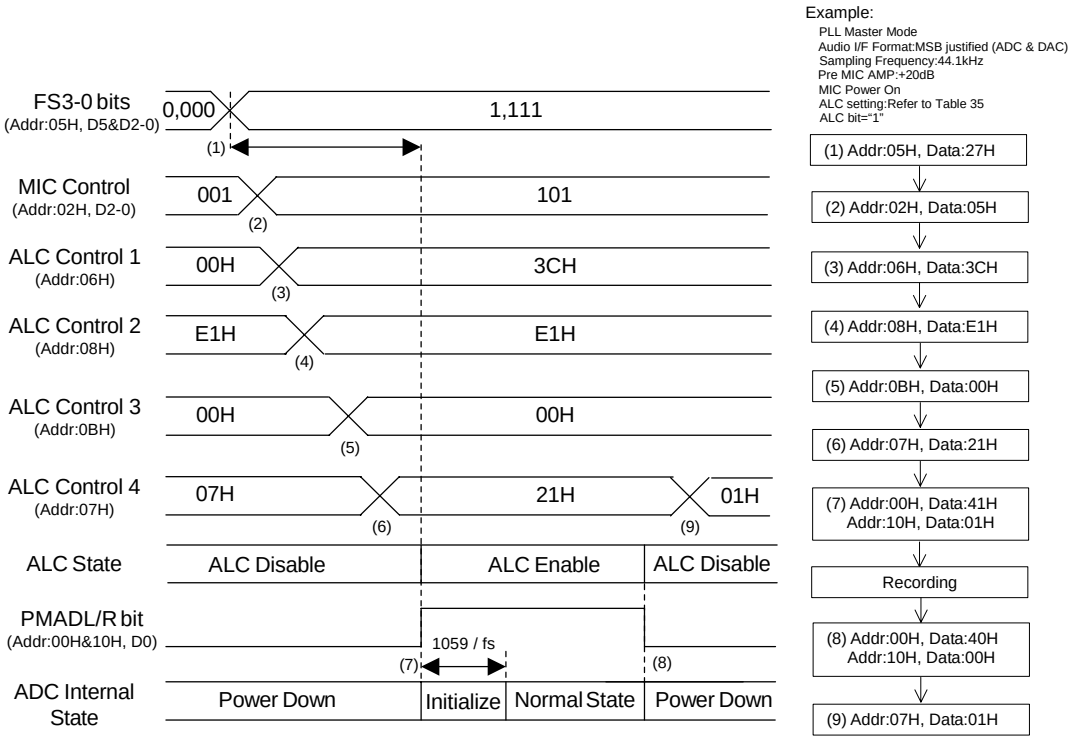



Figure 83. MIC Input Recording Sequence

<Example>

This sequence is an example of ALC setting at fs=44.1kHz. If the parameter of the ALC is changed, please refer to "Figure 36. Registers set-up sequence at ALC operation"

At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Set up a sampling frequency (FS3-0 bit). When the AK4643 is PLL mode, MIC and ADC should be powered-up in consideration of PLL lock time after a sampling frequency is changed.

(2) Set up MIC input (Addr: 02H)

(3) Set up Timer Select for ALC (Addr: 06H)

(4) Set up REF value for ALC (Addr: 08H)

(5) Set up LMTH1 and RGAIN1 bits (Addr: 0BH)

(6) Set up LMTH0, RGAIN0, LMAT1-0 and ALC bits (Addr: 07H)

(7) Power Up MIC and ADC: PMADL = PMADR bits = "0" → "1"

The initialization cycle time of ADC is 1059/fs=24ms@fs=44.1kHz.

After the ALC bit is set to "1" and MIC&ADC block is powered-up, the ALC operation starts from IVOL default value (+30dB).

The time of offset voltage going to "0" after the ADC initialization cycle depends on both the time of analog input pin going to the common voltage and the time constant of the offset cancel digital HPF. This time can be shorter by using the following sequence:

At first, PMVCM and PMMP bits should set to "1". Then, the ADC should be powered-up. The wait time to power-up the ADC should be longer than 4 times of the time constant that is determined by the AC coupling capacitor at analog input pin and the internal input resistance 60k(typ).

(8) Power Down MIC and ADC: PMADL = PMADR bits = "1" → "0"

When the registers for the ALC operation are not changed, ALC bit may be keeping "1". The ALC operation is disabled because the MIC&ADC block is powered-down. If the registers for the ALC operation are also changed when the sampling frequency is changed, it should be done after the AK4643 goes to the manual mode (ALC bit = "0") or MIC&ADC block is powered-down (PMADL=PMADR bits = "0"). IVOL gain is not reset when PMADL=PMADR bits = "0", and then IVOL operation starts from the setting value when PMADL or PMADR bit is changed to "1".

(9) ALC Disable: ALC bit = "1" → "0"

## ■ Speaker-amp Output

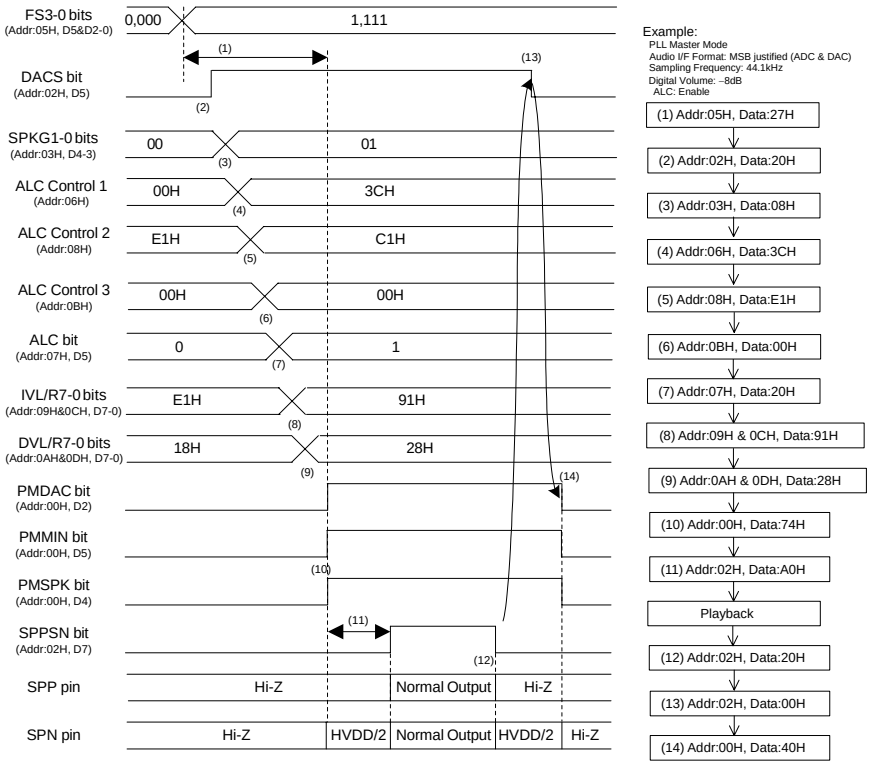



Figure 84. Speaker-Amp Output Sequence

<Example>

At first, clocks should be supplied according to “Clock Set Up” sequence.

(1) Set up a sampling frequency (FS3-0 bits). When the AK4643 is PLL mode, DAC and Speaker-Amp should be powered-up in consideration of PLL lock time after a sampling frequency is changed.

(2) Set up the path of “DAC → SPK-Amp”: DACS bit = “0” → “1”

(3) SPK-Amp gain setting: SPKG1-0 bits = “00” → “01”

(4) Set up Timer Select for ALC (Addr: 06H)

(5) Set up REF value for ALC (Addr: 08H)

(6) Set up LMTH1 and RGAIN1 bits (Addr: 0BH)

(7) Set up LMTH0, RGAIN0, LMAT1-0 and ALC bits (Addr: 07H)
When PMADL or PMADR bit is “1”, ALC for DAC path is disabled.

(8) Set up the input digital volume (Addr: 09H and 0CH)
When PMADL = PMADR bits = “0”, IVL7-0 and IVR7-0 bits should be set to “91H”(0dB).

(9) Set up the output digital volume (Addr: 0AH and 0DH).
When DVOLC bit is “1” (default), DVL7-0 bits set the volume of both channels. After DAC is powered-up, the digital volume changes from default value (0dB) to the register setting value by the soft transition.

(10) Power Up of DAC, MIN-Amp and Speaker-Amp: PMDAC = PMMIN = PMSPK bits = “0” → “1”
The DAC enters an initialization cycle that starts when the PMDAC bit is changed from “0” to “1” at PMADL and PMADR bits are “0”. The initialization cycle time is 1059/fs=24ms@fs=44.1kHz. During the initialization cycle, the DAC input digital data of both channels are internally forced to a 2's compliment, “0”. The DAC output reflects the digital input data after the initialization cycle is complete. When PMADL or PMADR bit is “1”, the DAC does not require an initialization cycle. When ALC bit is “1”, ALC is disable (ALC gain is set by IVL/R7-0 bits) during an intialization cycle (1059/fs=24ms@fs=44.1kHz). After the initialization cycle, ALC operation starts from the gain set by IVL/R7-0 bits.

(11) Exit the power-save-mode of Speaker-Amp: SPPSN bit = “0” → “1”

(12) Enter the power-save-mode of Speaker-Amp: SPPSN bit = “1” → “0”

(13) Disable the path of “DAC → SPK-Amp”: DACS bit = “1” → “0”

(14) Power Down DAC, MIN-Amp and Speaker-Amp: PMDAC = PMMIN = PMSPK bits = “1” → “0”

## ■ Mono signal output from Speaker-Amp

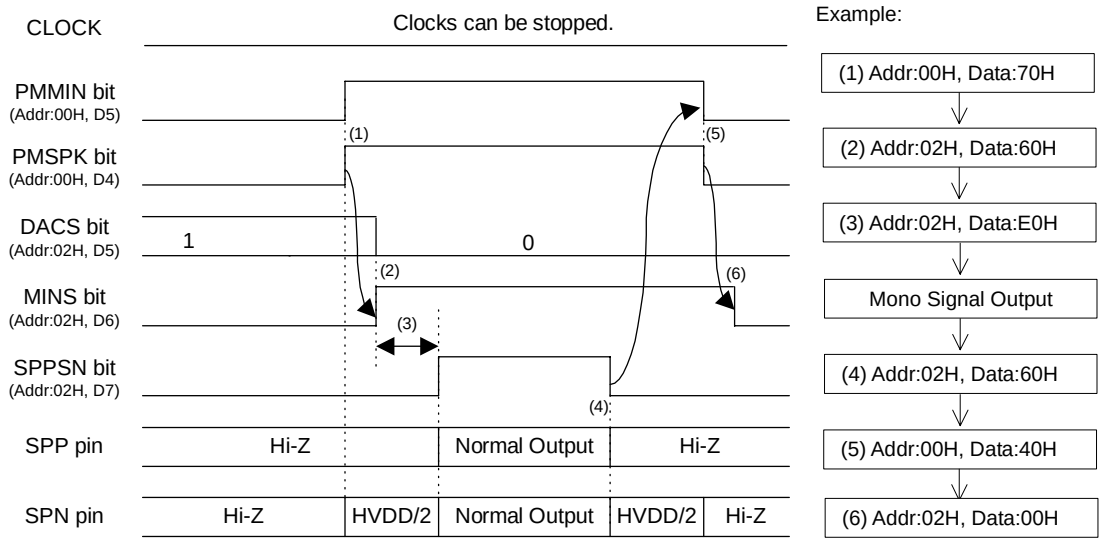



Figure 85. "MIN-Amp → Speaker-Amp" Output Sequence

<Example>

The clocks can be stopped when only MIN-Amp and Speaker-Amp are operating.

(1) Power Up MIN-Amp and Speaker-Amp: PMMIN = PMSPK bits = "0" → "1"
(2) Disable the path of "DAC → SPK-Amp": DACS bit = "0"
Enable the path of "MIN → SPK-Amp": MINS bit = "0" → "1"
(3) Exit the power-save-mode of Speaker-Amp: SPPSN bit = "0" → "1"
(4) Enter the power-save-mode of Speaker-Amp: SPPSN bit = "1" → "0"
(5) Power Down MIN-Amp and Speaker-Amp: PMMIN = PMSPK bits = "1" → "0"
(6) Disable the path of "MIN → SPK-Amp": MINS bit = "1" → "0"

## ■ Headphone-amp Output

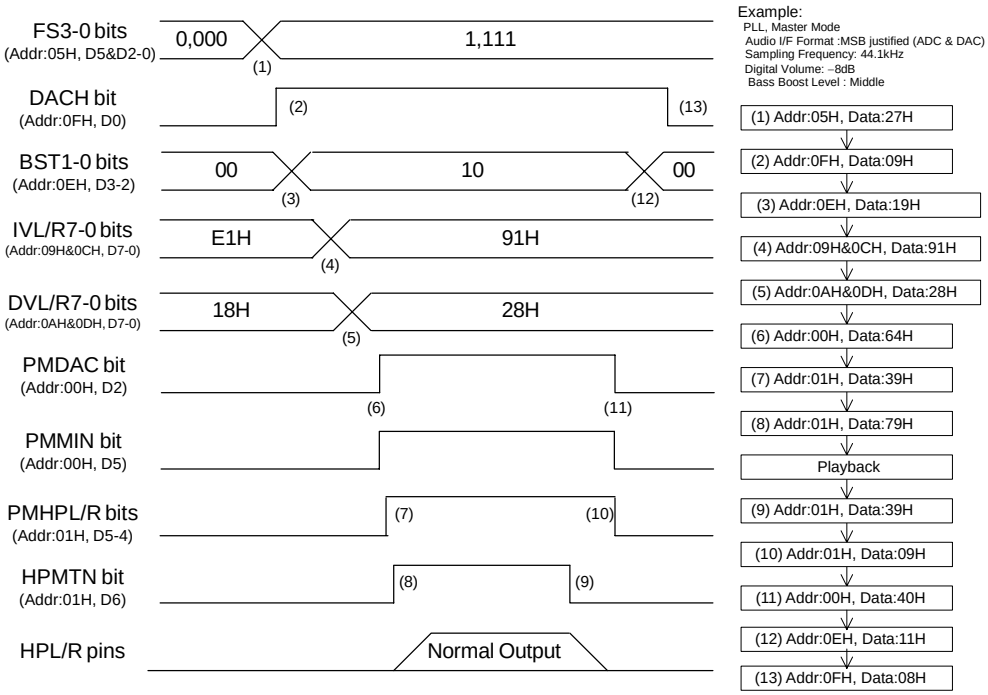



Figure 86. Headphone-Amp Output Sequence

<Example>

At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Set up a sampling frequency (FS3-0 bits). When the AK4643 is PLL mode, DAC and Speaker-Amp should be powered-up in consideration of PLL lock time after a sampling frequency is changed.

(2) Set up the path of "DAC → HP-Amp": DACH bit = "0" → "1"

(3) Set up the low frequency boost level (BST1-0 bits)

(4) Set up the input digital volume (Addr: 09H and 0CH)

When PMADL = PMADR bits = "0", IVL7-0 and IVR7-0 bits should be set to "91H"(0dB).

(5) Set up the output digital volume (Addr: 0AH and 0DH)

When DVOLC bit is "1" (default), DVL7-0 bits set the volume of both channels. After DAC is powered-up, the digital volume changes from default value (0dB) to the register setting value by the soft transition.

(6) Power up DAC and MIN-Amp: PMDAC = PMMIN bits = "0" → "1"

The DAC enters an initialization cycle that starts when the PMDAC bit is changed from "0" to "1" at PMADL and PMADR bits are "0". The initialization cycle time is 1059/fs=24ms@fs=44.1kHz. During the initialization cycle, the DAC input digital data of both channels are internally forced to a 2's compliment, "0". The DAC output reflects the digital input data after the initialization cycle is complete. When PMADL or PMADR bit is "1", the DAC does not require an initialization cycle. When ALC bit is "1", ALC is disable (ALC gain is set by IVL/R7-0 bits) during an intialization cycle (1059/fs=24ms@fs=44.1kHz). After the initialization cycle, ALC operation starts from the gain set by IVL/R7-0 bits.

(7) Power up headphone-amp: PMHPL = PMHPR bits = "0" → "1"

Output voltage of headphone-amp is still HVSS.

(8) Rise up the common voltage of headphone-amp: HPMTN bit = "0" → "1"

The rise time depends on HVDD and the capacitor value connected with the MUTET pin. When HVDD=3.3V and the capacitor value is 1.0μF, the time constant is $\tau_r$ = 100ms(typ), 250ms(max).

(9) Fall down the common voltage of headphone-amp: HPMTN bit = "1" → "0"

The fall time depends on HVDD and the capacitor value connected with the MUTET pin. When HVDD=3.3V and the capacitor value is 1.0μF, the time constant is $\tau_f$ = 100ms(typ), 250ms(max).

If the power supply is powered-off or headphone-Amp is powered-down before the common voltage goes to GND, the pop noise occurs. It takes twice of $\tau_f$ that the common voltage goes to GND.

(10) Power down headphone-amp: PMHPL = PMHPR bits = "1" → "0"

(11) Power down DAC and MIN-Amp: PMDAC = PMMIN bits = "1" → "0"

(12) Off the bass boost: BST1-0 bits = "00"

(13) Disable the path of "DAC → HP-Amp": DACH bit = "1" → "0"

## ■ Stereo Line Output

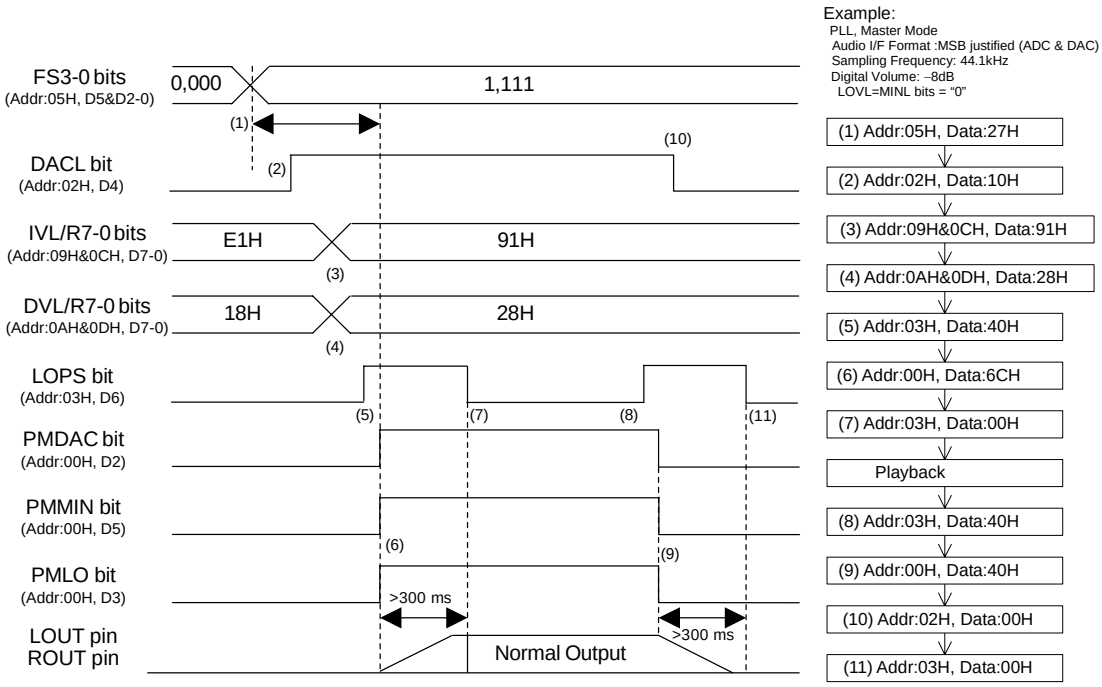



Figure 87. Stereo Lineout Sequence

<Example>

At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Set up the sampling frequency (FS3-0 bits). When the AK4643 is PLL mode, DAC and Stereo Line-Amp should be powered-up in consideration of PLL lock time after the sampling frequency is changed.

(2) Set up the path of "DAC → Stereo Line Amp": DACL bit = "0" → "1"

(3) Set up the input digital volume (Addr: 09H and 0CH)
When PMADL = PMADR bits = "0", IVL7-0 and IVR7-0 bits should be set to "91H"(0dB).

(4) Set up the output digital volume (Addr: 0AH and 0DH)
When DVOLC bit is "1" (default), DVL7-0 bits set the volume of both channels. After DAC is powered-up, the digital volume changes from default value (0dB) to the register setting value by the soft transition.

(5) Enter power-save mode of Stereo Line Amp: LOPS bit = "0" → "1"

(6) Power-up DAC, MIN-Amp and Stereo Line-Amp: PMDAC = PMMIN = PMLO bits = "0" → "1"
The DAC enters an initialization cycle that starts when the PMDAC bit is changed from "0" to "1" at PMADL and PMADR bits are "0". The initialization cycle time is 1059/fs=24ms@fs=44.1kHz. During the initialization cycle, the DAC input digital data of both channels are internally forced to a 2's compliment, "0". The DAC output reflects the digital input data after the initialization cycle is complete. When PMADL or PMADR bit is "1", the DAC does not require an initialization cycle. When ALC bit is "1", ALC is disable (ALC gain is set by IVL/R7-0 bits) during an intialization cycle (1059/fs=24ms@fs=44.1kHz). After the initialization cycle, ALC operation starts from the gain set by IVL/R7-0 bits.
LOUT and ROUT pins rise up to VCOM voltage after PMLO bit is changed to "1". Rise time is 300ms(max) at C=1μF and AVDD=3.3V.

(7) Exit power-save mode of Stereo Line-Amp: LOPS bit = "1" → "0"
LOPS bit should be set to "0" after LOUT and ROUT pins rise up. Stereo Line-Amp goes to normal operation by setting LOPS bit to "0".

(8) Enter power-save mode of Stereo Line-Amp: LOPS bit: "0" → "1"

(9) Power-down DAC, MIN-Amp and Stereo Line-Amp: PMDAC = PMMIN = PMLO bits = "1" → "0"
LOUT and ROUT pins fall down to AVSS. Fall time is 300ms(max) at C=1μF and AVDD=3.3V.

(10) Disable the path of "DAC → Stereo Line-Amp": DACL bit = "1" → "0"

(11) Exit power-save mode of Stereo Line-Amp: LOPS bit = "1" → "0"
LOPS bit should be set to "0" after LOUT and ROUT pins fall down.

## ■ Receiver-amp Output

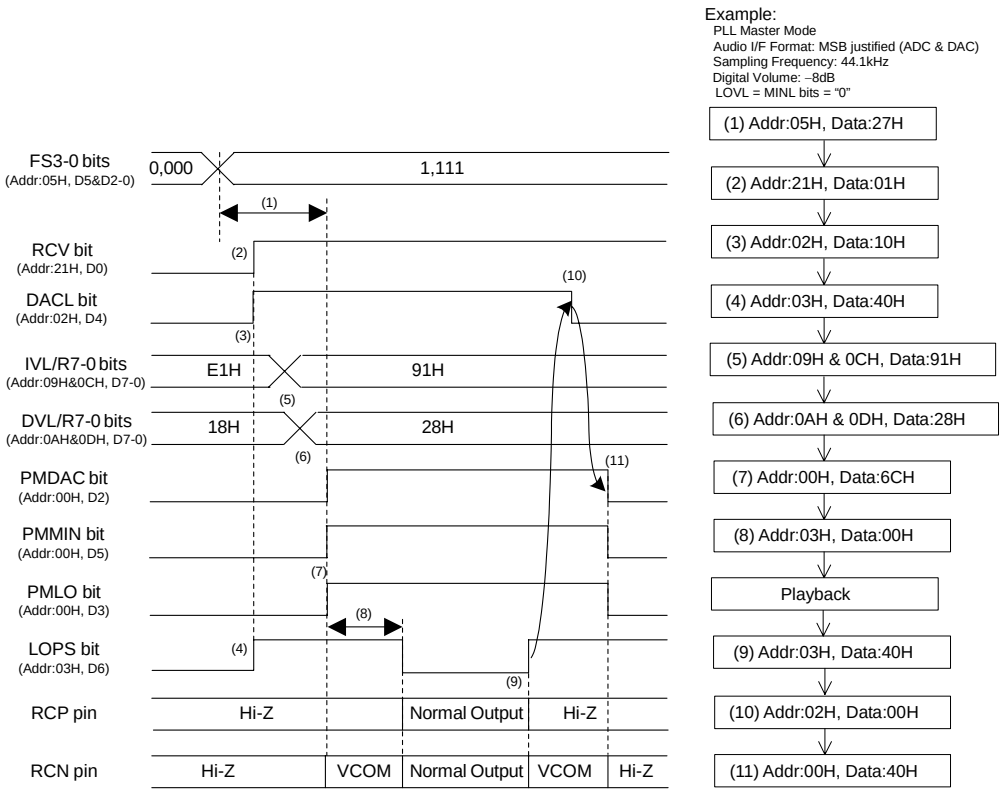



Figure 88. Receiver-Amp Output Sequence

<Example>

At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Set up a sampling frequency (FS3-0 bits). When the AK4643 is PLL mode, DAC and Receiver-Amp should be powered-up in consideration of PLL lock time after a sampling frequency is changed.

(2) Set up the path of "DAC → RCV-Amp and Power-save mode": DACL=LOPS bit = "0" → "1"

(3) Set up the input digital volume (Addr: 09H and 0CH)
When PMADL = PMADR bits = "0", IVL7-0 and IVR7-0 bits should be set to "91H"(0dB).

(4) Set up the output digital volume (Addr: 0AH and 0DH).
When DVOLC bit is "1" (default), DVL7-0 bits set the volume of both channels. After DAC is powered-up, the digital volume changes from default value (0dB) to the register setting value by the soft transition.

(5) Power Up of DAC, MIN-Amp and Receiver-Amp: PMDAC = PMMIN = PMLO bits = "0" → "1"
The DAC enters an initialization cycle that starts when the PMDAC bit is changed from "0" to "1" at PMADL and PMADR bits are "0". The initialization cycle time is 1059/fs=24ms@fs=44.1kHz. During the initialization cycle, the DAC input digital data of both channels are internally forced to a 2's compliment, "0". The DAC output reflects the digital input data after the initialization cycle (1059/fs=24ms@fs=44.1kHz) is complete. When PMADL or PMADR bit is "1", the DAC does not require an initialization cycle.

(6) Exit the power-save-mode of Receiver-Amp: LOPS bit = "1" → "0"

(7) Enter the power-save-mode of Receiver-Amp: LOPS bit = "0" → "1"

(8) Disable the path of "DAC → RCV-Amp": DACL bit = "1" → "0"

(9) Power Down DAC, MIN-Amp and Receiver-Amp: PMDAC = PMMIN = PMLO bits = "1" → "0"

## ■ Stop of Clock

Master clock can be stopped when ADC and DAC are not used.

1. PLL Master Mode

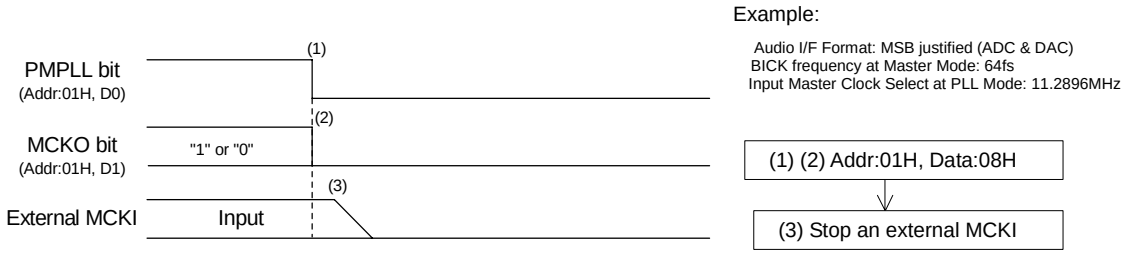



Figure 89. Clock Stopping Sequence (1)

<Example>
(1) Power down PLL: PMPLL bit = "1" → "0"
(2) Stop MCKO clock: MCKO bit = "1" → "0"
(3) Stop an external master clock.

2. PLL Slave Mode (LRCK or BICK pin)

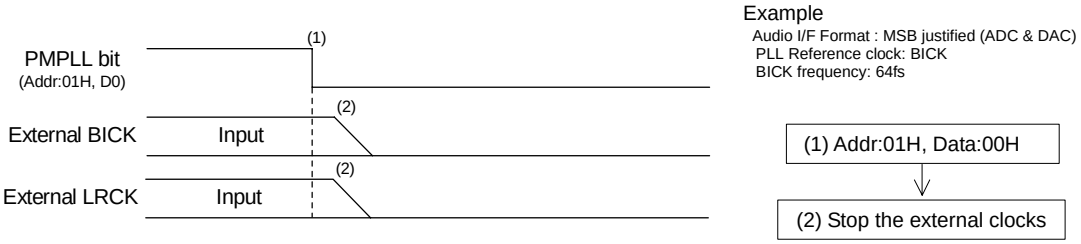



Figure 90. Clock Stopping Sequence (2)

<Example>
(1) Power down PLL: PMPLL bit = "1" → "0"
(2) Stop the external BICK and LRCK clocks

3. PLL Slave (MCKI pin)

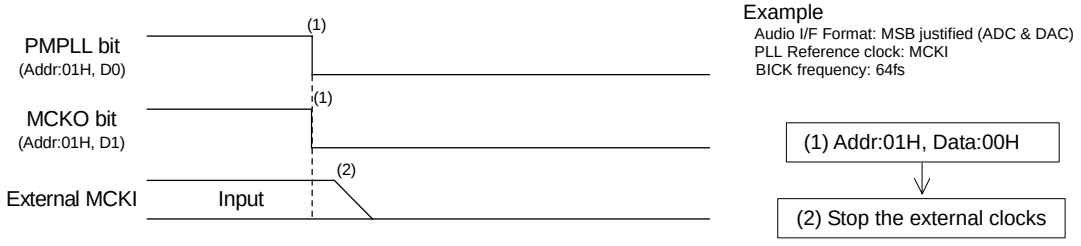



Figure 91. Clock Stopping Sequence (3)

<Example>
(1) Power down PLL: PMPLL bit = "1" → "0"
Stop MCKO output: MCKO bit = "1" → "0"
(2) Stop the external master clock.

4. EXT Slave Mode

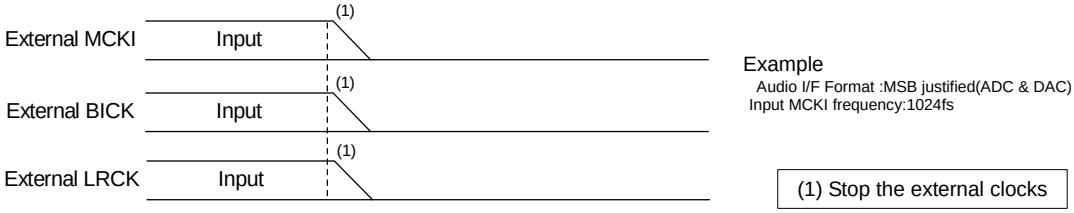



Figure 92. Clock Stopping Sequence (4)

<Example>
(1) Stop the external MCKI, BICK and LRCK clocks.

5. EXT Master Mode

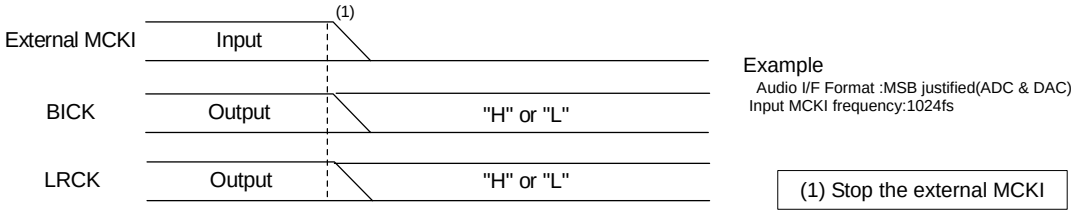



Figure 93. Clock Stopping Sequence (5)

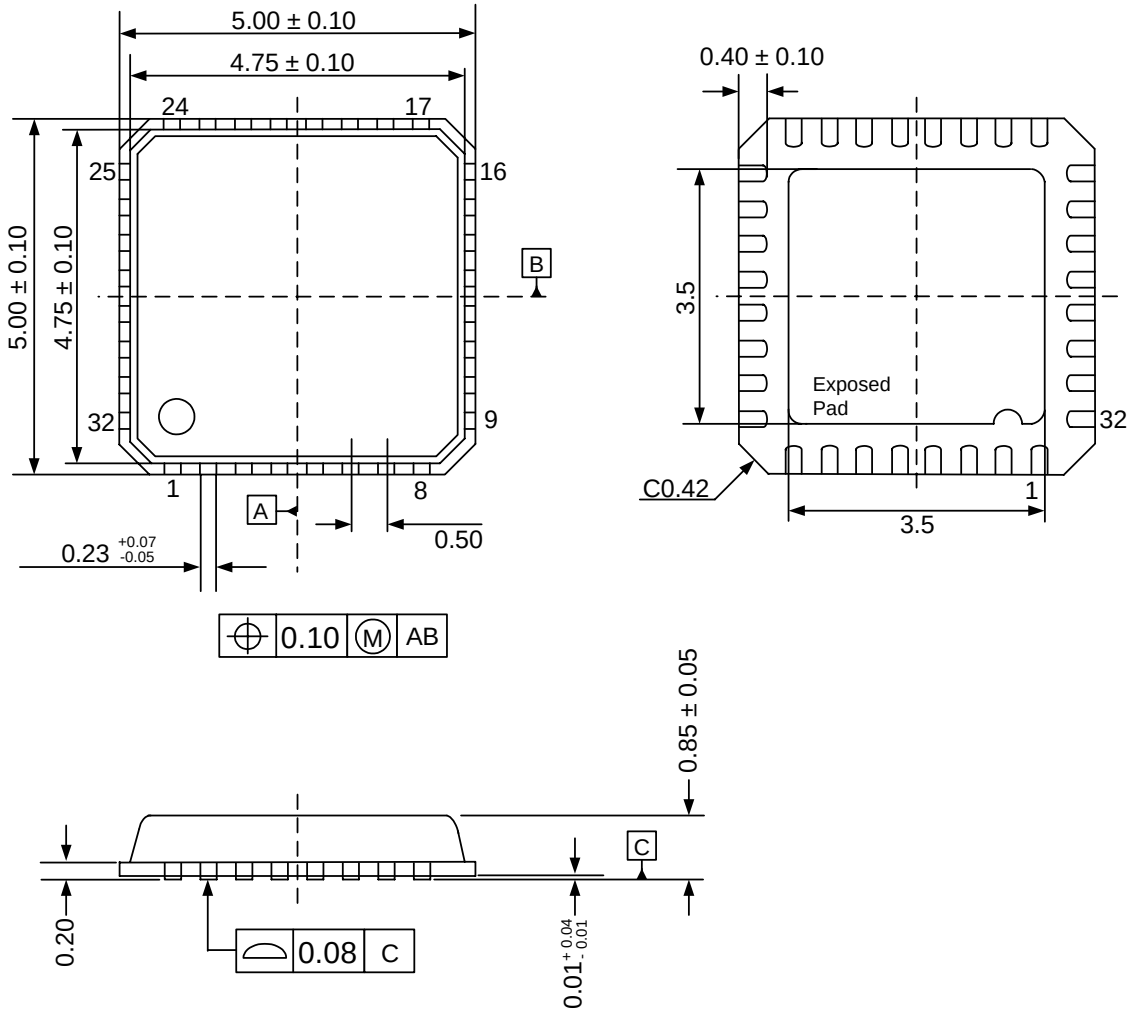
<Example>
(1) Stop MCKI clock. BICK and LRCK are fixed to “H” or “L”.

## ■ Power down

Power supply current can be shut down (typ. 10μA) by stopping clocks and setting PMVCM bit = “0” after all blocks except for VCOM are powered-down. Power supply current can be also shut down (typ. 10μA) by stopping clocks and setting PDN pin = “L”. When PDN pin = “L”, the registers are initialized.

## PACKAGE

### ● 32pin QFN (Unit: mm)

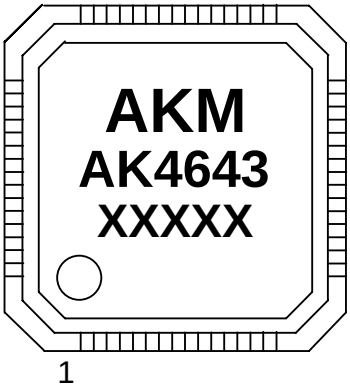



Note) The exposed pad on the bottom surface of the package must be open or connected to the ground.

### ■ Material & Lead finish

| | |
|---|---|
| Package molding compound: | Epoxy |
| Lead frame material: | Cu |
| Lead frame surface treatment: | Solder (Pb free) plate |

## MARKING




XXXXX : Date code identifier (5 digits)

## Revision History

| Date (YY/MM/DD) | Revision | Reason | Page | Contents |
|---|---|---|---|---|
| 06/04/04 | 00 | First Edition | | |
| 06/10/24 | 01 | Spec change | 38 | MIC/LINE Input Selector<br>"When full-differential input is used, the signal should not be input to the pins marked by "X" in Table 21." was added.<br>Table 21 (Handling of MIC/Line Input Pins) was added. |
| | | Error correct | 57 | Stereo Line Output Control Sequence<br>Power-down mode:<br>PMLO bit = "1" → PMLO bit = "0" |
| | | | 69 | $I^2C$ Bus Control Mode<br>"those most significant 3-bits are fixed to zeros"<br>→ "those most significant 2-bits are fixed to zeros" |
| | | | 79 | Register Definitions (Addr=0FH)<br>HPM bit: "When the HPM bit = "1", (L+R)/2 signals are output to Lch and Rch of the Headphone-Amp. Both PMHPL and PMHPR bits should be "1" when HPM bit is "1".<br>→ "When the HPM bit = "1", DAC output signal is output to Lch and Rch of the Headphone-Amp as (L+R)/2." |
| | | | 92 | Control Sequence (Clock Setup: Ext Slave Mode)<br>MCLK Frequency: 1024fs → 256fs<br>Addr=05H: Data=01H → 00H |
| | | | 93 | Control Sequence (Clock Setup: Ext Master Mode)<br>MCLK Frequency: 1024fs → 256fs<br>Addr=05H: Data=01H → 00H |
| | | | 94 | Control Sequence (Mic Recording)<br>ALC Setting: "Refer to Figure 23" → "Refer to Table 36" |

| Date (YY/MM/DD) | Revision | Reason | Page | Contents |
|---|---|---|---|---|
| 06/10/24 | 01 | Error correct | 97 | Control Sequence (Headphone Playback)<br>Digital Volume Level: 0dB → –8dB<br>Addr=0EH: Data=14H → 19H<br>Figure 86: (12) Addr=0EH: Data=00H → 11H |
| | | | 100 | Control Sequence (Stop of Clock: PLL Master Mode)<br>MCKO bits = “H” or “L” → “1” or “0” |

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