

BATTERY PROTECTION IC FOR 2-SERIAL OR 3-SERIAL-CELL PACK

S-8253A/B Series

The S-8253A/B Series are protection ICs for 2-serial or 3-serial cell lithium-ion rechargeable batteries and include high-accuracy voltage detectors and delay circuits.

These ICs are suitable for protecting lithium-ion battery packs from overcharge, overdischarge and overcurrent.

■ Features

- (1) High-accuracy voltage detection for each cell
 - Overcharge detection voltage n (n = 1 to 3) 3.9 V to 4.4 V (50 mV steps) Accuracy ± 25 mV
 - Overcharge release voltage n (n = 1 to 3) 3.8 V to 4.4 V ^{*1} Accuracy ± 50 mV
 - Overdischarge detection voltage n (n = 1 to 3) 2.0 V to 3.0 V (100 mV steps) Accuracy ± 80 mV
 - Overdischarge release voltage n (n = 1 to 3) 2.0 V to 3.4 V ^{*2} Accuracy ± 100 mV
- (2) Three-level overcurrent detection (Including load short circuiting detection)
 - Overcurrent detection voltage 1 0.05 V to 0.30 V (50 mV steps) Accuracy ± 25 mV
 - Overcurrent detection voltage 2 0.5 V (Fixed)
 - Overcurrent detection voltage 3 1.2 V (Fixed)
- (3) Delay times (Overcharge, Overdischarge, Overcurrent) are generated by an internal circuit. (External capacitors are unnecessary).
- (4) Charge / discharge operation can be inhibited via the control pin.
- (5) 0 V battery charge function available / unavailable are selectable.
- (6) High-voltage withstand devices Absolute maximum rating 26 V
- (7) Wide operating voltage range 2 to 24 V
- (8) Wide operating temperature range -40 to $+85$ °C
- (9) Low current consumption
 - Operation mode 28 μ A max. ($+25$ °C)
 - Power-down mode 0.1 μ A max. ($+25$ °C)
- (10) Lead-free products

*1. Overcharge release voltage = Overcharge detection voltage – Overcharge hysteresis voltage
(Overcharge hysteresis voltage n (n = 1 to 3) can be selected as 0 V or from a range of 0.1 to 0.4 V in 50 mV steps.)

*2. Overdischarge release voltage = Overdischarge detection voltage + Overdischarge hysteresis voltage
(Overdischarge hysteresis voltage n (n = 1 to 3) can be selected as 0 V or from a range of 0.2 to 0.7 V in 100 mV steps.)

■ Applications

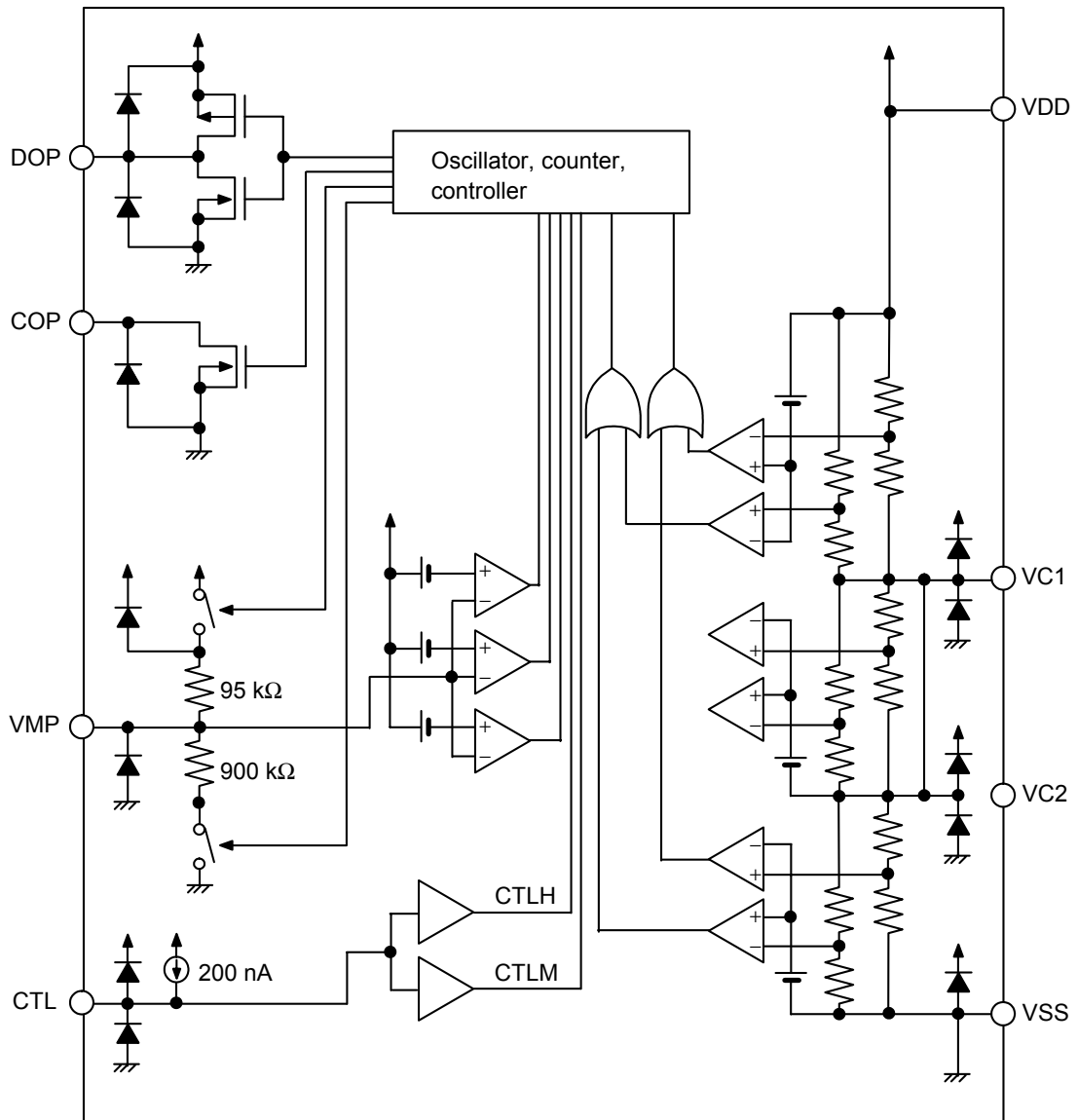
- Lithium-ion rechargeable battery packs
- Lithium polymer rechargeable battery packs

■ Package

Package Name	Drawing Code		
	Package	Tape	Reel
8-Pin TSSOP	FT008-A	FT008-E	FT008-E

■ **Block Diagrams**

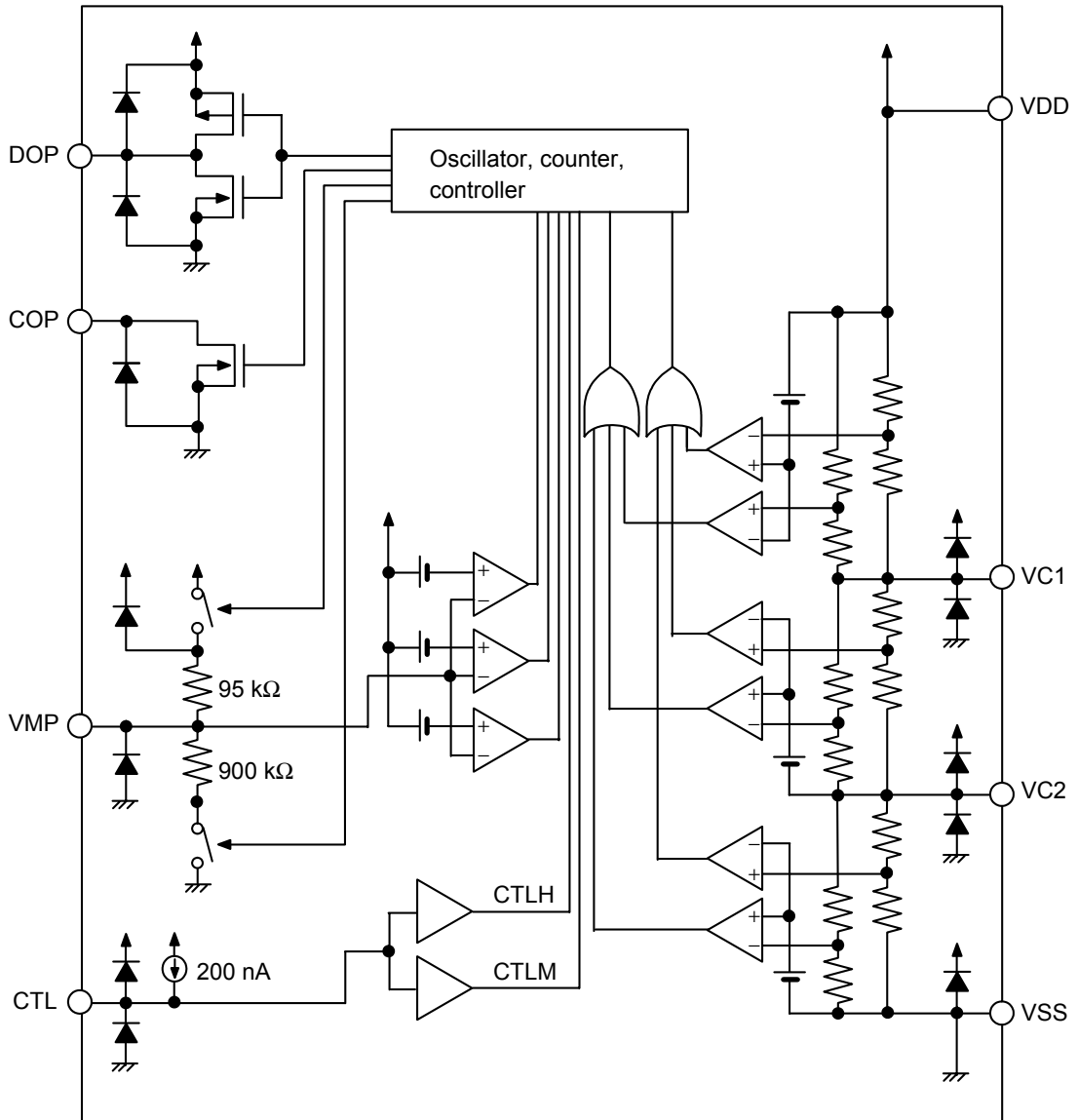
1. S-8253A Series



Remark All diodes shown in figure are parasitic diodes.

Figure 1

2. S-8253B Series

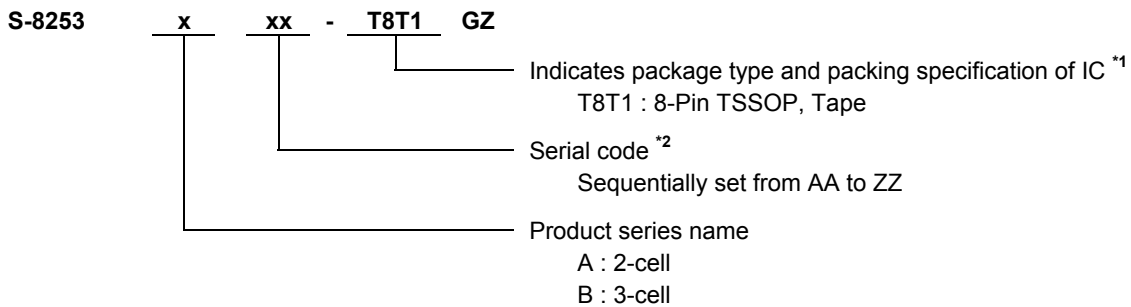


Remark All diodes shown in figure are parasitic diodes.

Figure 2

■ **Product Name Structure**

1. **Product Name**



*1. Refer to the taping specifications at the end of this book.

*2. Refer to the “2. Product Name List”.

2. **Product Name List**

Table 1 S-8253A Series (For 2-Serial Cell)

Model No.	Overcharge detection voltage V_{CU}	Overcharge release voltage V_{CL}	Overdischarge detection voltage V_{DL}	Overdischarge release voltage V_{DU}	Overcurrent detection voltage V_{IOV1}	0 V battery charge function
S-8253AAA-T8T1GZ	4.350 ±0.025 V	4.050 ±0.050 V	2.40 ±0.080 V	2.70 ±0.100 V	0.300 ±0.025 V	Available
S-8253AAB-T8T1GZ	4.350 ±0.025 V	4.050 ±0.050 V	2.70 ±0.080 V	2.70 ±0.080 V	0.300 ±0.025 V	Available
S-8253AAC-T8T1GZ	4.350 ±0.025 V	4.050 ±0.050 V	2.40 ±0.080 V	2.70 ±0.100 V	0.080 ±0.025 V	Available
S-8253AAD-T8T1GZ	4.250 ±0.025 V	4.050 ±0.050 V	2.40 ±0.080 V	2.70 ±0.100 V	0.120 ±0.025 V	Available
S-8253AAE-T8T1GZ	4.350 ±0.025 V	4.050 ±0.050 V	2.80 ±0.080 V	3.00 ±0.100 V	0.300 ±0.025 V	Available
S-8253AAF-T8T1GZ	4.350 ±0.025 V	4.050 ±0.050 V	2.40 ±0.080 V	2.60 ±0.100 V	0.300 ±0.025 V	Unavailable
S-8253AAG-T8T1GZ	4.280 ±0.025 V	4.080 ±0.050 V	2.40 ±0.080 V	2.70 ±0.100 V	0.150 ±0.025 V	Unavailable
S-8253AAH-T8T1GZ	4.350 ±0.025 V	4.150 ±0.050 V	2.30 ±0.080 V	2.30 ±0.080 V	0.090 ±0.025 V	Available

Remark Please contact the SII marketing department for the products with the detection voltage value other than those specified above.

Table 2 S-8253B Series (For 3-Serial Cell)

Model No.	Overcharge detection voltage V_{CU}	Overcharge release voltage V_{CL}	Overdischarge detection voltage V_{DL}	Overdischarge release voltage V_{DU}	Overcurrent detection voltage V_{IOV1}	0 V battery charge function
S-8253BAA-T8T1GZ	4.350 ±0.025 V	4.050 ±0.050 V	2.40 ±0.080 V	2.70 ±0.100 V	0.300 ±0.025 V	Available
S-8253BAB-T8T1GZ	4.325 ±0.025 V	4.075 ±0.050 V	2.20 ±0.080 V	2.90 ±0.100 V	0.200 ±0.025 V	Unavailable
S-8253BAC-T8T1GZ	4.350 ±0.025 V	4.050 ±0.050 V	2.40 ±0.080 V	2.70 ±0.100 V	0.080 ±0.025 V	Available
S-8253BAD-T8T1GZ	4.250 ±0.025 V	4.050 ±0.050 V	2.40 ±0.080 V	2.70 ±0.100 V	0.120 ±0.025 V	Available
S-8253BAE-T8T1GZ	4.350 ±0.025 V	4.150 ±0.050 V	2.20 ±0.080 V	2.40 ±0.100 V	0.100 ±0.025 V	Available
S-8253BAF-T8T1GZ	4.280 ±0.025 V	4.180 ±0.050 V	2.20 ±0.080 V	2.50 ±0.100 V	0.190 ±0.025 V	Unavailable
S-8253BAG-T8T1GZ	4.280 ±0.025 V	4.180 ±0.050 V	2.20 ±0.080 V	2.50 ±0.100 V	0.125 ±0.025 V	Unavailable
S-8253BAH-T8T1GZ	4.350 ±0.025 V	4.150 ±0.050 V	2.20 ±0.080 V	2.40 ±0.100 V	0.250 ±0.025 V	Available
S-8253BAI-T8T1GZ	4.350 ±0.025 V	4.150 ±0.050 V	2.20 ±0.080 V	2.40 ±0.100 V	0.160 ±0.025 V	Available

Remark Please contact the SII marketing department for the products with the detection voltage value other than those specified above.

■ **Pin Configuration**

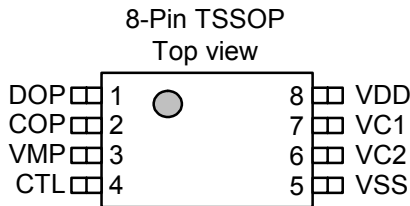


Figure 3

Table 3 S-8253A Series

Pin No.	Symbol	Description
1	DOP	Connection pin for discharge control FET gate (CMOS output)
2	COP	Connection pin for charge control FET gate (Nch open-drain output)
3	VMP	Pin for voltage detection between VDD and VMP (Detection pin for overcurrent)
4	CTL	Input pin for charge / discharge control signal, Pin for shortening test time (L : Normal operation, H : inhibit charge / discharge M ($V_{DD} \times 1 / 2$) : shorten test time)
5	VSS	Input pin for negative power supply, Connection pin for negative voltage of battery 2
6	VC2	No connection ^{*1}
7	VC1	Connection pin for negative voltage of battery 1, for positive voltage of battery 2
8	VDD	Input pin for positive power supply, Connection pin for positive voltage of battery 1

*1. No connection is electrically open. This pin can be connected to VDD or VSS.

Remark Refer to the package drawings for the external views.

Table 4 S-8253B Series

Pin No.	Symbol	Description
1	DOP	Connection pin for discharge control FET gate (CMOS output)
2	COP	Connection pin for charge control FET gate (Nch open-drain output)
3	VMP	Pin for voltage detection between VDD and VMP (Detection pin for overcurrent)
4	CTL	Input pin for charge / discharge control signal, pin for shortening test time (L : Normal operation, H : inhibit charge / discharge, M ($V_{DD} \times 1 / 2$) : shorten test time)
5	VSS	Input pin for negative power supply, Connection pin for negative voltage of battery 3
6	VC2	Connection pin for negative voltage of battery 2, for positive voltage of battery 3
7	VC1	Connection pin for negative voltage of battery 1, for positive voltage of battery 2
8	VDD	Input pin for positive power supply, Connection pin for positive voltage of battery 1

Remark Refer to the package drawings for the external views.

■ **Absolute Maximum Ratings**

Table 5

(Ta = 25 °C unless otherwise specified)

Item	Symbol	Applicable Pins	Absolute Maximum Ratings	Unit
Input voltage between VDD and VSS	V _{DS}	—	V _{SS} - 0.3 to V _{SS} + 26	V
Input pin voltage	V _{IN}	VC1, VC2	V _{SS} - 0.3 to V _{DD} + 0.3	V
VMP pin input voltage	V _{VMP}	VMP	V _{SS} - 0.3 to V _{SS} + 26	V
DOP pin output voltage	V _{DOP}	DOP	V _{SS} - 0.3 to V _{DD} + 0.3	V
COP pin output voltage	V _{COP}	COP	V _{SS} - 0.3 to V _{VMP} + 0.3	V
CTL input pin voltage	V _{IN_CTL}	CTL	V _{SS} - 0.3 to V _{DD} + 0.3	V
Power dissipation	P _D	—	300 (When not mounted on board)	mW
			700*1	mW
Operating ambient temperature	T _{opr}	—	- 40 to + 85	°C
Storage temperature	T _{stg}	—	- 40 to + 125	°C

*1. When mounted on board

[Mounted board]

- (1) Board size : 114.3 mm × 76.2 mm × t1.6 mm
- (2) Board name : JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

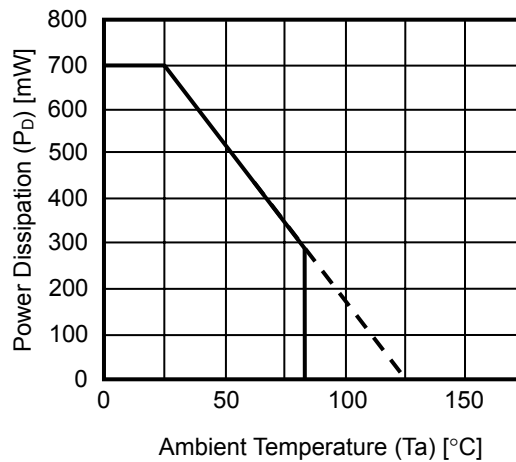


Figure 4 Power Dissipation of Package (When Mounted on Board)

BATTERY PROTECTION IC FOR 2-SERIAL OR 3-SERIAL-CELL PACK
S-8253A/B Series

Rev.3.7_00

■ **Electrical Characteristics**

1. Except Detection Delay Time

Table 6 (1/2)

(Ta = 25 °C unless otherwise specified)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Test condition	Test circuit
DETECTION VOLTAGE								
Overcharge detection voltage n	V _{CU_n}	3.90 to 4.40 V, Adjustable	V _{CU_n} -0.025	V _{CU_n}	V _{CU_n} +0.025	V	1	1
Overcharge release voltage n	V _{CL_n}	3.80 to 4.40 V, Adjustable	V _{CL} ≠ V _{CU}	V _{CL_n} -0.05	V _{CL_n} +0.05	V	1	1
			V _{CL} = V _{CU}	V _{CL_n} -0.025	V _{CL_n} +0.025	V	1	1
Overdischarge detection voltage n	V _{D_L_n}	2.0 to 3.0 V, Adjustable	V _{D_L_n} -0.080	V _{D_L_n}	V _{D_L_n} +0.080	V	1	1
Overdischarge release voltage n	V _{D_U_n}	2.0 to 3.40 V, Adjustable	V _{D_L} ≠ V _{D_U}	V _{D_U_n} -0.10	V _{D_U_n} +0.10	V	1	1
			V _{D_L} = V _{D_U}	V _{D_U_n} -0.08	V _{D_U_n} +0.08	V	1	1
Overcurrent detection voltage 1	V _{IOV1}	0.05 to 0.30 V, Adjustable	V _{DD} -V _{IOV1} -0.025	V _{DD} -V _{IOV1}	V _{DD} -V _{IOV1} +0.025	V	2	1
Overcurrent detection voltage 2	V _{IOV2}	—	V _{DD} -0.60	V _{DD} -0.50	V _{DD} -0.40	V	2	1
Overcurrent detection voltage 3	V _{IOV3}	—	V _{DD} -1.5	V _{DD} -1.2	V _{DD} -0.9	V	2	1
Temperature coefficient 1 **1	T _{COE1}	Ta = 0 to 50 °C	-1.0	0	1.0	mV / °C	—	—
Temperature coefficient 2 **2	T _{COE2}	Ta = 0 to 50 °C	-0.5	0	0.5	mV / °C	—	—
0 V BATTERY CHARGE FUNCTION								
0 V battery charge starting charger voltage	V _{0CHA}	0 V battery charging available	—	0.8	1.5	V	12	5
0 V battery charge inhibition battery voltage	V _{0INH}	0 V battery charging unavailable	0.4	0.7	1.1	V	12	5
INTERNAL RESISTANCE								
Resistance between VMP and VDD	R _{VMD}	V1 = V2 = V3**3 = 3.5 V, V _{VMP} = V _{SS}	70	95	120	kΩ	6	2
Resistance between VMP and VSS	R _{VMS}	V1 = V2 = V3**3 = 1.8 V, V _{VMP} = V _{DD}	450	900	1800	kΩ	6	2

Table 6 (2/2)

(Ta = 25 °C unless otherwise specified)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Test condition	Test circuit
INPUT VOLTAGE								
Operating voltage between VDD and VSS	V _{DSOP}	Output voltage of DOP and COP fixed	2	—	24	V	—	—
CTL input voltage "H"	V _{CTLH}	—	V _{DD} -0.5	—	—	V	7	1
CTL input voltage "L"	V _{CTLL}	—	—	—	V _{SS} +0.5	V	7	1
INPUT CURRENT								
Current consumption on operation	I _{OPe}	V1 = V2 = V3 ^{*3} = 3.5 V	—	14	28	μA	5	2
Current consumption at power down	I _{PDN}	V1 = V2 = V3 ^{*3} = 1.5 V	—	—	0.1	μA	5	2
VC1 pin current	I _{VC1}	V1 = V2 = V3 ^{*3} = 3.5 V	-0.3	0	0.3	μA	9	3
VC2 pin current	I _{VC2}	V1 = V2 = V3 ^{*3} = 3.5 V	-0.3	0	0.3	μA	9	3
CTL pin current "H"	I _{CTLH}	V1 = V2 = V3 ^{*3} = 3.5 V, V _{CTL1} = V _{DD}	—	—	0.1	μA	8	3
CTL pin current "L"	I _{CTLL}	V1 = V2 = V3 ^{*3} = 3.5 V, V _{CTL1} = V _{SS}	-0.4	-0.2	—	μA	8	3
OUTPUT CURRENT								
COP pin leakage current	I _{COH}	V _{COP} = 24 V	—	—	0.1	μA	10	4
COP pin sink current	I _{COL}	V _{COP} = V _{SS} + 0.5 V	10	—	—	μA	10	4
DOP pin source current	I _{DOH}	V _{DOP} = V _{DD} - 0.5 V	10	—	—	μA	11	4
DOP pin sink current	I _{DOL}	V _{DOP} = V _{SS} + 0.5 V	10	—	—	μA	11	4

*1. Voltage temperature coefficient 1 : Overcharge detection voltage

*2. Voltage temperature coefficient 2 : Overcurrent detection voltage 1

*3. Because S-8253A Series are the protection ICs for 2-serial cell, there is no V3 for them.

2. Detection Delay Time

- (1) **S-8253AAA, S-8253AAB, S-8253AAC, S-8253AAD, S-8253AAE, S-8253AAF, S-8253AAG, S-8253BAA, S-8253BAC, S-8253BAD, S-8253BAE, S-8253BAH**

Table 7

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Condition	Test Circuit
DELAY TIME (Ta = 25 °C)								
Overcharge detection delay time	t _{CU}	—	0.92	1.15	1.38	s	3	1
Overdischarge detection delay time	t _{DL}	—	115	144	173	ms	3	1
Overcurrent detection delay time 1	t _{IOV1}	—	7.2	9	10.8	ms	4	1
Overcurrent detection delay time 2	t _{IOV2}	—	3.6	4.5	5.4	ms	4	1
Overcurrent detection delay time 3	t _{IOV3}	—	220	300	380	μs	4	1

- (2) **S-8253BAB, S-8253BAF, S-8253BAG, S-8253BAI**

Table 8

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Condition	Test Circuit
DELAY TIME (Ta = 25 °C)								
Overcharge detection delay time	t _{CU}	—	0.92	1.15	1.38	s	3	1
Overdischarge detection delay time	t _{DL}	—	115	144	173	ms	3	1
Overcurrent detection delay time 1	t _{IOV1}	—	3.6	4.5	5.4	ms	4	1
Overcurrent detection delay time 2	t _{IOV2}	—	0.89	1.1	1.4	ms	4	1
Overcurrent detection delay time 3	t _{IOV3}	—	220	300	380	μs	4	1

- (3) **S-8253AAH**

Table 9

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Condition	Test Circuit
DELAY TIME (Ta = 25 °C)								
Overcharge detection delay time	t _{CU}	—	0.92	1.15	1.38	s	3	1
Overdischarge detection delay time	t _{DL}	—	115	144	173	ms	3	1
Overcurrent detection delay time 1	t _{IOV1}	—	14.5	18	22	ms	4	1
Overcurrent detection delay time 2	t _{IOV2}	—	3.6	4.5	5.4	ms	4	1
Overcurrent detection delay time 3	t _{IOV3}	—	220	300	380	μs	4	1

■ Test Circuits

1. Overcharge Detection Voltage 1, Overcharge Release Voltage 1, Overdischarge Detection Voltage 1, Overdischarge Release Voltage 1 (Test Condition 1, Test Circuit 1)

Confirm that $V1 = V2 = 3.5\text{ V}$ (S-8253A Series), $V1 = V2 = V3 = 3.5\text{ V}$ (S-8253B Series), $V4 = 0\text{ V}$, $V5 = 0\text{ V}$, and the COP and DOP pins are "L" ($V_{DD} \times 0.1\text{ V}$ or lower) (this status is referred to as the initial status).

1.1 Overcharge Detection Voltage 1 (V_{CU1}), Overcharge Release Voltage 1 (V_{CL1})

Overcharge detection voltage 1 (V_{CU1}) is the voltage of V1 when the voltage of the COP pin is "H" ($V_{DD} \times 0.9\text{ V}$ or more) after the V1 voltage has been gradually increased starting at the initial status. Overcharge release voltage 1 (V_{CL1}) is the voltage of V1 when the voltage at the COP pin is low after the V1 voltage has been gradually decreased.

1.2 Overdischarge Detection Voltage 1 (V_{DL1}), Overdischarge Release Voltage 1 (V_{DU1})

Overdischarge detection voltage 1 (V_{DL1}) is the voltage of V1 when the voltage of the DOP pin is high after the V1 voltage has been gradually decreased starting at the initial status. Overdischarge release voltage 1 (V_{DU1}) is the voltage of V1 when the voltage at the DOP pin is low after the V1 voltage has been gradually increased.

By changing Vn ($n = 2$: S-8253A Series, $n = 2, 3$: S-8253B Series) the overcharge detection voltage (V_{CU_n}), overcharge release voltage (V_{CL_n}), overdischarge detection voltage (V_{DL_n}), and overdischarge release voltage (V_{DU_n}) can be measured in the same way as when $n = 1$.

2. Overcurrent Detection Voltage 1, Overcurrent Detection Voltage 2, Overcurrent Detection Voltage 3 (Test Condition 2, Test Circuit 1)

Confirm that $V1 = V2 = 3.5\text{ V}$ (S-8253A Series), $V1 = V2 = V3 = 3.5\text{ V}$ (S-8253B Series), $V4 = 0\text{ V}$, $V5 = 0\text{ V}$, and the COP pin and DOP pin are low (this status is referred to as the initial status).

2.1 Overcurrent Detection Voltage 1 (V_{IOV1})

Overcurrent detection voltage 1 (V_{IOV1}) is the voltage of V5 when the voltages of the COP pin and DOP pin are high after the V5 voltage has been gradually increased starting at the initial status.

2.2 Overcurrent Detection Voltage 2 (V_{IOV2})

Overcurrent detection voltage 2 (V_{IOV2}) is the voltage of V5 when the voltages of the COP pin and DOP pin are high within the minimum and maximum values of overcurrent detection time 2 (t_{IOV2}) after the voltage of V5 was instantaneously increased (within $10\text{ }\mu\text{s}$) starting at the initial status.

2.3 Overcurrent Detection Voltage 3 (V_{IOV3})

Overcurrent detection voltage 3 (V_{IOV3}) is the voltage of V5 when the voltages of the COP pin and DOP pin are high within the minimum and maximum values of overcurrent detection time 3 (t_{IOV3}) after the voltage of V5 was instantaneously increased (within $10\text{ }\mu\text{s}$) starting at the initial status.

3. Overcharge Detection Delay Time, Overdischarge Detection Delay Time (Test Condition 3, Test Circuit 1)

Confirm that $V1 = V2 = 3.5\text{ V}$ (S-8253A Series), $V1 = V2 = V3 = 3.5\text{ V}$ (S-8253B Series), $V4 = 0\text{ V}$, $V5 = 0\text{ V}$, and the COP pin and DOP pin are low (this status is referred to as the initial status).

3.1 Overcharge Detection Delay Time (t_{CU})

The overcharge detection delay time (t_{CU}) is the time it takes for the voltage of the COP pin to change from low to high after the voltage of V1 is instantaneously changed from overcharge detection voltage 1 ($V_{CU1} - 0.2\text{ V}$) to overcharge detection voltage 1 ($V_{CU1} + 0.2\text{ V}$) (within $10\text{ }\mu\text{s}$) starting at the initial status.

3.2 Overdischarge Detection Delay Time (t_{DL})

The overdischarge detection delay time (t_{DL}) is the time it takes for the voltage of the DOP pin to change from low to high after the voltage of V1 is instantaneously changed from overdischarge detection voltage 1 ($V_{DL1} + 0.2\text{ V}$) to overdischarge detection voltage 1 ($V_{DL1} - 0.2\text{ V}$) (within $10\text{ }\mu\text{s}$) starting at the initial status.

4. Overcurrent Detection Delay Time 1, Detection Delay Time 2, Detection Delay Time 3 (Test Condition 4, Test Circuit 1)

Confirm that $V1 = V2 = 3.5\text{ V}$ (S-8253A Series), $V1 = V2 = V3 = 3.5\text{ V}$ (S-8253B Series), $V4 = 0\text{ V}$, $V5 = 0\text{ V}$, and the COP pin and DOP pin are low (this status is referred to as the initial status).

4.1 Overcurrent Detection Delay Time 1 (t_{IOV1})

Overcurrent detection delay time 1 (t_{IOV1}) is the time it takes for the voltage of the DOP pin to change from low to high after the voltage of V5 is instantaneously changed to 0.35 V (within $10\text{ }\mu\text{s}$) starting at the initial status.

4.2 Overcurrent Detection Delay Time 2 (t_{IOV2})

Overcurrent detection delay time 2 (t_{IOV2}) is the time it takes for the voltage of the DOP pin to change from low to high after the voltage of V5 is instantaneously changed to 0.7 V (within $10\text{ }\mu\text{s}$) starting at the initial status.

4.3 Overcurrent Detection Delay Time 3 (t_{IOV3})

Overcurrent detection delay time 3 (t_{IOV3}) is the time it takes for the voltage of the DOP pin to change from low to high after the voltage of V5 is instantaneously changed to 1.6 V (within $10\text{ }\mu\text{s}$) starting at the initial status.

5. Consumption on Operation, Power Consumption at Power-down (Test Condition 5, Test Circuit 2)

5.1 Power Consumption on Operation (I_{OPE})

The power consumption during operation (I_{OPE}) is the current of the VSS pin (I_{SS}) when $V1 = V2 = 3.5\text{ V}$ (S-8253A Series), $V1 = V2 = V3 = 3.5\text{ V}$ (S-8253B Series), S1 = ON, and S2 = OFF.

5.2 Power Consumption at Power-down (I_{PDN})

The power consumption at power-down (I_{PDN}) is the current of the VSS pin (I_{SS}) when $V1 = V2 = 1.5\text{ V}$ (S-8253A Series), $V1 = V2 = V3 = 1.5\text{ V}$ (S-8253B Series), S1 = OFF, and S2 = ON.

6. Resistance between VMP and VDD, Resistance between VMP and VSS
(Test Condition 6, Test Circuit 2)

Confirm that $V1 = V2 = 3.5\text{ V}$ (S-8253A Series), $V1 = V2 = V3 = 3.5\text{ V}$ (S-8253B Series), $S1 = \text{ON}$, and $S2 = \text{OFF}$ (this status is referred to as the initial status).

6.1 Resistance between VMP and VDD (R_{VMD})

The resistance between VMP and VDD (R_{VMD}) is determined based on the current of the VMP pin (I_{VMD}) after $S1$ and $S2$ are switched to OFF and ON, respectively, starting at the initial status.

$$\text{S-8253A Series : } R_{VMD} = (V1 + V2) / I_{VMD}$$

$$\text{S-8253B Series : } R_{VMD} = (V1 + V2 + V3) / I_{VMD}$$

6.2 Resistance between VMP and VSS (R_{VMS})

The resistance between VMP and VSS (R_{VMS}) is determined based on the current of the VMP pin (I_{VMS}) after $V1 = V2 = 1.8\text{ V}$ (S-8253A Series) or $V1 = V2 = V3 = 1.8\text{ V}$ (S-8253B Series) are set starting at the initial status.

$$\text{S-8253A Series : } R_{VMS} = (V1 + V2) / I_{VMS}$$

$$\text{S-8253B Series : } R_{VMS} = (V1 + V2 + V3) / I_{VMS}$$

7. CTL Pin Input Voltage “H”
(Test Condition 7, Test Circuit 1)

Confirm that $V1 = V2 = 3.5\text{ V}$ (S-8253A Series), $V1 = V2 = V3 = 3.5\text{ V}$ (S-8253B Series), $V4 = 0\text{ V}$, $V5 = 0\text{ V}$, and the COP pin and DOP pin are low (this status is referred to as the initial status).

7.1 CTL Pin Input Voltage “H” (V_{CTLH})

The CTL pin input voltage “H” (V_{CTLH}) is the voltage of $V4$ when the voltages of the COP pin and DOP pin are high after the voltage of $V4$ has been gradually increased starting at the initial status.

8. CTL Pin Input Voltage “L”
(Test condition 7, Test circuit 1)

Confirm that $V1 = V2 = 3.5\text{ V}$ (S-8253A Series), $V1 = V2 = V3 = 3.5\text{ V}$ (S-8253B Series), $V4 = 0\text{ V}$, $V5 = 0.35\text{ V}$, and the COP pin and DOP pin are high (this status is referred to as the initial status).

8.1 CTL Pin Input Voltage “L” ($V_{CTL L}$)

The CTL pin input voltage “L” ($V_{CTL L}$) is the voltage of $V4$ when the voltages of the COP pin and DOP pin are low after the voltage of $V4$ has been gradually decreased starting at the initial status.

9. CTL Pin Current “H”, CTL Pin Current “L”
(Test Condition 8, Test Circuit 3)

9.1 CTL Pin Current “H” (I_{CTLH}), CTL Pin Current “L” ($I_{CTL L}$)

The CTL pin current “H” (I_{CTLH}) is the current that flows through the CTL pin when $V1 = V2 = 3.5\text{ V}$ (S-8253A Series), $V1 = V2 = V3 = 3.5\text{ V}$ (S-8253B Series), and $S3 = \text{ON}$, $S4 = \text{OFF}$. The CTL current “L” ($I_{CTL L}$) is the current that flows through the CTL pin when $S3 = \text{OFF}$ and $S4 = \text{ON}$ after that.

10. VC1 Pin Current, VC2 Pin Current
(Test Condition 9, Test Circuit 3)

10.1 VC1 Pin Current (I_{VC1}), VC2 Pin Current (I_{VC2})

The VC1 pin current (I_{VC1}) is the current that flows through the VC1 pin when $V1 = V2 = 3.5\text{ V}$ (S-8253A Series), $V1 = V2 = V3 = 3.5\text{ V}$ (S-8253B Series), and $S3 = \text{OFF}$, $S4 = \text{ON}$. Similarly, the VC2 pin current (I_{VC2}) is the current that flows through the VC2 pin under these conditions (S-8253B Series only).

11. COP Pin Leakage Current, COP Pin Sink Current
(Test Condition 10, Test Circuit 4)

11.1 COP Pin Leakage Current (I_{COH})

The COP pin leakage current (I_{COH}) is the current that flows through the COP pin when $V1 = V2 = 12\text{ V}$ (S-8253A Series), $V1 = V2 = V3 = 8\text{ V}$ (S-8253B Series), $S6 = S7 = S8 = \text{OFF}$, and $S5 = \text{ON}$.

11.2 COP Pin Sink Current (I_{COL})

The COP pin sink current (I_{COL}) is the current that flows through the COP pin when $V1 = V2 = 3.5\text{ V}$ (S-8253A Series), $V1 = V2 = V3 = 3.5\text{ V}$ (S-8253B Series), $V6 = 0.5\text{ V}$, $S5 = S7 = S8 = \text{OFF}$, and $S6 = \text{ON}$.

12. DOP Pin Source Current, DOP Pin Sink Current
(Test Condition 11, Test Circuit 4)

12.1 DOP Pin Source Current (I_{DOH})

The DOP pin source current (I_{DOH}) is the current that flows through the DOP pin when $V1 = V2 = 1.8\text{ V}$ (S-8253A Series), $V1 = V2 = V3 = 1.8\text{ V}$ (S-8253B Series), $V7 = 0.5\text{ V}$, $S5 = S6 = S8 = \text{OFF}$, and $S7 = \text{ON}$.

12.2 DOP Pin Sink Current (I_{DOL})

The DOP pin sink current (I_{DOL}) is the current that flows through the DOP pin when $V1 = V2 = 3.5\text{ V}$ (S-8253A Series), $V1 = V2 = V3 = 3.5\text{ V}$ (S-8253B Series), $V8 = 0.5\text{ V}$, $S5 = S6 = S7 = \text{OFF}$, and $S8 = \text{ON}$.

**13. 0 V Battery Charge Starting Battery Charger Voltage (Product with 0 V Battery Charge Function),
0 V Battery Charge Inhibition Battery Voltage (Product with 0 V Battery Charge Inhibition Function)**
(Test Condition 12, Test Circuit 5)

13.1 0 V Battery Charge Starting Battery Charger Voltage (V_{0CHA}) (Product with 0 V Battery Charge Function)

The COP pin voltage should be lower than $V_{0CHA\text{ max.}} - 1\text{ V}$ when $V1 = V2 = 0\text{ V}$ (S-8253A Series), $V1 = V2 = V3 = 0\text{ V}$ (S-8253B Series), and $V9 = V_{VMP} = V_{0CHA\text{ max.}}$

13.2 0 V Battery Charge Inhibition Battery Voltage (V_{0INH}) (Product with 0 V Battery Charge Inhibition Function)

The COP pin voltage should be higher than $V_{VMP} - 1\text{ V}$ when $V1 = V2 = V_{0INH\text{ min.}}$ (S-8253A Series), $V1 = V2 = V3 = V_{0INH\text{ min.}}$ (S-8253B Series), and $V9 = V_{VMP} = 24\text{ V}$.

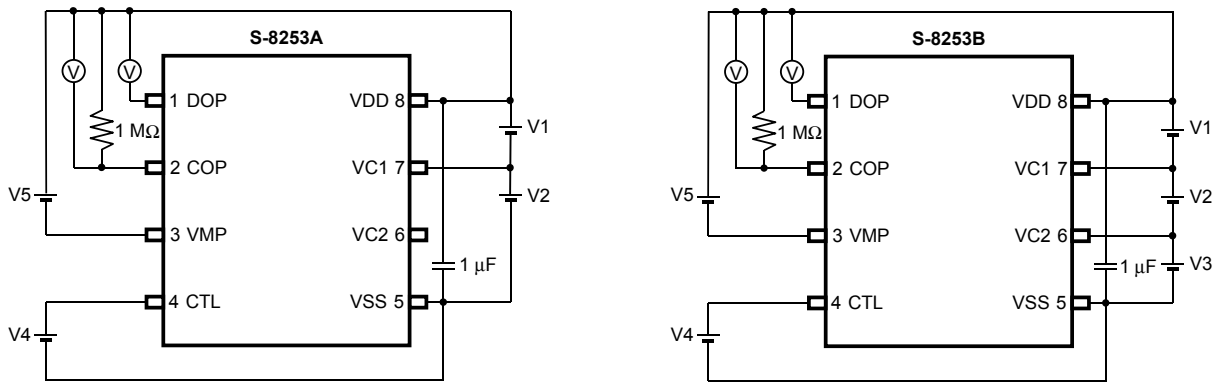


Figure 5 Test Circuit 1

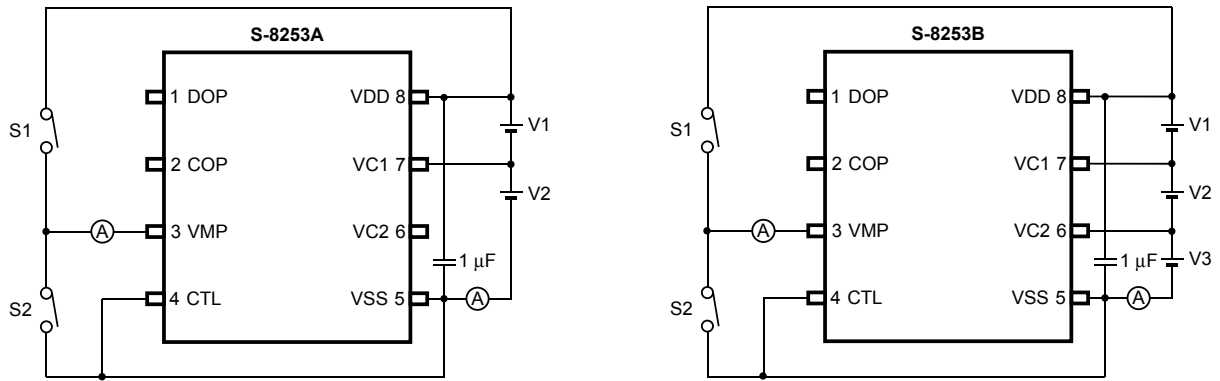


Figure 6 Test Circuit 2

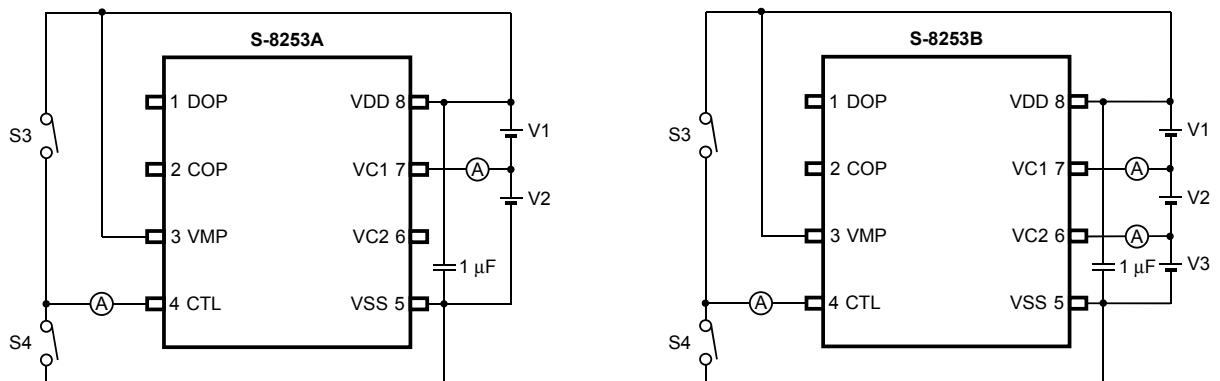


Figure 7 Test Circuit 3

BATTERY PROTECTION IC FOR 2-SERIAL OR 3-SERIAL-CELL PACK
S-8253A/B Series

Rev.3.7_00

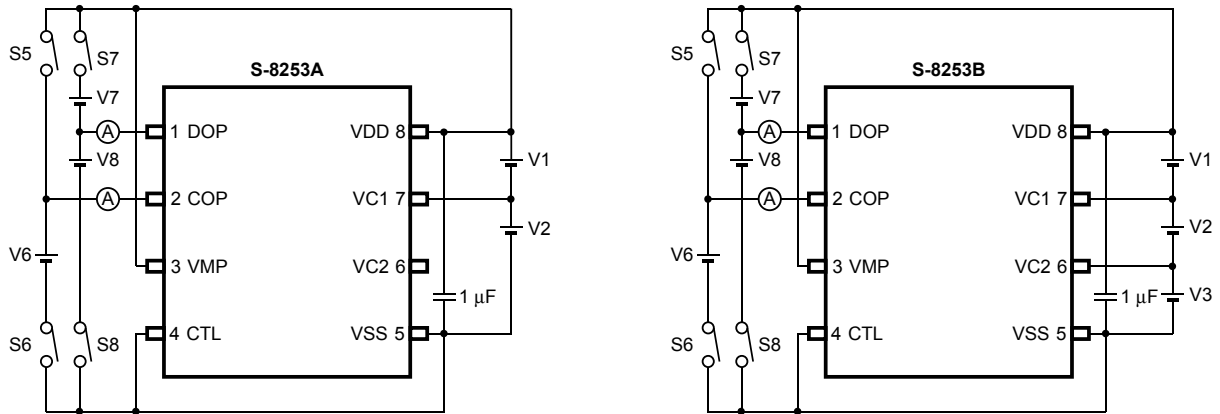


Figure 8 Test Circuit 4

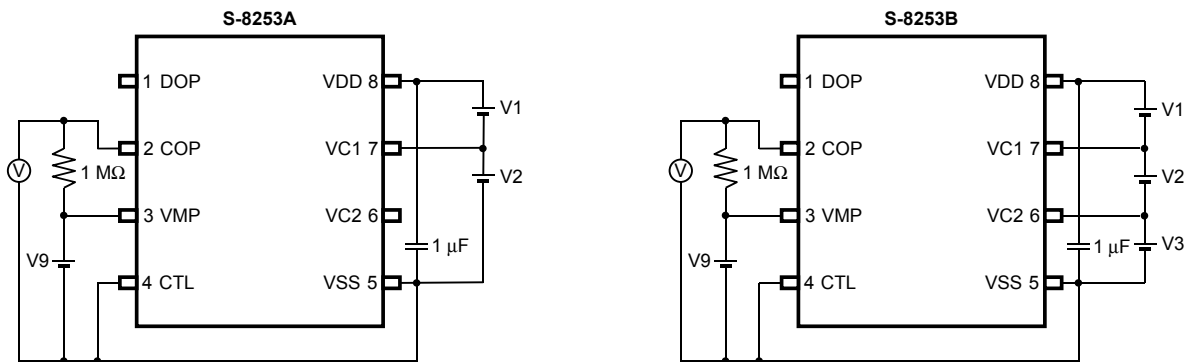


Figure 9 Test Circuit 5

■ Operation

Remark Refer to “ ■ Battery Protection IC Connection Example”.

1. Normal Status

When all of the battery voltages are in the range from V_{DLn} to V_{CUn} and the discharge current is lower than the specified value (the VMP pin voltage is higher than $V_{DD} - V_{IOV1}$), the charging and discharging FETs are turned on.

Caution When the battery is connected for the first time, discharging may not be enabled. In this case, short the VMP pin and VDD pin or connect the charger to restore the normal status.

2. Overcharge Status

When any one of the battery voltages becomes higher than V_{CUn} and the state continues for t_{CU} or longer, the COP pin becomes high impedance. Because the COP pin is pulled up to the EB+ pin voltage by an external resistor, the charging FET is turned off to stop charging. This is called the overcharge status. The overcharge status is released when one of the following two conditions holds.

- (1) All battery voltages become V_{CLn} or lower.
- (2) All of the battery voltages are V_{CUn} or lower, and the VMP pin voltage is $V_{DD} - V_{IOV1}$ or lower (since the discharge current flows through the body diode of the charging FET immediately after discharging is started when the charger is removed and a load is connected, the VMP pin voltage momentarily decreases by approximately 0.6 V from the VDD pin voltage. The IC detects this voltage and releases the overcharging status).

3. Overdischarge Status

When any one of the battery voltages becomes lower than V_{DLn} and the state continues for t_{DL} or longer, the DOP pin voltage becomes V_{DD} level, and the discharging FET is turned off to stop discharging. This is called the overdischarging status. After discharging is stopped due to the overdischarge status, the S-8253A/B Series enters the power-down status.

4. Power-down Status

When discharging has stopped due to the overdischarge status, the VMP pin is pulled down to the V_{SS} level by the R_{VMS} resistor. When the VMP pin voltage is lower than Typ. 0.8 V, the S-8253A/B Series enters the power-down status. In the power-down status, almost all the circuits of the S-8253A/B Series stop and the current consumption is I_{PDN} or lower. The conditions of each output pin are as follows.

- (1) COP pin : High-Z
- (2) DOP pin : V_{DD}

The power-down status is released when the following condition holds.

- (1) The VMP pin voltage is Typ. 0.8 V or higher.

The overdischarging status is released when the following two conditions hold.

- (1) All battery voltage is released at $V_{DU n}$ or higher when the VMP pin voltage is Typ. 0.8 V or higher and the VMP pin voltage is lower than V_{DD} .
- (2) All battery voltage is released at $V_{DL n}$ or higher when the VMP pin voltage is Typ. 0.8 V or higher and the VMP pin voltage is V_{DD} or higher (when a charger is connected and VMP pin voltage is V_{DD} or higher, overdischarge hysteresis is released and electric discharge control FET is turned on at $V_{DL n}$).

5. Overcurrent Status

The S-8253A/B Series has three overcurrent detection levels (V_{IOV1} , V_{IOV2} , and V_{IOV3}) and three overcurrent detection delay times (t_{IOV1} , t_{IOV2} , and t_{IOV3}) corresponding to each overcurrent detection level. When the discharging current becomes higher than the specified value (the difference of the voltages of the VMP pin and VDD pin is greater than V_{IOV1}) and the state continues for t_{IOV1} or longer, the S-8253A/B Series enters the overcurrent status, in which the DOP pin voltage becomes V_{DD} level to turn off the discharging FET to stop discharging, the COP pin becomes high impedance and is pulled up to the EB+ pin voltage to turn off the charging FET to stop charging, and the VMP pin is pulled up to the V_{DD} voltage by the internal resistor (R_{VMD}). Operation of overcurrent detection levels 2, 3 (V_{IOV2} , V_{IOV3}) and overcurrent detection delay times 2, 3 (t_{IOV2} , t_{IOV3}) are the same as for V_{IOV1} and t_{IOV1} .

The overcurrent status is released when the following condition holds.

- (1) The VMP pin voltage is $V_{DD} - V_{IOV1}$ or higher because a charger is connected or the load is released.

Caution The impedance that enables automatic restoration varies depending on the battery voltage and set value of overcurrent detection voltage 1.

6. 0 V Battery Charge Function

Regarding the charging of a self-discharged battery (0 V battery), the S-8253A/B Series has two functions from which one should be selected.

- (1) 0 V battery charging is allowed (0 V battery charging is available.)
When the charger voltage is higher than V_{0CHA} , the 0 V battery can be charged.
- (2) 0 V battery charging is prohibited (0 V battery charging is unavailable.)
When one of the battery voltages is lower than V_{0INH} , the 0 V battery cannot be charged.

Caution When the VDD pin voltage is lower than the minimum value of V_{DSOP} , the operation of the S-8253A/B Series is not guaranteed.

7. Delay Circuit

The following detection delay times are determined by dividing a clock of approximately 3.57 kHz by the counter.

(Example) Oscillator clock cycle (T_{CLK}) :	280 μ s
Overcharge detection delay time (t_{CU}) :	1.15 s
Overdischarge detection delay time (t_{DL}) :	144 ms
Overcurrent detection delay time 1 (t_{IOV1}) :	9 ms
Overcurrent detection delay time 2 (t_{IOV2}) :	4.5 ms

Remark The overcurrent detection delay time 2 (t_{IOV2}) and overcurrent detection delay time 3 (t_{IOV3}) start when the overcurrent detection voltage 1 (V_{IOV1}) is detected. As soon as the overcurrent detection voltage 2 (V_{IOV2}) or overcurrent detection voltage 3 (V_{IOV3}) is detected over the detection delay time for overcurrent 2 (t_{IOV2}) or overcurrent 3 (t_{IOV3}) after the detection of overcurrent 1 (V_{IOV1}), the S-8253A/B turns the discharging control FET off within t_{IOV2} or t_{IOV3} of each detection.

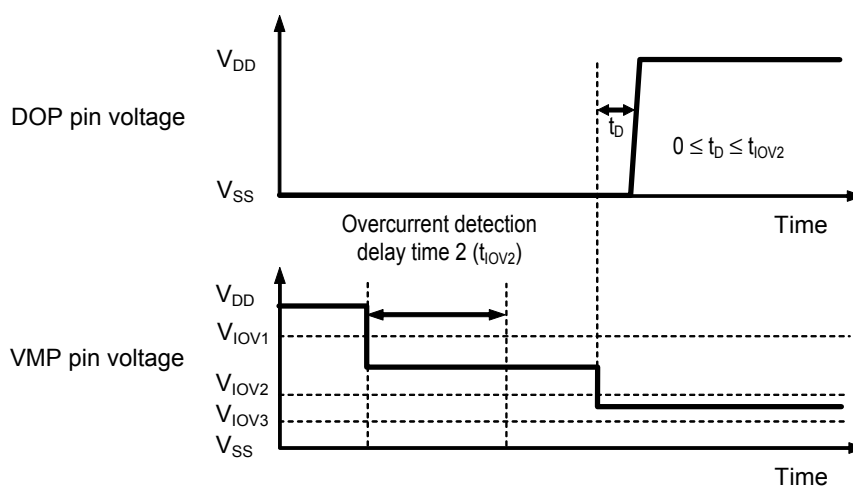


Figure 10

8. CTL Pin

The S-8253A/B Series has a control pin for charge / discharge control and shortening the test time. The levels, “L”, “H”, and “M”, of the voltage input to the CTL pin determine the status of the S-8253A/B Series: normal operation, charge / discharge inhibition, or test time shortening. The CTL pin takes precedence over the battery protection circuit. During normal use, short the CTL pin and VSS pin.

Table 10 Conditions Set by CTL Pin

CTL Pin Potential	Status of IC	COP Pin	DOP Pin
Open	Charge / discharge inhibited status	High-Z	V_{DD}
High ($V_{CTL} \geq V_{CTLH}$)	Charge / discharge inhibited status	High-Z	V_{DD}
Middle ($V_{CTLL} < V_{CTL} < V_{CTLH}$)	Delay time-shortening status *1	(*2)	(*2)
Low ($V_{CTLL} \geq V_{CTL}$)	Normal status	(*2)	(*2)

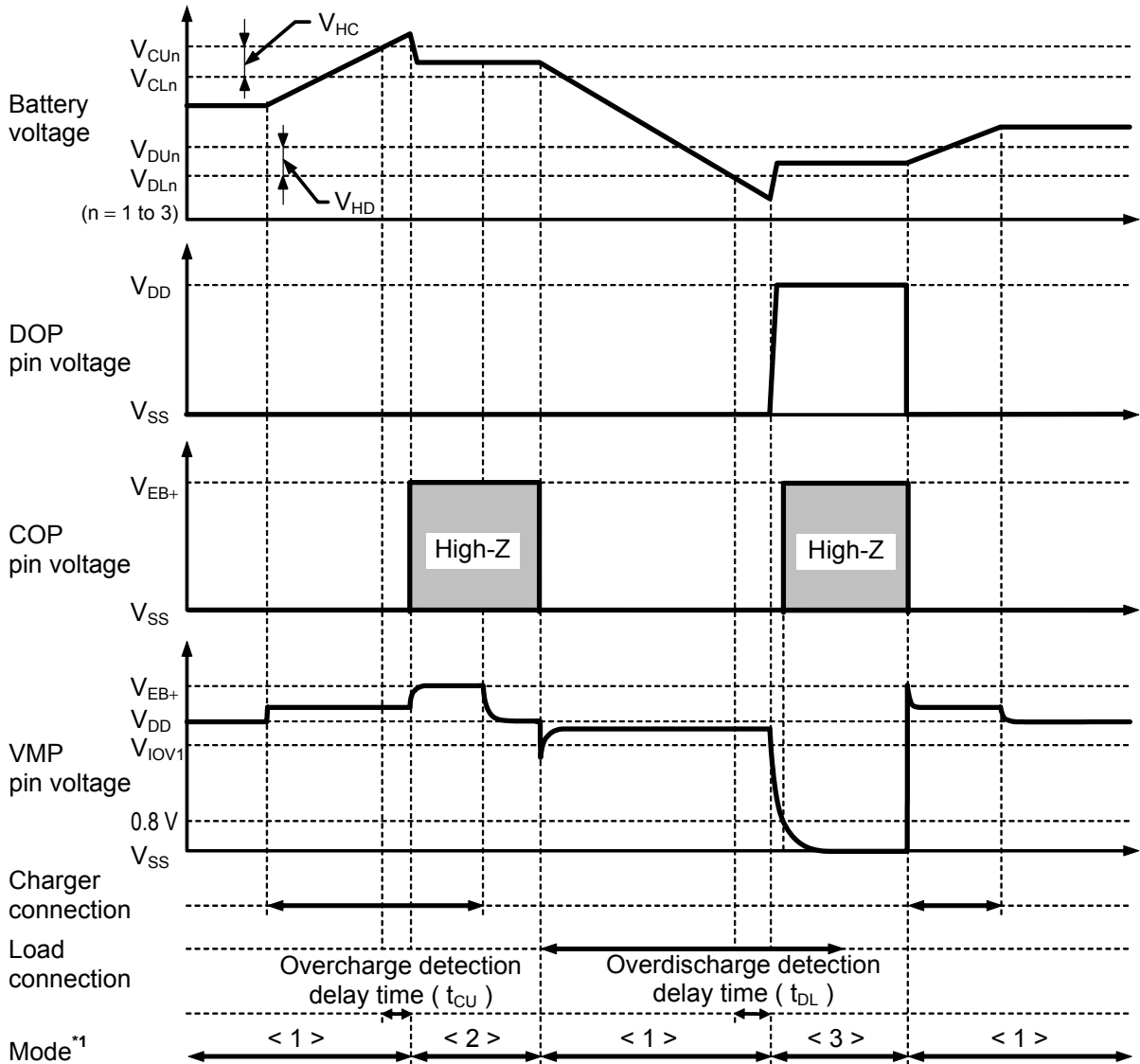
*1. In this status, delay times are shortened in 1 / 60 to 1 / 30 scale.

*2. The pin status is controlled by the voltage detection circuit.

- Caution**
1. If the potential of the CTL pin is middle, overcurrent detection voltage 1 (V_{IOV1}) does not operate.
 2. If you use the middle potential of the CTL pin, contact SII marketing department.
 3. Please note unexpected behavior might occur when electrical potential difference between the CTL pin (“L” level) and VSS is generated through the external filter (R_{VSS} and C_{VSS}) as a result of input voltage fluctuations.

■ Timing Chart

1. Overcharge Detection and Overdischarge Detection

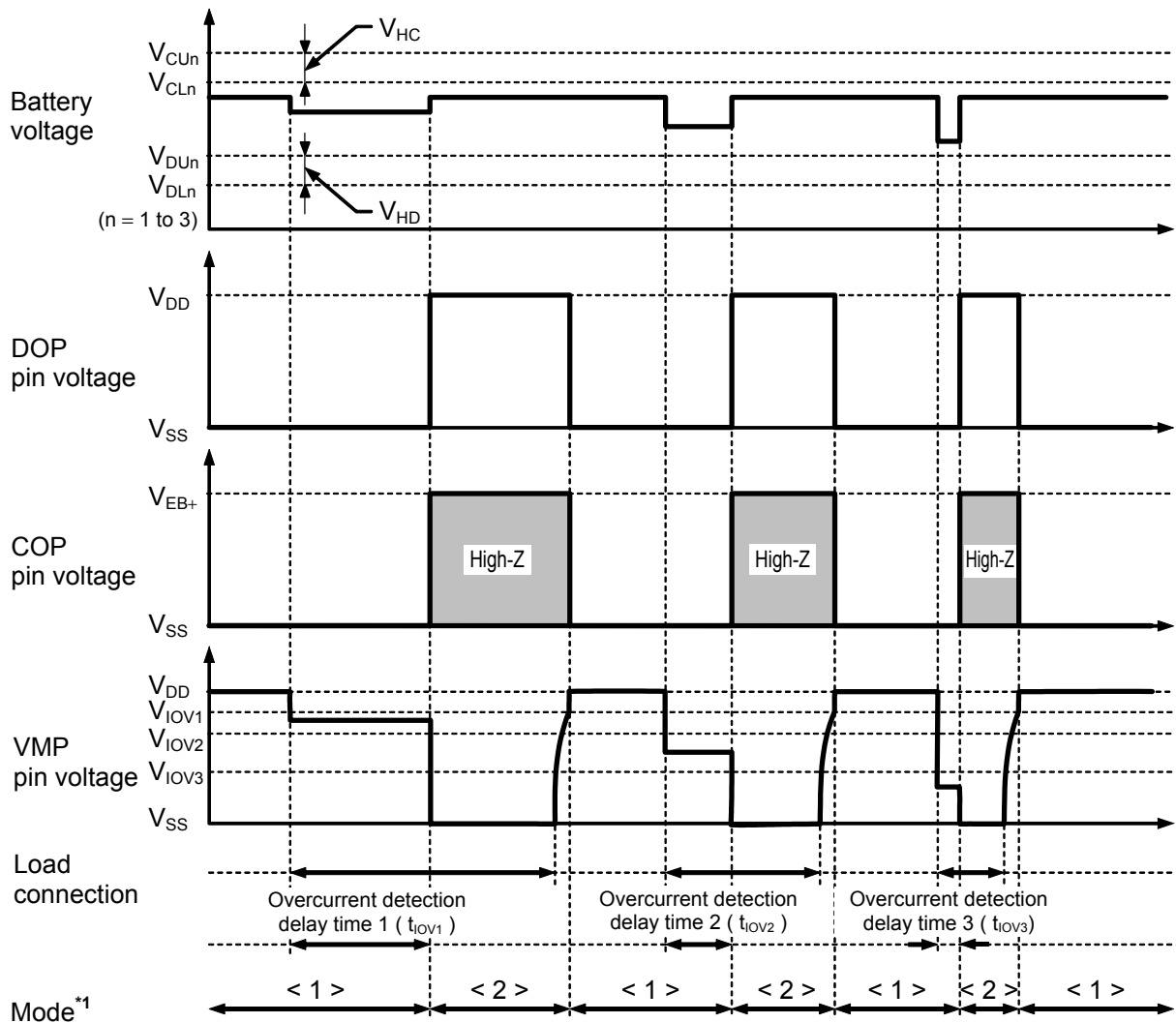


- *1. < 1 > : Normal mode
 < 2 > : Overcharge mode
 < 3 > : Overdischarge mode

Remark The charger is assumed to charge with a constant current. V_{EB+} indicates the open voltage of the charger.

Figure 11

2. Overcurrent Detection



*1. $\langle 1 \rangle$: Normal mode
 $\langle 2 \rangle$: Overcurrent mode

Remark The charger is assumed to charge with a constant current. V_{EB+} indicates the open voltage of the charger.

Figure 12

Table 11 Constants for External Components

No.	Symbol	Typ.	Range	Unit
1	R _{VC1}	1	0.51 to 1 ^{*1}	kΩ
2	R _{VC2}	1	0.51 to 1 ^{*1}	kΩ
3	R _{DOP}	5.1	2 to 10	kΩ
4	R _{COP}	1	0.1 to 1	MΩ
5	R _{VMP}	5.1	1 to 10	kΩ
6	R _{CTL}	1	1 to 100	kΩ
7	R _{VSS}	51	5.1 to 51 ^{*1}	Ω
8	C _{VC1}	0.1	0.1 to 0.47 ^{*1}	μF
9	C _{VC2}	0.1	0.1 to 0.47 ^{*1}	μF
10	C _{VSS}	2.2	1 to 10 ^{*1}	μF

*1. Please set up a filter constant to be $R_{VSS} \times C_{VSS} \geq 51 \mu\text{F} \cdot \Omega$ and to be
 $R_{VC1} \times C_{VC1} = R_{VC2} \times C_{VC2} = R_{VSS} \times C_{VSS}$.

Caution 1. The above constants may be changed without notice.

2. It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant do not guarantee proper operation. Perform through evaluation using the actual application to set the constant.

■ Precautions

- In case of designing a circuit by using the CTL pin, as seen in **Figure 15**, note that discharging may stop during connecting a battery pack and the device.

【Cause】

This is because the overcurrent detection voltage $3 (V_{IOV3})$ is detected due to the rush current which flows into the device while a battery pack is in the delay time-shortening status.

【Mechanism】

As seen in **Figure 15**, before a battery pack is connected to the device, the battery pack may be in the charge / discharge inhibited status in which the CTL pin is internally pulled-up. From this status, if connecting the battery pack to the device, the CTL pin will be pulled-down in a time-constant $C1 \times (R1 + R_{PD})$ by a pull-down resistor in the device. If the CTL's potential reaches $V_{CTL} < V_{CTLH}$, the battery pack goes in the delay time-shortening status so that it releases charging and discharging, hence it starts charging a parasitic capacitor in the device. In this case, if the rush current, which makes the S-8253A/B Series to detect the overcurrent detection voltage $3 (V_{IOV3})$, flows into the device, the overcurrent detection delay time $3 (t_{IOV3} = 300 \mu s \text{ typ.})$ will be shortened. So that the battery pack goes in the overcurrent status in several 10 μs . However, the battery pack goes in the normal status by connecting the device to the charger.

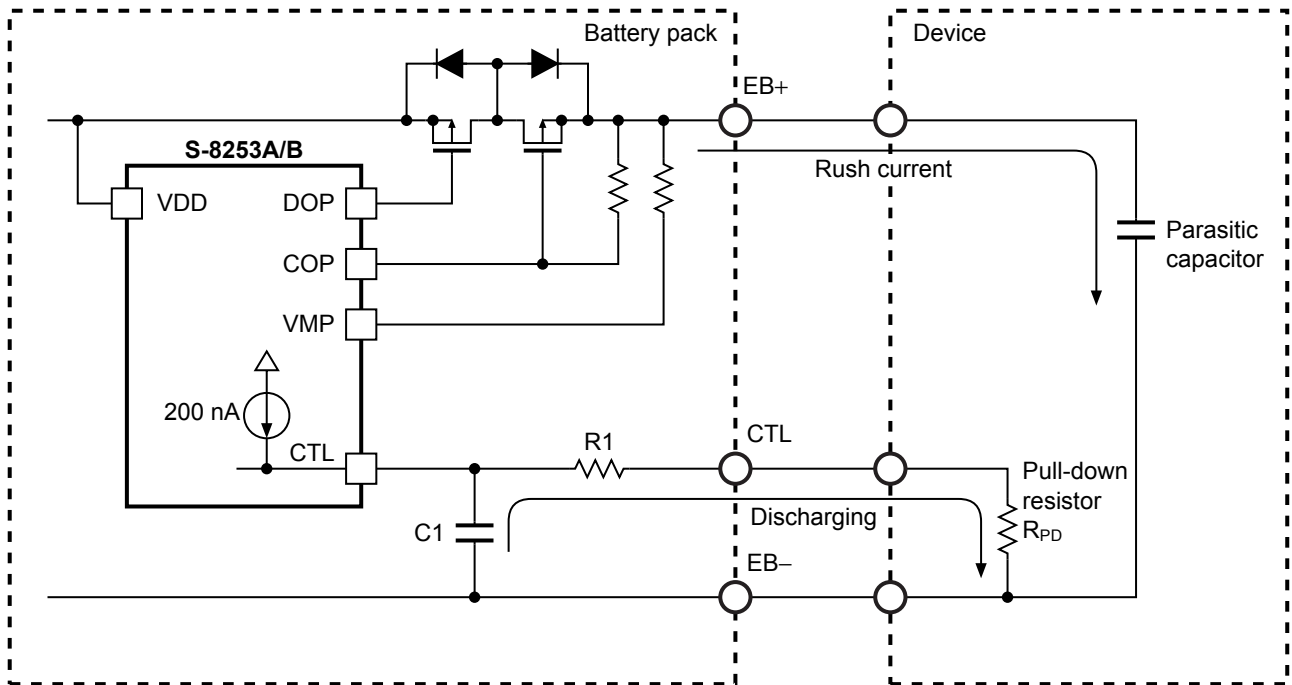


Figure 15

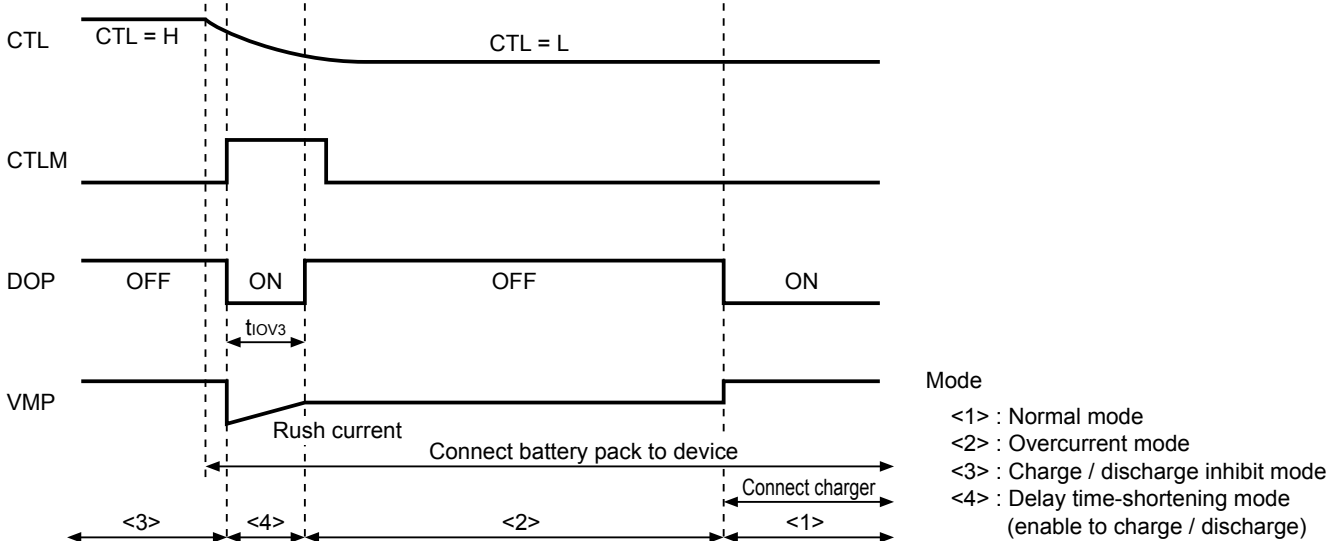


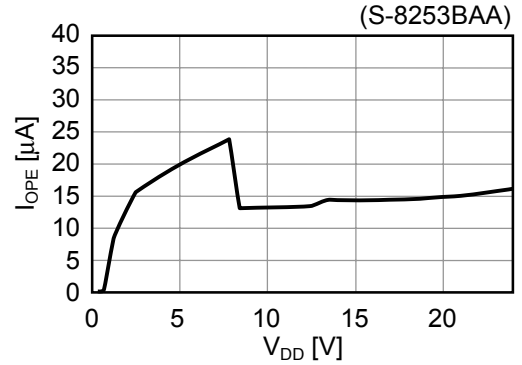
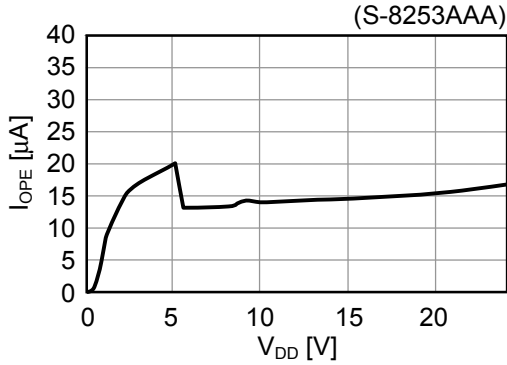
Figure 16

- The application conditions for the input voltage, output voltage, and load current should not exceed the package power dissipation.
- Batteries can be connected in any order, however, there may be cases when discharging cannot be performed when a battery is connected. In this case, short the VMP pin and VDD pin or connect the battery charger to return to the normal mode.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- SII claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

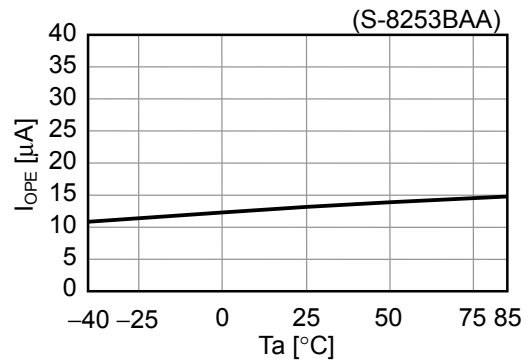
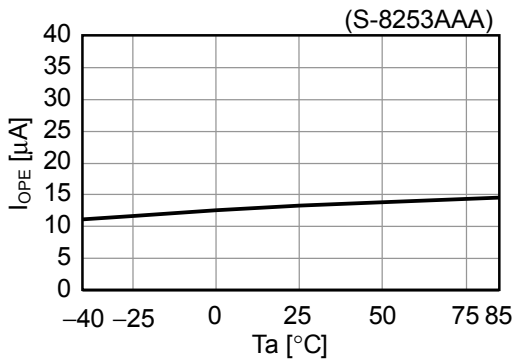
■ **Characteristics (Typical Data)**

1. Current Consumption

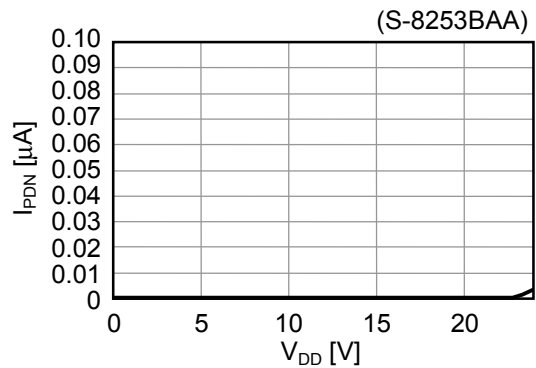
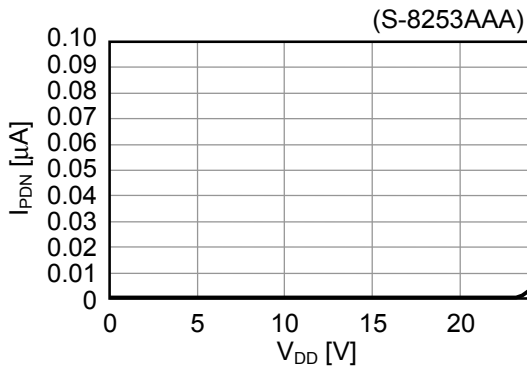
1.1 I_{OPE} vs. V_{DD}



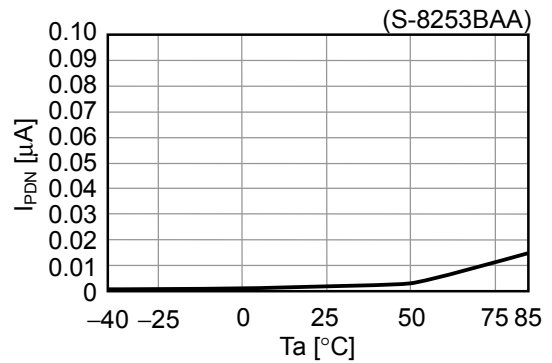
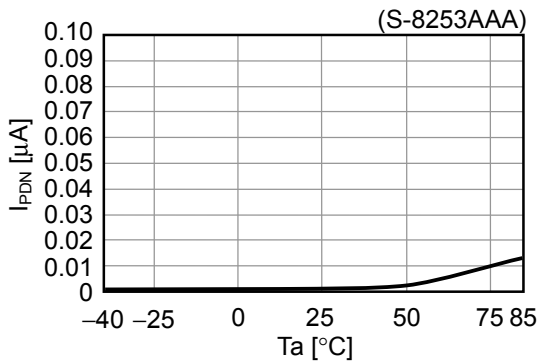
1.2 I_{OPE} vs. T_a



1.3 I_{PDN} vs. V_{DD}

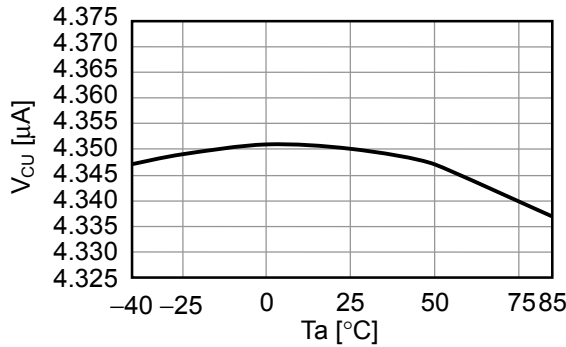


1.4 I_{PDN} vs. T_a

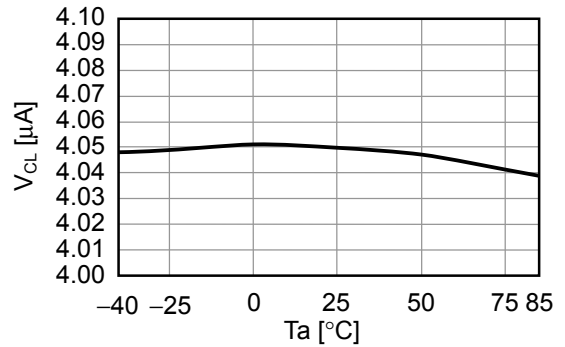


2. Overcharge Detection / Release Voltage, Overdischarge Detection / Release Voltage, Overcurrent Detection Voltage, and Delay Times (S-8253AAA, S-8253BAA)

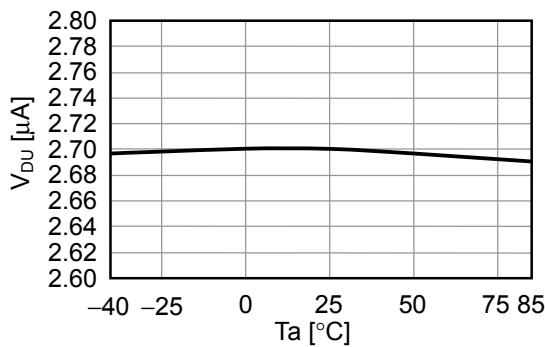
2.1 V_{CU} vs. T_a



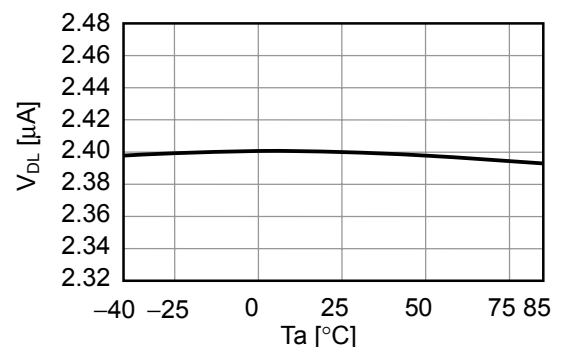
2.2 V_{CL} vs. T_a



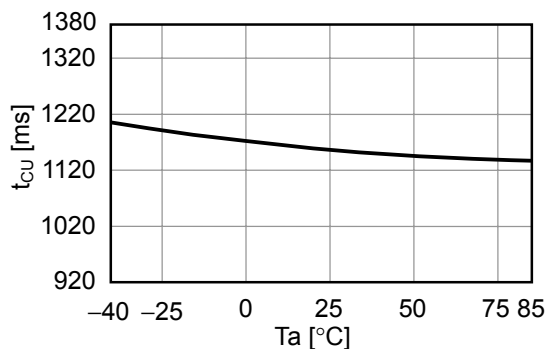
2.3 V_{DU} vs. T_a



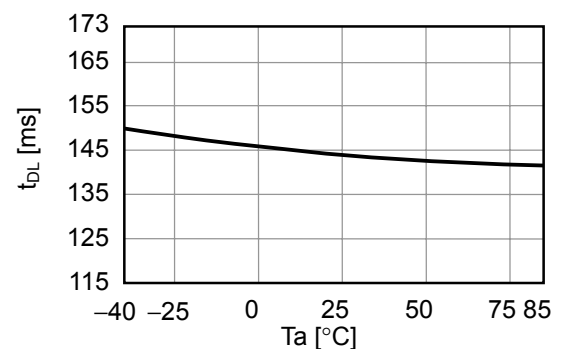
2.4 V_{DL} vs. T_a



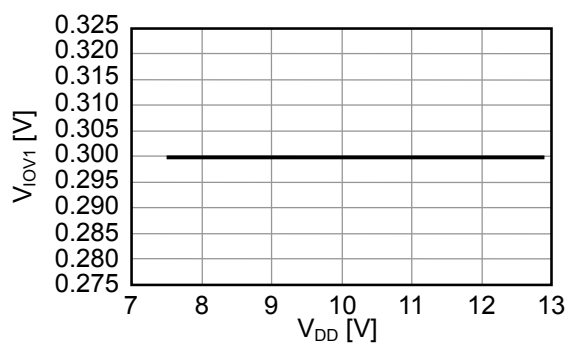
2.5 t_{CU} vs. T_a



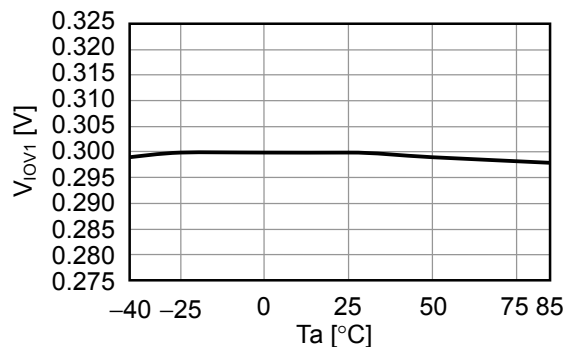
2.6 t_{DL} vs. T_a



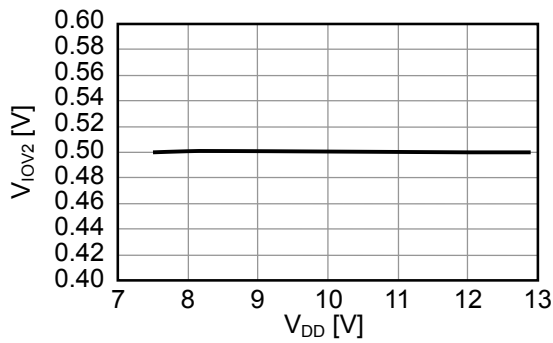
2.7 V_{IOV1} vs. V_{DD}



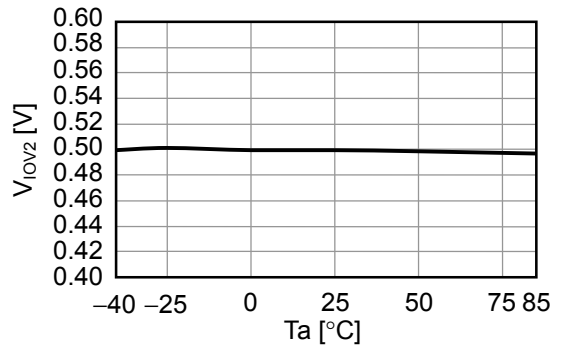
2.8 V_{IOV1} vs. T_a



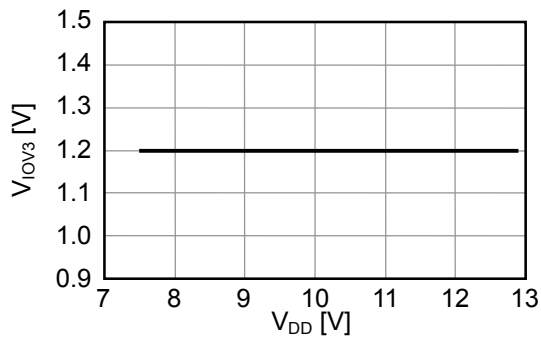
2. 9 V_{IOV2} vs. V_{DD}



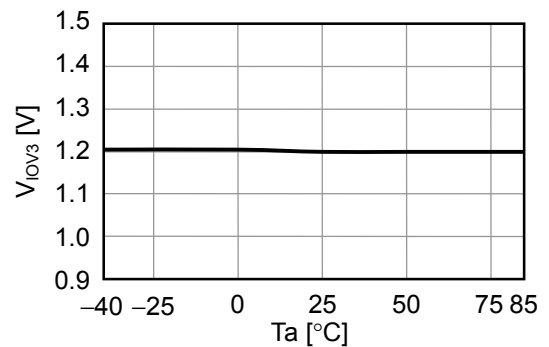
2. 10 V_{IOV2} vs. T_a



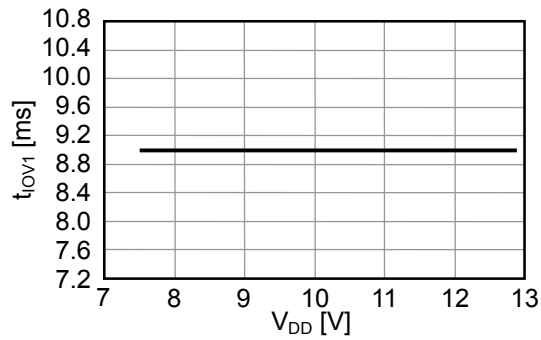
2. 11 V_{IOV3} vs. V_{DD}



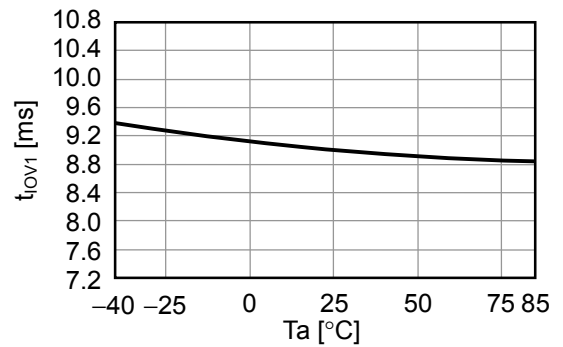
2. 12 V_{IOV3} vs. T_a



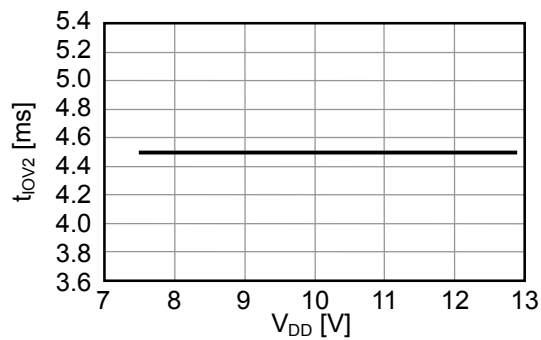
2. 13 t_{IOV1} vs. V_{DD}



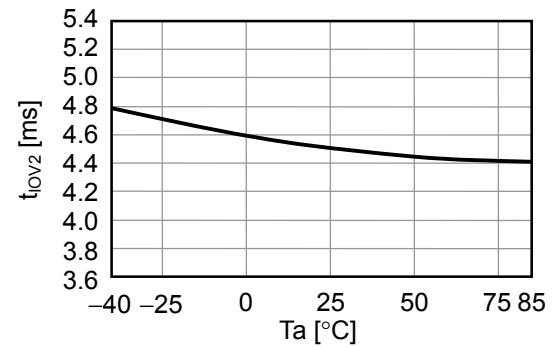
2. 14 t_{IOV1} vs. T_a



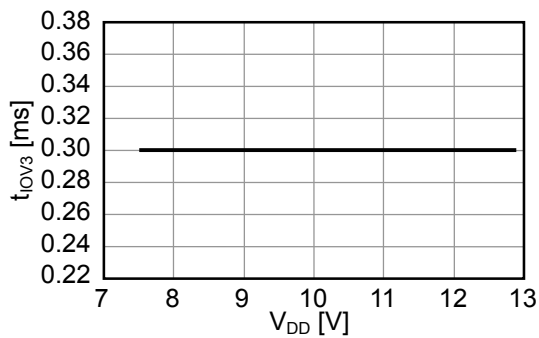
2. 15 t_{IOV2} vs. V_{DD}



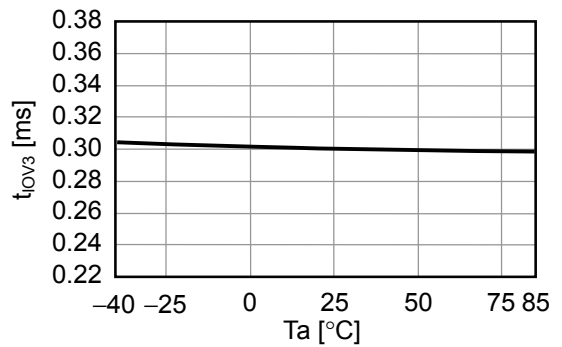
2. 16 t_{IOV2} vs. T_a



2. 17 t_{IOV3} vs. V_{DD}

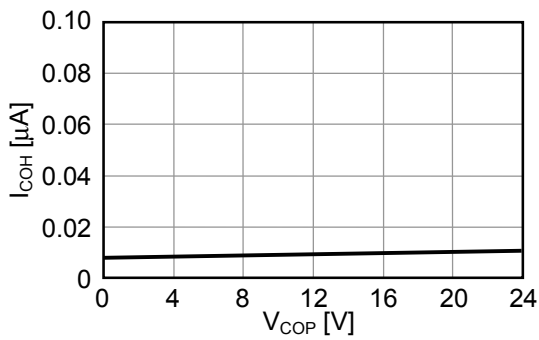


2. 18 t_{IOV3} vs. T_a

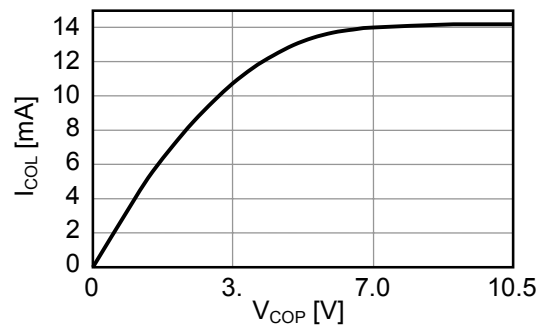


3. COP / DOP Pin (S-8253AAA, S-8253BAA)

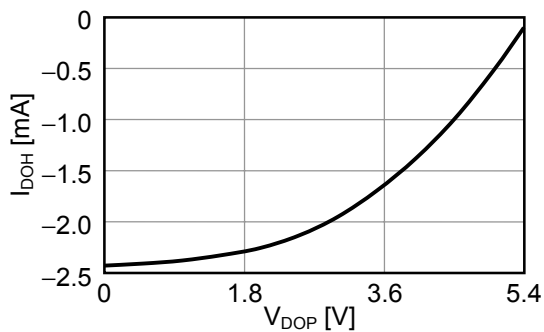
3. 1 I_{COH} vs. V_{COP}



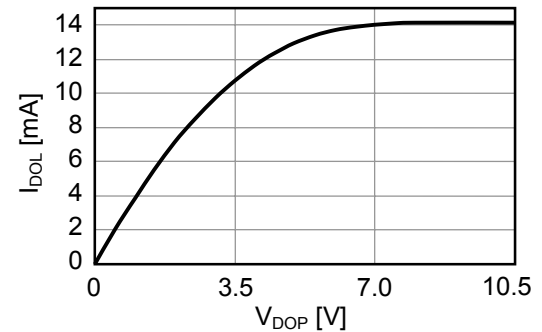
3. 2 I_{COL} vs. V_{COP}

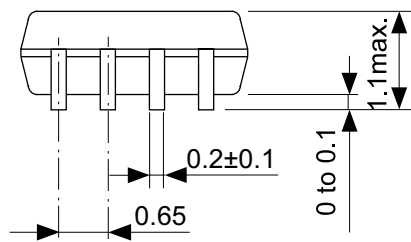
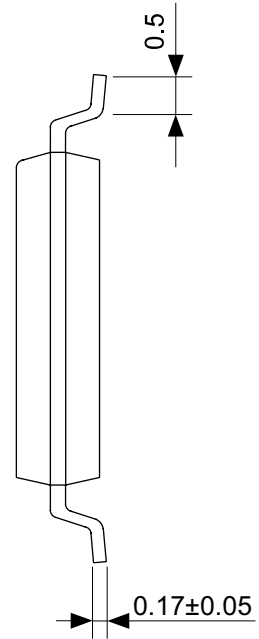
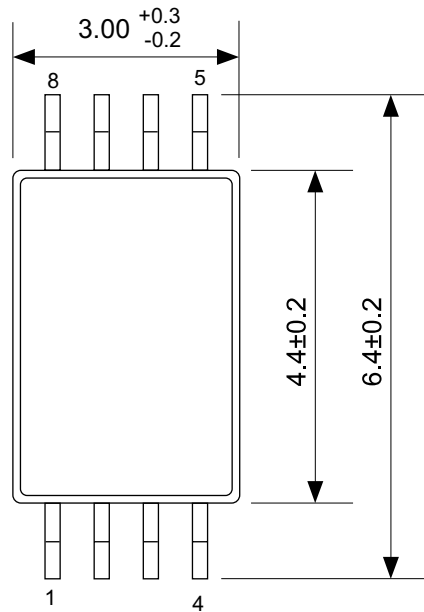


3. 3 I_{DOH} vs. V_{DOP}



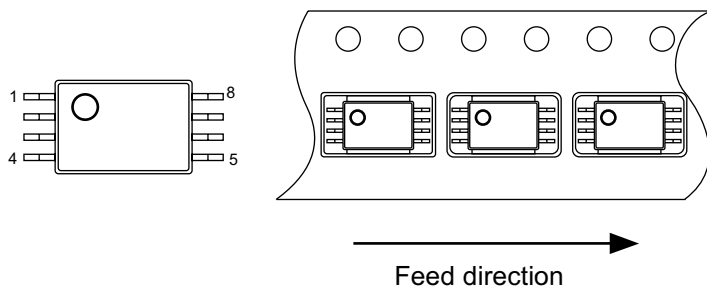
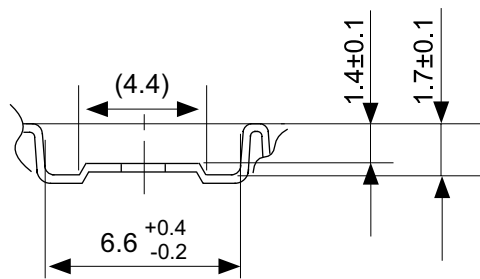
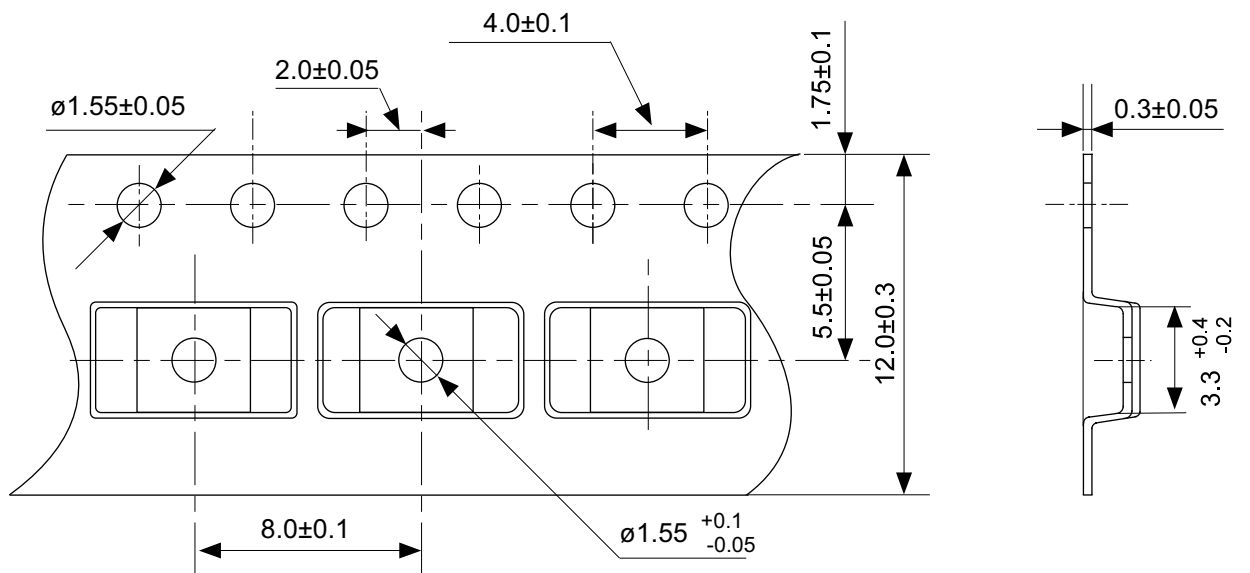
3. 4 I_{DOL} vs. V_{DOP}





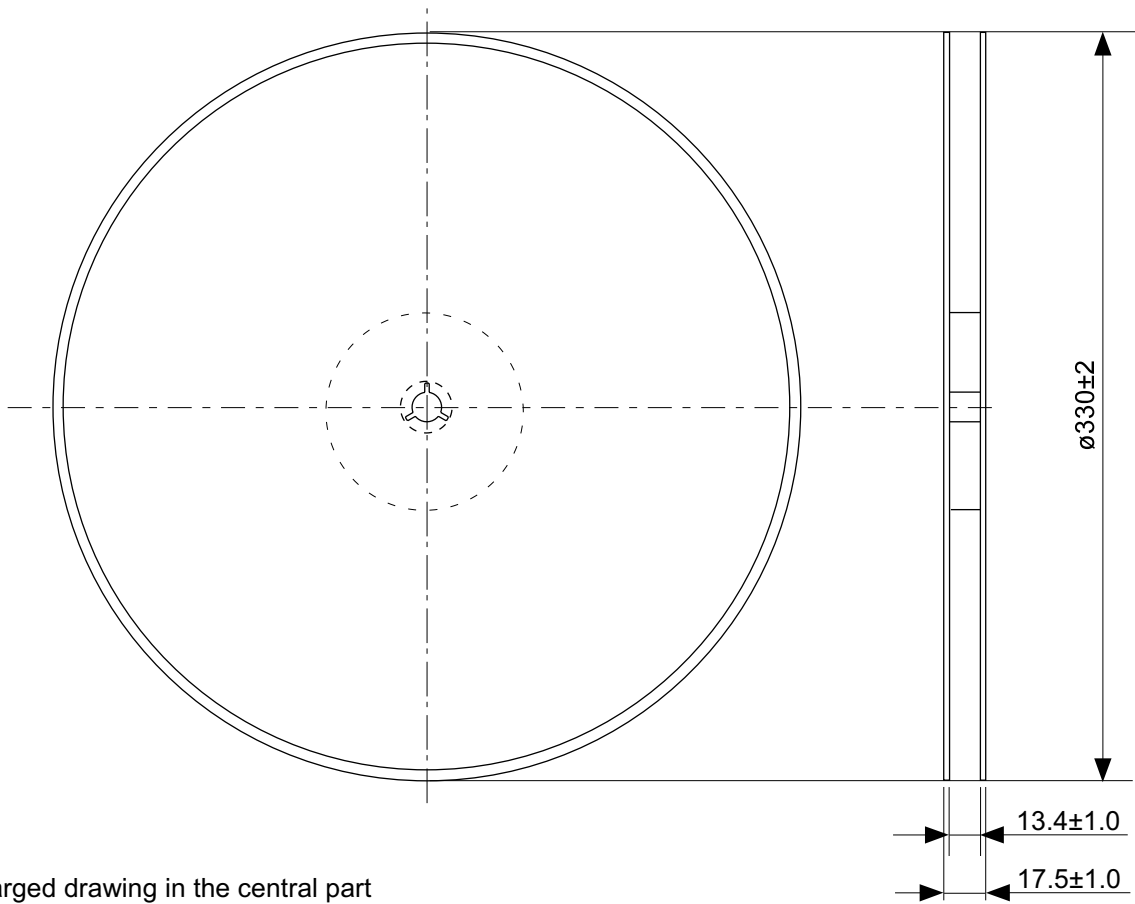
No. FT008-A-P-SD-1.1

TITLE	TSSOP8-E-PKG Dimensions
No.	FT008-A-P-SD-1.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	

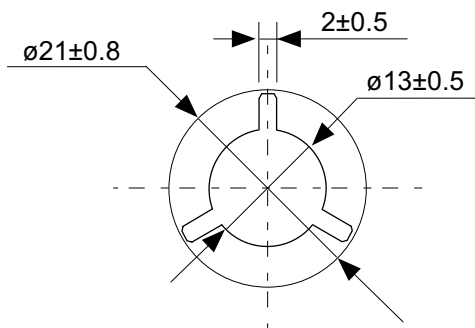


No. FT008-E-C-SD-1.0

TITLE	TSSOP8-E-Carrier Tape
No.	FT008-E-C-SD-1.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	



Enlarged drawing in the central part



No. FT008-E-R-SD-1.0

TITLE	TSSOP8-E-Reel		
No.	FT008-E-R-SD-1.0		
SCALE		QTY.	3,000
UNIT	mm		
Seiko Instruments Inc.			

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