AL460
Full HD FIFO Memory
Datasheet - Brief

Version 1.2

Doc Number: 1-D-PMK262-0001

Amendments

Revise Date	Contents	Page
2008.07.01	Preliminary version 0.01	
2009.06.04	Revised Reference design schematic: XIN = 14.31818 MHz; CSEL[1:0] = VDD33	8
2009.08.06	Revised Pin definitions: Pin 98 = ROINV; Pin 99 =ROEN.	7
2010.03.12	Update DC and AC Characteristics	10
2010.09.30	Correct Pin Description (ROEN, ROINV)	7

Disclaimer

Table of Contents

1 GENERAL DESCRIPTION

The AL460 consists of 128-Mbits of memory density and can be configured as an 8M x 16-bit FIFO (first in first out) at maximum R/W operating speed of 150 MHz. The full HD FIFO can be used in a wide range of applications such as multimedia, video capture systems and many other varieties of video data buffering applications. The size and high-speed data access allow full HD video frame capture up to 1080p resolutions.

The AverLogic AL460 FIFO memory provides completely independent input and output ports. The built-in address and pointer control circuits provide a straightforward bus interface to sequentially read/write memory that can reduce inter-chip design efforts.

The AL460 uses high performance process technologies with extended controller functions (write mask, read skip etc.); it allows easy operation of non-linearity FIFO read/write for use in broadcasting systems, security systems, cameras and many other applications.

The AL460 is designed and manufactured using state-of-the-art technologies with low power consumption AC characteristics (2.5V & 3.3V power supply) facilitating high performance and high quality applications.

The chip is available in LQFP 128-pin with exposed die pad package; the small footprint allows product designers to keep board real estate to a minimum.

2 FEATURES

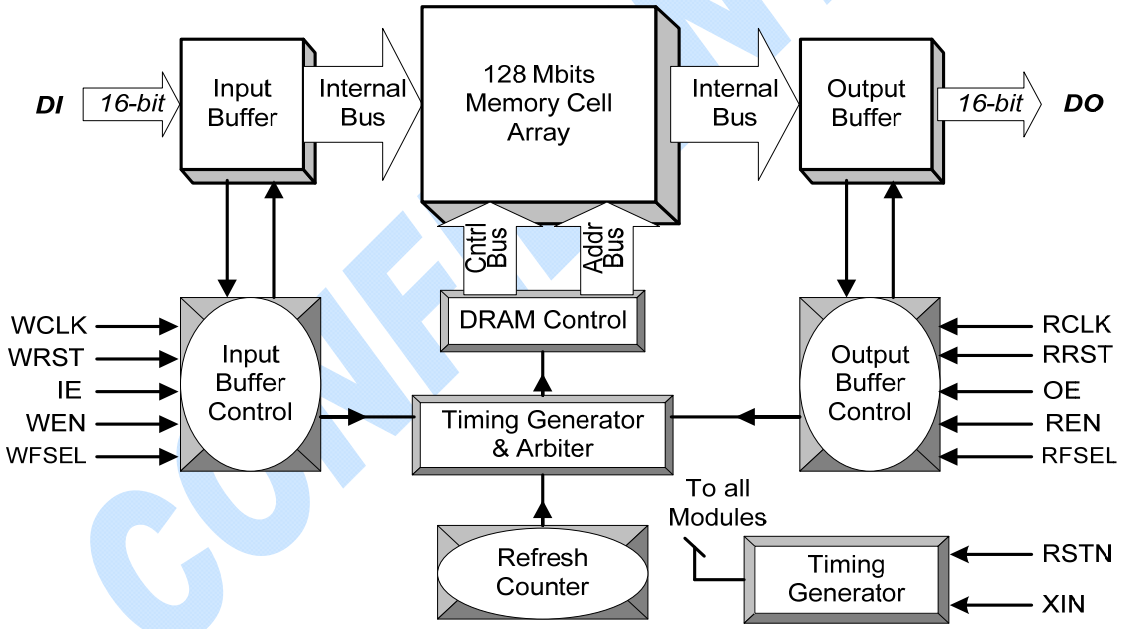
- 128-Mbit density, 8M x 16-bit configuration
- Supports video NTSC, PAL and HDTV up to 1080p resolution
- Independent 16-bit read/write operations (different I/O data rates acceptable) at a maximum speed of 150 MHz
- High speed synchronous sequential access
- Input/Output enable control
- Polarity Selectable
- 2.5V& 3.3V power supply
- Standard 128-pin LQFP with exposed die pad package

3 APPLICATIONS

- HD video capture and editing systems
- Switcher or format converter boxes
- Video capture or editing systems
- Video data buffering for security systems
- Scan rate converters
- TBC (Time Base Correction) systems
- Frame synchronizers
- Digital video cameras
- Hard disk cache memory
- Buffer for communication systems
- 1080p video data stream buffering

4 FUNCTION BLOCK DIAGRAM

The internal structure of each AL460 consists of Input/Output buffers, Write Data Registers, Read Data Registers and main 8M x 16-bit memory cell array and state-of-the-art logic design that takes care of addressing and controlling the read/write data.



AL460 Block Diagram

5 ORDERING INFORMATION

Part number	Speed Grade	Package	Power Supply	Status
AL460A-7-PBF	150 MHz	LQFP-128	+2.5V & +3.3 V	2009
AL460A-13-PBF	75 MHz	LQFP-128	+2.5V & +3.3 V	2009

Note: AverLogic Technologies PB-free products employ special PB-free material sets; molding compounds/die that attach materials and 100% matte tin plate termination finish do not use materials containing PBB, PBDE or red phosphorus for green-product chips. AverLogic's PB-free products are MSL classified at PB-free peak reflow temperatures that meet or exceed the PB-free requirements of IPC/JEDEC J Std-020C."

6 PIN DIAGRAM

6.1 Pin Description

Write Bus Signals

Pin name	Pin number	I/O type	Description
DI[15:0]	58, 56~51, 49~46, 44~41, 39	I	16-bit data inputs; synchronized with the WCLK clock. Data is acquired at the rising edge of WCLK clock.
WEN	37	I	WEN is the write enable signal that controls the 16-bit input data write and write pointer operation
IE	36	I	IE is the data input enable signal that controls the enabling/ disabling of the 16-bit data input pins. The internal write address pointer is always incremented at the rising edge of WCLK by enabling WEN regardless of the IE level.
WCLK	38	I	WCLK is the write clock input pin. The write data input is synchronized with this clock.
WRST	35	I	The WRST is the write rest signal that resets the write address pointer to 0.
WFSEL	34	I	Write Frame select pin in Two Frame Mode (TFEN = H): 0: Frame 0 1: Frame 1

*Note: For the polarity definition of all write control signals (WEN, IE and WRST), please refer to the PLRTY pin definition and “Memory Operation” section for details.

Read Bus Signals

Pin name	Pin number	I/O type	Description
DO[15:0]	102, 104~107, 109~111, 113~115, 117~120, 122	O	16-bit data outputs; synchronized with the RCLK clock. Data is output at the rising edge of the RCLK clock.
REN	125	I	REN is the read enable signal that controls the 16-bit output data read and read pointer operation.
OE	126	I	OE is the data input enable signal that controls the enabling/ disabling of the 16-bit data output pins. The internal read address pointer is always incremented at the rising edge of RCLK by enabling REN regardless of the OE level.
RCLK	124	I	RCLK is the read clock input pin. The read data output is synchronized with this clock.
RCLKO	123	O	RCLK loop-out clock
ROEN	99	I	RCLKO output clock ENABLE, 0: Disable 1: Enable
ROINV	98	I	RCLK loop-out clock inverts control signal, 0: Normal 1: Invert
RRST	127	I	The RRST is the read reset signal that resets the read address pointer to 0.
RFSEL	128	I	Read Frame select pin in Two Frame Mode (TFEN = H): 0: Frame 0 1: Frame 1

*Note: For the polarity definition of all read control signals (REN, OE, RRST,), please refer to PLRTY pin definition and “Memory Operation” section for details.

Power/Ground Signals

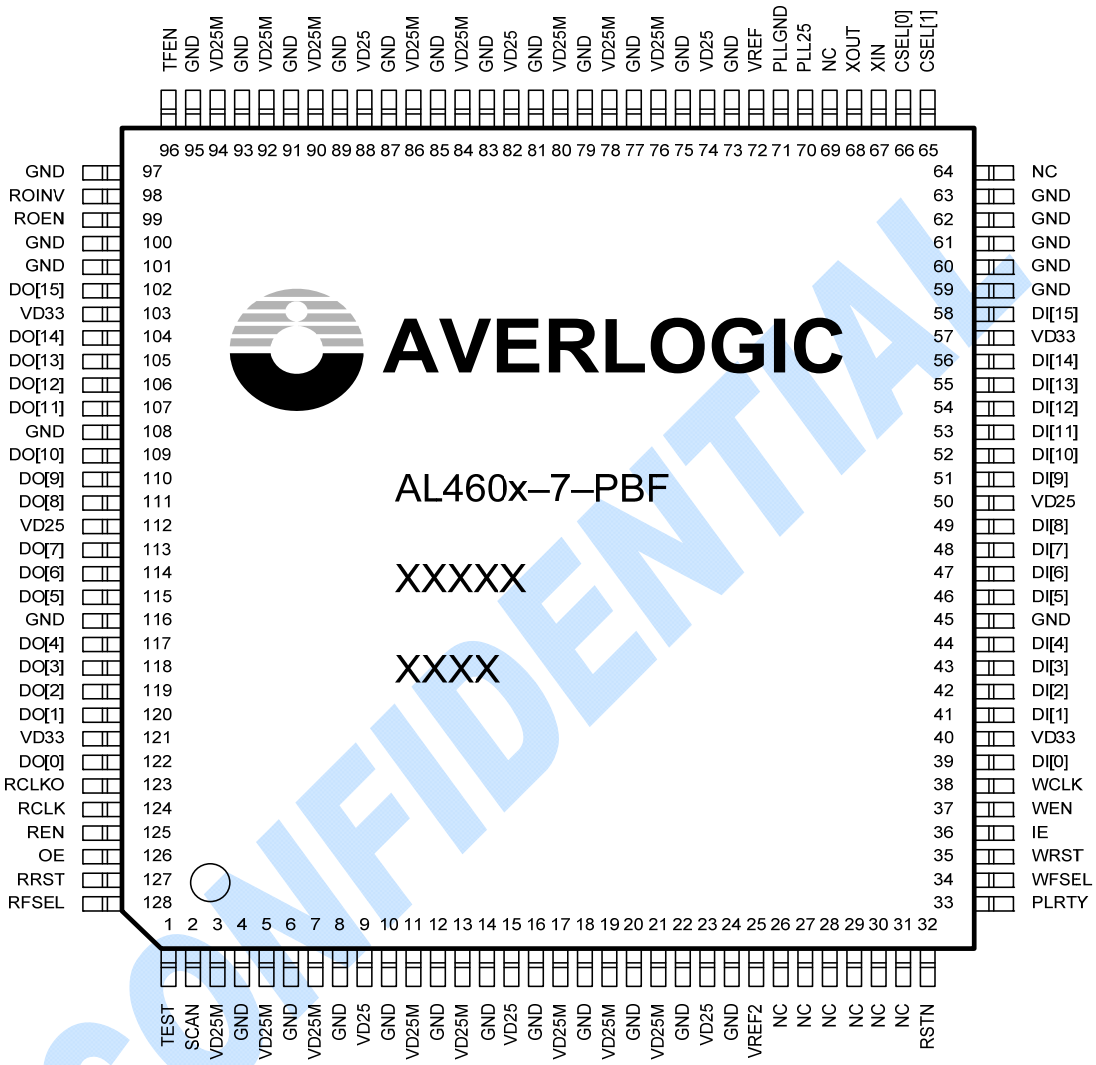
Pin name	Pin number	I/O type	Description
VD25M	3, 5, 7, 11, 13, 17, 19, 21, 76, 78, 80, 84, 86, 90, 92, 94	-	2.5V ± 5% power supply for internal memory
VD25	9, 15, 23, 50, 74, 82, 88, 112	-	2.5V ± 5% power supply for internal control logic
PLL25	70	-	2.5V ± 5% power supply for internal PLL
PLLGND	71	-	PLL GND
VD33	40, 57, 103, 121	-	3.3V ± 10% I/O power supply
GND	4, 6, 8, 10, 12, 14, 16, 18,		GND

	20, 22, 24, 45, 59~63, 73, 75, 77, 79, 81, 83, 85, 87, 89, 91, 93, 95, 97, 100, 101, 108, 116		

Miscellaneous Signals

Pin name	Pin number	I/O type	Description
RSTN	32	I	Global reset (active Low)
PLRTY	33	I	Select active polarity of the control signals including WEN, REN, WRST, RRST, IE, OE, ROEN and ROINV (total of 8 signals) PLRTY = VD33, active low. PLRTY = GND, active high. Note: during memory operation, the pin must be permanently connected to VD33 or GND. If PLRTY level is changed during memory operation, memory data is not guaranteed.
XIN	67	I	Crystal input
XOUT	68	O	Crystal output
CSEL[1:0]	65, 66	I	Crystal input frequency select pins ▪ "00" - 11.059200 MHz ▪ "01" - 20.000000 MHz ▪ "10" - 24.576000 MHz ▪ "11" – 14.318180 MHz * Minimum crystal frequency accuracy: ±100 ppm
VREF	72	AI	Reference voltage input * Please refer to "External decoupling circuit" application note for details
VREF2	25	AI	Reference voltage input 2 * Please refer to "External decoupling circuit" application note for details
TFEN	96	I	Two frame mode enable: ▪ "0" – Standard FIFO Mode ▪ "1" – Two Frame Mode
TEST	1	I	Test pin (pull-down for normal operation)
SCAN	2	I	Scan mode Enable (pull-down for normal operation)
NC	26~31, 64, 69	-	No connect

6.2 Pin Diagram



7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings under Free-Air Temperature

(Excessive ratings are harmful to the lifetime of the product. These are guidelines that are not yet tested.)

Parameter		Rating	Unit
VD33	3.3V I/O Supply Voltage	-0.3 ~ +4.5	V
VD25M	2.5V Memory Voltage	-0.3 ~ +3.4	V
VD25	2.5V Core Voltage	-0.3 ~ +3.4	V
PLL25	2.5V PLL Voltage	-0.3 ~ +3.4	V
V_P	Pin Voltage	-0.3 ~ +(VD33 + 0.3)	V
I_O	Output Current	-20 ~ +20	mA
T_{AMB}	Ambient Op. Temperature	0 ~ +70	°C
T_{stg}	Storage temperature	-40 ~ +125	°C

7.2 Recommended Operating Conditions

Parameter		Min	Typ	Max	Unit
VD33	3.3V I/O Supply Voltage	3.0	3.3	3.6	V
VD25M	2.5V Memory Voltage	2.37	2.5	2.63	V
VD25	2.5V Core Voltage	2.37	2.5	2.63	V
PLL25	2.5V PLL Voltage	2.37	2.5	2.63	V
V_{IH}	High Level Input Voltage	0.7VD33	-	VD33	V
V_{IL}	Low Level Input Voltage	0	-	0.3VD33	V

7.3 DC Characteristics

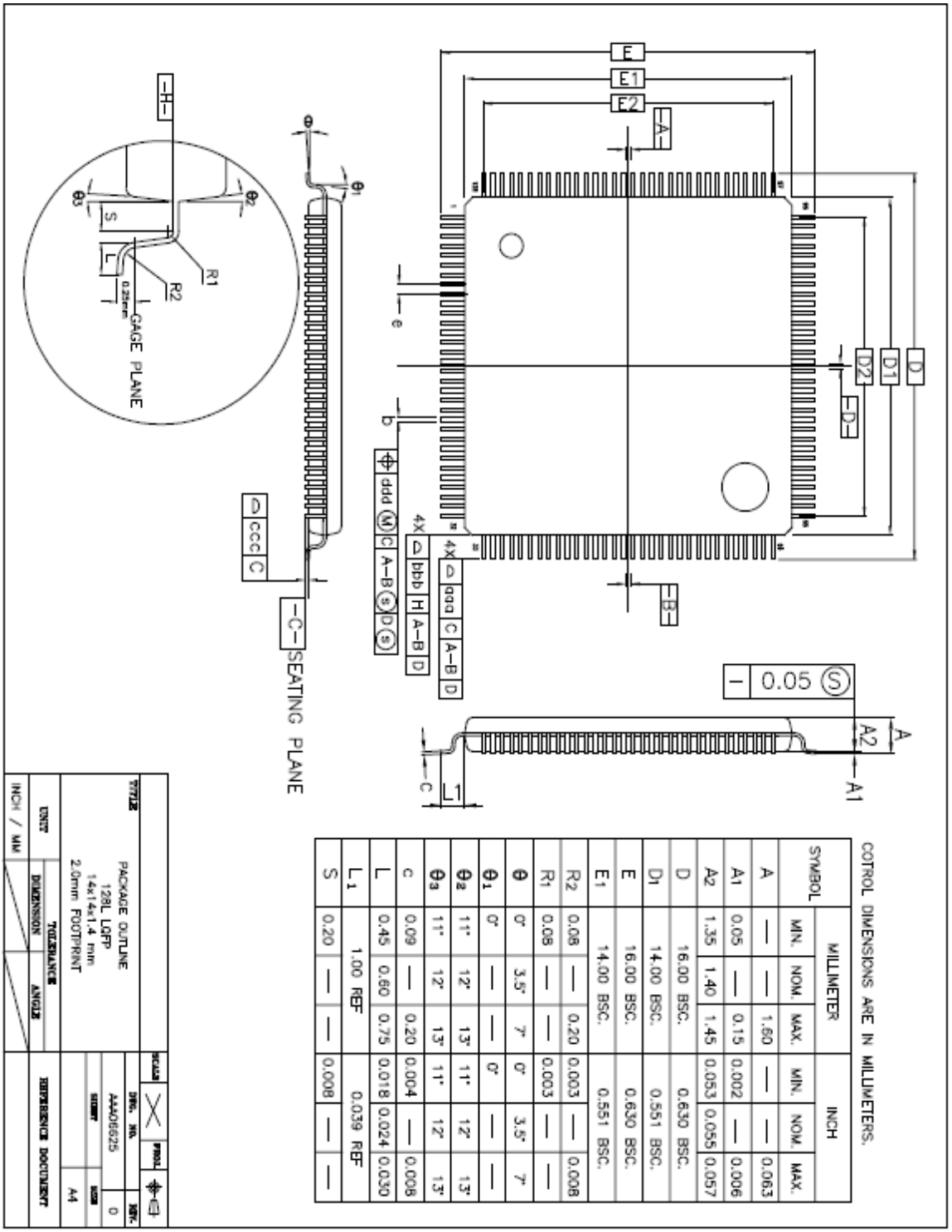
(VD33 = 3.3V, VD25M = VD25 = PLL25 = 2.5V; T_{AMB} = 0 to 70°C)

Parameter		Min	Typ	Max	Unit
I_{DD33}	Operating Current		100		mA
I_{DD25}	Operating Current		185		mA
I_{DD25M}	Operating Current		78		mA

* Operating condition: WCLK = RCLK = 150 MHz; Data toggle rate = 20 MHz					
I_{DD33}	Operating Current		62		mA
I_{DD25}	Operating Current		125		mA
I_{DD25M}	Operating Current		55		mA
* Operating condition: WCLK = RCLK = 75 MHz; Data toggle rate = 20 MHz					
I_{SB33}	Standby Current		4		mA
I_{SB25}	Standby Current		80		mA
I_{SB25M}	Standby Current		25		mA
* Standby condition: WCLK = RCLK = 0 MHz					
V_{OH}	Hi-level Output Voltage	VD33-0.4			V
V_{OL}	Lo-level Output Voltage			0.4	V
I_{LI}	Input Leakage Current (No pull-up or pull-down)	-10		+10	μA
I_{LO}	Output Leakage Current (No pull-up or pull-down)	-10		+10	μA
R_L	Input Pull-up/Pull-down Resistance		60		KΩ

8 Mechanical Drawing – 128-PIN LQFP

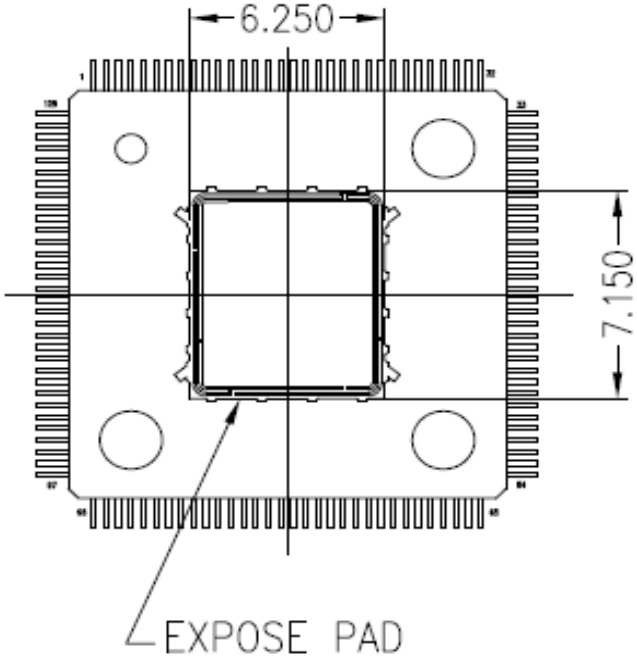
8.1 14x14x1.4mm 128-Pin LQFP Package



CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	16.00 BSC.			0.630 BSC.		
D1	14.00 BSC.			0.551 BSC.		
E	16.00 BSC.			0.630 BSC.		
E1	14.00 BSC.			0.551 BSC.		
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—

UNIT	TOLERANCE	PACKAGE OUTLINE 128L LQFP 14x14x1.4 mm 2.0mm FOOTPRINT	SCALE: X
INCH / MM	DIMENSION: ANGLE:		DWG. NO.: AAA08625 REV.: 0 SHEET: A4
			REFERENCE DOCUMENT



SYMBOL	128L					
	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.016 BSC.		
D2	12.40			0.488		
E2	12.40			0.488		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003		

NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUN PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.
   DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm FOR 0.4mm and 0.5mm PITCH PACKAGES.
3. ALL DIMENSION OF 128L WERE BASE ON THOSE OF 120L SINCE THEY ARE NOT MENTIONED IN JEDEC SPEC MS-026.

TITLE: PACKAGE OUTLINE 128L LQFP 14x14x1.4 mm 2.0mm FOOTPRINT		SCALE:	PROJ.
		DWG. NO.: AAA06825	REV.: 0
		SHEET:	SIZE: A4
UNIT: INCH / MM	TOLERANCE: DIMENSION / ANGLE	REFERENCE DOCUMENT	

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