

Two-Phase Interleaved CCM PFC Controller

FEATURES

- Interleaved Average Current-Mode PWM Control with Inherent Current Matching
- Advanced Current Synthesizer Current Sensing for Superior Efficiency and PF
- Highly-Linear Multiplier Output with Internal Quantized Voltage Feed-Forward Correction for Near-Unity PF
- Programmable Frequency (up to 300 kHz)
- Programmable Maximum Duty-Cycle Clamp
- Programmable Frequency Dithering Rate and Magnitude for Enhanced EMI Reduction
 - Magnitude: Up to 30 kHz
 - Rate: Up to 30 kHz
- External Clock Synchronization Capability
- Enhanced Load and Line Transient Response through Voltage Amplifier Output Slew-Rate Correction
- Programmable Peak Current Limiting
- Bias-Supply UVLO, Over-Voltage Protection, Open-Loop Detection, and PFC-Enable Monitoring
- External PFC-Disable Interface
- Open-Circuit Protection on VSENSE and VINAC pins
- Programmable Soft Start
- 20-Lead TSSOP Package

APPLICATIONS

- High-Efficiency Server and Desktop Power Supplies
- Telecom Rectifiers

DESCRIPTION

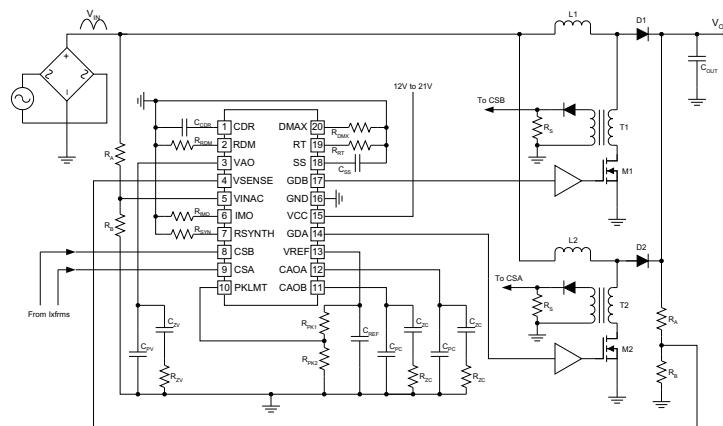
The UCC28070 is an advanced power factor correction device that integrates two pulse-width modulators (PWMs) operating 180° out of phase. This Natural Interleaved PWM operation generates substantial reduction in the input and output ripple currents, and the conducted-EMI filtering becomes easier and less expensive. A significantly improved multiplier design provides a shared current reference to two independent current amplifiers that ensures matched average current mode control in both PWM outputs while maintaining a stable, low-distortion sinusoidal input line current.

The UCC28070 contains multiple innovations including current synthesis and quantized voltage feed-forward to promote performance enhancements in PF, efficiency, THD, and transient response. Features including frequency dithering, clock synchronization, and slew rate enhancement further expand the potential performance enhancements.

The UCC28070 also contains a variety of protection features including output over-voltage detection, programmable peak-current limit, in-rush current detection, under-voltage lockout, and open-loop protection.

PRODUCT PREVIEW

Typical Application Diagram



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ORDERING INFORMATION

PART NUMBER	PACKAGE	PACKING
UCC28070PW	Plastic, 20-Pin TSSOP (PW)	70-Pc. Tube
UCC28070PWR	Plastic, 20-Pin TSSOP (PW)	2000-Pc. Tape and Reel

ABSOLUTE MAXIMUM RATINGS⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾

over operating free-air temperature range (unless otherwise noted)

PARAMETER	LIMIT	UNIT
Supply voltage: VCC	22	V
Supply current: I _{VCC}	20	mA
Voltage: GDA, GDB	-0.5 to VCC+0.3	V
Gate drive current – continuous: GDA, GDB	+/- 0.25	A
Gate drive current – pulsed: GDA, GDB	+/- 0.75	
Voltage: DMAX, RDM, RT, CDR, VINAC, VSENSE, SS, VAO, IMO, CSA, CSB, CAO, CAOB, PKLMT, VREF	-0.5 to +7	V
Current: RT, DMAX, RDM, RSYNTH	-0.5	mA
Current: VREF, VAO, CAO, CAOB, IMO	10	
Operating junction temperature, T _J	-40 to +125	°C
Storage temperature, T _{STG}	-65 to +150	
Lead temperature (10 seconds)	260	

- (1) These are stress limits. Stress beyond these limits may cause permanent damage to the device. Functional operation of the device at these or any conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS is not implied. Exposure to absolute maximum rated conditions for extended periods of time may affect device reliability.
- (2) All voltages are with respect to GND.
- (3) All currents are positive into the terminal, negative out of the terminal.
- (4) In normal use, terminals GDA and GDB are connected to an external gate driver and are internally limited in output current.

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

	RATING	UNIT
Human Body Model (HBM)	2,000	V
Charged Device Model (CDM)	500	

DISSIPATION RATINGS

PACKAGE	THERMAL IMPEDANCE JUNCTION-TO-AMBIENT	T _A = 25°C POWER RATING	T _A = 85°C POWER RATING
20-Pin TSSOP	125 °C/Watt ⁽¹⁾ and ⁽²⁾	800 mW ⁽¹⁾	320 mW ⁽¹⁾

- (1) Thermal resistance is a strong function of board construction and layout. Air flow reduces thermal resistance. This number is only a general guide.
- (2) Thermal resistance calculated with a low-K methodology.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	MIN	MAX	UNIT
VCC Input Voltage (from a low-impedance source)	V _{UVLO} + 1 V	21	V
VREF Load Current		2	mA
VINAC Input Voltage Range	0	3	V
IMO Voltage Range	0	3.3	
PKLMT, CSA, & CSB Voltage Range	0	3.7	
RSYNTH Resistance (R _{SYN})	15	750	kΩ
RDM Resistance (R _{RDM})	30	330	

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range $-40^{\circ}\text{C} < T_A < 125^{\circ}\text{C}$, $T_J = T_A$, $V_{CC} = 12\text{ V}$, $GND = 0\text{ V}$, $R_{RT} = 75\text{ k}\Omega$, $R_{DMX} = 67.5\text{ k}\Omega$, $R_{RDM} = R_{SYN} = 100\text{ k}\Omega$, $R_{IMO} = 16\text{ k}\Omega$, $C_{CDR} = 625\text{ pF}$, $C_{SS} = C_{VREF} = 0.1\text{ }\mu\text{F}$, $C_{VCC} = 1\text{ }\mu\text{F}$, (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Bias Supply						
$V_{CC\text{SHUNT}}$	VCC shunt voltage ⁽¹⁾	$I_{VCC} = 10\text{ mA}$	21	23	25	V
	VCC current, disabled	$V_{SENSE} = 0\text{ V}$		7		mA
	VCC current, enabled	$V_{SENSE} = 3\text{ V}$ (no switching)		8	TBD	
	VCC current, UVLO	$V_{CC} = 7\text{ V}$			100	μA
		$V_{CC} = 9\text{ V}$		4	TBD	mA
V_{UVLO}	UVLO turn-on threshold	Measured at VCC (rising)	9.8	10.2	10.6	V
	UVLO hysteresis	Measured at VCC (falling)		1		
	VREF enable threshold	Measured at VCC (rising)	TBD	8	TBD	
Linear Regulator						
	VREF voltage, no load	$I_{VREF} = 0\text{ mA}$	5.9	6	6.1	V
	VREF voltage, full load	$I_{VREF} = -2\text{ mA}$	5.8	6	6.1	
	VREF voltage, over line	$11\text{ V} < V_{CC} < 20\text{ V}$, $I_{REF} = 0\text{ mA}$	5.9	6	6.1	
PFC Enable						
V_{EN}	Enable threshold	Measured at VSENSE (rising)	0.65	0.75	0.85	V
	Enable hysteresis			0.15		
External PFC Disable						
	Disable threshold	Measured at SS (falling)	TBD	0.6		V
	Hysteresis	$V_{SENSE} > 0.85\text{ V}$		0.15		
Oscillator						
	Output phase shift	Measured between GDA and GDB	TBD	180	TBD	Degree
$V_{D\text{MAX}}$, V_{RT} , and V_{RDM}	Timing regulation voltages	Measured at DMAX, RT, & RDM		3		V
f_{PWM}	PWM switching frequency	$R_{RT} = 250\text{ k}\Omega$, $R_{DMX} = 225\text{ k}\Omega$, $V_{RDM} = 0\text{ V}$, $V_{CDR} = 6\text{ V}$	27	30	33	kHz
		$R_{RT} = 25\text{ k}\Omega$, $R_{DMX} = 22.5\text{ k}\Omega$, $V_{RDM} = 0\text{ V}$, $V_{CDR} = 6\text{ V}$	270	300	330	
D_{MAX}	Duty-cycle clamp	$R_{RT} = 75\text{ k}\Omega$, $R_{DMX} = 67.5\text{ k}\Omega$, $V_{RDM} = 0\text{ V}$, $V_{CDR} = 6\text{ V}$	TBD%	95%	TBD%	
	Minimum programmable off-time	$R_{RT} = 25\text{ k}\Omega$, $R_{DMX} = 22.5\text{ k}\Omega$, $V_{RDM} = 0\text{ V}$, $V_{CDR} = 6\text{ V}$	TBD	133	TBD	ns
f_{DM}	Frequency dithering magnitude	$R_{RDM} = 313\text{ k}\Omega$, $R_{RT} = 75\text{ k}\Omega$	2.5	3	3.5	kHz
	Change in f_{PWM}	$R_{RDM} = 31\text{ k}\Omega$, $R_{RT} = 25\text{ k}\Omega$	27	30	33	
f_{DR}	Frequency dithering rate	$C_{CDR} = 2.2\text{ nF}$, $R_{RDM} = 100\text{ k}\Omega$		3		
	Rate of change in f_{PWM}	$C_{CDR} = 0.22\text{ nF}$, $R_{RDM} = 100\text{ k}\Omega$		30		
I_{CDR}	Dither rate current	Measure at CDR (sink and source)		10		μA
	Dither disable threshold	Measured at C_{CDR} (rising)		5	TBD	V

(1) Excessive VCC input voltage and/or current damages the device. This clamp will not protect the device from an unregulated supply. If an unregulated supply is used, a series-connected fixed positive voltage regulator such as a UA78L15A is recommended. See the Absolute Maximum Ratings section for the limits on VCC voltage and current.

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range $-40^{\circ}\text{C} < T_A < 125^{\circ}\text{C}$, $T_J = T_A$, $V_{CC} = 12\text{ V}$, $GND = 0\text{ V}$, $R_{RT} = 75\text{ k}\Omega$, $R_{DMX} = 67.5\text{ k}\Omega$, $R_{RDM} = R_{SYN} = 100\text{ k}\Omega$, $R_{IMO} = 16\text{ k}\Omega$, $C_{CDR} = 625\text{ pF}$, $C_{SS} = C_{VREF} = 0.1\text{ }\mu\text{F}$, $C_{VCC} = 1\text{ }\mu\text{F}$, (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Clock Synchronization						
V_{CDR}	SYNC enable threshold	Measured at CDR (rising)		5	TBD	V
	SYNC propagation delay	$V_{CDR} = 6\text{ V}$, Measured from RDM (rising) to GDx (rising)		50	TBD	ns
	SYNC threshold (Rising)	$V_{CDR} = 6\text{ V}$, Measured at RDM (rising)		1.2	1.5	V
	SYNC threshold (Falling)	$V_{CDR} = 6\text{ V}$, Measured at RDM (falling)	0.4	0.7		
	SYNC pulses	Positive pulse width	0.2			μs
		Maximum duty cycle ⁽²⁾		75		%
Voltage Amplifier						
	VSENSE voltage	In regulation, $T_A = 25^{\circ}\text{C}$	2.97	3	3.03	V
	VSENSE voltage	In regulation	2.94	3	3.06	
	VSENSE input bias current	In regulation		250	TBD	nA
	VAO high voltage	$V_{SENSE} = 2.9\text{ V}$	4.8	5	5.2	V
	VAO low voltage	$V_{SENSE} = 3.1\text{ V}$		0.05	TBD	
g_{MV}	VAO transconductance	$2.8\text{ V} < V_{SENSE} < 3.2\text{ V}$, $VAO = 3\text{ V}$		70		μS
	VAO sink current, overdriven limit	$V_{SENSE} = 3.5\text{ V}$, $VAO = 3\text{ V}$		30		μA
	VAO source current, overdriven	$V_{SENSE} = 2.5\text{ V}$, $VAO = 3\text{ V}$, $SS = 3\text{ V}$		-30		
	VAO source current, overdriven limit + I_{SRC}	$V_{SENSE} = 2.5\text{ V}$, $VAO = 3\text{ V}$		-130		
	Slew-rate correction threshold	Measured as V_{SENSE} (falling) / V_{SENSE} (regulation)	92	93	95	%
	Slew-rate correction hysteresis	Measured at V_{SENSE} (rising)		6	TBD	mV
I_{SRC}	Slew-rate correction current	Measured at VAO, in addition to VAO source current.		-100		μA
	Slew-rate correction enable threshold	Measured at SS (rising)		4		V
	VAO discharge current	$V_{SENSE} = 0.5\text{ V}$, $VAO = 1\text{ V}$		10		μA
Soft Start						
I_{SS}	SS source current	$V_{SENSE} = 0.9\text{ V}$, $SS = 1\text{ V}$		-10		μA
	Adaptive source current	$V_{SENSE} = 1.1\text{ V}$, $SS = 1\text{ V}$		-1		mA
	Adaptive SS disable	Measured as $V_{SENSE} - SS$		0		mV
	SS sink current	$V_{SENSE} = 0.5\text{ V}$, $SS = 0.2\text{ V}$	0.5	0.9		mA

(2) Due to the programmability of the maximum PWM switching duty cycle (D_{MAX}), the maximum duty cycle of a synchronization pulse must be reasonably (~5-10%) less than $2 \times D_{MAX} - 1$.

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range $-40^{\circ}\text{C} < T_A < 125^{\circ}\text{C}$, $T_J = T_A$, $V_{CC} = 12\text{ V}$, $GND = 0\text{ V}$, $R_{RT} = 75\text{ k}\Omega$, $R_{DMX} = 67.5\text{ k}\Omega$, $R_{RDM} = R_{SYN} = 100\text{ k}\Omega$, $R_{IMO} = 16\text{ k}\Omega$, $C_{CDR} = 625\text{ pF}$, $C_{SS} = C_{VREF} = 0.1\text{ }\mu\text{F}$, $C_{VCC} = 1\text{ }\mu\text{F}$, (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Over Voltage						
V_{OVP}	OVP threshold	Measured as VSENSE (rising) / VSENSE (regulation)	104	106	108	%
	OVP hysteresis	Measured at VSENSE (falling)		100		mV
	OVP propagation delay	Measured between VSENSE (rising) and GDx (falling)		TBD	0.5	μs
Zero-Power						
V_{ZPWR}	Zero-power detect threshold	Measured at VAO (falling)	TBD	0.75		V
	Zero-power hysteresis			0.15		
Multiplier						
k_{MULT}	Gain constant	$VAO > 1.5\text{ V}$	16	17	18	μA
		$VAO = 1.2\text{ V}$	15	17	19	
I_{IMO}	Output current: zero	$VINAC = 0.9 V_{PK}$, $VAO = 0.8\text{ V}$	-0.2	0	0.2	μA
		$VINAC = 0\text{ V}$, $VAO = 5\text{ V}$	-0.2	0	0.2	
Quantized Voltage Feed Forward						
V_{LVL1}	Level 1 threshold ⁽³⁾	Measured at VINAC (rising)	0.6	0.7	0.8	V
V_{LVL2}	Level 2 threshold			1		
V_{LVL3}	Level 3 threshold			1.2		
V_{LVL4}	Level 4 threshold			1.4		
V_{LVL5}	Level 5 threshold			1.65		
V_{LVL6}	Level 6 threshold			1.95		
V_{LVL7}	Level 7 threshold			2.25		
V_{LVL8}	Level 8 threshold			2.6		
Current Amplifiers						
	CAOx high voltage		TBD	6		V
	CAOx low voltage			TBD	0.1	
g_{MC}	CAOx transconductance			100		μS
	CAOx sink current, overdriven			50		μA
	CAOx source current, overdriven			-50		
	Input common mode range		0		3.6	V
	Input offset voltage	$IMO = 0\text{ V}$	-1	-3	-5	mV
	Phase mismatch	Measured as Phase A's input offset minus Phase B's input offset	TBD	0	TBD	
	CAOx pull-down current	$VSENSE = 0.5\text{ V}$, $CAOx = 0.2\text{ V}$	0.5	0.9		mA

(3) The Level 1 threshold represents the “zero-crossing detection” threshold above which VINAC must rise to initiate a new input half-cycle, and below which VINAC must fall to terminate that half-cycle.

ELECTRICAL CHARACTERISTICS (continued)

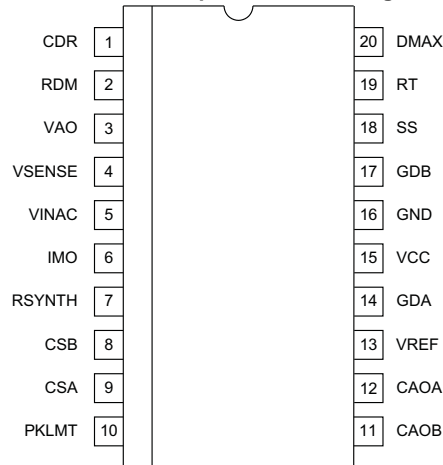
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SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Synthesizer						
V_{RSYNTH}	Regulation voltage	$V_{SENSE} = 3\text{ V}$, $V_{INAC} = 0\text{ V}$		3		V
		$V_{SENSE} = 3\text{ V}$, $V_{INAC} = 2.85\text{ V}$		0.15		
	Synthesizer disable threshold	Measured at R_{SYNTH} (rising)		5	TBD	
	VINAC input bias current			250	TBD	nA
Peak Current Limit						
	Peak current limit threshold	$PKLMT = 3.30\text{ V}$, measured at CSx (rising)	3.27	3.3	3.33	V
	Peak current limit propagation delay	Measured between CSx (rising) and GDx (falling) edges		TBD	100	ns
PWM Ramp						
V_{RMP}	PWM ramp amplitude			4		V
	PWM ramp offset voltage	$T_A = 25^{\circ}\text{C}$, $R_{RT} = 75\text{ k}\Omega$	TBD	0.7	TBD	
	PWM ramp offset temperature coefficient			-2		mV/ $^{\circ}\text{C}$
In-Rush Current Detection						
	In-rush detection threshold	Measured as $V_{SENSE} - V_{INAC}$		0		mV
	In-rush detection hyst.			20		
Gate Drive						
	GDA, GDB output voltage, high, clamped	$V_{CC} = 20\text{ V}$, $C_{LOAD} = 1\text{ nF}$	11.5	13	15	V
	GDA, GDB output voltage, High	$C_{LOAD} = 1\text{ nF}$	10	10.5	11.5	
	GDA, GDB output voltage, Low	$C_{LOAD} = 1\text{ nF}$		0.2	0.3	
	Rise time GDx	1 V to 9 V, $C_{LOAD} = 1\text{ nF}$		18	30	ns
	Fall time GDx	9 V to 1 V, $C_{LOAD} = 1\text{ nF}$		12	25	
	GDA, GDB output voltage, UVLO	$V_{CC} = 0\text{ V}$, I_{GDA} , $I_{GDB} = 2.5\text{ mA}$		1.6	2	V
Thermal Shutdown						
	Thermal shutdown threshold			160		$^{\circ}\text{C}$
	Thermal shutdown recovery			140		

PRODUCT PREVIEW

DEVICE INFORMATION

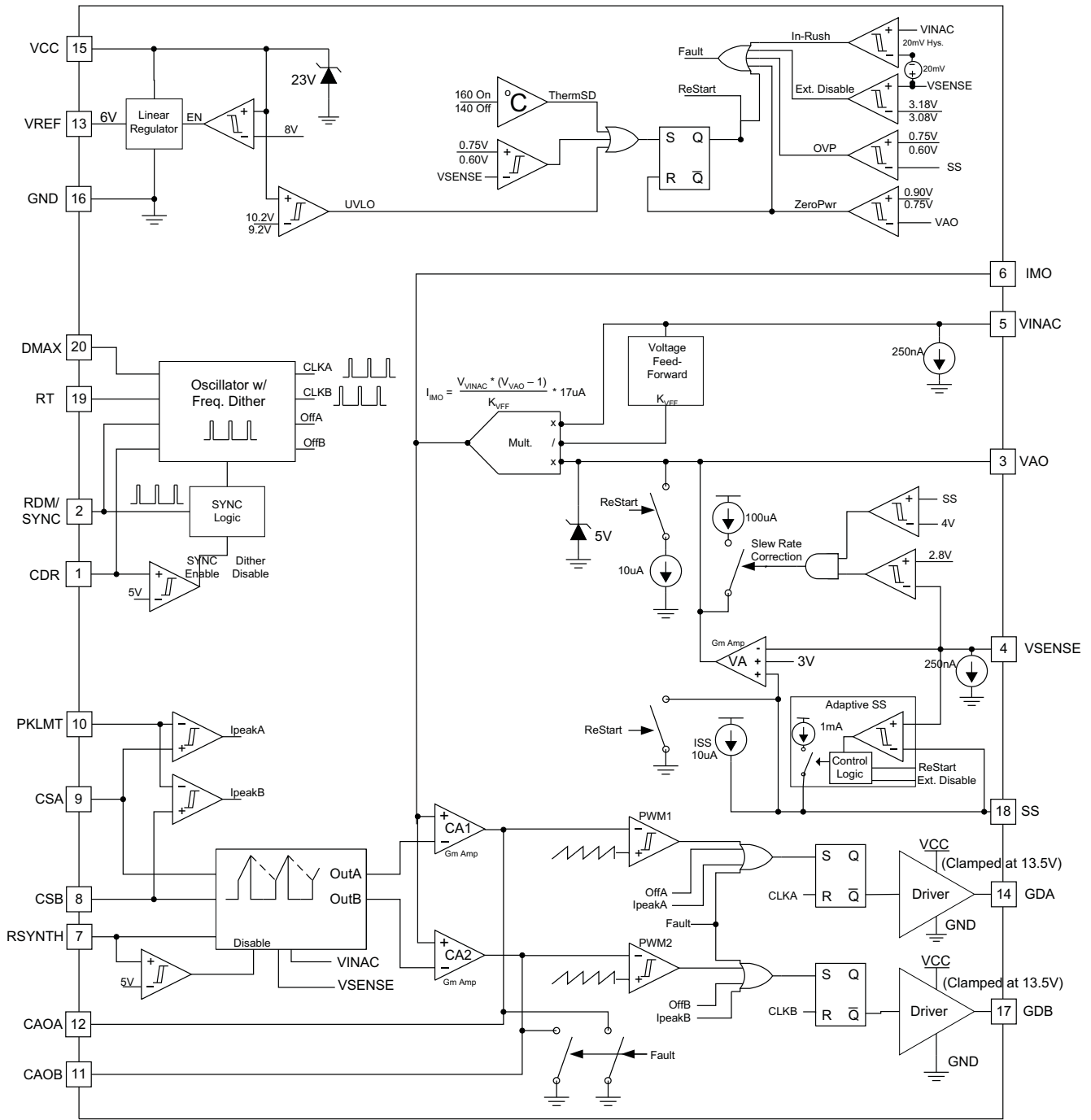
TSSOP-20 Top View, PW Package



TERMINAL FUNCTIONS

NAME	PIN #	I/O	DESCRIPTION
CDR	1	I	Dither Rate Capacitor. Frequency-dithering timing pin. An external capacitor to GND programs the rate of oscillator dither. Connect the CDR pin to the VREF pin to disable dithering.
RDM (SYNC)	2	I	Dither Magnitude Resistor. Frequency-dithering magnitude and external synchronization pin. An external resistor to GND programs the magnitude of oscillator frequency dither. When frequency dithering is disabled (CDR > 5 V), the internal master clock will synchronize to positive edges presented on the RDM pin. Connect RDM to GND when dithering is disabled and synchronization is not desired.
VAO	3	O	Voltage Amplifier Output. Output of transconductance voltage error amplifier. Internally connected to Multiplier input and Zero-Power comparator. Connect the voltage regulation loop compensation components between this pin and GND.
VSENSE	4	I	Output Voltage Sense. Internally connected to the inverting input of the transconductance voltage error amplifier in addition to the positive terminal of the Current Synthesis difference amplifier. Also connected to the OVP, PFC Enable, and slew-rate comparators. Connect to PFC output with a resistor-divider network.
VINAC	5	I	Scaled AC Line Input Voltage. Internally connected to the Multiplier and negative terminal of the Current Synthesis difference amplifier. Connect a resistor-divider network between V_{IN} , VINAC, and GND identical to the PFC output divider network connected at VSENSE.
IMO	6	O	Multiplier Current Output. Connect a resistor between this pin and GND to set the multiplier gain.
RSYNTH	7	I	Current Synthesis Down-Slope Programming. Connect a resistor between this pin and GND to set the magnitude of the current synthesizer down-slope.
CSB	8	I	Phase B Current Sense Input. During the on-time of GDB, CSB is internally connected to the inverting input of Phase B's current amplifier.
CSA	9	I	Phase A Current Sense Input. During the on-time of GDA, CSA is internally connected to the inverting input of Phase A's current amplifier.
PKLMT	10	I	Peak Current Limit Programming. Connect a resistor-divider network between VREF and this pin to set the voltage threshold of the cycle-by-cycle peak current limiting comparators. Allows adjustment for desired ΔI_{LB} .
CAOB	11	O	Phase B Current Amplifier Output. Output of phase B's transconductance current amplifier. Internally connected to the inverting input of phase B's PWM comparator for trailing-edge modulation. Connect the current regulation loop compensation components between this pin and GND.
CAOA	12	O	Phase A Current Amplifier Output. Output of phase A's transconductance current amplifier. Internally connected to the inverting input of phase A's PWM comparator for trailing-edge modulation. Connect the current regulation loop compensation components between this pin and GND.
VREF	13	O	6-V Reference Voltage and Internal Bias Voltage. Connect a 0.1- μ F ceramic bypass capacitor as close as possible to this pin and GND.
GDA	14	O	Phase A's Gate Drive. This limited-current output is intended to connect to a separate gate-drive device suitable for driving the Phase A switching component(s). The output voltage is typically clamped to 13.5 V.
VCC	15	I	Bias Voltage Input. Connect a 0.1- μ F ceramic bypass capacitor as close as possible to this pin and GND.
GND	16	I/O	Device Ground Reference. Connect all compensation and programming resistor and capacitor networks to this pin. Connect this pin to the system through a separate trace for high-current noise isolation.
GDB	17	O	Phase B's Gate Drive. This limited-current output is intended to connect to a separate gate-drive device suitable for driving the Phase B switching component(s). The output voltage is typically clamped to 13.5 V.
SS	18	I	Soft-Start and External Fault Interface. Connect a capacitor to GND on this pin to set the soft-start slew rate based on an internally-fixed 10- μ A current source. The regulation reference voltage for VSENSE is clamped to V_{SS} until V_{SS} exceeds 3 V. Upon recovery from certain fault conditions a 1-mA current source is present at the SS pin until the SS voltage equals the VSENSE voltage. Pulling the SS pin below 0.6 V immediately disables both GDA and GDB outputs.
RT	19	I	Timing Resistor. Oscillator frequency programming pin. A resistor to GND sets the running frequency of the internal oscillator.
DMAX	20	I	Maximum Duty-Cycle Resistor. Maximum PWM duty-cycle programming pin. A resistor to GND sets the PWM maximum duty-cycle based on the ratio of R_{DMX}/R_{RT} .

Functional Block Diagram



PRODUCT PREVIEW

APPLICATION INFORMATION

THEORY OF OPERATION

Natural Interleaving

One of the main benefits from the natural interleaving of phases is significant reductions in the high-frequency ripple components of both the input current and the current into the output capacitor of the PFC pre-regulator. Compared to that of a single-phase PFC stage of equal power, the reduced ripple on the input current eases the burden of filtering conducted-EMI noise and helps reduce the EMI filter and C_{IN} sizes. Additionally, reduced high-frequency ripple current into the PFC output capacitor, C_{OUT} , helps to reduce its size and cost. Furthermore, with reduced ripple and average current in each phase, the boost inductor size can be smaller than in a single-phase design [1].

Ripple current reduction due to interleaving is often referred to as “ripple cancellation”, but strictly speaking, the peak-to-peak ripple is completely cancelled only at 50% duty-cycle in a 2-phase system. At duty-cycles other than 50%, ripple reduction occurs in the form of partial cancellation due to the superposition of the individual phase currents. Nevertheless, compared to the ripple currents of an equivalent single-phase PFC pre-regulator, those of a 2-phase naturally-interleaved design are extraordinarily smaller [1]. Independent of ripple cancellation, the frequency of the naturally-interleaved ripple, at both the input and output, is $2 \times f_{PWM}$.

On the input, natural interleaving reduces the peak-to-peak ripple amplitude to 1/2 or less of the ripple amplitude of the equivalent single-phase current.

On the output, Natural Interleaving reduces the rms value of the PFC-generated ripple current in the output capacitor by a factor of slightly more than $\sqrt{2}$, for PWM duty-cycles $> 50\%$ as derived from following Erickson’s method [2].

Programming the PWM Frequency and Maximum Duty-Cycle Clamp

The PWM frequency and maximum duty-cycle clamps for both GDx outputs of the UCC28070 are set through the selection of the resistors connected to the RT and DMAX pins, respectively. The selection of the RT resistor (R_{RT}) directly sets the PWM frequency (f_{PWM}).

$$R_{RT} (k\Omega) = \frac{7500}{f_{PWM} (kHz)}$$

Once R_{RT} has been determined, the D_{MAX} resistor (R_{DMX}) may be derived.

$$R_{DMX} = R_{RT} \times (2 \times D_{MAX} - 1)$$

where D_{MAX} is the desired maximum PWM duty-cycle.

Frequency Dithering (Magnitude and Rate)

Frequency dithering refers to modulating the switching frequency to achieve a reduction in conducted-EMI noise beyond the capability of the line filter alone. The UCC28070 implements a triangular modulation method which results in equal time spent at every point along the switching frequency range. This total range from minimum to maximum frequency is defined as the dither magnitude, and is centered around the nominal switching frequency f_{PWM} set with R_{RT} . For example, a dither magnitude of 20 kHz on a nominal f_{PWM} of 100 kHz results in a frequency range of 100 kHz \pm 10 kHz. Furthermore, the programmed duty-cycle clamp set by R_{DMX} remains constant at the programmed value across the entire range of the frequency dithering.

The rate at which f_{PWM} traverses from one extreme to the other and back again is defined as the dither rate. For example, a dither rate of 1 kHz would linearly modulate the nominal frequency from 110 kHz to 90 kHz to 110 kHz once every millisecond. A good initial design target for dither magnitude is \pm 10% of f_{PWM} . Most boost components can tolerate such a spread in f_{PWM} . The designer can then iterate around there to find the best compromise between EMI reduction, component tolerances, and loop stability.

The desired dither magnitude is set by a resistor from the RDM pin to GND, of value calculated by the following equation:

$$R_{RDM} (k\Omega) = \frac{937.5}{f_{DM} (kHz)}$$

Once the value of R_{RDM} is determined, the desired dither rate may be set by a capacitor from the CDR pin to GND, of value calculated by the following equation:

$$C_{CDR} (pF) = 66.7 \times \left(\frac{R_{RDM}}{f_{DR}} \right) (k\Omega / kHz)$$

Frequency dithering may be fully disabled by forcing the CDR pin $>$ 5 V or by connecting it to VREF (6 V) and connecting the RDM pin directly to GND. (If populated, the relatively high impedance of the RDM resistor may allow system switching noise to couple in and interfere with the controller timing functions if not bypassed with a low impedance path when dithering is disabled.)

If an external frequency source is used to synchronize f_{PWM} and frequency dithering is desired, the external frequency source must provide the dither magnitude and rate functions as the internal dither circuitry is disabled to prevent undesired performance during synchronization. (See [SubSec2 0.1](#) section for more details.)

External Clock Synchronization

The UCC28070 has also been designed to be easily synchronized to almost any external frequency source. By disabling frequency dithering (pulling CDR > 5 V), the UCC28070's SYNC circuitry is enabled permitting the internal oscillator to be synchronized with pulses presented on the RDM pin. In order to ensure a precise 180 degree phase shift is maintained between the GDA and GDB outputs, the frequency (f_{SYNC}) of the pulses presented at the RDM pin needs to be at twice the desired f_{PWM} . For example, if a 100-kHz switching frequency is desired, the f_{SYNC} should be 200 kHz.

In order to ensure the internal oscillator does not interfere with the SYNC function, R_{RT} should be sized to set the internal oscillator frequency at least 10% below the f_{SYNC} . It must be noted that the PWM modulator gain will be reduced by a factor equivalent to the scaled R_{RT} due to a direct correlation between the PWM ramp current and R_{RT} . Adjustments to the current loops should be made accordingly.

The maximum duty-cycle clamp programmability is still maintained via the selection of R_{DMX} based on the second and third equations below.

$$f_{PWM} = \frac{f_{SYNC}}{2}$$

$$R'_{RT} (k\Omega) = \frac{15000}{f_{SYNC} (kHz)}$$

$$R_{DMX} (k\Omega) = R'_{RT} \times (2 \times D_{MAX} - 1)$$

$$R_{RT} (k\Omega) = 1.1 \times \frac{15000}{f_{SYNC} (kHz)}$$

$$f_{SYN(maxD)} \leq 0.9 \times (2 \times D_{MAX} - 1)$$

NOTE:

When external synchronization is used, a propagation delay of approximately 50 ns to 100 ns exists between internal timing circuits and the SYNC signal's rising edge, which may result in reduced off-time at the highest of switching frequencies. Therefore, R_{DMX} should be adjusted downward slightly by $(T_{SYNC} - 0.1 \mu s) / T_{SYNC}$ to compensate. At lower SYNC frequencies, this delay becomes an insignificant fraction of the PWM period, and can be neglected.

Multi-phase Operation

External synchronization also facilitates using more than 2 phases for interleaving. Multiple UCC28070s can easily be paralleled to add an even number of additional phases for higher-power applications. With appropriate phase-shifting of the synchronization signals, even more input and output ripple current cancellation can be obtained. (An odd number of phases can be accommodated if desired, but the ripple cancellation would not be optimal.) For 4-, 6-, or any 2 x n-phases (where n = the number of UCC28070 controllers), each controller should receive a SYNC signal which is 360/n degrees out of phase with each other. For a 4-phase application interleaving with two controllers, SYNC1 should be 180° out of phase with SYNC2 for optimal ripple cancellation. Similarly for a 6-phase system, SYNC1, SYNC2, and SYNC3 should be 120° out of phase with each other for optimal ripple cancellation.

In a multi-phase interleaved system, each current loop is independent and treated separately, however there is only one common voltage loop. To maintain a single control loop, all VSENSE, VINAC, SS, IMO and VAO signals are paralleled, respectively between the n controllers. Where current-source outputs are combined (SS, IMO, VAO), the calculated load impedances must be adjusted by 1/n to maintain the same performance as with a single controller.

Figure 20 illustrates the paralleling of two controllers for a 4-phase 90°-interleaved PFC system.

VSENSE and VINAC Resistor Configuration

The primary purpose of the VSENSE input is to provide the voltage feedback from the output to the voltage control loop. Thus, a traditional resistor-divider network needs to be sized and connected between the output capacitor and the VSENSE pin to set the desired output voltage based on the 3-V regulation voltage on VSENSE.

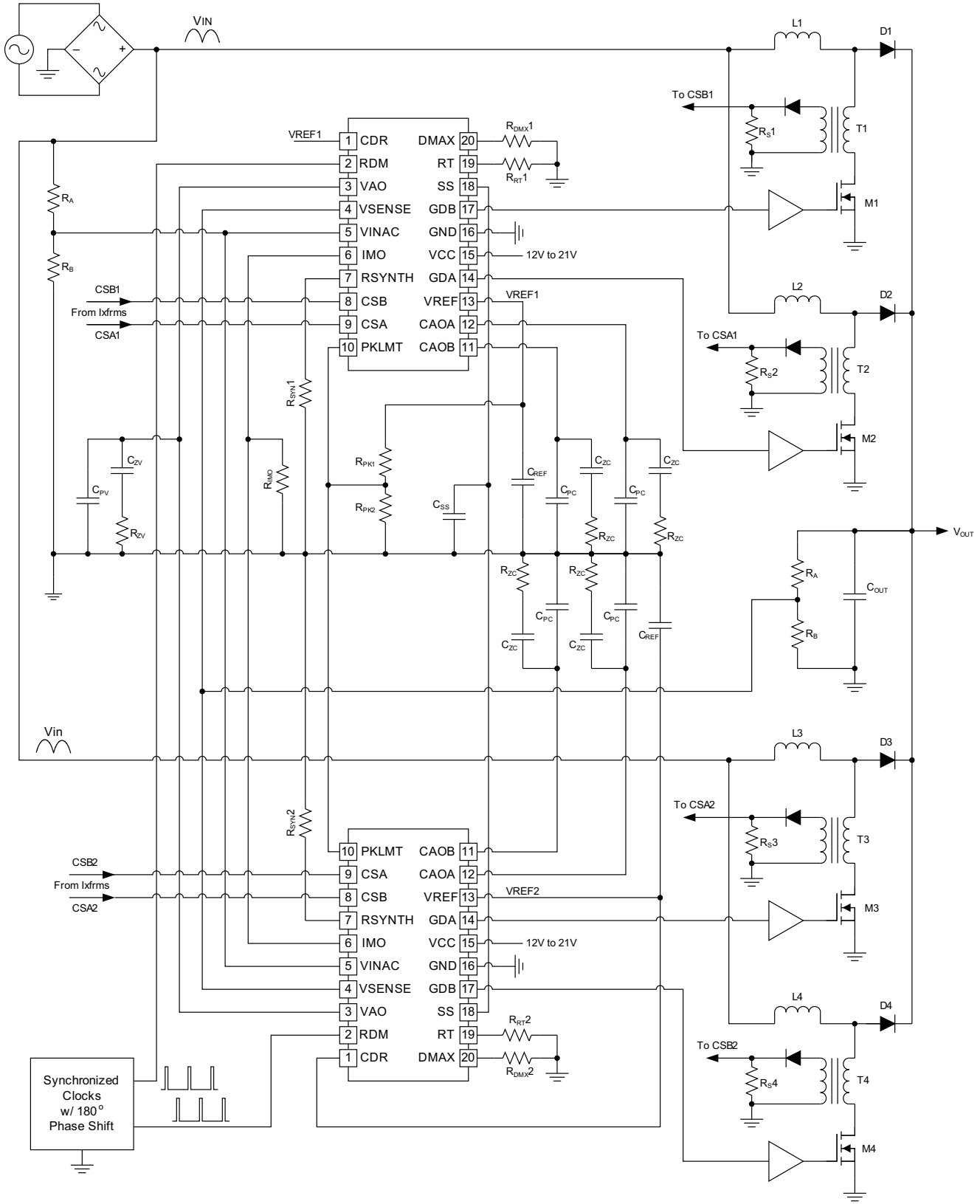
A unique aspect of the UCC28070 is the need to place the same resistor-divider network on the V_{IN} side of the inductor to the VINAC pin. This provides the scaled input voltage monitoring needed for the linear multiplier and current synthesizer circuitry. It is not required that the actual resistance of the VINAC network be identical to the VSENSE network, but it is necessary that the attenuation (k_R) of the two divider networks be equivalent for proper PFC operation.

$$k_R = \frac{R_B}{(R_A + R_B)}$$

In noisy environments, it may be beneficial for small filter capacitors to be applied to the VSENSE and VINAC inputs to avoid the destabilizing effects of excessive noise on these inputs. If applied, the RC time-constant should not exceed 100µs on the VSENSE input to avoid significant delay in the output transient response. The RC time-constant should also not exceed 100 µs on the VINAC input to avoid degrading of the wave-shape zero-crossings. Usually, a time constant of $3/f_{PWM}$ is adequate to filter out typical noise on VSENSE and VINAC. Some design and test iteration may be required to find the optimal amount of filtering required in a particular application.

VSENSE and VINAC Open Circuit Protection

Both the VSENSE and VINAC pins have been designed with an internal 250-nA current sink to ensure that in the event of an open circuit at either pin, the voltage is not left undefined, and the UCC28070 remains in a “safe” operating mode.



PRODUCT PREVIEW

Figure 20. Functional Four-Phase Application Schematic Using Two UCC28070

Current Synthesizer

One of the most prominent innovations in the UCC28070 design is the current synthesizer circuitry that synchronously monitors the instantaneous inductor current through a combination of on-time sampling and off-time down-slope emulation.

During the on-time of the GDA and GDB outputs, the inductor current is recorded at the CSA and CSB pins respectively via the current transformer network in each output phase. Meanwhile, the continuous monitoring of the input and output voltage via the VINAC and VSENSE pins permits the UCC28070 to internally recreate the inductor current's down-slope during each output's respective off-time. Through the selection of the R_{SYNTH} resistor (R_{SYN}), based on the equation below, the internal circuitry may be adjusted to accommodate the wide range of inductances expected across the wide array of applications.

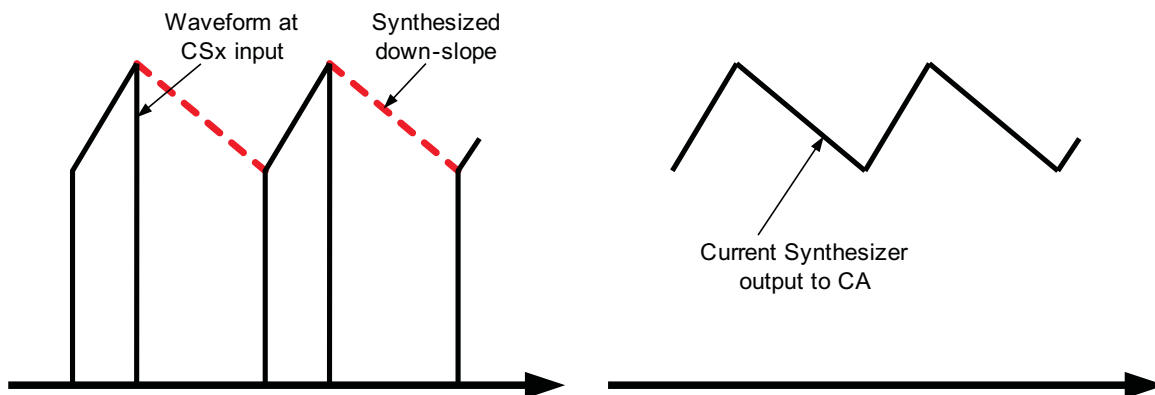


Figure 21. Inductor Current's Down Slope

$$R_{SYN} (k\Omega) = \frac{(10 \times N_{CT} \times L_B (\mu H) \times k_R)}{R_S (\Omega)}$$

Variables

- L_B = Nominal Boost Inductance (μH),
- R_S = Sense Resistor (Ω),
- N_{CT} = Current-sense Transformer turns ratio,
- k_R = R_B/(R_A+R_B) = the resistor-divider attenuation at the VSENSE and VINAC pins.

Programmable Peak Current Limit

The UCC28070 has been designed with a programmable cycle-by-cycle peak current limit dedicated to disabling either GDA or GDB output whenever the corresponding current-sense input (CSA or CSB respectively) rises above the voltage established on the PKLMT pin. Once an output has been disabled via the detection of peak current limit, the output remains disabled until the next clock cycle initiates a new PWM period. The programming range of the PKLMT voltage extends to upwards of 4 V to permit the full utilization of the 3-V average current sense signal range.

A resistor-divider network from VREF to GND can easily program the peak current limit voltage on PKLMT, provided the total current out of VREF is less than 2 mA to avoid drooping of the 6-V VREF voltage. A load of less than 0.5 mA is suggested, but if the resistance on PKLMT is very high, a small filter capacitor on PKLMT is recommended to avoid operational problems in high-noise environments.

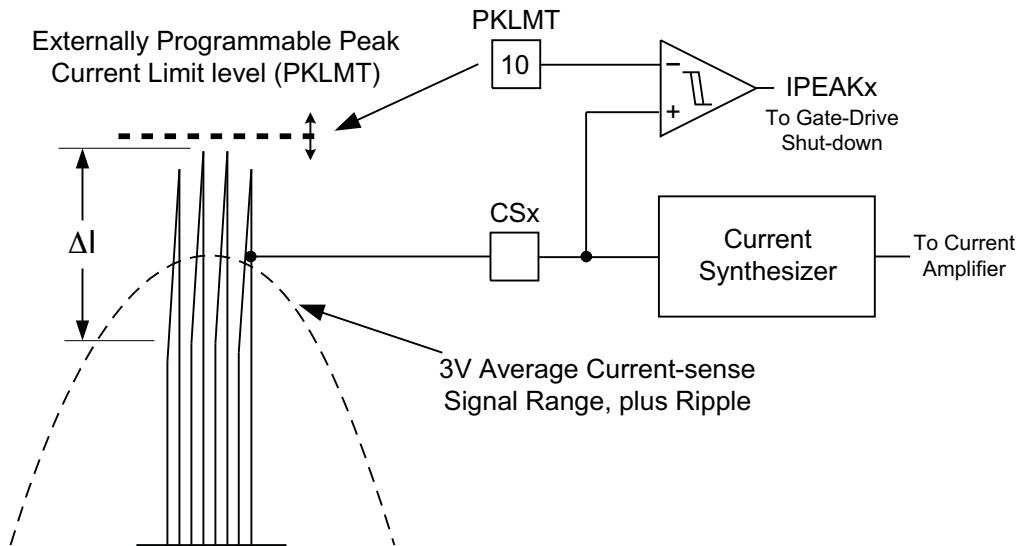


Figure 22. Externally Programmable Peak Current Limit

Linear Multiplier

The multiplier of the UCC28070 generates a reference current which represents the desired wave shape and proportional amplitude of the ac input current. This current is converted to a reference voltage signal by the R_{IMO} resistor, which is scaled in value to match the voltage of the current-sense signals. The instantaneous multiplier current is dependent upon the rectified, scaled input voltage V_{VINAC} and the voltage-error amplifier output V_{VAO} . The V_{VINAC} signal conveys three pieces of information to the multiplier:

1. The overall wave-shape of the input voltage (typically sinusoidal),
2. the instantaneous input voltage magnitude at any point in the line cycle,
3. and the rms level of the input voltage.

The V_{VAO} signal represents the total output power of the PFC pre-regulator.

A major innovation in the UCC28070 multiplier architecture is the internal quantized V_{RMS} feed-forward (Q_{VFF}) circuitry, which eliminates the requirement for external filtering of the V_{INAC} signal and the subsequent slow response to transient line variations. A unique circuit algorithm detects the transition of the peak of V_{VINAC} through seven thresholds and generates an equivalent VFF level centered within the eight Q_{VFF} ranges. The boundaries of the ranges expand with increasing V_{IN} to maintain an approximately equal-percentage delta between levels. These eight Q_{VFF} levels are spaced to accommodate the full “universal” line range of 85 V-265 V_{RMS} .

A great benefit of the Q_{VFF} architecture is that the fixed k_{VFF} factors eliminate any contribution to distortion of the multiplier output, unlike an externally-filtered V_{INAC} signal which unavoidably contains 2nd-harmonic distortion components. Furthermore, the Q_{VFF} algorithm allows for rapid response to both increasing and decreasing changes in input rms voltage so that disturbances transmitted to the PFC output are minimized. 5% hysteresis in the level thresholds help avoid “chattering” between Q_{VFF} levels for V_{VINAC} voltage peaks near a particular threshold or containing mild ringing or distortion. The Q_{VFF} architecture requires that the input voltage be largely sinusoidal, and relies on detecting zero-crossings to adjust Q_{VFF} downward on decreasing input voltage. Zero-crossings are defined as V_{VINAC} falling below 0.7 V for at least 50 μ s typically.

Table 1 reflects the relationship between the various V_{INAC} peak voltages and the corresponding k_{VFF} terms for the multiplier equation.

Table 1. V_{INAC} Peak Voltages

LEVEL	V_{VINAC} PEAK VOLTAGE	k_{VFF} (V^2)	V_{IN} PEAK VOLTAGE ⁽¹⁾
8	$2.60\text{ V} \leq V_{VINAC(pk)}$	3.857	> 345 V
7	$2.25\text{ V} \leq V_{VINAC(pk)} < 2.60\text{ V}$	2.922	300 V to 345 V
6	$1.95\text{ V} \leq V_{VINAC(pk)} < 2.25\text{ V}$	2.199	260 V to 300 V
5	$1.65\text{ V} \leq V_{VINAC(pk)} < 1.95\text{ V}$	1.604	220 V to 260 V
4	$1.40\text{ V} \leq V_{VINAC(pk)} < 1.65\text{ V}$	1.156	187 V to 220 V
3	$1.20\text{ V} \leq V_{VINAC(pk)} < 1.40\text{ V}$	0.839	160 V to 187 V
2	$1.00\text{ V} \leq V_{VINAC(pk)} < 1.20\text{ V}$	0.600	133 V to 160 V
1	$V_{VINAC(pk)} \leq 1.00\text{ V}$	0.398	< 133 V

(1) The V_{IN} peak voltage boundary values listed above are calculated based on a 400-V PFC output voltage and the use of a matched resistor-divider network ($k_R = 3\text{ V}/400\text{ V} = 0.0075$) on V_{INAC} and V_{SENSE} (as required for current synthesis). When V_{OUT} is designed to be higher or lower than 400 V, $k_R = 3\text{ V}/V_{OUT}$, and the V_{IN} peak voltage boundary values for each Q_{VFF} level adjust to $V_{VINAC(pk)}/k_R$.

The multiplier output current I_{IMO} for any line and load condition can thus be determined by the equation

$$I_{IMO} = \frac{17\mu A \times (V_{VINAC}) \times (V_{VAO} - 1)}{k_{VFF}}$$

Because the k_{VFF} value represents the scaled V_{RMS}^2 at the center of a level, V_{VAO} will adjust slightly upwards or downwards when $VINAC_{pk}$ is either lower or higher than the center of the Q_{VFF} voltage range to compensate for the difference. This is automatically accomplished by the voltage loop control when V_{IN} varies, both within a level and after a transition between levels.

The output of the voltage-error amplifier VAO is clamped at 5.0 V, which represents the maximum PFC output power. This value is used to calculate the maximum reference current at the IMO pin, and sets a limit for the maximum input power allowed (and, as a consequence, limits maximum output power).

Unlike a continuous V_{FF} situation, where maximum input power is a fixed power at any V_{RMS} input, the discrete Q_{VFF} levels permit a variation in maximum input power within limited boundaries as the input V_{RMS} varies within each level.

The lowest maximum power limit occurs at the VINAC voltage of 0.76 V, while the highest maximum power limit occurs at the increasing threshold from level-1 to level-2. This pattern repeats at every level transition threshold, keeping in mind that decreasing thresholds are 95% of the increasing threshold values. Below $VINAC = 0.76$ V, P_{IN} is always less than $P_{IN(max)}$, falling linearly to zero with decreasing input voltage.

For example, to design for the lowest maximum power allowable, determine the maximum steady-state (average) output power required of the PFC pre-regulator and add some additional percentage to account for line drop-out recovery power (to recharge C_{OUT} while full load power is drawn) such as 10% or 20% of $P_{OUT(max)}$. Then apply the expected efficiency factor to find the lowest maximum input power allowable:

$$P_{IN(max)} = \frac{1.10 \times P_{OUT(max)}}{\eta}$$

At the $P_{IN(max)}$ design threshold, $V_{VINAC} = 0.76$ V, hence $Q_{VFF} = 0.398$ and input $V_{AC} = 73 V_{RMS}$ (accounting for 2-V bridge-rectifier drop) for a nominal 400-V output system.

$$\text{Thus } I_{IN(rms)} = \frac{P_{IN(max)}}{73V_{RMS}}, \text{ and } I_{IN(pk)} = 1.414 \times I_{IN(rms)}$$

This $I_{IN(pk)}$ value represents the combined average current through the boost inductors at the peak of the line voltage. Each inductor current is detected and scaled by a current-sense transformer (CT). Assuming equal currents through each interleaved phase, the signal voltage at each current sense input pin (CSA and CSB) is developed across a sense resistor selected to generate ~ 3 V based on $(1/2) \times I_{IN(pk)} \times R_S/N_{CT}$, where R_S is the burden current sense resistor and N_{CT} is the CT turns-ratio.

I_{IMO} is then calculated at that same lowest maximum-power point, as

$$I_{IMO(max)} = 17 \mu A \times \frac{(0.76V)(5V - 1V)}{0.398} = 130 \mu A$$

R_{IMO} is selected such that:

$$R_{IMO} \times I_{IMO(max)} = \left(\frac{1}{2}\right) \times I_{IN(pk)} \times \frac{R_S}{N_{CT}}$$

Therefore:

$$R_{IMO} = \frac{\left(\left(\frac{1}{2}\right) \times I_{IN(pk)} \times R_S\right)}{\left(N_{CT} \times I_{IMO(max)}\right)}$$

At the increasing side of the level-1 to level-2 threshold, it should be noted that the IMO current would allow much higher input currents at low-line:

$$I_{IMO(L1-L2)} = 17 \mu A \times \frac{(1.0V)(5V - 1V)}{0.398} = 171 \mu A$$

However, this current may easily be limited by the programmable peak current limiting (PKLMT) feature of the UCC28070 if required by the power stage design.

The same procedure can be used to find the lowest and highest input power limits at each of the Q_{VFF} level transition thresholds. At higher line voltages, where the average current with inductor ripple is traditionally below the PKLMT threshold, the full variation of maximum input power will be seen, but the input currents will inherently be below the maximum acceptable current levels of the power stage.

The performance of the multiplier in the UCC28070 has been significantly enhanced when compared to previous generation PFC controllers, with high linearity and accuracy over most of the input ranges. The accuracy is at its worst as V_{VAO} approaches 1 V because the error of the $(V_{VAO}-1)$ subtraction increases and begins to distort the IMO reference current to a greater degree.

Enhanced Transient Response (VA Slew-Rate Correction)

Due to the low voltage loop bandwidth required to maintain proper PFC and ignore the slight 120-Hz ripple on the output, the response of ordinary controllers to input voltage and load transients will also be slow. However, the Q_{VFF} function effectively handles the line transient response with the exception of any minor adjustments needed within a Q_{VFF} level. Load transients on the other hand can only be handled by the voltage loop, therefore, the UCC28070 has been designed to improve its transient response by pulling up on the output of the voltage amplifier (VAO) with an additional 100 μA of current in the event the VSENSE voltage drops below 93% of regulation (2.79 V). During a soft-start cycle, when VSENSE is ramping up from the 0.75-V PFC Enable threshold, the 100- μA correction current source is disabled to ensure the gradual and controlled ramping of output voltage and current during a soft start.

Voltage Biasing (VCC and VREF)

The UCC28070 operates within a VCC bias supply range of 10 V to 21 V. An Under-Voltage Lock-Out (UVLO) threshold prevents the PFC from activating until $V_{CC} > 10.2$ V, and 1 V of hysteresis assures reliable start-up from a possibly low-compliance bias source. An internal 23-V zener-like clamp on VCC is intended only to protect the device from brief energy-limited surges from the bias supply, and should NOT be used as a regulator with a current-limited source.

At minimum, a 0.1- μ F ceramic bypass capacitor must be applied from VCC to GND close to the device pins to provide local filtering of the bias supply. Larger values may be required depending on I_{CC} peak current magnitudes and durations to minimize ripple voltage on VCC.

In order to provide a smooth transition out of UVLO and to make the 6-V voltage reference available as early as possible, the VREF output is enabled when VCC exceeds 8 V typically.

The VREF circuitry is designed to provide the biasing of all internal control circuits and for limited use externally. At minimum, a 22-nF ceramic bypass capacitor must be applied from VREF to GND close to the device pins to ensure stability of the circuit. External load current on VREF should be limited to less than 2 mA, or degraded regulation may result.

PFC Enable and Disable

The UCC28070 contains two independent circuits dedicated to disabling the GDx outputs based on the biasing conditions of the VSENSE or SS pins. The first circuit which monitors the V_{VSENSE} , is the traditional PFC Enable that holds off soft-start and the overall PFC function until the output has pre-charged to ~25%. Prior to V_{VSENSE} reaching 0.75 V, almost all of the internal circuitry is disabled. Once V_{VSENSE} reaches 0.75 V and $V_{AO} < 0.75$ V, the oscillator, multiplier, and current synthesizer are enabled and the SS circuitry begins to ramp up the voltage on the SS pin. The second circuit provides an external interface to emulate an internal fault condition to disable the GDx output without fully disabling the voltage loop and multiplier. By externally pulling the SS pin below 0.6 V, the GDx outputs are immediately disabled and held low. Assuming no other fault conditions are present, normal PWM operation resumes when the external SS pull-down is released. It must be noted that the external pull-down needs to be sized large enough to override the internal 1-mA adaptive SS pull-up once the SS voltage falls below the disable threshold. It is recommended that a MOSFET with less than 100- Ω $R_{DS(on)}$ resistance be used to ensure the SS pin is held adequately below the disable threshold.

Adaptive Soft Start

In order to maintain a controlled power up, the UCC28070 has been designed with an adaptive soft-start function that overrides the internal reference voltage with a controlled voltage ramp during power up. On initial power up, once V_{VSENSE} exceeds the 0.75-V enable threshold (V_{EN}), the internal pull down on the SS pin is released, and the 1-mA adaptive soft-start current source is activated. This 1-mA pull-up almost immediately pulls the SS pin to 0.75 V (V_{VSENSE}) to bypass the initial 25% of dead time during a traditional 0 V to Vregulation SS ramp. Once the SS pin has reached the voltage on VSENSE, the 10- μ A soft-start current (I_{SS}) takes over. Thus, through the selection of the soft-start capacitor (C_{SS}), the effective soft-start time (t_{SS}) may be easily programmed based on the equation below.

$$t_{SS} = C_{SS} \times \left(\frac{2.25V}{10\mu A} \right)$$

Often, a system restart is desired following a brief shut-down. In such a case, VSENSE may still have substantial voltage if V_{OUT} has not fully discharged or if high line has peak charged C_{OUT} . To eliminate the delay caused by charging C_{SS} from 0 V up to the pre-charged V_{VSENSE} with only the 10- μ A current source and any further output voltage sag, the adaptive soft start uses a 1-mA current source to rapidly charge C_{SS} to V_{VSENSE} , after which time the 10- μ A source controls the V_{SS} ascent to the desired soft-start ramp rate. In such a case, t_{SS} is estimated as follows:

$$t_{SS} = C_{SS} \times \left(\frac{3V - V_{VSENSE0}}{10\mu A} \right)$$

where $V_{VSENSE0}$ is the voltage at VSENSE at the moment a soft start or restart is initiated.

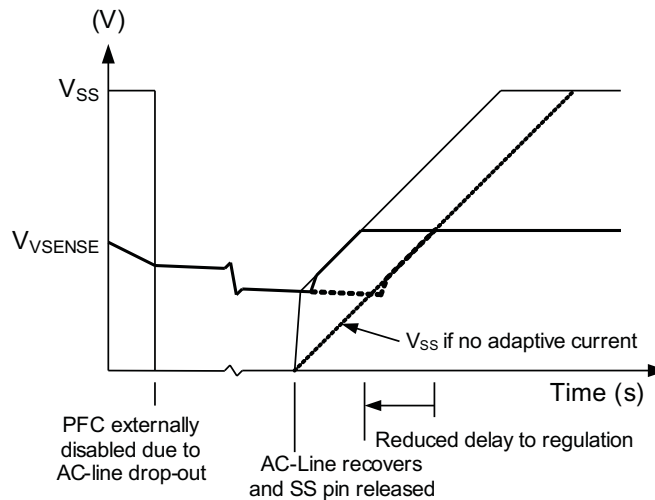


Figure 23. Soft-Start Ramp Rate

PFC Start-Up Hold Off

An additional feature designed into the UCC28070 is the “Start-Up Hold Off” logic that prevents the device from initiating a soft-start cycle until the VAO is below the zero-power threshold (0.75 V). This feature ensures that the SS cycle will initiate from zero-power and zero duty-cycle while preventing the potential for any significant inrush currents due to stored charge in the VAO compensation network.

Output Over-Voltage Protection (OVP)

Because of the high voltage output and a limited design margin on the output capacitor, output over-voltage protection is essential for PFC circuits. The UCC28070 implements OVP through the continuous monitoring of the VSENSE voltage. In the event V_{VSENSE} rises above 106% of regulation (3.18 V), the GDx outputs are immediately disabled to prevent the output voltage from reaching excessive levels. Meanwhile the CA0x outputs are pulled low in order to ensure a controlled recovery starting from 0% duty-cycle after an OVP fault is released. Once the V_{VSENSE} voltage has dropped below 3.08 V, the PWM operation resumes normal operation.

Zero-Power Detection

In order to prevent undesired performance under no-load and near no-load conditions, the UCC28070 zero-power detection comparator is designed to disable both GDA and GDB output in the event the VAO voltage falls below 0.75 V. The 150 mV of hysteresis ensures that the output remains disabled until the VAO has nearly risen back into the linear range of the multiplier ($VAO \geq 0.9$ V).

Thermal Shutdown

In order to protect the power supplies from silicon failures at excessive temperatures, the UCC28070 has an internal temperature-sensing comparator that shuts down nearly all of the internal circuitry, and disables the GDA and GDB outputs, if the die temperature rises above 160°C. Once the die temperature falls below 140°C, the device brings the outputs up through a typical soft start.

Advanced Design Techniques

Current Loop Feedback Configuration (Sizing of the Current Transformer Turns Ratio and Sense Resistor (R_S))

A current-sense transformer (C_T) is typically used in high-power applications to sense inductor current while avoiding significant losses in the sensing resistor. For average current-mode control, the entire inductor current waveform is required; however low-frequency CTs are obviously impracticable. Normally, two high-frequency CTs are used, one in the switching leg to obtain the up-slope current and one in the diode leg to obtain the down-slope current. These two current signals are summed together to form the entire inductor current, but this is not the case for the UCC28070.

A major advantage of the UCC28070 design is the current synthesis function, which internally recreates the inductor current down-slope during the switching period off-time. This eliminates the need for the diode-leg CT in each phase, significantly reducing space, cost and complexity. A single resistor programs the synthesizer down slope, as previously discussed in [SubSec2 0.2](#).

A number of trade-offs must be made in the selection of the CT. Various internal and external factors influence the size, cost, performance, and distortion contribution of the CT.

These factors include, but are not limited to:

- Turns-ratio (N_{CT})
- Magnetizing inductance (L_M)
- Leakage inductance (L_{LK})
- Volt-microsecond product ($V\mu s$)
- Distributed capacitance (C_d)
- Series resistance (R_{SER})
- External diode drop (V_D)
- External current sense resistor (R_S)
- External reset network

Traditionally, the turns-ratio and the current sense resistor are selected first. Some iterations may be needed to refine the selection once the other considerations are included.

In general, $50 \leq N_{CT} \leq 200$ is a reasonable range from which to choose. If N_{CT} is too low, there may be high power loss in R_S and insufficient L_M . If too high, there could be excessive L_{LK} and C_d . (A one-turn primary winding is assumed.)

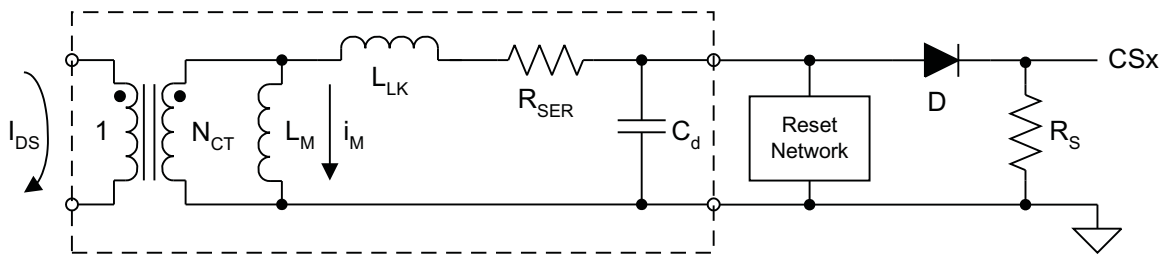


Figure 28. Current Sense Transformer Equivalent Circuit

A major contributor to distortion of the input current is the effect of magnetizing current on the CT output signal (i_{RS}). A higher turns-ratio results in a higher L_M for a given core size. L_M should be high enough that the magnetizing current (i_M) generated is a very small percentage of the total transformed current. This is an impossible criterion to maintain over the entire current range, because i_M unavoidably becomes a larger fraction of i_{RS} as the input current decreases toward zero. The effect of i_M is to “steal” some of the signal current away from R_S , reducing the CSx voltage and effectively understating the actual current being sensed. At low currents, this understatement can be significant and CA0x increases the current-loop duty-cycle in an attempt to correct the CSx input(s) to match the IMO reference voltage. This unwanted correction results in overstated current on the input wave shape in the regions where the CT understatement is significant, such as near the ac line zero crossings. It can affect the entire waveform to some degree under the high line, light-load conditions.

The sense resistor R_S is chosen, in conjunction with N_{CT} , to establish the sense voltage at CSx to be about 3 V at the center of the reflected inductor ripple current under maximum load. The goal is to maximize the average signal within the common-mode input range V_{CMCAO} of the CA0x current-error amplifiers, while leaving room for the peaks of the ripple current within V_{CMCAO} . The design condition should be at the lowest maximum input power limit as determined in the Multiplier Section. If the inductor ripple current is so high as to cause V_{CSx} to exceed V_{CMCAO} , then R_S or N_{CT} or both must be adjusted to reduce peak V_{CSx} , which could reduce the average sense voltage center below 3 V. There is nothing wrong with this situation; but be aware that the signal is more compressed between full- and no-load, with potentially more distortion at light loads.

The matter of volt-second balancing is important, especially with the widely varying duty-cycles in the PFC stage. Ideally, the CT is reset once each switching period; that is, the off-time $V_{\mu s}$ product equals the on-time $V_{\mu s}$ product. (Because a switching period is usually measured in microseconds, it is convenient to convert the volt-second product to volt-microseconds to avoid sub-decimal numbers.) On-time $V_{\mu s}$ is the time-integral of the voltage across L_M generated by the series elements R_{SER} , L_{LK} , D, and R_S . Off-time $V_{\mu s}$ is the time-integral of the voltage across the reset network during the off-time. With passive reset, $V_{\mu s-off}$ is unlikely to exceed $V_{\mu s-on}$. Sustained unbalance in the on or off $V_{\mu s}$ products will lead to core saturation and a total loss of the current-sense signal. Loss of V_{CSx} causes V_{CAOx} to quickly rise to its maximum, programming a maximum duty-cycle at any line condition. This, in turn causes the boost inductor current to increase without control, until the system fuse or some component failure interrupts the input current.

It is vital that the CT has plenty of $V_{\mu s}$ design-margin to accommodate various special situations where there to be several consecutive maximum duty-cycle periods at maximum input current, such as during peak current limiting.

Maximum $V_{\mu s(on)}$ can be estimated by:

$$V_{\mu s(on)max} = t_{ON(max)} \times (V_{RS} + V_D + V_{RSEr} + V_{LK})$$

where all factors are maximized to account for worst-case transient conditions and $t_{ON(max)}$ occurs during the lowest dither frequency when frequency dithering is enabled. For design margin, a CT rating of $\sim 5 \times V_{\mu s(on)max}$ or higher is suggested. The contribution of V_{RS} varies directly with the line current. However, V_D may have a significant voltage even at near-zero current, so substantial $V_{\mu s(on)}$ may accrue at the zero-crossings where the duty-cycle is maximum. V_{RSEr} is the least contributor, and often can be neglected if $R_{SEr} \ll R_S$. V_{LK} is developed by the di/dt of the sensed current, and is not observable externally. However, its impact is considerable, given the sub-microsecond rise-time of the current signal plus the slope of the inductor current. Fortunately, most of the built-up $V_{\mu s}$ across L_M during the on-time is removed during the fall-time at the end of the duty-cycle, leaving a lower net $V_{\mu s(on)}$ to be reset during the off-time. Nevertheless, the CT must, at the very minimum, be capable of sustaining the full internal $V_{\mu s(on)max}$ built up until the moment of turn-off within a switching period.

$V_{\mu s(off)}$ may be generated with a resistor or zener diode, using the i_M as bias current.

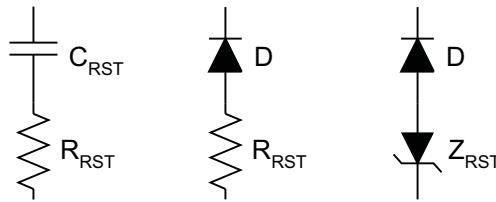


Figure 29. Possible Reset Networks

In order to accommodate various CT circuit designs and prevent the potentially destructive result due to CT saturation, the UCC28070's maximum duty-cycle needs to be programmed such that the resulting minimum off-time accomplishes the required worst-case reset. (See the PWM Frequency and Duty-Cycle Clamp section of the data sheet for more information on sizing R_{DMX}) Be aware that excessive C_d in the CT can interfere with effective resetting, because the maximum reset voltage is not reached until after 1/4-period of the CT self-resonant frequency. A higher turns-ratio results in higher C_d [3], so a trade-off between N_{CT} and D_{MAX} must be made.

The selected turns-ratio also affects L_M and L_{LK} , which vary proportionally to the square of the turns. Higher L_M is good, while higher L_{LK} is not. If the voltage across L_M during the on-time is assumed to be constant (which it is not, but close enough to simplify) then the magnetizing current is an increasing ramp.

This upward ramping current subtracts from i_{RS} , which affects V_{CSx} especially heavily at the zero-crossings and light loads, as stated earlier. With a reduced peak at V_{CSx} , the current synthesizer starts the down-slope at a lower voltage, further reducing the average signal to CA0x and further increasing the distortion under these conditions. If low input current distortion at very light loads is required, special mitigation methods may need to be developed to accomplish that goal.

Current-Sense Transformer (C_T) Issue(s) When Operating In DCM

To maintain low THD over a wide range of line and load, AND keep a simple circuit, requires that Continuous Conduction Mode (CCM) be maintained in the boost inductor over that same wide range. This requirement arises out of the following situation:

The trend in PFC toward high-ripple, low-inductance design to reduce magnetics size and cost results in early onset of discontinuous conduction mode (DCM) at high-line and/or lighter loads. Ordinarily, DCM can be averaged as well as CCM, however a side-effect of DCM in conjunction with CT use leads to waveform distortion in the following manner.

During the dead-time of DCM, when the boost inductor current has discharged to zero, the high voltage stored on the MOSFET's C_{OSS} begins to ring back reverse current through the boost inductor and hence necessarily backwards through the CT.

This reverse inductor current through the CT drives a reverse magnetizing current through the CT's inductance which subsequently adds to the V_{RS} signal level during the next switching cycle on-time. This additional signal level overstates the scaled inductor current to the Current Amplifier (CA) with respect to the V_{IMO} reference and the CA acts to reduce the duty-cycle, thus maintaining and reinforcing the DCM. So it is a positive feedback situation whereby DCM is artificially maintained along substantial portions of the lower sinewave, until V_{IN} becomes high enough to instigate CCM. Once in CCM, the current waveform faithfully follows V_{IMO} until DCM begins again some time after the peak of V_{IN} .

For a given power level and input voltage, an ideal current sinewave can be calculated. The regions of inductor DCM have less actual current than the ideal sinewave requires, and so VAO voltage increases V_{IMO} to inflate the CCM portion to compensate for the difference. Hence a significant amount of distortion can result from a small amount of DCM.

The simplest way to avoid this is to design the inductance high enough to avoid DCM under all conditions where low THD is required. Otherwise, additional compensating circuitry will be necessary to mitigate the DCM situation, with complexity increasing as low-THD conditions are expanded.

To maintain <5% THD over 85 V-265 V_{RMS} at full load only,

- Design L_B to avoid DCM up to 250 V-260 V_{RMS} , and
- Add a positive bias current injection circuit to V_{CSA} and V_{CSB} , which activates only at low-line (below ~155 V_{RMS}). Bias current is adjusted empirically.

This is crude, fairly simple, and effective, but works only for full-load. The fixed bias current optimized for full load is insufficient for lighter loads.

At lighter loads (say to 50%), one can follow the same method as above, with yet larger L_B , or employ additional, more complicated compensation techniques with variable bias levels and polarities under different conditions.

Ultimately, all compensation techniques are attempts to remove the influence of negative or positive magnetizing current (i_M) of the CT from the V_{RS} signal. A fixed bias current has limited success in canceling a variable i_M , and more sophisticated adaptable bias-adjusting circuits are obviously more complicated and expensive.

Adjusting the switching period (T_{SW}) by manipulating the values of R_T and R_{DMX} can be another technique, with the objective to maintain CCM over more of the range of possible operating conditions. This can be effective as long as variable switching frequency is permissible.

Also, low-loss resistive sensing can replace the CT if very wide GBW operational amplifiers are available. But drawbacks of this approach include cost, complexity, leading-edge spikes (from gate drive), etc.

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PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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