SamHop Microelectronics Corp.

SC8100S

Ver 2.0

Dual N-Channel Enhancement Mode Field Effect Transistor

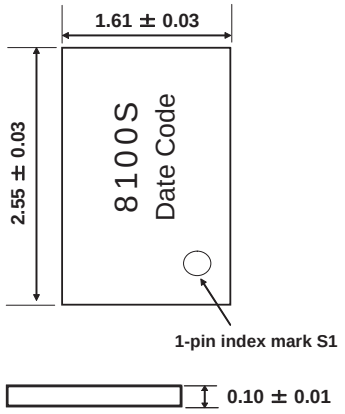
PRODUCT SUMMARY		
V_{SSS}	I_S	$R_{SS(ON)}$ (mΩ) Typ
12V	8A	4.6 @ VGS=4.5V
		4.8 @ VGS=4.0V
		4.9 @ VGS=3.8V
		5.7 @ VGS=3.1V
		7.1 @ VGS=2.5V

FEATURES

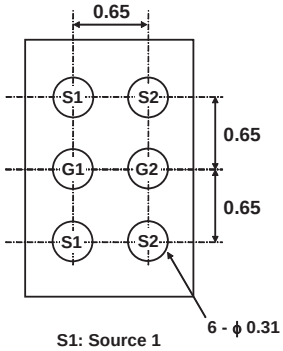
- Super high dense cell design for low $R_{DS(ON)}$.
- Rugged and reliable.
- Wafer level CSP.
- ESD Protected.

WLCSP

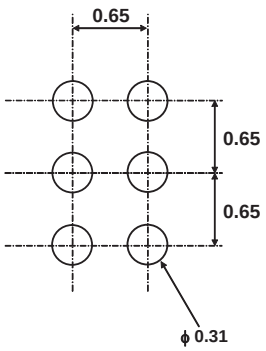
TOP VIEW



BOTTOM VIEW



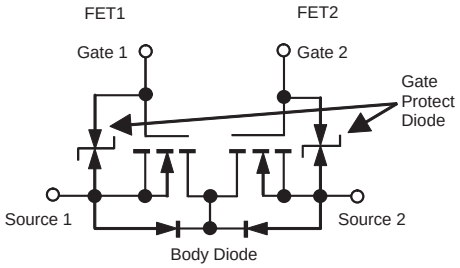
LAND PATTERN (REFERENCE)



Unit : mm

ABSOLUTE MAXIMUM RATINGS (T_A=25°C)

Symbol	Parameter	Limit	Units
V_{SSS}	Source-Source Voltage	12	V
V_{GSS}	Gate-Source Voltage	±8	V
I_S	Source Current-Continuous [c]	8	A
I_{SP}	-Pulsed [a c]	80	A
P_T	Total Power Dissipation	1.3	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	°C



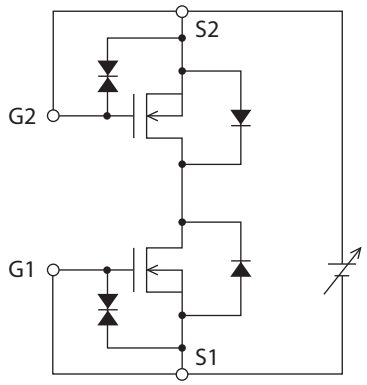
ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{SSS}	Source-Source Breakdown Voltage	V_{GS}=0V , I_S=250uA	12			V
I_{SSS}	Zero Gate Voltage Source Current	V_{SS}=12V , V_{GS}=0V			1	uA
I_{GSS}	Gate-Body Leakage Current	V_{GS}= ±5V , V_{SS}=0V			±1	uA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{SS}=V_{GS} , I_S=1mA	0.5	0.8	1.3	V
$R_{SS(ON)}$	Source-Source On-State Resistance	V_{GS}=4.5V , I_S=4A	3.6	4.6	5.7	m ohm
		V_{GS}=4.0V , I_S=4A	3.7	4.8	5.9	m ohm
		V_{GS}=3.8V , I_S=4A	3.8	4.9	6.3	m ohm
		V_{GS}=3.1V , I_S=4A	4.2	5.7	7.8	m ohm
		V_{GS}=2.5V , I_S=4A	4.8	7.1	11.0	m ohm
g_{FS}	Forward Transconductance	V_{SS}=5V , I_S=4A		16		S
SWITCHING CHARACTERISTICS [b]						
$t_{D(ON)}$	Turn-On Delay Time	V_{DD}=12V I_S=4A V_{GS}=4.0V R_{GEN}=6 ohm		296		ns
t_r	Rise Time			1080		ns
$t_{D(OFF)}$	Turn-Off Delay Time			3267		ns
t_f	Fall Time			2555		ns
Q_g	Total Gate Charge	V_{DD}=12V,I_S=4A, V_{G1S1}=4.0V		18.4		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
V_{FSS}	Diode Forward Voltage	V_{GS}=0V,I_S=2A		0.77	1.2	V

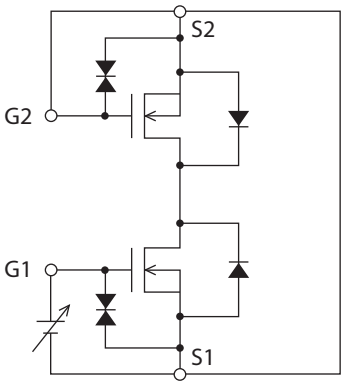
Notes

a.Pulse Test:Pulse Width ≤ 10us, Duty Cycle ≤ 1%.
b.Guaranteed by design, not subject to production testing.
c.Drain current limited by maximum junction temperature.

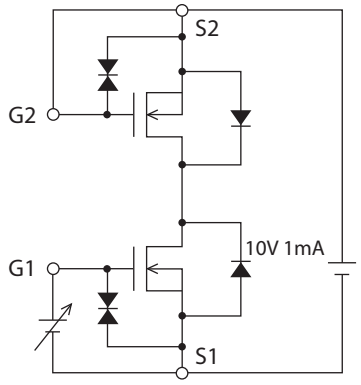
V_{SSS} / I_{SSS}



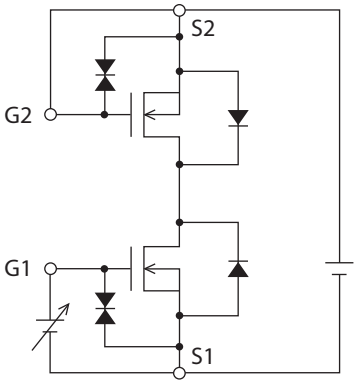
I_{GSS} (+) / (--)



V_{GS} (off)

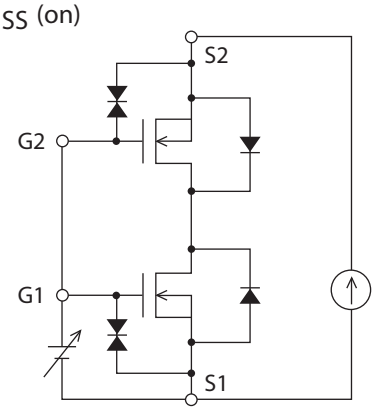


| yfs |

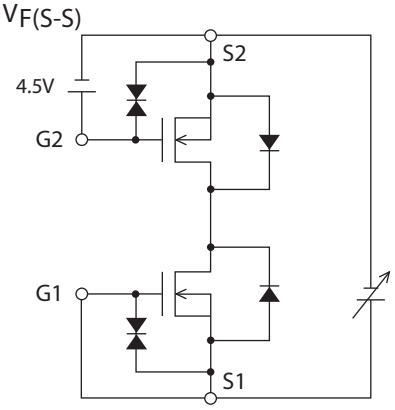


* Note: Connect the mesurement terminal reversely if you want to measure the FET2 side.

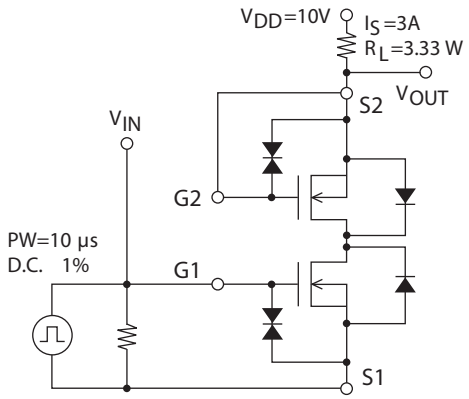
R_{SS} (on)



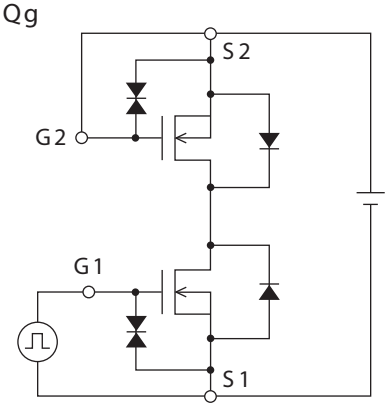
$V_{F(S-S)}$



$t_{d(on)}$, t_r, $t_{d(off)}$, t_f

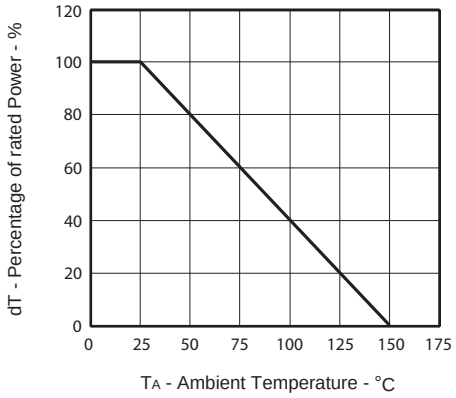


Qg

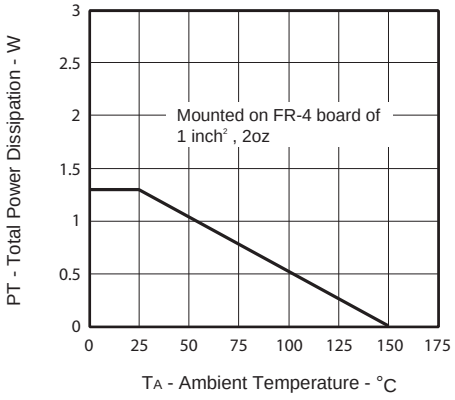


* Note: Connect the mesurement terminal reversely if you want to measure the FET2 side.

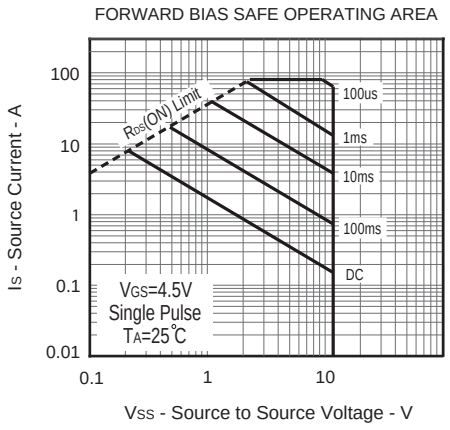
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



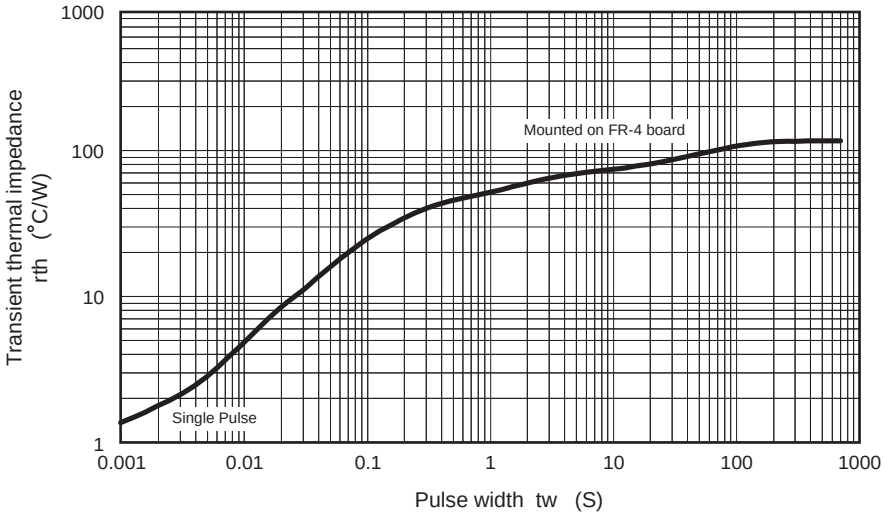
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



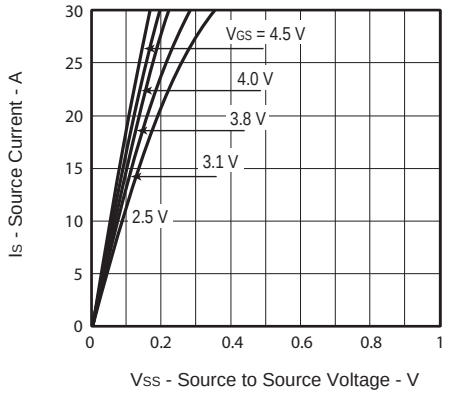
FORWARD BIAS SAFE OPERATING AREA



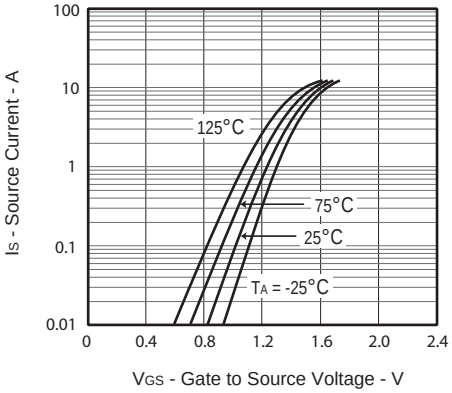
rth - tw



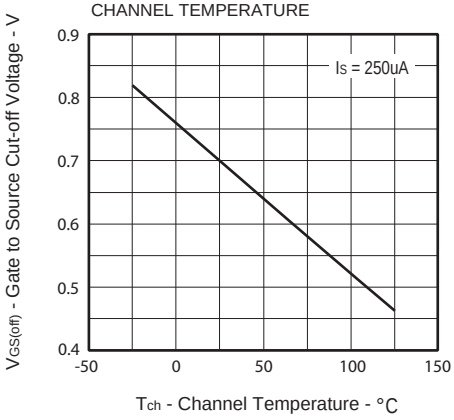
SOURCE CURRENT vs.
SOURCE TO SOURCE VOLTAGE



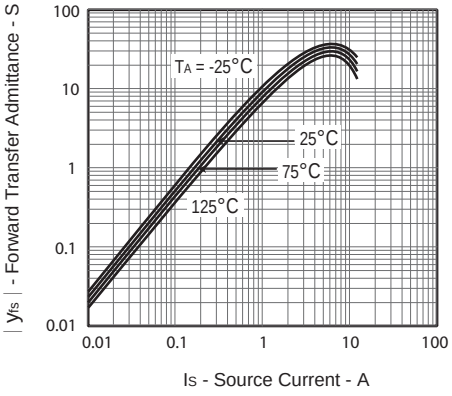
FORWARD TRANSFER CHARACTERISTICS



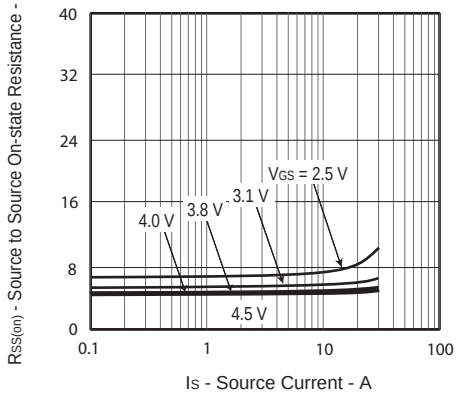
GATEBTO SOURE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



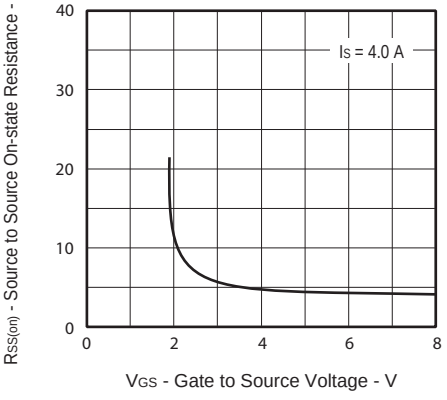
FORWARD TRANSFER ADMITTANCE vs.
SOURCE CURRENT



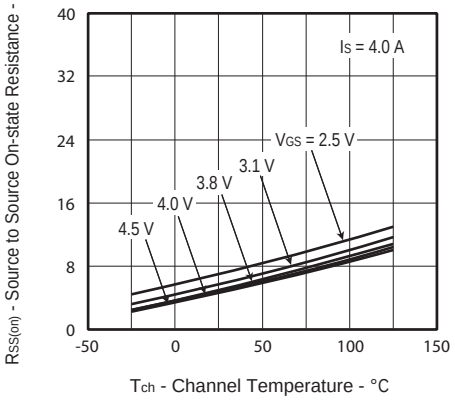
SOURCE TO SOURCE ON-STATE RESISTANCE vs.
SOURCE CURRENT



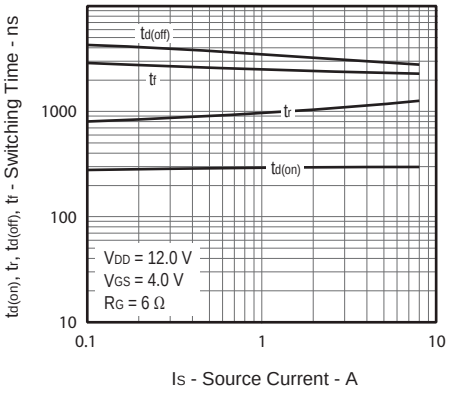
SOURCE TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



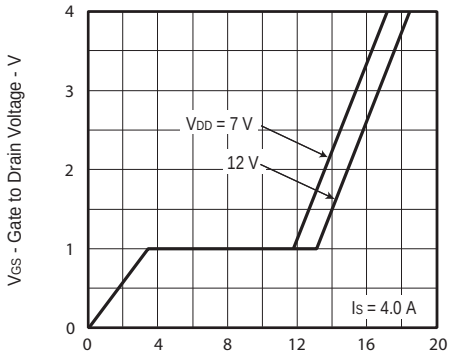
SOURCE TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



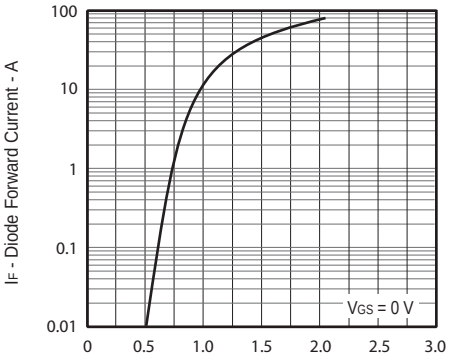
SWITCHING CHARACTERISTICS



DYNAMIC INPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



TOP MARKING DEFINITION

WLCSP

