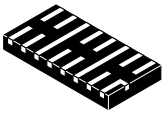
EMI4183MU

Product Preview

Common Mode Filter with ESD Protection

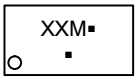
ON Semiconductor®

http://onsemi.com



UDFN16
CASE 517CK

MARKING DIAGRAMS



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(*Note: Microdot may be in either location)

Functional Description

The EMI4183MU is an integrated common mode filter providing both ESD protection and EMI filtering for high speed digital serial interfaces such as MIPI D-PHY.

The EMI4183MU provides protection for three differential data line pairs in a small RoHS-compliant UDFN16 package.

Features

- Highly Integrated Common Mode Filter (CMF) with ESD Protection provides protection and EMI reduction for systems using High Speed Serial Data Lines with cost and space savings over discrete solutions
- Large Differential Mode Bandwidth with Cutoff Frequency > 2 GHz
- High Common Mode Stop Band Attenuation: >25 dB at 700 MHz, >30 dB at 800 MHz
- Provides ESD Protection to IEC61000-4-2 Level 4, ±15 kV Contact Discharge
- Low Channel Input Capacitance Provides Superior Impedance Matching Performance
- Low Profile Package with Small Footprint in UDFN16 2 x 4 mm Pb−Free Package
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- MIPI D-PHY (CSI-2, DSI, etc) in Mobile Phones and Digital Still Cameras

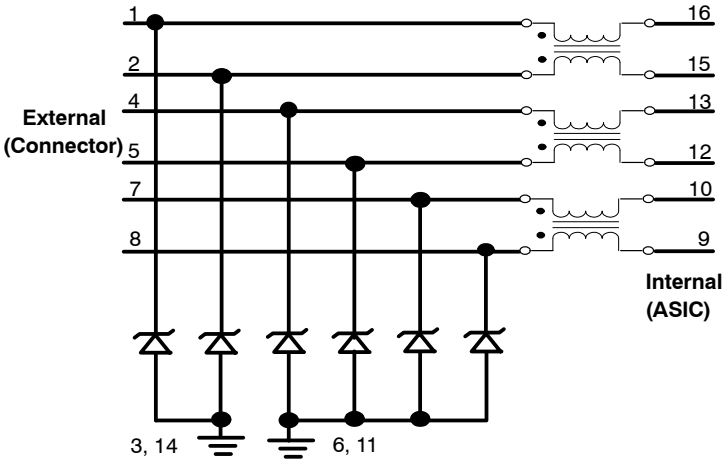
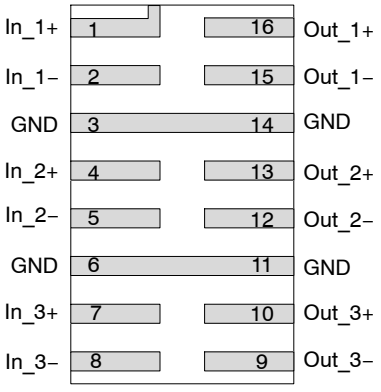


Figure 1. EMI4183MU Electrical Schematic

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
EMI4183MUTAG	UDFN16 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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PIN FUNCTION DESCRIPTION

Pin Name	Pin No.	Type	Description
In_1+	1	I/O	CMF Channel 1+ to Connector (External)
In_1−	2	I/O	CMF Channel 1− to Connector (External)
Out_1+	16	I/O	CMF Channel 1+ to ASIC (Internal)
Out_1−	15	I/O	CMF Channel 1− to ASIC (Internal)
In_2+	4	I/O	CMF Channel 2+ to Connector (External)
In_2−	5	I/O	CMF Channel 2− to Connector (External)
Out_2+	13	I/O	CMF Channel 2+ to ASIC (Internal)
Out_2−	12	I/O	CMF Channel 2− to ASIC (Internal)
In_3+	7	I/O	CMF Channel 3+ to Connector (External)
In_3−	8	I/O	CMF Channel 3− to Connector (External)
Out_3+	10	I/O	CMF Channel 3+ to ASIC (Internal)
Out_3−	9	I/O	CMF Channel 3− to ASIC (Internal)
GND	3, 14	GND	Ground
GND	6, 11	GND	Ground

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Operating Temperature Range	T_{OP}	−40 to +85	°C
Storage Temperature Range	T_{STG}	−65 to +150	°C
Maximum Lead Temperature for Soldering Purposes (1/8” from Case for 10 seconds)	T_L	260	°C
DC Current per Line	I_{LINE}	100	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{LEAK}	Channel Leakage Current	T_A = 25°C, V_{IN} = 5 V, GND = 0 V			1.0	μA
V_F	Channel Negative Voltage	T_A = 25°C, I_F = 10 mA	0.1		1.5	V
C_{IN}	Channel Input Capacitance to Ground (Pins 1,2,4,5,7,8 to Pins 3,6,11,14)	T_A = 25°C, At 1 MHz, GND = 0 V, V_{IN} = 1.65 V		0.8	1.3	pF
R_{CH}	Channel Resistance (Pins 1−16, 2−15, 4−13, 5−12, 7−10 & 8−9)			8.0		Ω
f_{3dB}	Differential Mode Cut−off Frequency	50 Ω Source and Load Termination		2.0		GHz
F_{atten}	Common Mode Stop Band Attenuation	@ 800 MHz		30		dB
V_{ESD}	In−system ESD Withstand Voltage a) Contact discharge per IEC 61000−4−2 standard, Level 4 **(External Pins)** b) Contact discharge per IEC 61000−4−2 standard, Level 1 **(Internal Pins)**	(Notes 1 and 2)	 ±15 ±2			kV
V_{CL}	TLP Clamping Voltage (See Figure 12)	Forward I_{PP} = 8 A Forward I_{PP} = 16 A Forward I_{PP} = −8 A Forward I_{PP} = −16 A		12 18 −6 −12		V V V V
R_{DYN}	Dynamic Resistance Positive Transients Negative Transients	T_A = 25°C, I_{PP} = 1 A, t_P = 8/20 μs Any I/O pin to Ground; (Notes 1 and 3)		 1.36 0.6		
V_{RWM}	Reverse Working Voltage	(Note 3)			5.0	V
V_{BR}	Breakdown Voltage	I_T = 1 mA; (Note 4)	5.6		9.0	V

1. Standard IEC61000−4−2 with $C_{Discharge}$ = 150 pF, $R_{Discharge}$ = 330, GND grounded.
2. These measurements performed with no external capacitor.
3. TVS devices are normally selected according to the working peak reverse voltage (V_{RWM}), which should be equal to or greater than the DC or continuous peak operating voltage level.
4. V_{BR} is measured at pulse test current I_T.

TYPICAL CHARACTERISTICS

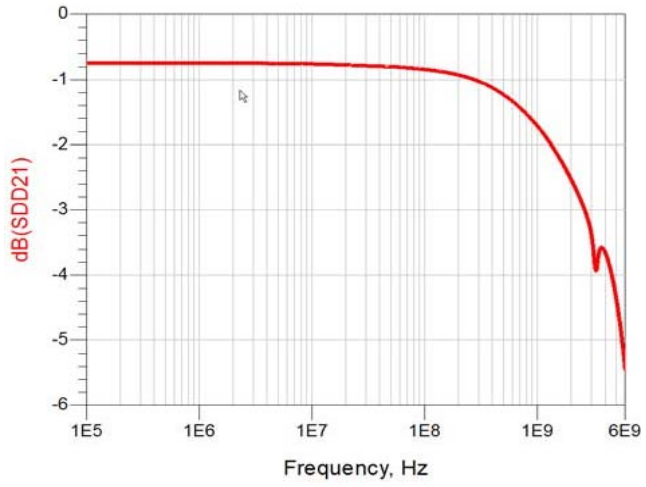


Figure 2. Differential Mode Attenuation vs. Frequency (Zdiff = 100 Ω)

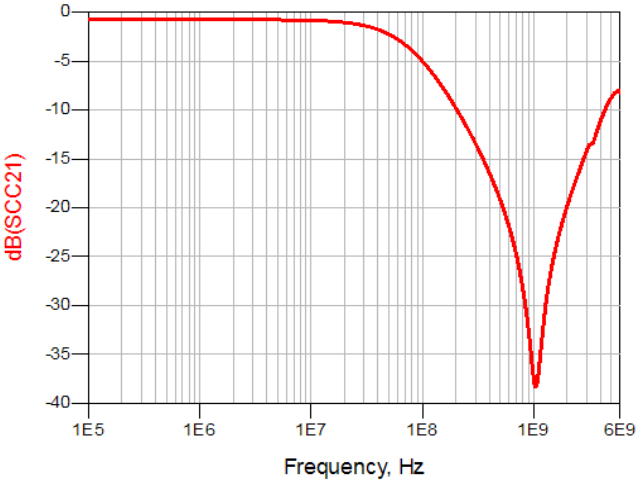


Figure 3. Common Mode Attenuation vs. Frequency (Zcomm = 50 Ω)

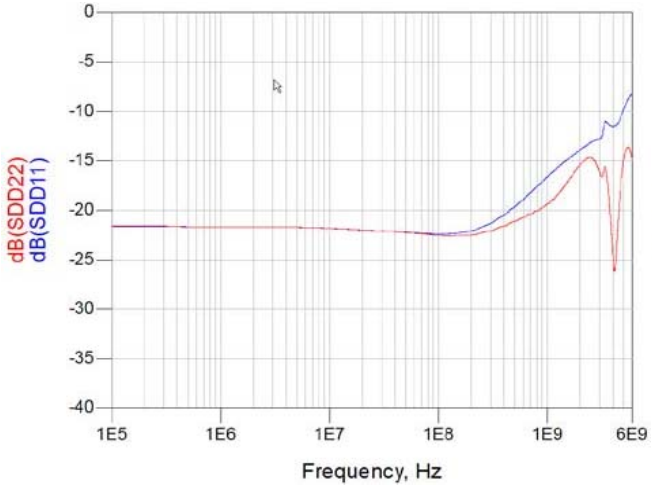


Figure 4. Differential Return Loss vs. Frequency (Zdiff = 100 Ω)

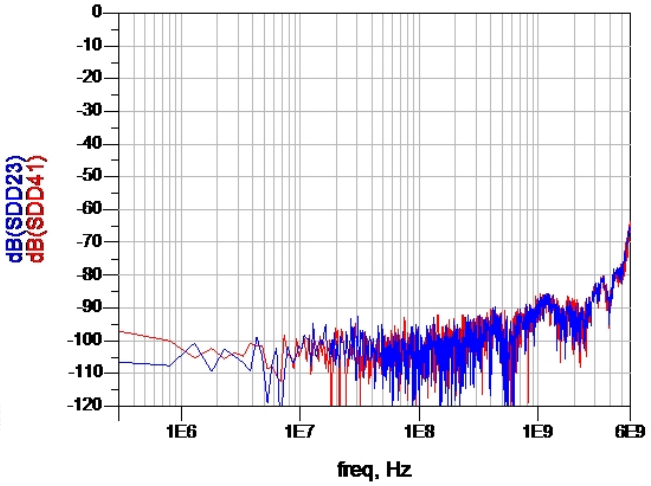


Figure 5. Differential Inter−Lane Cross−Coupling

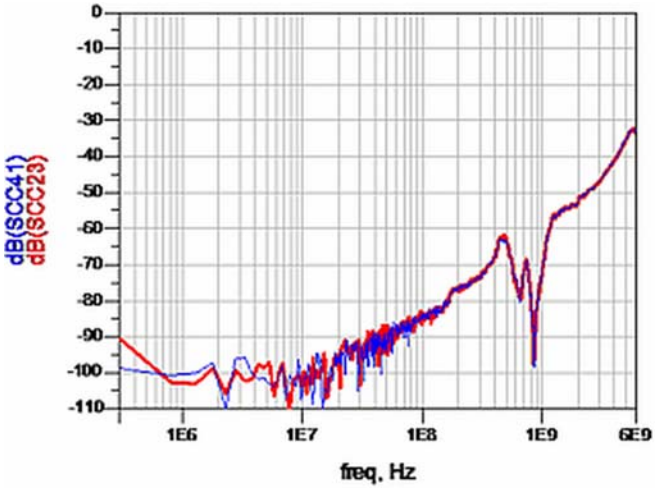


Figure 6. Common Mode Inter−Lane Cross−Coupling

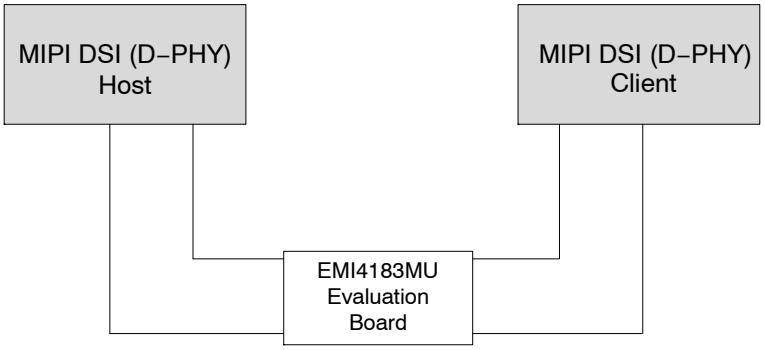


Figure 7. MIPI D−PHY LP Mode Test Setup



Figure 8. EMI4183MU MIPI D−PHY LP Mode Measured Results

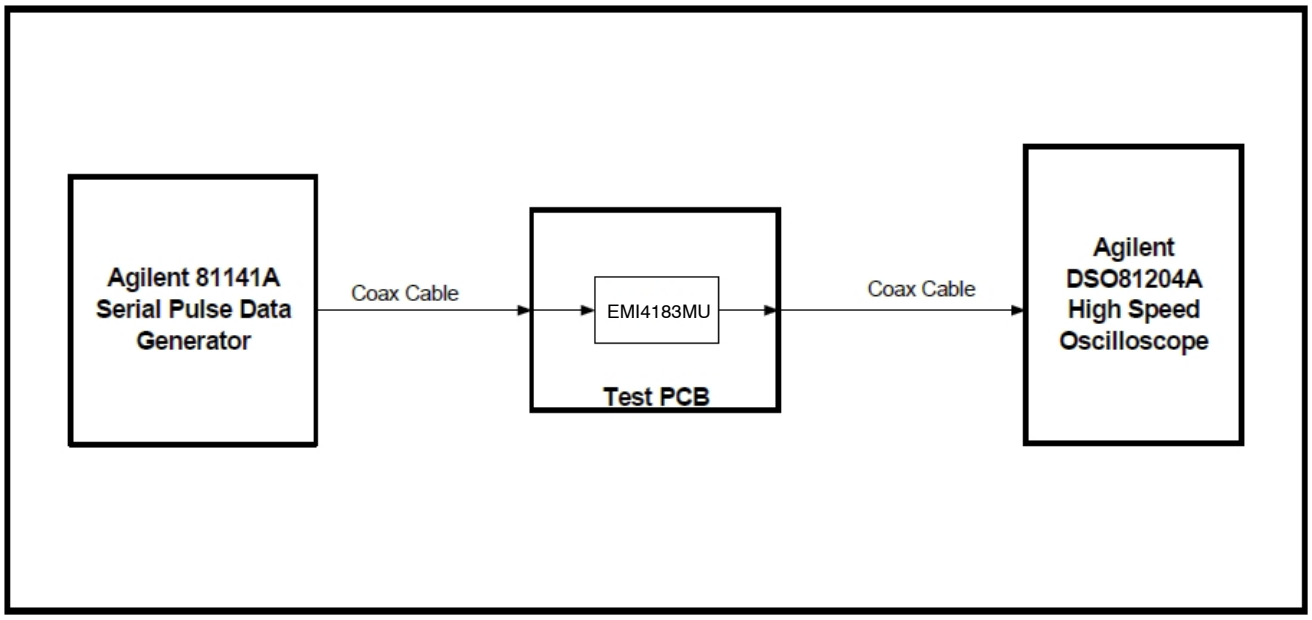


Figure 9. EMI4183MU Eye Diagram Test Setup

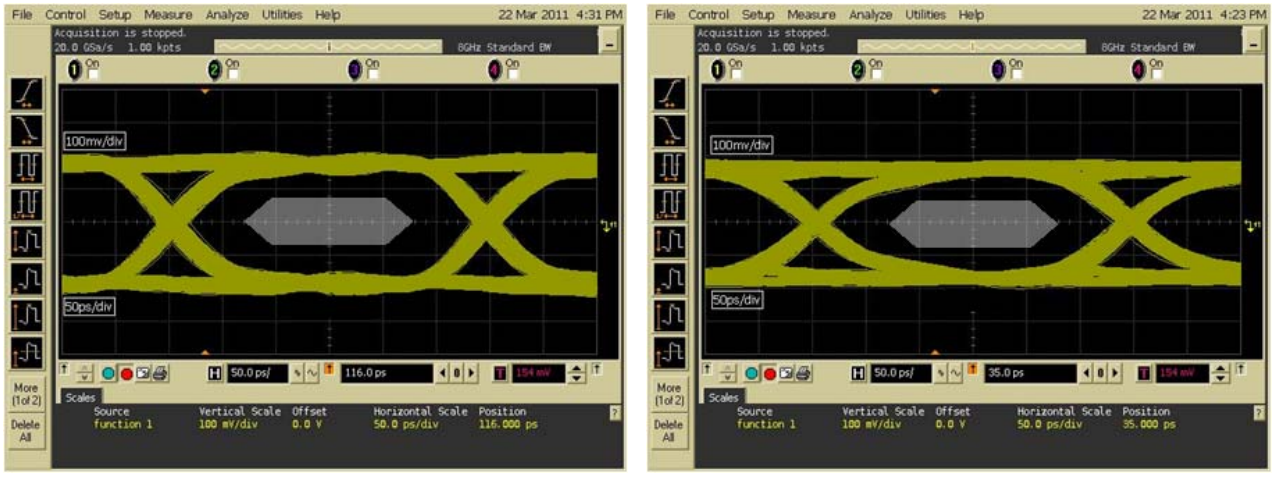


Figure 10. EMI4183MU Measured Eye Diagram @ 3.4Gbps (EVB through on left, EVB with EMI4183MU on right)

Transmission Line Pulse (TLP) Measurements

Transmission Line Pulse (TLP) provides current versus voltage (I-V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 11. TLP I-V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10 s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 12 where an 8 kV IEC61000-4-2 current waveform is compared with TLP current pulses at 8 and 16 A. A TLP curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels. Typical TLP I-V curves for the EMI4183MU are shown in Figure 13.

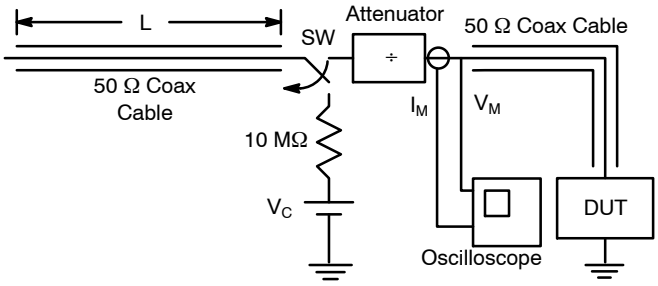


Figure 11. Simplified Schematic of a Typical TLP System

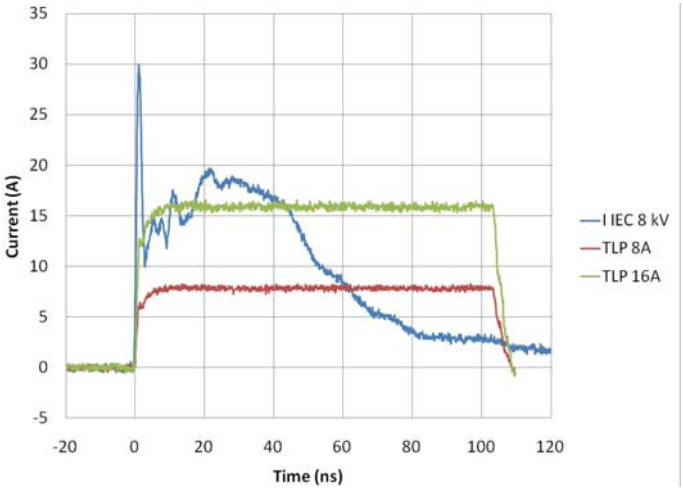


Figure 12. Comparison Between 8 kV IEC61000−4−2 and 8 A and 16 A TLP Waveforms

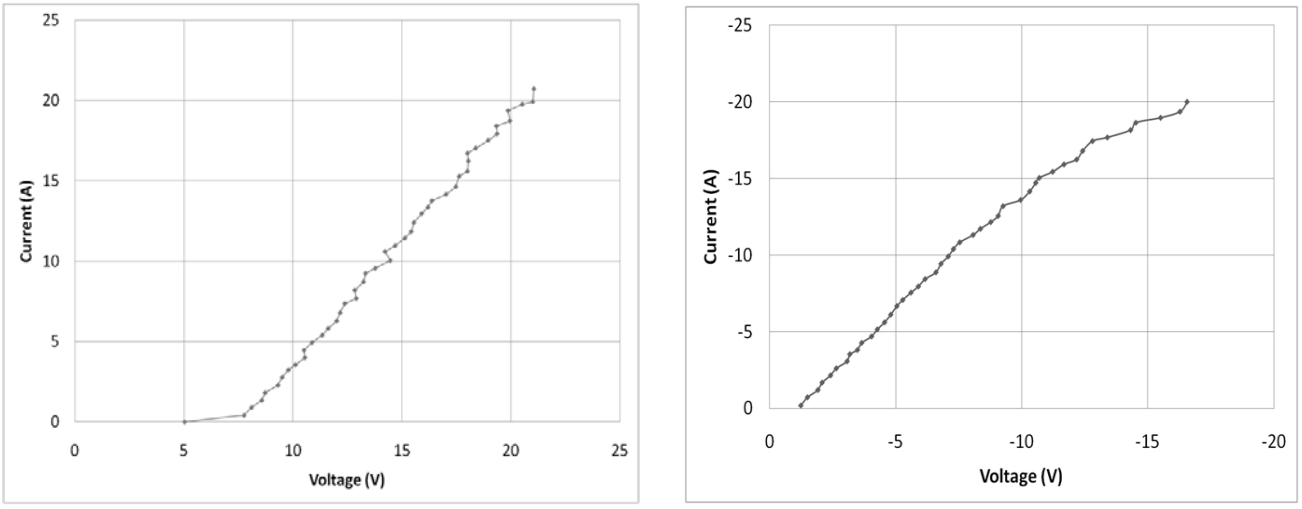


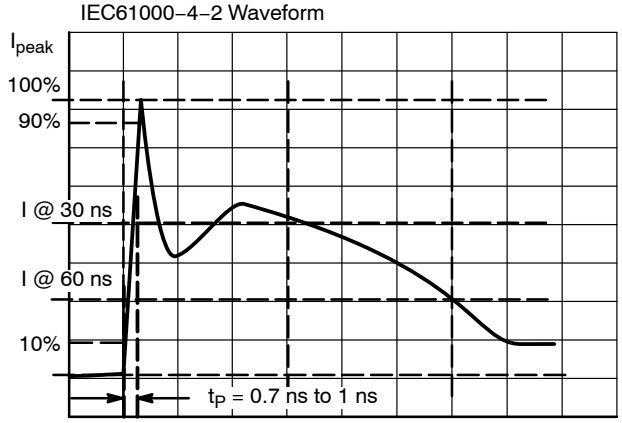
Figure 13. Positive and Negative TLP Waveforms

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to On Semiconductor Application Notes AND8307/D and AND8308/D.

IEC61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8



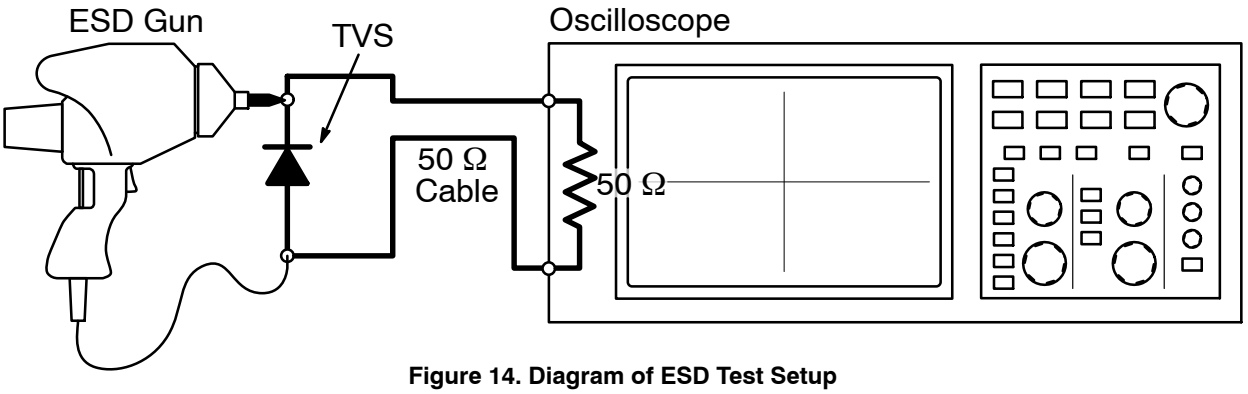


Figure 14. Diagram of ESD Test Setup

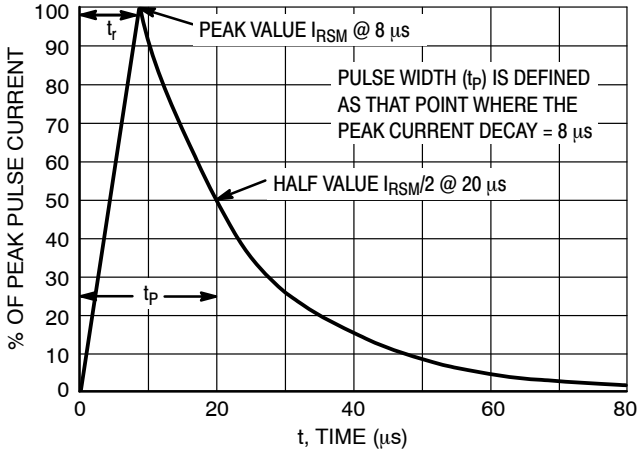


Figure 15. 8 x 20 μs Pulse Waveform

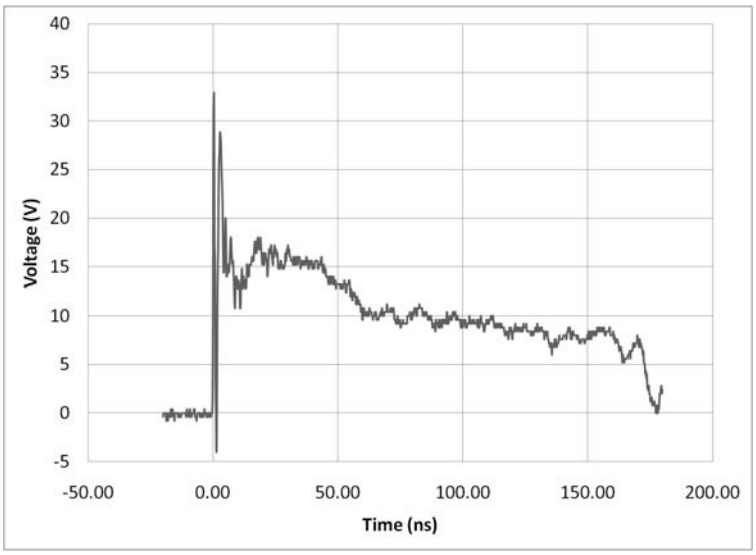


Figure 16. ESD Clamping Voltage +8 kV per IEC6100−4−2 (external to internal pin)

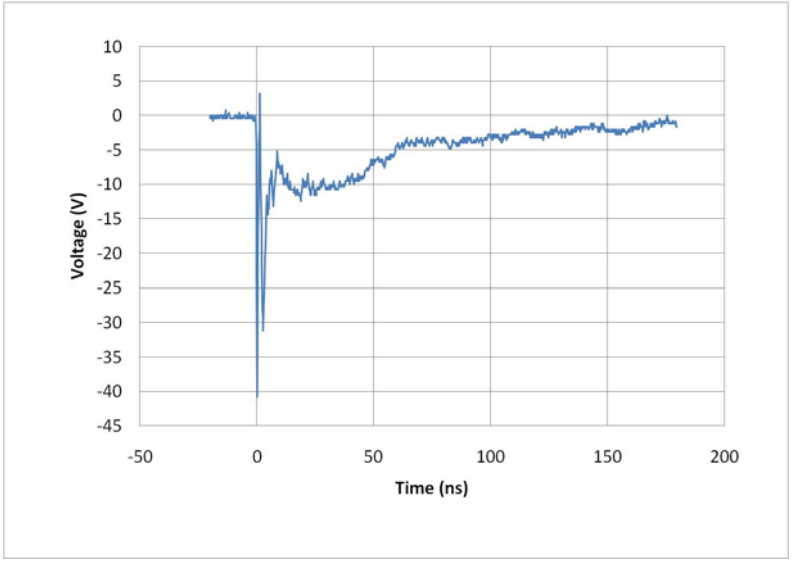


Figure 17. ESD Clamping Voltage −8 kV per IEC6100−4−2 (external to internal pin)

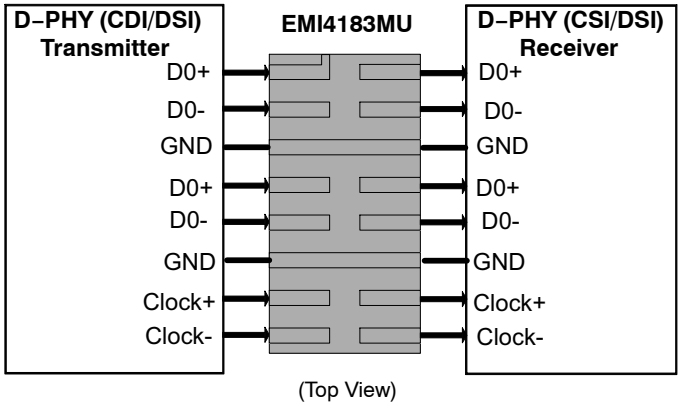
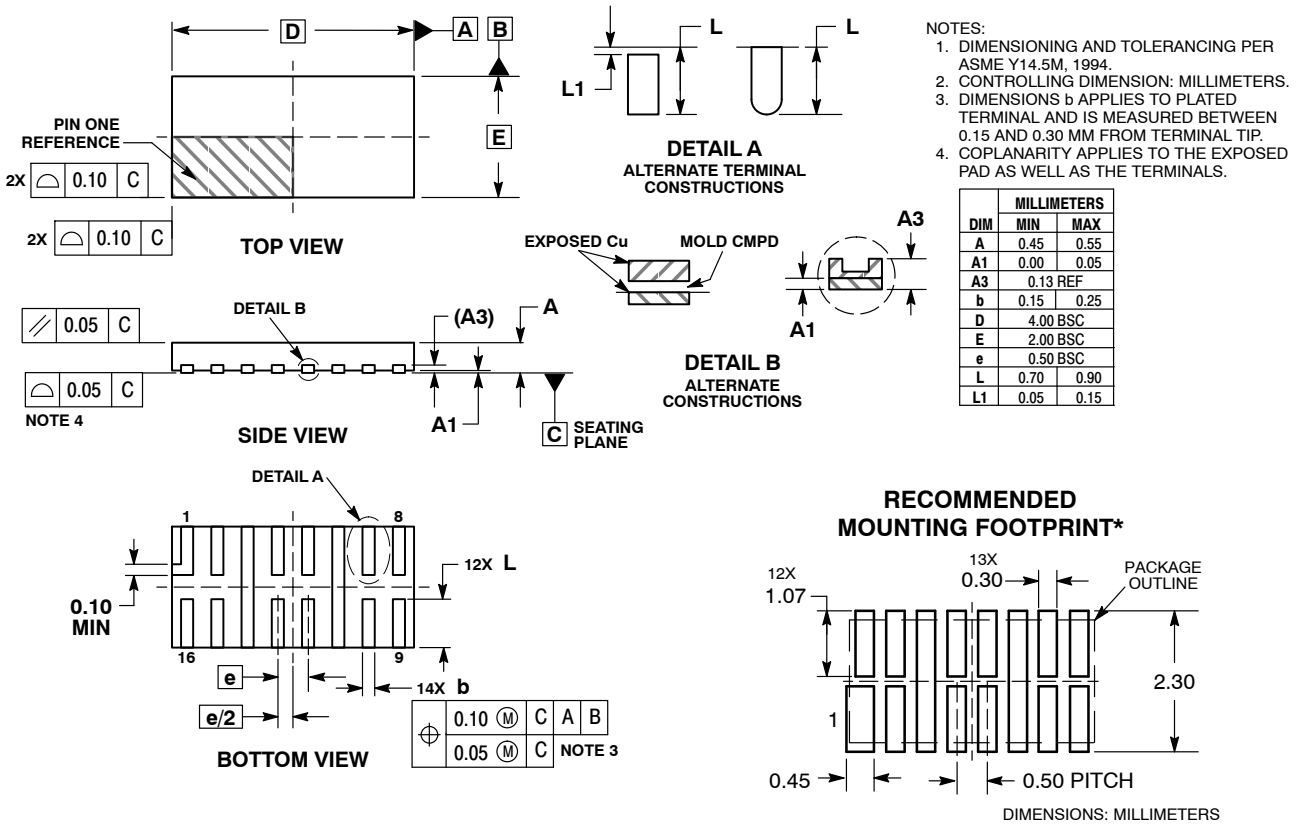


Figure 18. EMI4183MU MIPI D−PHY Application Diagram

EMI4183MU

PACKAGE DIMENSIONS

UDFN16 4x2, 0.5P
CASE 517CK
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.15	0.25
D	4.00 BSC	
E	2.00 BSC	
e	0.50 BSC	
L	0.70	0.90
L1	0.05	0.15

RECOMMENDED MOUNTING FOOTPRINT*

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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