



UNIVERSAL DEMULTIPLEXER/ DECODER

SY100S370

FEATURES

- Max. propagation delay of 1200ps
- IEE min. of -92mA
- Industry standard 100K ECL levels
- Extended supply voltage option:
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75KΩ input pull-down resistors
- 60% faster than National or Signetics
- Approximately 40% lower power than Fairchild
- Function and pinout compatible with Fairchild F100K
- Available in 24-pin CERPAC and 28-pin PLCC packages

DESCRIPTION

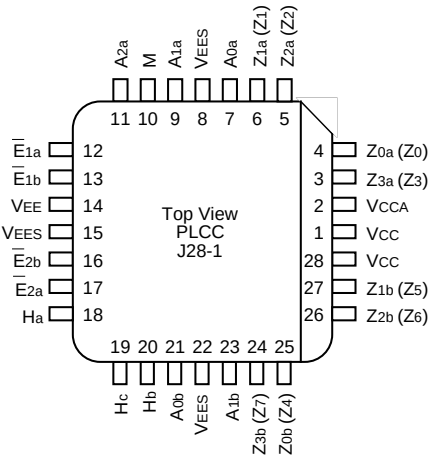
The SY100S370 is a universal demultiplexer/decoder that can be used as either a dual 1-of-4 decoder or as a single 1-of-8 decoder and is designed for use in high-performance ECL systems. The Mode control (M) input determines the function. In the dual 1-of-4 mode, each 4-input group has a pair of active-LOW Enable ($\bar{E}$) inputs. The Enable pins are assigned such that in the single 1-of-8 mode they can be tied together in pairs to result in two active-LOW Enable inputs. $\bar{E}_{1a}$ will be tied to $\bar{E}_{1b}$ and $\bar{E}_{2a}$ to $\bar{E}_{2b}$.

The auxiliary inputs (H_n) are used to determine whether the outputs are active-HIGH or active-LOW. The address inputs for the dual 1-of-4 mode are A_{0a} , A_{1a} , A_{0b} . A_{2a} is unused. In the 1-of-8 mode, the address inputs are A_{0a} , A_{1a} , A_{2a} . The inputs on the device have 75KΩ pull-down resistors.

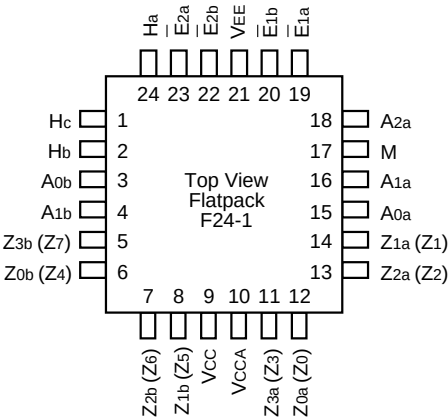
PIN NAMES

Pin	Function
A_{na} , A_{nb}	Address Inputs ($n = 0,1,2$)
$\bar{E}_{na}$, $\bar{E}_{nb}$	Enable Inputs ($n = 1,2$)
M	Mode Control Input
H_a	$Z_0 - Z_3$ ($\bar{Z}_{0a} - \bar{Z}_{3a}$) Polarity Select Input
H_b	$Z_4 - Z_7$ ($\bar{Z}_{0b} - \bar{Z}_{3b}$) Polarity Select Input
H_c	Common Polarity Select Input
$Z_0 - Z_7$	Single 1-of-8 Data Outputs
Z_{na} , Z_{nb}	Dual 1-of-4 Data Outputs ($n = 1...4$)
VEES	VEE Substrate
VCCA	VCCO for ECL Outputs

PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)

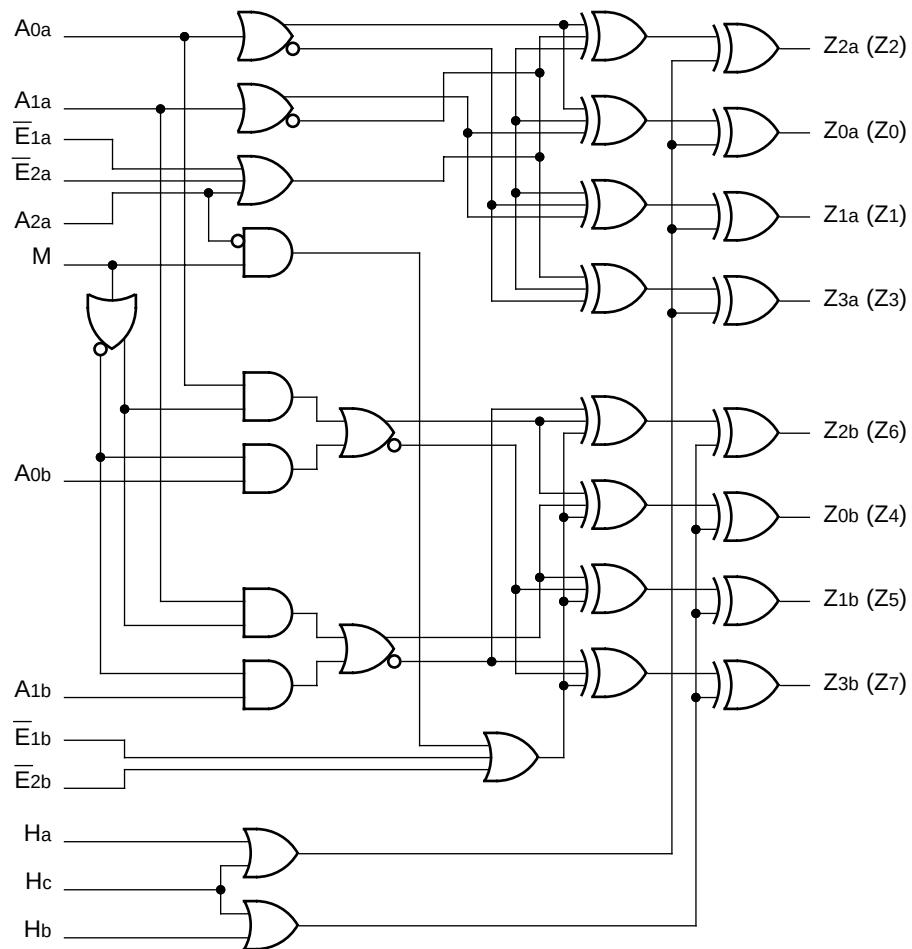


24-Pin Cerpack (F24-1)

Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S370FC	F24-1	Commercial	SY100S370FC	Sn-Pb
SY100S370FCTR ⁽¹⁾	F24-1	Commercial	SY100S370FC	Sn-Pb
SY100S370JC	J28-1	Commercial	SY100S370JC	Sn-Pb
SY100S370JCTR ⁽¹⁾	J28-1	Commercial	SY100S370JC	Sn-Pb
SY100S370JZ ⁽²⁾	J28-1	Commercial	SY100S370JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S370JZTR ^(1, 2)	J28-1	Commercial	SY100S370JZ with Pb-Free bar-line indicator	Matte-Sn

- Notes:
- 1. Tape and Reel.
 - 2. Pb-Free package is recommended for new designs.

BLOCK DIAGRAM

TRUTH TABLES⁽¹⁾

Dual 1-of-4 Mode (M = A2a = Hc = LOW)											
Inputs				Active HIGH Outputs (Ha and Hb Inputs HIGH)				Active LOW Outputs (Ha and Hb Inputs LOW)			
$\bar{E}1a, \bar{E}1b$	$\bar{E}2a, \bar{E}2b$	A1a, A1b	A0a, A0b	Z0a, Z0b	Z1a, Z1b	Z2a, Z2b	Z3a, Z3b	Z0a, Z0b	Z1a, Z1b	Z2a, Z2b	Z3a, Z3b
H	X	X	X	L	L	L	L	H	H	H	H
X	H	X	X	L	L	L	L	H	H	H	H
L	L	L	L	H	L	L	L	L	H	H	H
L	L	L	H	L	H	L	L	H	L	H	H
L	L	H	L	L	L	H	L	H	H	L	H
L	L	H	H	L	L	L	H	H	H	H	L

Single 1-of-8 Mode (M = HIGH; A0b = A1b = Ha = Hb = LOW)												
Inputs					Active HIGH Outputs* (Hc Input HIGH)							
$\bar{E}1$	$\bar{E}2$	A2a	A1a	A0a	Z0	Z1	Z2	Z3	Z4	Z5	Z6	Z7
H	X	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	L	L	L	L	L	L	L	L
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	L	L	H	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	L	H	H	L	L	L	H	L	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H

Note:

1. H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

* for Hc = LOW, output states are complemented

 $\bar{E}1 = \bar{E}1a$ and $\bar{E}1b$ wired; $\bar{E}2 = \bar{E}2a$ and $\bar{E}2b$ wired**DC ELECTRICAL CHARACTERISTICS** $V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current Hc, A0a, A1a, A2a All Others	— —	— —	310 250	μA	$V_{IN} = V_{IH} (Max.)$
I_{EE}	Power Supply Current	-92	-73	-46	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERPACK

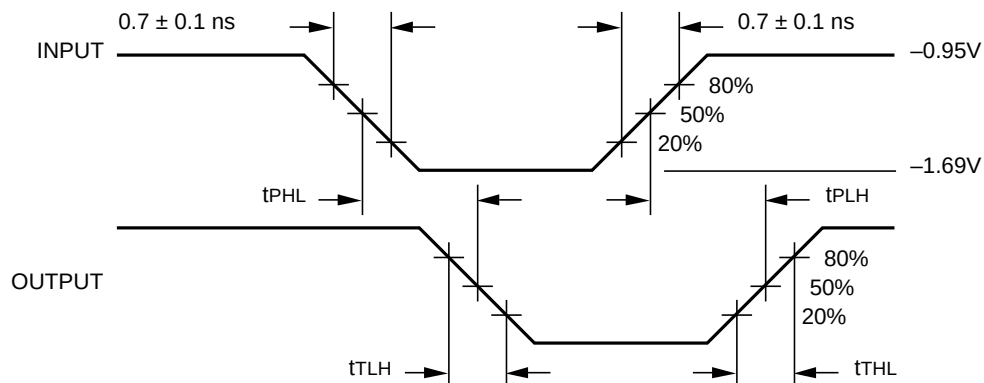
$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_A = 0^{\circ}C$		$T_A = +25^{\circ}C$		$T_A = +85^{\circ}C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
tPLH tPHL	Propagation Delay $\bar{E}_{na}, \bar{E}_{nb}$ to Output	300	1300	300	1300	300	1300	ps	
tPLH tPHL	Propagation Delay A_{na}, A_{nb} to Output	500	1600	500	1600	500	1600	ps	
tPLH tPHL	Propagation Delay H_a, H_b, H_c to Output	500	1600	500	1600	500	1600	ps	
tPLH tPHL	Propagation Delay M to Output	600	2100	600	2100	600	2100	ps	
tTLH tTHL	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

PLCC

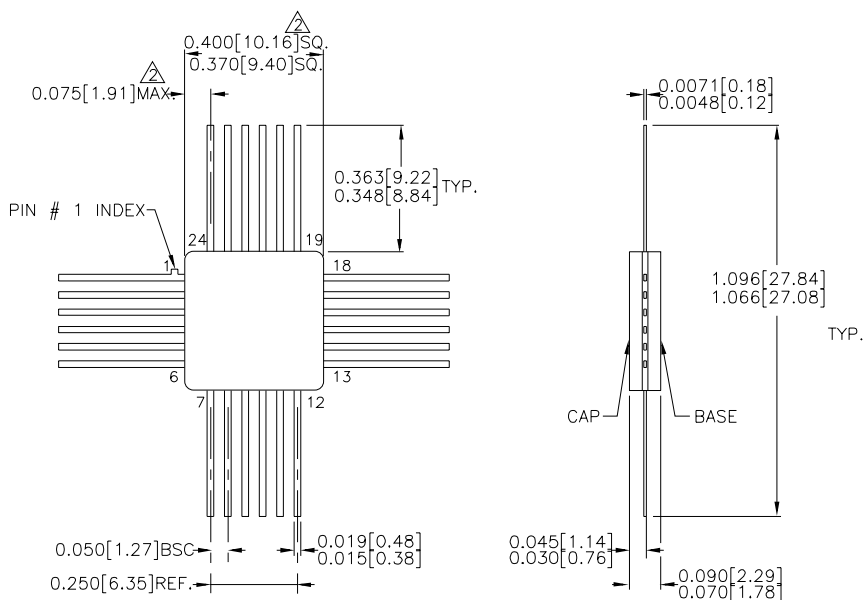
$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_A = 0^{\circ}C$		$T_A = +25^{\circ}C$		$T_A = +85^{\circ}C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
tPLH tPHL	Propagation Delay $\bar{E}_{na}, \bar{E}_{nb}$ to Output	300	1200	300	1200	300	1200	ps	
tPLH tPHL	Propagation Delay A_{na}, A_{nb} to Output	500	1500	500	1500	500	1500	ps	
tPLH tPHL	Propagation Delay H_a, H_b, H_c to Output	500	1500	500	1500	500	1500	ps	
tPLH tPHL	Propagation Delay M to Output	600	2100	600	2100	600	2100	ps	
tTLH tTHL	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

TIMING DIAGRAM**Propagation Delay and Transition Times****Note:**

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$

24-PIN CERPACK (F24-1)

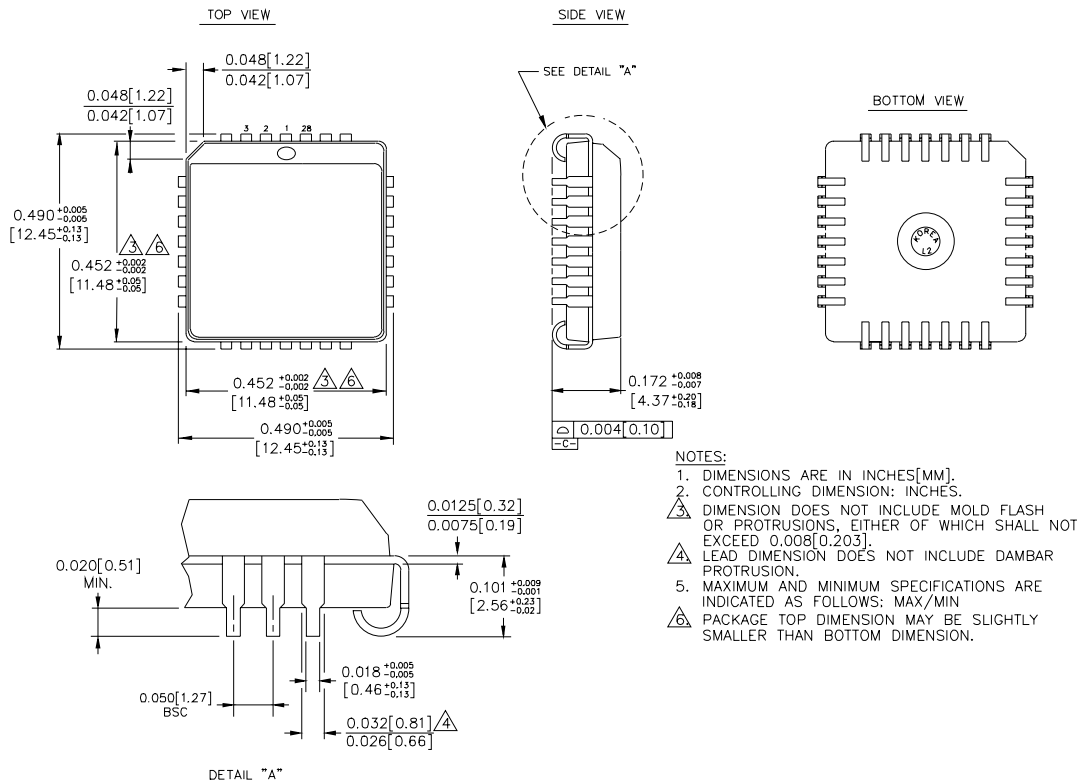


NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.

Rev. 03

28-PIN PLCC (J28-1)



Rev. 03

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