LME49990 Overture™ E-Series
Ultra-low Distortion, Ultra-low Noise Operational Amplifier

Check for Samples: LME49990

FEATURES

- **Easily Drives 600Ω Load**
- **Output Short Circuit Protection**

APPLICATIONS

- **Ultra High Quality Audio Signal Processing**
- **Active Filters**
- **Preamplifiers**
- **Spectrum Analyzers**
- **Ultrasound Preamplifiers**
- **Sigma-Delta ADC/DAC Buffers**
- **The Exposed Pad (DAP) of Unit Should NOT be Grounded. It is Internally Connected to V_{EE}.**

KEY SPECIFICATIONS

- **Input Noise Density (f = 1kHz)**
  - **0.9 nV/√Hz (typ)**
  - **1.3 nV/√Hz (max)**
- **THD+N**
  - **(A_V = 1, V_{OUT} = 3V_{RMS}, f_{IN} = 1kHz) R_L = 600Ω: 0.00001 %**
- **1/f Corner Frequency: 43 Hz (typ)**
- **Slew Rate: ±22 V/µs (max)**
- **Gain Bandwidth**
  - **(A_V = 10^4, R_L = 2kΩ, f = 90kHz) 110 MHz (typ)**
- **PSRR: 144 dB (typ)**
- **CMRR: 137 dB (typ)**
- **Power Supply Voltage Range: ±5V to ±18 V**

DESCRIPTION

The LME49990 is part of the ultra-low distortion, low noise, high slew rate operational amplifier series optimized and fully specified for high performance, high fidelity applications. The LME49990 combines low voltage noise density (0.9nV/√Hz) with vanishing low THD+N (0.00001%). The LME49990 has a high slew rate of ±22V/µs and an output current capability of ±27mA. It drives 600Ω loads to within 2V of either power supply voltage.

The LME49990's outstanding Gain (135dB), CMRR (137dB), PSRR (144dB), and V_{OS} (130µV) give the amplifier excellent operational amplifier DC performance. The LME49990 has a wide supply range of ±5V to ±18V. The LME49990 is unity gain stable and is available in an 8-lead narrow body SOIC and VQFN.

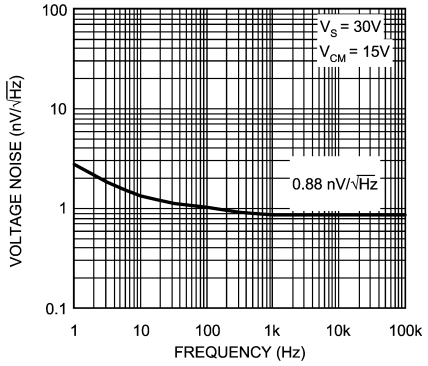


Figure 1. Voltage Noise Spectral Density

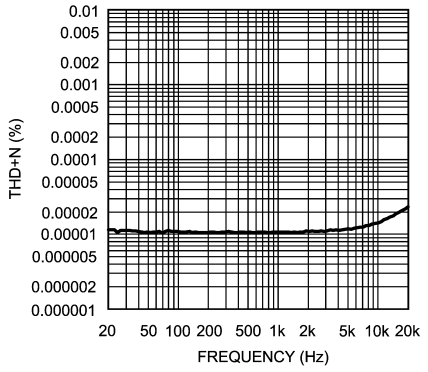


Figure 2. THD+N vs Frequency

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Connection Diagram

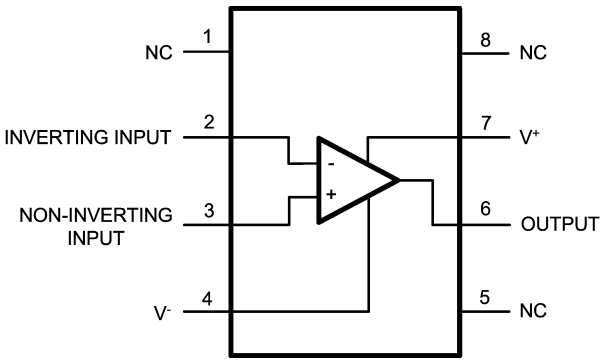


Figure 3. See Package Number D0008A
See Package Number NKQ0008B

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

Power Supply Voltage ($V_S = V^+ - V^-$)	38V
Storage Temperature	−65°C to 150°C
Input Voltage	(V-) - 0.3V to (V+) + 0.3V
Output Short Circuit (3)	Continuous
Power Dissipation	Internally Limited
ESD Rating (4)	2000V
ESD Rating (5)	200V
ESD Rating (6)	1000V
Junction Temperature	150°C
Thermal Resistance	
θ_{JA} (SOIC)	145°C/W
θ_{JA} (VQFN)	52.5°C/W
Soldering Information	
Infrared or Convection (20 sec)	260°C

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Amplifier output connected to GND, any number of amplifiers within a package.
(4) Human body model, applicable std. JESD22-A114C.
(5) Machine model, applicable std. JESD22-A115-A.
(6) Charge device model, applicable std JESD22–C101–A.

OPERATING RATINGS(1)

Temperature Range	
$T_{MIN} \le T_A \le T_{MAX}$	$-40°C \le T_A \le 85°C$
Supply Voltage Range	$\pm 5V \le V_S \le \pm 18V$

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.

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ELECTRICAL CHARACTERISTICS(1)

The following specifications apply for V_S = ±15V, R_L = 2kΩ, f_{IN} = 1kHz, and T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	LME49990		Units (Limits)
			Typical (2)	Limit (3)	
POWER SUPPLY					
V_{CC}	Operating Supply Voltage			±5 ±18	V (min) V (max)
I_{CCQ}	Quiescent Current	V_{CM} = 0V, V_O = 0V, I_O = 0mA V_{CC} = ±5V V_{CC} = ±15V V_{CC} = ±18V	 8 9 9	 10 11 12	 mA (max)
PSRR	Power Supply Rejection Ratio	V_{CC} = ±5V to ±18V T_{MIN}–T_{MAX}	144 137	119 116	dB (min) dB (min)
DYNAMIC PERFORMANCE					
THD+N	Total Harmonic Distortion + Noise	A_V = 1, V_O = 3V_{RMS}, R_L= 1kΩ f = 1kHz f = 20kHz	 0.00001 0.00003	 0.00002	 % (max) %
IMD	Intermodulation Distortion	A_V = 1, V_O = 3V_{RMS} Two-tone 60Hz & 7kHz 4:1	 0.000017		 %
GBWP	Gain Bandwith Product	A_V = 10^4, R_L = 2kΩ, f = 90kHz	110		MHz
FPBW	Full Power Bandwidth	A_V = –1, V_O = 20V_{PP}, R_L = 1kΩ	291		kHz
SR	Slew Rate	A_V = –1, V_O = 20V_{PP} R_L = 1kΩ	 22	 16.5	 V/µs (min)
t_s	Settling time	A_V = –1, V_O = 10V_{PP}, R_L = 1kΩ 0.01%	 590		 ns
A_{VOL}	Open-Loop Gain	V_O = ±10V			
		R_L = 2kΩ T_{MIN} – T_{MAX}	135 124	120	dB (min) dB
		R_L = 600Ω T_{MIN} – T_{MAX}	130 122	120	dB (min) dB
NOISE					
e_N	Input Noise Voltage Density	f = 10Hz	1.4		nV/√Hz
		f = 100Hz	1.0		nV/√Hz
		f = 1kHz	0.88	1.3	nV/√Hz (max)
		f = 10kHz	0.88		nV/√Hz
V_NOISE	RMS Voltage Noise	BW = 0.1Hz to 10Hz BW = 10Hz to 20kHz BW = 10Hz to 1MHz	30 0.12 1	 0.2 1.2	nV_{PP} µV (max) µV (max)
i_N	Input Current Noise Density	f = 1kHz	2.8		pA/√Hz

(1) The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured

(2) Typical values represent most likely parametric norms at T_A = +25ºC, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.

(3) Datasheet min/max specification limits are specified by test or statistical analysis.

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ELECTRICAL CHARACTERISTICS[1] (continued)

The following specifications apply for V_S = ±15V, R_L = 2kΩ, f_{IN} = 1kHz, and T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	LME49990		Units (Limits)
			Typical [2]	Limit [3]	
INPUT CHARACTERISTICS					
V_{OS}	Offset Voltage	V_{CC} = ±18V, V_{CM} = 0v, V_O = 0V V_{CC} = ±18V, T_{MIN} – T_{MAX}	130 300	1000 2000	µV (max) µV (max)
V_{OS} Drift	Input Offset Voltage Drift vs Temperature ($\Delta V_{OS}/\Delta$Temp)	V_{CC} = ±18V, T_{MIN} – T_{MAX}	2		µV/°C
I_{BIAS}	Input Bias Current	V_{CC} = ±18V, V_{CM} = 0v, V_O = 0V V_{CC} = ±18V, T_{MIN} – T_{MAX}	30 150	500 1000	nA (max) nA (max)
I_{OS}	Input Offset Current	V_{CC} = ±18V, V_{CM} = 0v, V_O = 0V V_{CC} = ±18V, T_{MIN} – T_{MAX}	35 95	400 1000	nA (max) nA (max)
V_{IN-CM}	Common-Mode Input Voltage Range		12	11	V (min)
CMRR	Common-Mode Rejection	–10V<V_{CM}<10V T_{MIN} – T_{MAX}	137 132	118 110	dB (min) dB (min)
OUTPUT CHARACTERISTICS					
V_{OUT}	Output Voltage Swing	V_{CC} = ±15V, R_L = 2kΩ V_{CC} = ±15V, R_L = 600Ω V_{CC} = ±18V, R_L = 600Ω	±13 ±13 ±16	12.5 12 14.0	V (min) V (min) V (min)
I_{SHIRT}	Output Short-Circuit Current	V_{CC} = ±18V	+75/-70	+55/-50	mA (min)
I_{OUT}	Output Current	V_{CC} = ±18V, R_L = 600Ω	26	24	mA (min)

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TYPICAL PERFORMANCE CHARACTERISTICS

THD+N vs Output Voltage
V_{CC} = –V_{EE} = 15V, R_L = 2kΩ

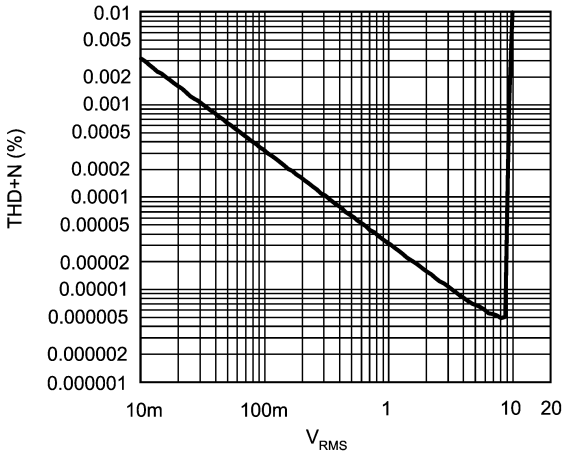


Figure 4.

THD+N vs Output Voltage
V_{CC} = –V_{EE} = 18V, R_L = 2kΩ

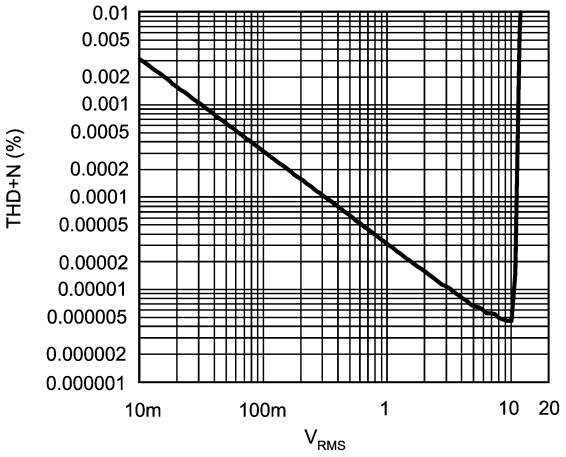


Figure 5.

THD+N vs Output Voltage
V_{CC} = –V_{EE} = 5V, R_L = 2kΩ

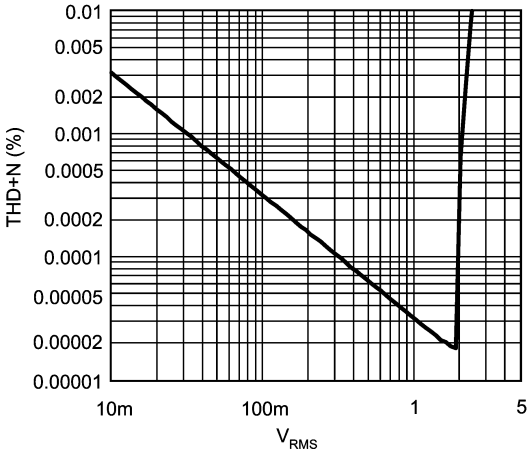


Figure 6.

THD+N vs Output Voltage
V_{CC} = –V_{EE} = 15V, R_L = 600Ω

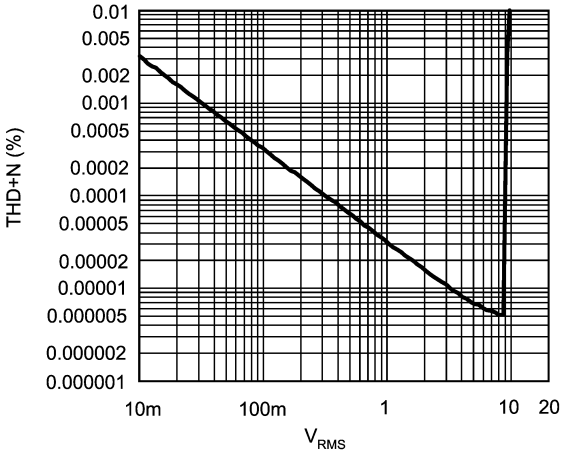


Figure 7.

THD+N vs Output Voltage
V_{CC} = –V_{EE} = 18V, R_L = 600Ω

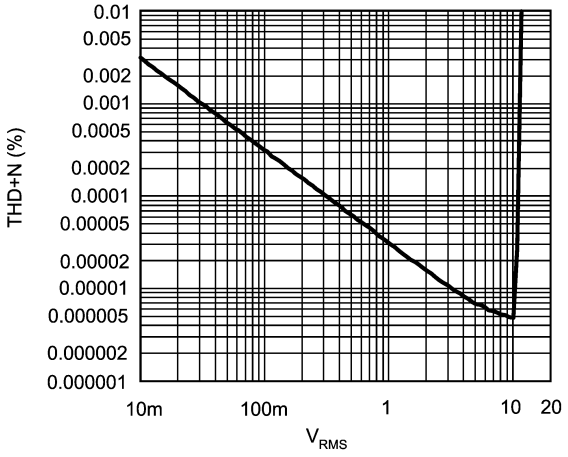


Figure 8.

THD+N vs Output Voltage
V_{CC} = –V_{EE} = 5V, R_L = 600Ω

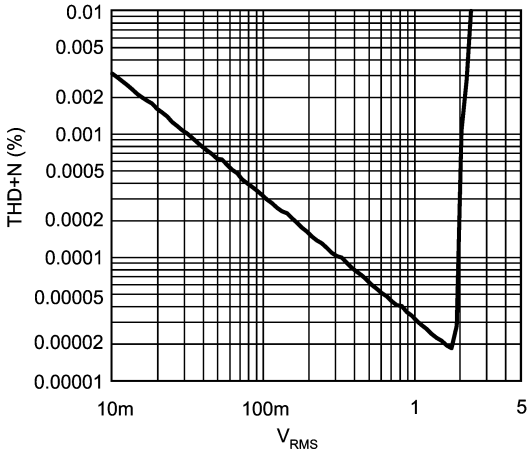


Figure 9.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

THD+N vs Frequency
V_{CC} = −V_{EE} = 15V,
R_L = 2kΩ, V_{OUT} = 3V_{RMS}

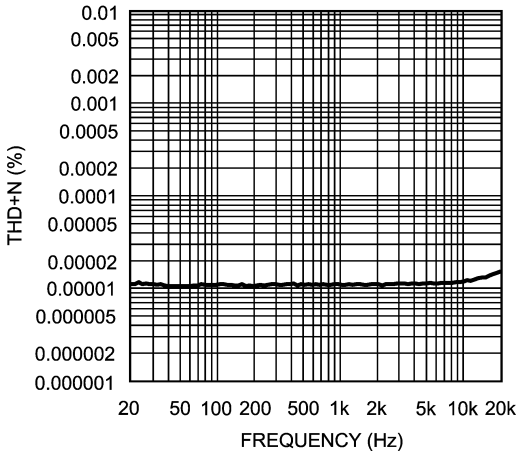


Figure 10.

THD+N vs Frequency
V_{CC} = −V_{EE} = 18V,
R_L = 2kΩ, V_{OUT} = 3V_{RMS}

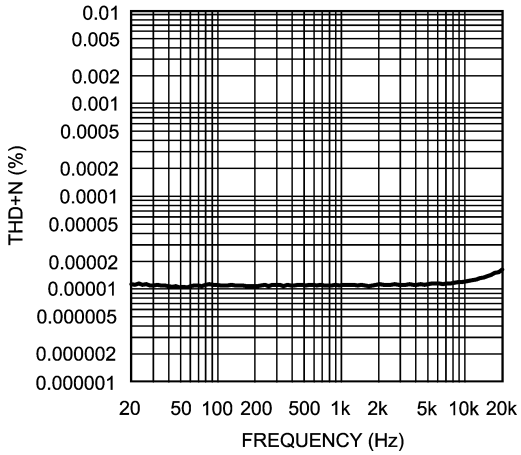


Figure 11.

THD+N vs Frequency
V_{CC} = −V_{EE} = 15V,
R_L = 600Ω, V_{OUT} = 3V_{RMS}

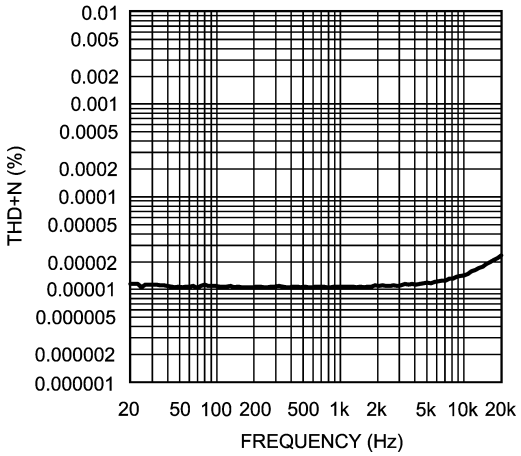


Figure 12.

THD+N vs Frequency
V_{CC} = −V_{EE} = 18V,
R_L = 600Ω, V_{OUT} = 3V_{RMS}

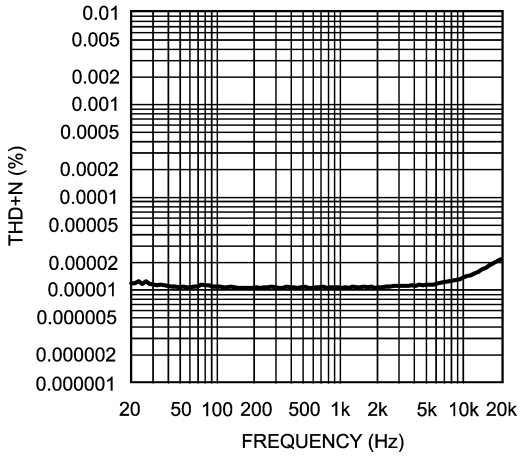


Figure 13.

IMD vs Output Voltage
V_{CC} = −V_{EE} = 15V, R_L = 2kΩ

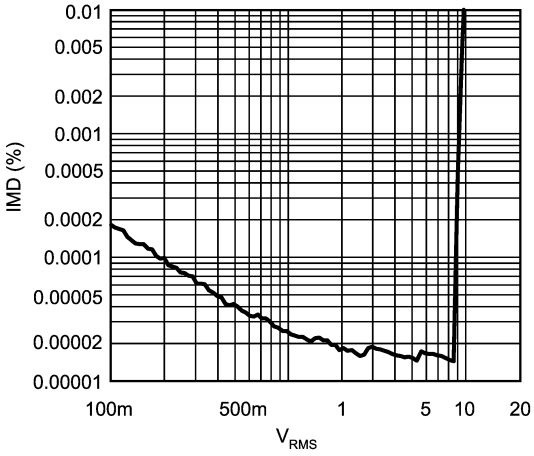


Figure 14.

IMD vs Output Voltage
V_{CC} = −V_{EE} = 18V, R_L = 2kΩ

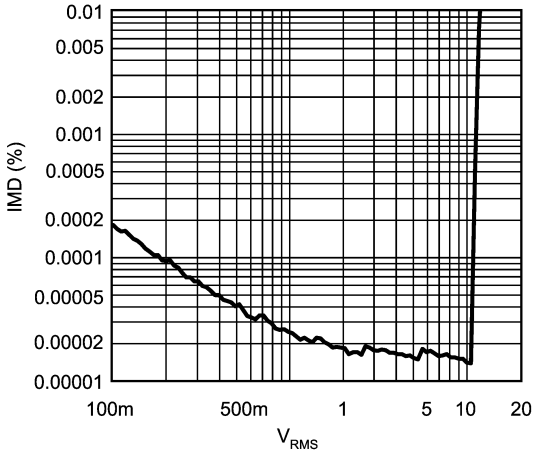


Figure 15.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

IMD vs Output Voltage
V_{CC} = –V_{EE} = 5V, R_L = 2kΩ

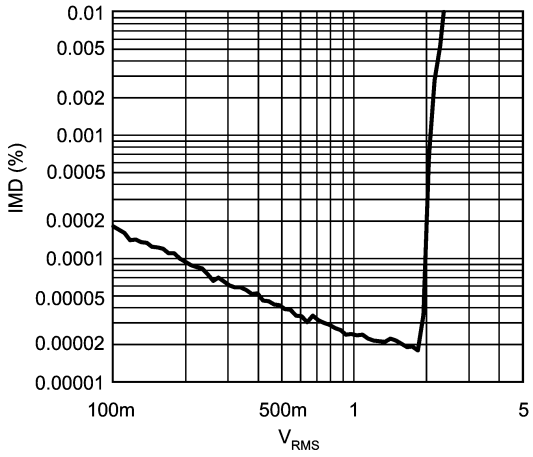


Figure 16.

IMD vs Output Voltage
V_{CC} = –V_{EE} = 15V, R_L = 600Ω

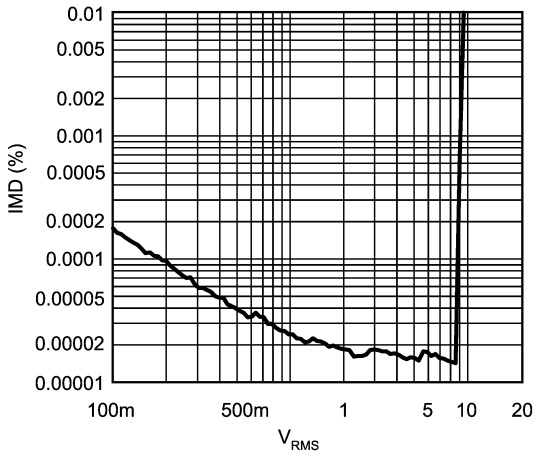


Figure 17.

IMD vs Output Voltage
V_{CC} = –V_{EE} = 18V, R_L = 600Ω

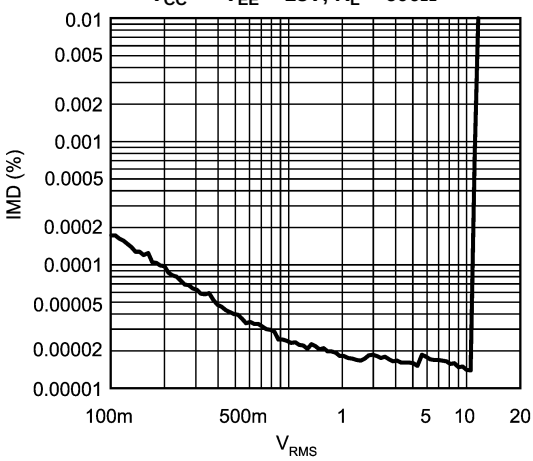


Figure 18.

IMD vs Output Voltage
V_{CC} = –V_{EE} = 5V, R_L = 600Ω

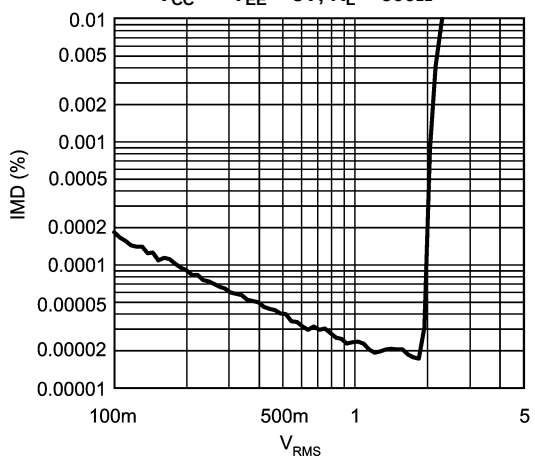


Figure 19.

Voltage Noise Density vs Frequency

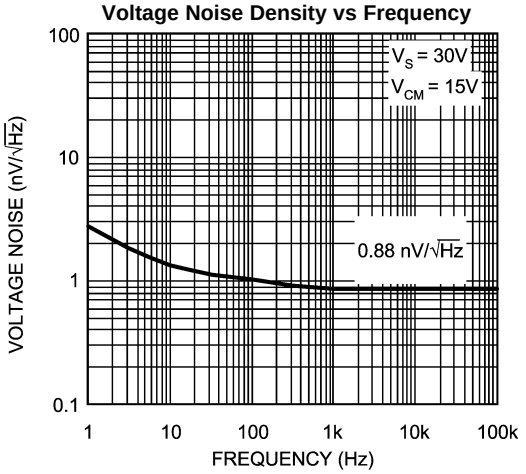


Figure 20.

Current Noise Density vs Frequency

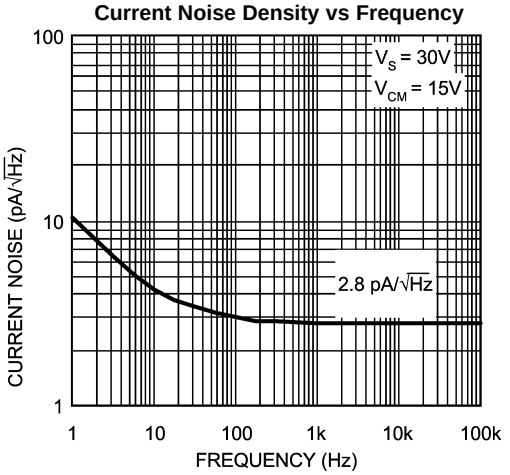


Figure 21.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

PSRR vs Frequency
V_{CC} = –V_{EE} = 15V,
R_L = 2kΩ, V_{RIPPLE} = 200mVpp

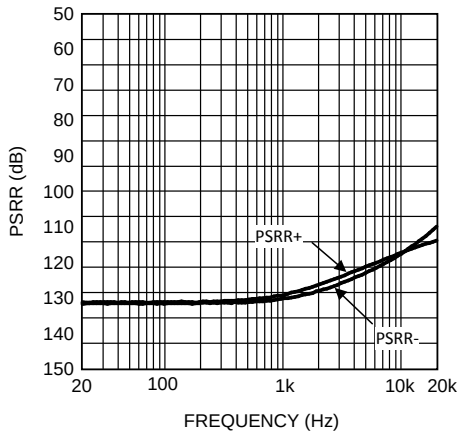


Figure 22.

+PSRR vs Frequency

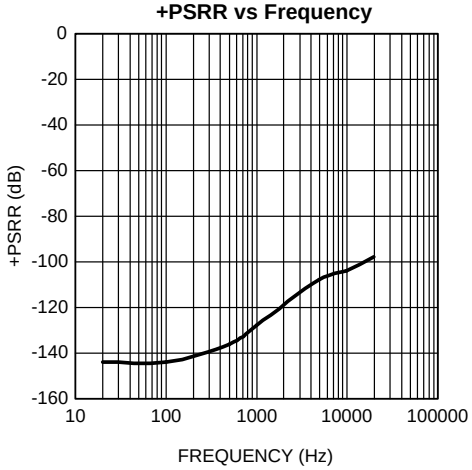


Figure 23.

—PSRR vs Frequency

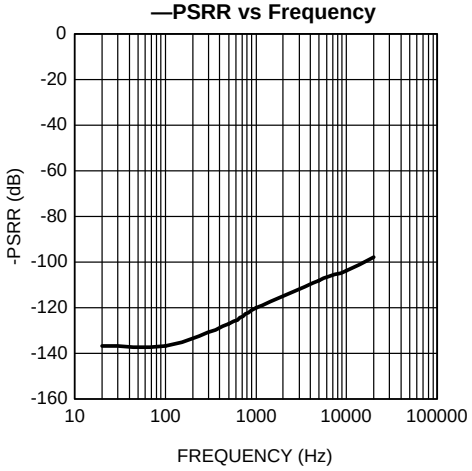


Figure 24.

Output Voltage vs Supply Voltage
R_L = 2kΩ, THD+N = 1%

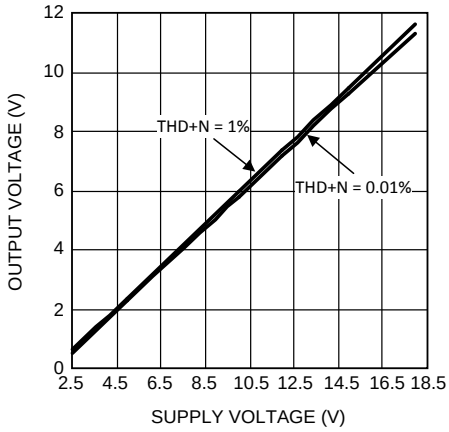


Figure 25.

Output Voltage vs Supply Voltage
R_L = 600Ω, THD+N = 1%

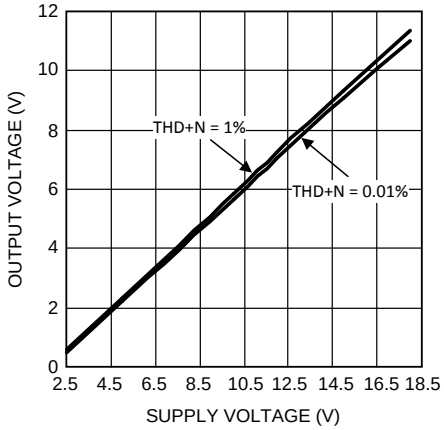


Figure 26.

Large-Signal Transient Response
A_V = –1, C_L = 100pF

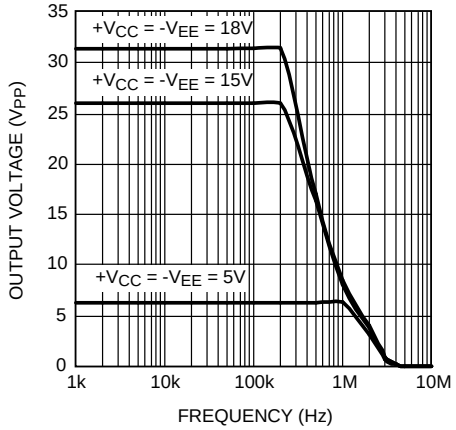


Figure 27.

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APPLICATION HINTS

OUTPUT DRIVE AND STABILITY

The LME49990 is unity gain stable from both input (both stable when gain = -1 or gain = 1). It able to drive resistive load 600Ω with output circuit with a typical 27mA. Capacitive loads up to 100pF will cause little change in the phase characteristics of the amplifiers and are therefore allowable.

Capacitive loads greater than 100pF must be isolated from the output. The most straight forward way to do this is to put a resistor in series with the output. This resistor will also prevent excess power dissipation if the output is accidentally shorted.

The effective load impedance (including feedback resistance) should be kept above 600Ω for fast settling. Load capacitance should also be minimized if good settling time is to be optimized. Large feedback resistors will make the circuit more susceptible to stray capacitance, so in high-speed applications keep the feedback resistors in the 1kΩ to 2 kΩ range whenever practical.

OUTPUT COMPENSATION

In most of the audio applications, the device will be operated in a room temperature and compensation networks are not necessary. However, the consideration of output network as shown in Figure 28 may be taken into account for some of the high performance audio applications such as high speed data conversion or when operating in a relatively low junction temperature. The compensation network will also provide a small improvement in settling time for the response time demanding applications.

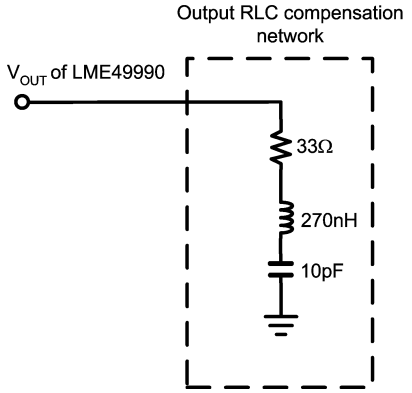


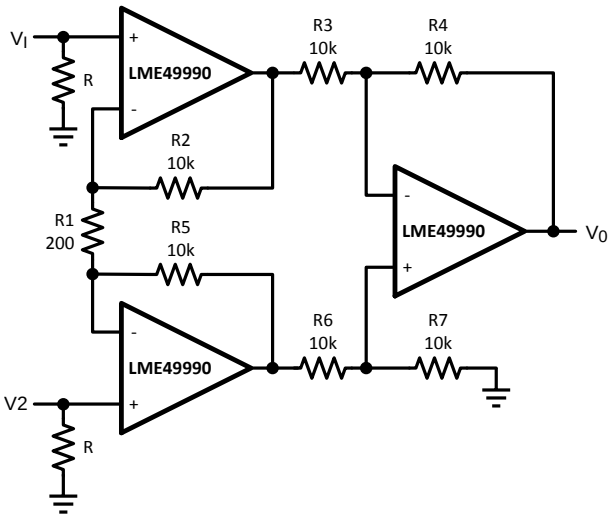
Figure 28. LME4990 Output Compensation Network

SUPPLY BYPASSING

To achieve a low noise and high-speed audio performance, power supply bypassing is extremely important. Applying multiple bypass capacitors is highly recommended. From experiment results, a 10μF tantalum, 2.2μF ceramic, and a 0.47μF ceramic work well. All bypass capacitors leads should be very short. The ground leads of capacitors should also be separated to reduce the inductance to ground. To obtain the best result, a large ground plane layout technique is recommended and it was applied in the LME49990 evaluation board.

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Typical Applications



If R2 = R5, R3 = R6, R4 = R7

$$V0 = \left(1 + \frac{2R2}{R1}\right)\frac{R4}{R3}(V2 - V1)$$

Illustration is:

V0 = 101(V2 − V1)

Figure 29. Balanced Input Mic Amp

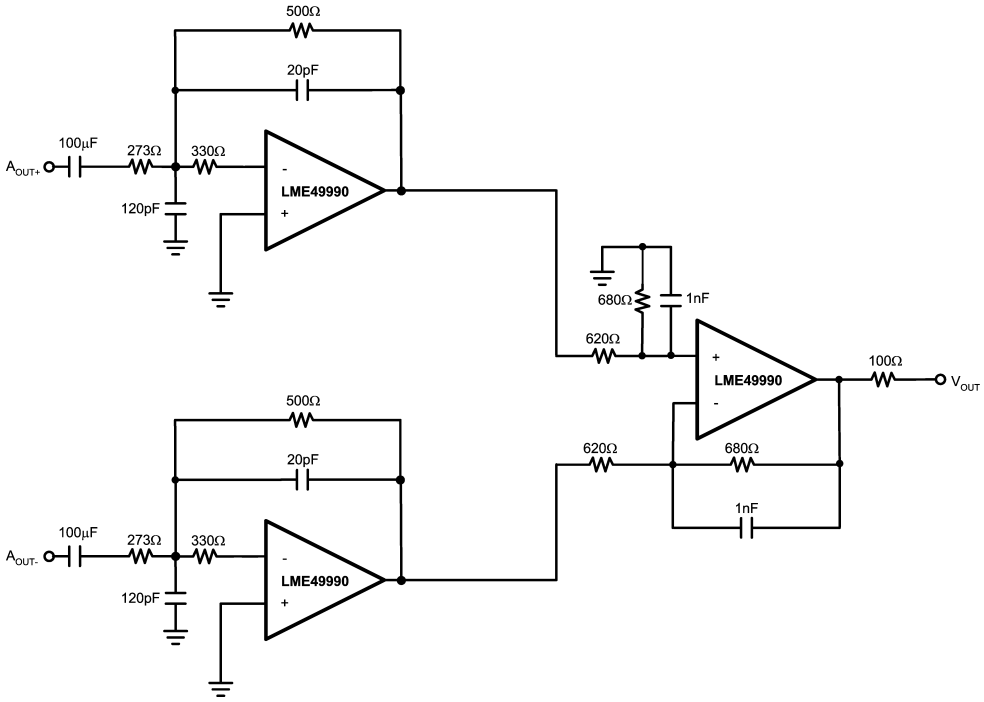


Figure 30. MFB 3rd Order PCM LPF

Application Information

SETTLING TIME AND SLEW RATE MEASUREMENTS

The settling time of LME49990 may be verified using the test circuit in Figure 31. The LME49990 is connected for inverting operation, and the output voltage is summed with the input voltage step. When the LME49990's output voltage is equal to the input voltage, the voltage on the PROBE 1 will be zero. Any voltage appearing at this point will represent an error. And the settling time is equal to the time required for the error signal displayed on the oscilloscope to decay to less than one-half the necessary accuracy (See Settling Time – Output Swing photo). For a 10V input signal, settling time to 0.01% (1mV) will occur when the displayed error is less than 0.5mV. Since settling time is strongly dependent on slew rate, settling will be faster for smaller signal swings. The LME49990's inverting slew rate is faster than its non-inverting slew rate, so settling will be faster for inverting applications, as well.

It is important to note that the oscilloscope input amplifier may be overdriven during a settling time measurement, so the oscilloscope must be capable of recovering from overdrive very quickly. The signal generator used for this measurement must be able to drive 50Ω with a very clean $\pm 10V_{PP}$ square wave.

The Slew Rate of LME49990 tells how fast it responses to a transient or a step input. It may be measured by the test circuit in Figure 32. The Slew Rate of LME49990 is specified in close-loop gain = -1 when the output driving a 1kΩ load at $20V_{PP}$. The LME49990 behaves very stable in shape step response and have a minimal ringing in both small and large signal step response (See TYPICAL PERFORMANCE CHARACTERISTICS). The slew rate typical value reach as high as ±18V/μS was measured when the output reach -20V refer to the start point when input voltage equals to zero.

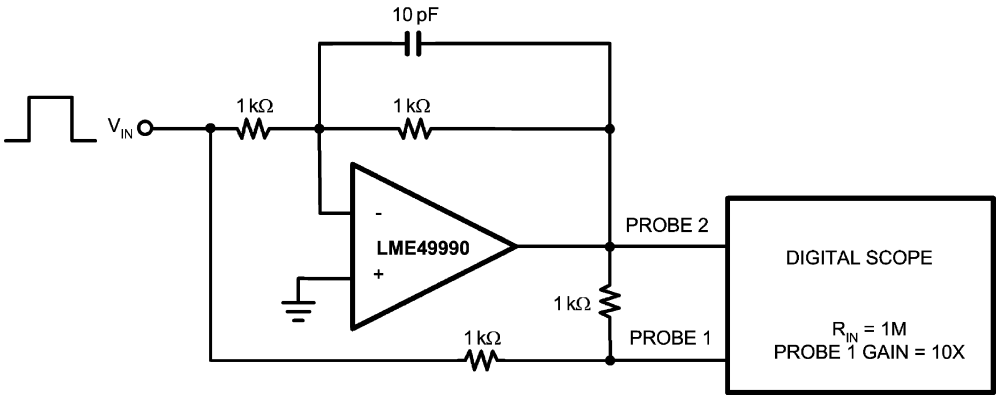


Figure 31. Settling Time Test Circuit

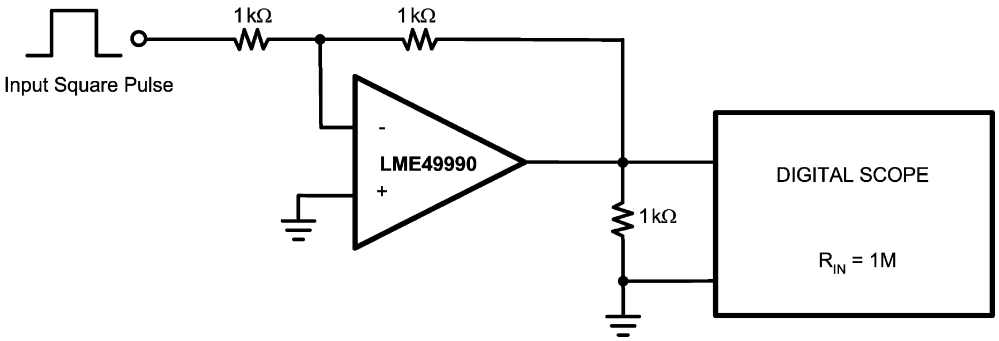


Figure 32. Slew Rate Test Circuit

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DISTORTION MEASUREMENTS

The vanishingly low residual distortion produced by LME49990 is below the capabilities of all commercially available equipment. This makes distortion measurements just slightly more difficult than simply connecting a distortion meter to the amplifier's inputs and outputs. The solution, however, is quite simple: an additional resistor. Adding this resistor extends the resolution of the distortion measurement equipment.

The LME49990's low residual distortion is an input referred internal error. As shown in Figure 33, adding the 10Ω resistor connected between the amplifier's inverting and non-inverting inputs changes the amplifier's noise gain. The result is that the error signal (distortion) is amplified by a factor of 101. Although the amplifier's closed-loop gain is unaltered, the feedback available to correct distortion errors is reduced by 101, which means that measurement resolution increases by 101. To ensure minimum effects on distortion measurements, keep the value of R1 low as shown in Figure 33.

This technique is verified by duplicating the measurements with high closed loop gain and/or making the measurements at high frequencies. Doing so produces distortion components that are within the measurement equipment's capabilities. This datasheet's THD+N and IMD values were generated using the above described circuit connected to an Audio Precision System Two Cascade.

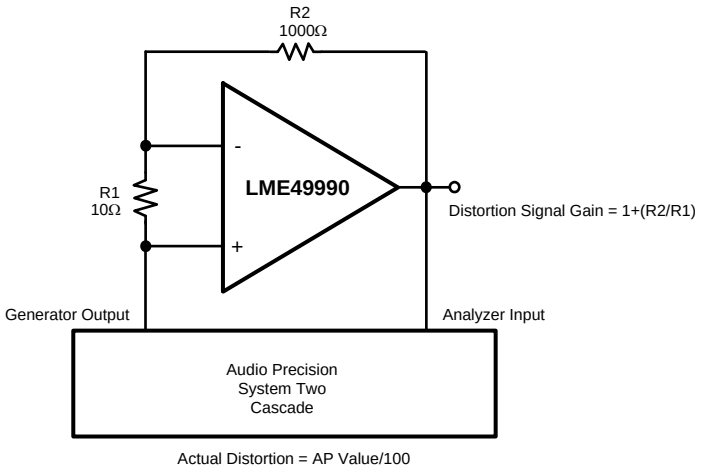


Figure 33. THD+N and IMD Distortion Test Circuit

Revision History

Revision	Date	Description
1.0	12/16/09	Initial released.
1.01	01/08/10	Input text edits.
1.02	02/08/11	Added the SDB08B package.
1.03	02/15/11	Updated the Ordering Information table.
1.04	07/08/11	Added the MA and LLP Top Markings and input text edits.
1.05	07/11/11	Added the θ_{JA} (LLP) limit = 52.5°C/W (under Thermal Resistance) in the Abs. Max. section
1.06	07/12/11	Added "The exposed pad (DAP) of unit should NOT be grounded. (It should be left floating)", in the Applications section (cover page).
1.07	07/21/11	Changed "The exposed pad (DAP) of unit should NOT be grounded. (It should be left floating)", in the Applications section (cover page). **Changed to:** "The exposed pad (DAP) of unit should not be grounded. It is internally connected to V_{EE}".
C	04/02/13	Changed layout of National Data Sheet to TI format.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LME49990MA/NOPB	LIFEBUY	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L49990 MA	
LME49990MAX/NOPB	LIFEBUY	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L49990 MA	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

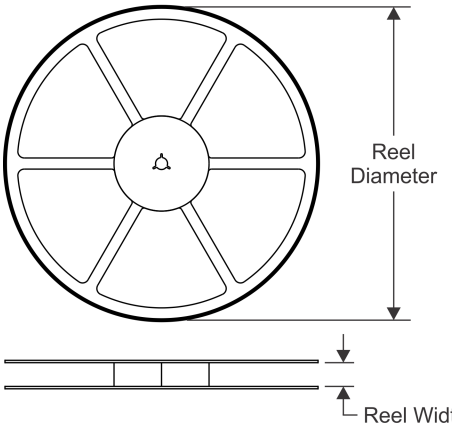
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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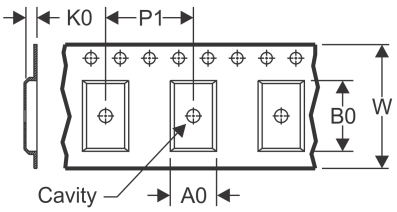
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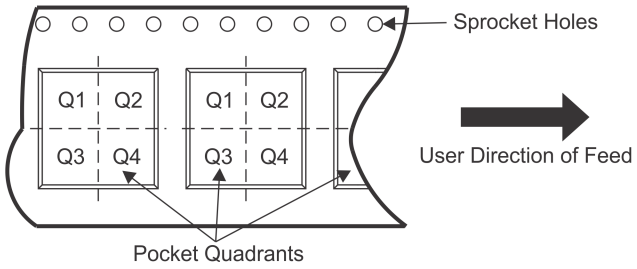


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

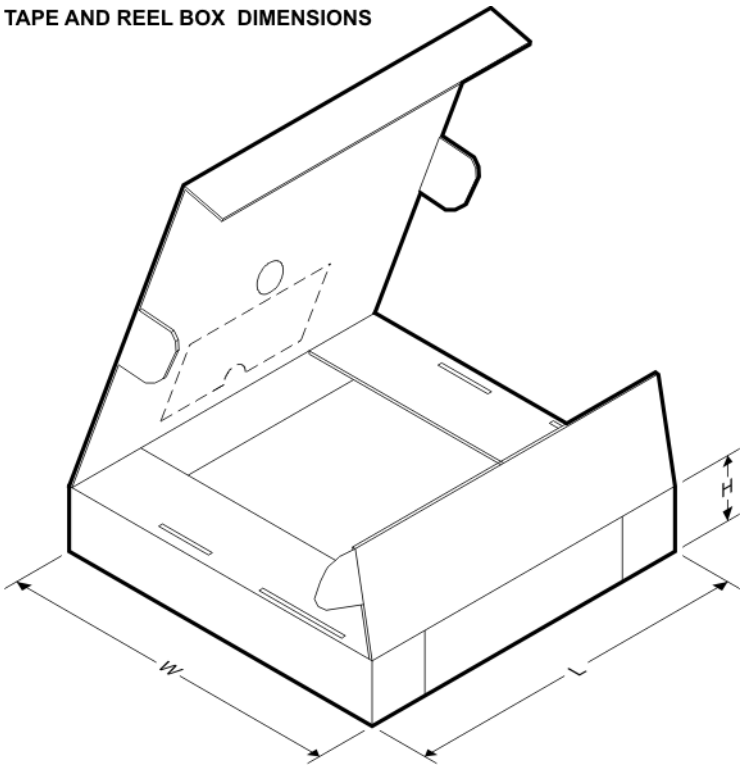
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LME49990MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

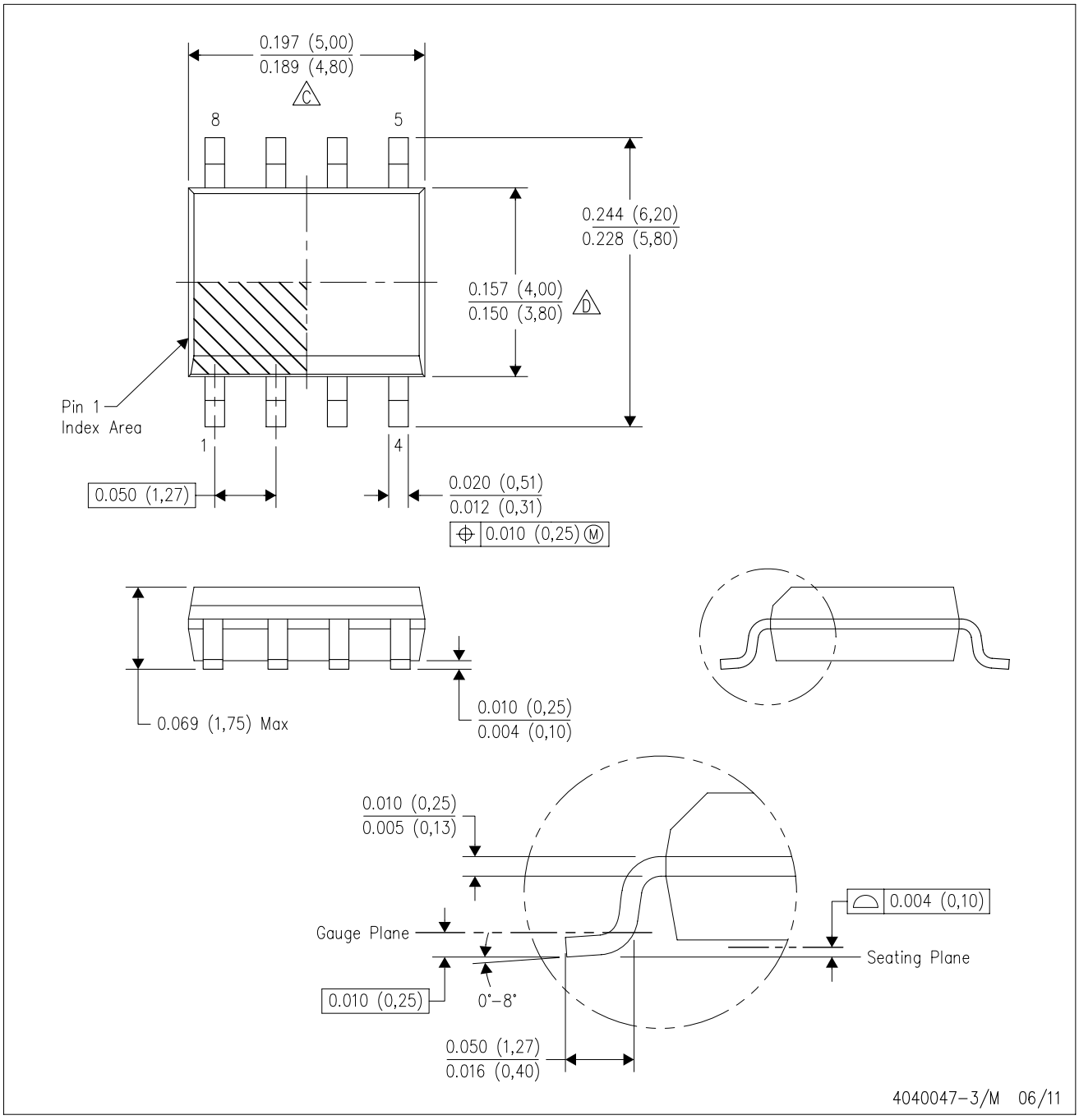
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LME49990MAX/NOPB	SOIC	D	8	2500	349.0	337.0	45.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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