MM54C910,MM74C910

MM54C910 MM74C910 256-Bit TRI-STATE Random Access Read/Write Memory



Literature Number: SNOS343A

National Semiconductor

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MM54C910/MM74C910 256 Bit TRI-STATE® Random Access Read/Write Memory

General Description

The MM54C910/MM74C910 is a 64 word by 4-bit random access memory. Inputs consist of six address lines, four data input lines, a $\overline{WE}$, and a $\overline{ME}$ line. The six address lines are internally decoded to select one of the 64 word locations. An internal address register latches the address information on the positive to negative transition of $\overline{ME}$. The TRI-STATE outputs allow for easy memory expansion.

Address Operation: Address inputs must be stable (t_{SA}) prior to the positive to negative transition of $\overline{ME}$, and (t_{HA}) after the positive to negative transition of $\overline{ME}$. The address register holds the information and stable address inputs are not needed at any other time.

Write Operation: Data is written into memory at the selected address if $\overline{WE}$ goes low while $\overline{ME}$ is low. $\overline{WE}$ must be held low for $t_{\overline{WE}}$ and data must remain stable t_{HD} after $\overline{WE}$ returns high.

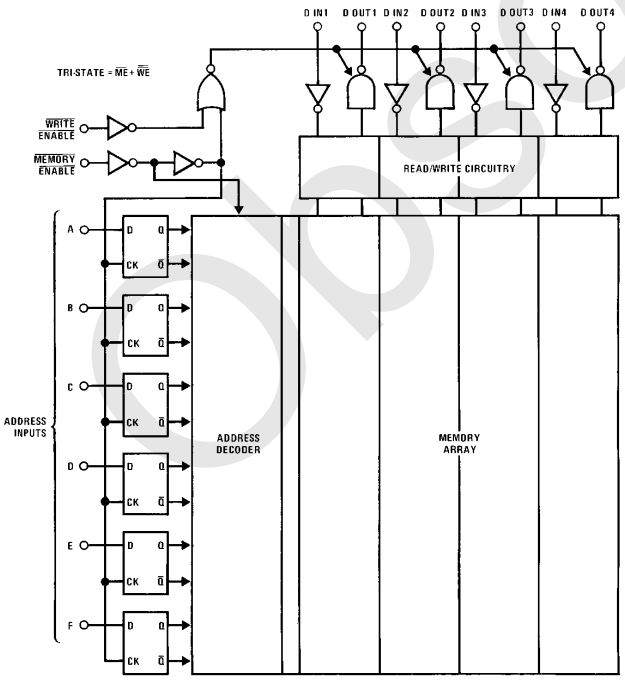
Read Operation: Data is nondestructively read from a memory location by an address operation with $\overline{WE}$ held high.

Outputs are in the TRI-STATE (Hi-Z) condition when the device is writing or disabled.

Features

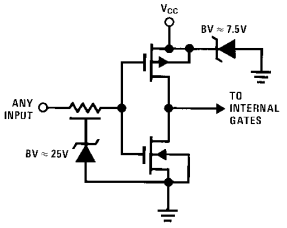
- Supply voltage range — 3.0V to 5.5V
- High noise immunity — $0.45V_{CC}$ (typ.)
- TTL compatible fan out — 1 TTL load
- Input address register
- Low power consumption — 250 nW/package (typ.) (chip enabled or disabled)
- Fast access time — 250 ns (typ.) at 5.0V
- TRI-STATE outputs
- High voltage inputs

Logic Diagrams



TL/F/5914–1

Input Protection



TL/F/5914–2

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RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Output Pin	−0.3V to V_{CC} +0.3V
Voltage at Any Input Pin	−0.3V to +15V
Power Dissipation	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3.0V to 5.5V
Standby V_{CC} Range	1.5V to 5.5V
Absolute Maximum (V_{CC})	6.0V
Lead Temperature (T_L) (Soldering, 10 sec.)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
MM54C910	4.5	5.5	V
MM74C910	4.75	5.25	V
Temperature (T_A)			
MM54C910	−55	+125	°C
MM74C910	−40	+85	°C

DC Electrical Characteristics

Min/Max limits apply accross the temperature and power supply range indicated

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{IN(1)}$	Logical "1" Input Voltage	Full Range	V_{CC} − 1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	Full Range			0.8	V
$I_{IN(1)}$	Logical "1" Input Current	V_{IN} = 15V V_{IN} = 5V		0.005 0.005	2.0 1.0	μA μA
$I_{IN(0)}$	Logical "0" Input Current	V_{IN} = 0V	−1.0	−0.005		μA
$V_{OUT(1)}$	Logical "1" Output Voltage	I_O = −150 μA I_O = −400 μA	V_{CC} − 0.5 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	I_O = 1.6 mA			0.4	V
I_{OZ}	Output Current in High Impedance State	V_O = 5V V_O = 0V	−1.0	0.005 −0.005	1.0	μA μA
I_{CC}	Supply Current	V_{CC} = 5V		5.0	300	μA

AC Electrical Characteristics* T_A = 25°C, V_{CC} = 5.0V, C_L = 50 pF

Symbol	Parameter	Min	Typ	Max	Units
t_{ACC}	Access Time from Address		250	500	ns
t_{pd}	Propagation Delay from $\overline{ME}$		180	360	ns
t_{SA}	Address Input Set-Up Time	140	70		ns
t_{HA}	Address Input Hold Time	20	10		ns
$t_{\overline{ME}}$	$\overline{\text{Memory Enable}}$ Pulse Width	200	100		ns
$t_{\overline{ME}}$	$\overline{\text{Memory Enable}}$ Pulse Width	400	200		ns
t_{SD}	Data Input Set-Up Time	0			ns
t_{HD}	Data Input Hold Time	30	15		ns
$t_{\overline{WE}}$	$\overline{\text{Write Enable}}$ Pulse Width	140	70		ns
t_{1H}, t_{0H}	Delay to TRI-STATE (Note 4)		100	200	ns
CAPACITANCE					
C_{IN}	Input Capacity Any Input (Note 2)		5.0		pF
C_{OUT}	Output Capacity Any Output (Note 2)		9.0		pF
C_{PD}	Power Dissipation Capacity (Note 3)		350		pF

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AC Electrical Characteristics* (Continued) $T_A = 25°C$, $V_{CC} = 5.0V$, $C_L = 50$ pF

Symbol	Parameter	MM54C910 $T_A = -55°C$ to $+125°C$ $V_{CC} = 4.5V$ to $5.5V$		MM74C910 $T_A = -40°C$ to $+85°C$ $V_{CC} = 4.75V$ to $5.25V$		Units
		Min	Max	Min	Max	
t_{ACC}	Access Time from Address		860		700	ns
t_{pd1}, t_{pd0}	Propagation Delay from $\overline{ME}$		660		540	ns
t_{SA}	Address Input Set-Up Time	200		160		ns
t_{HA}	Address Input Hold Time	20		20		ns
$t_{\overline{ME}}$	$\overline{\text{Memory Enable}}$ Pulse Width	280		260		ns
$t_{\overline{ME}}$	$\overline{\text{Memory Enable}}$ Pulse Width	750		600		ns
t_{SD}	Data Input Set-Up Time	0		0		ns
t_{HD}	Data Input Hold Time	50		50		ns
$t_{\overline{WE}}$	$\overline{\text{Write Enable}}$ Pulse Width	200		180		ns
t_{1H}, t_{0H}	Delay to TRI-STATE (Note 4)		200		200	ns

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

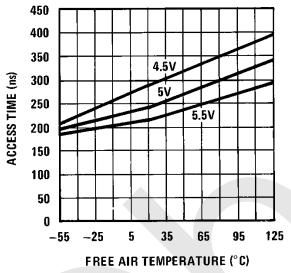
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption for any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

Note 4: See AC test circuits for t_{1H}, t_{0H}.

Typical Performance Characteristics

Typical Access Time vs Ambient Temperature



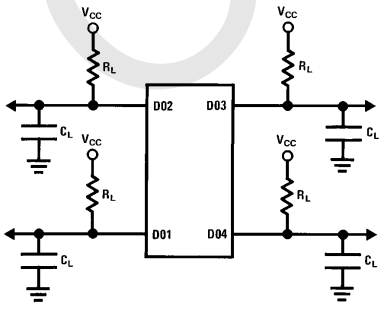
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Truth Table

$\overline{ME}$	$\overline{WE}$	Operation	Outputs
L	L	Write	TRI-STATE
L	H	Read	Data
H	L	Inhibit, Store	TRI-STATE
H	H	Inhibit, Store	TRI-STATE

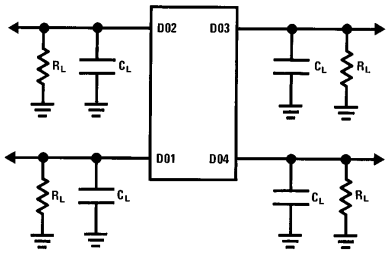
AC Test Circuits

t_{0H}



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t_{1H}

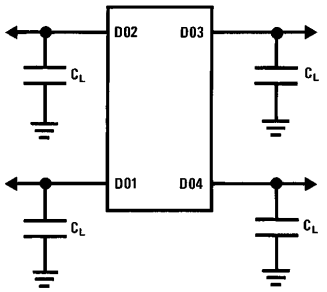


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AC Test Circuits (Continued)

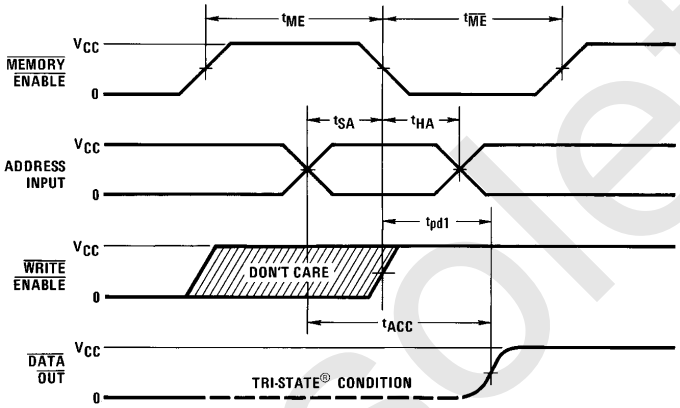
All Other AC Tests



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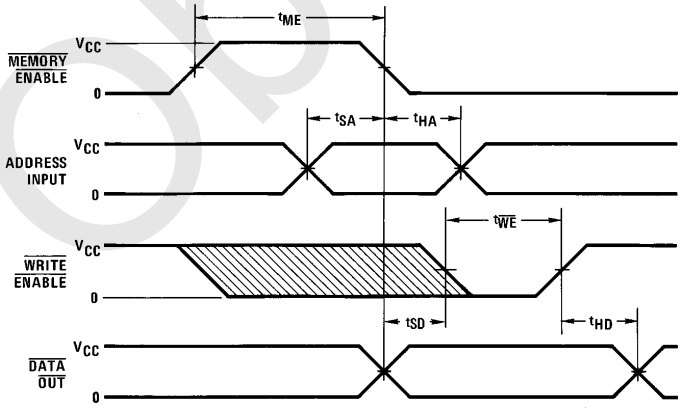
Switching Time Waveforms

Read Cycle
(See Note 1)



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Write Cycle
(See Note 1)

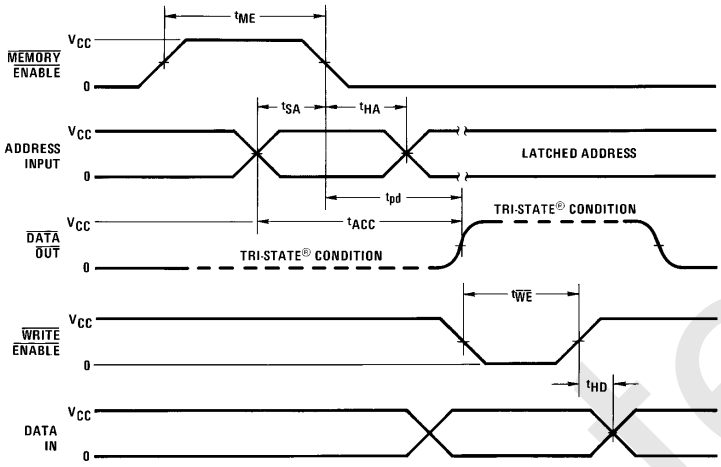


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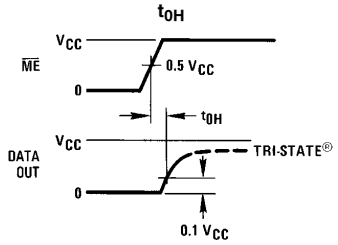
Obsolete

Switching Time Waveforms (Continued)

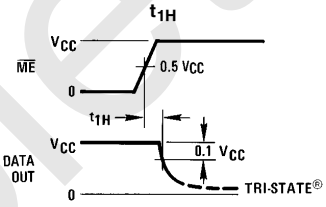
Read Modify Write Cycle
(See Note 1)



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TL/F/5914–11



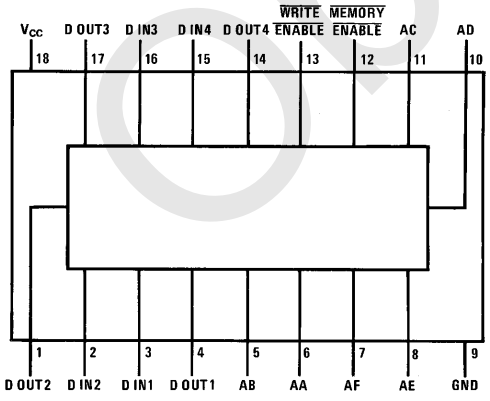
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Note 1: $\overline{\text{MEMORY}}$ $\overline{\text{ENABLE}}$ must be brought high for t_{ME} nanoseconds between every address change.

Note 2: $t_r = t_f = 20$ ns for all inputs.

Connection Diagram

Dual-In-Line Package

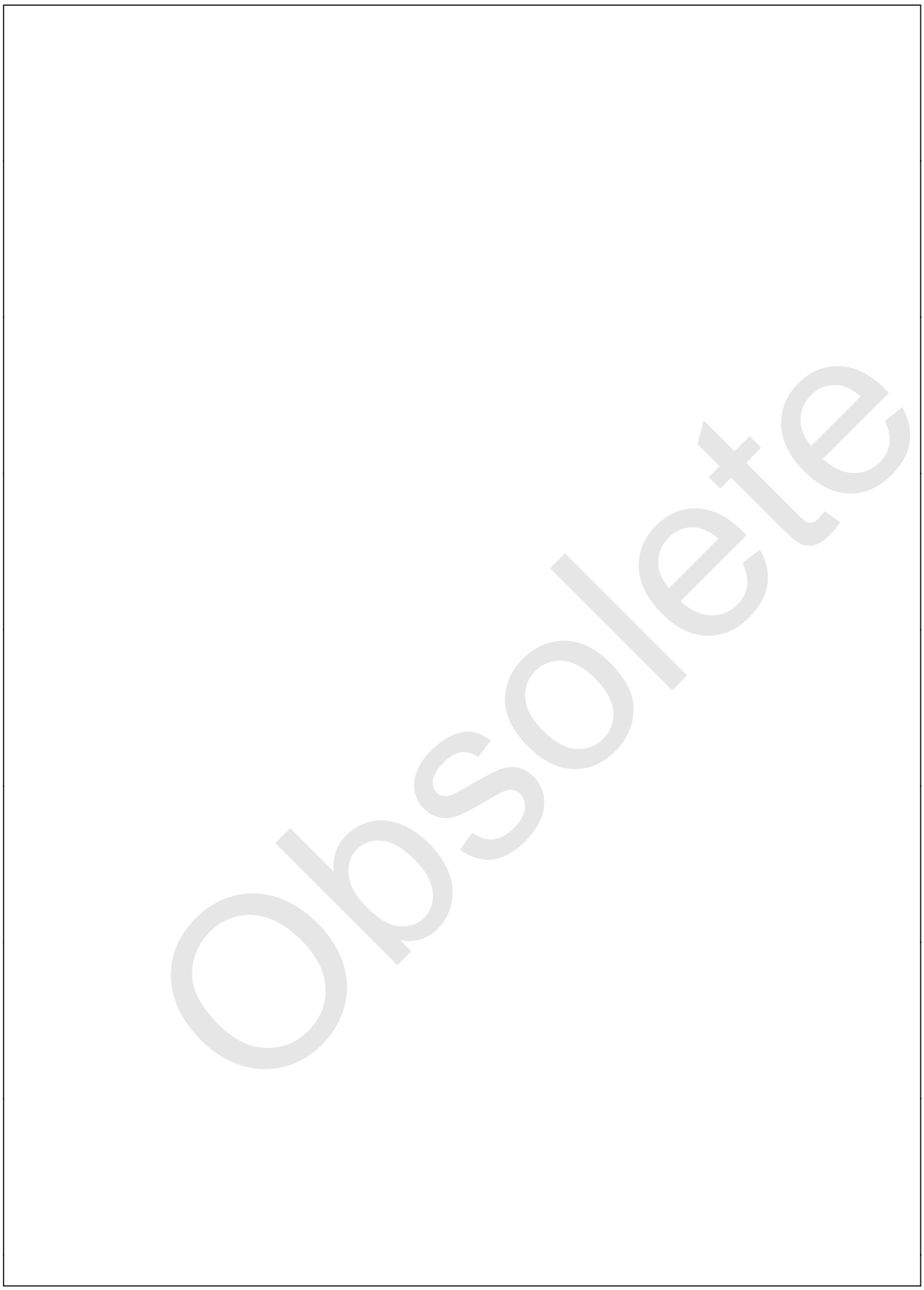


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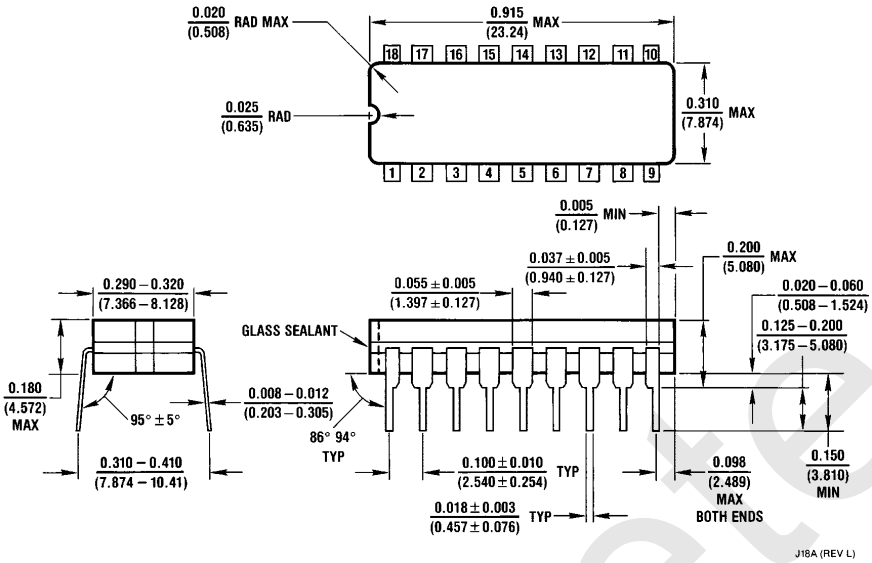
Top View

Order Number MM54C910 or MM74C910

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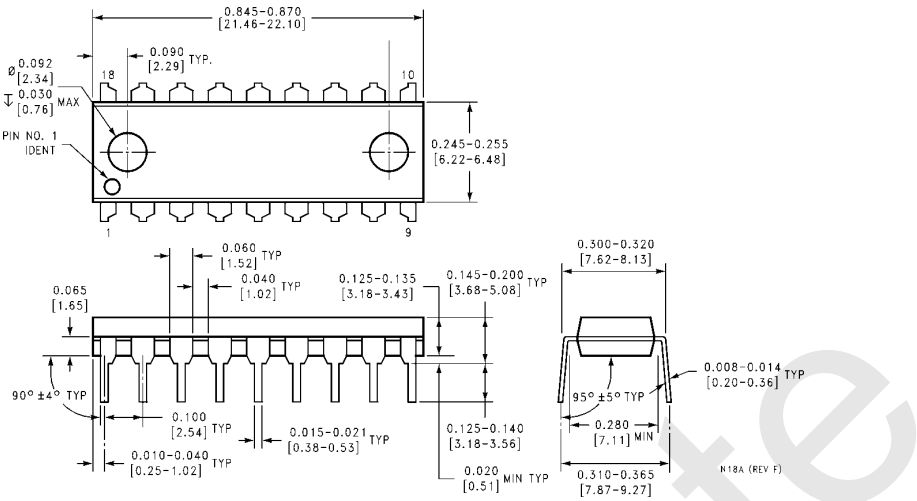
Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number MM54C910J or MM74C910J
NS Package Number J18A

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Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number MM54C910N or MM74C910N
NS Package Number N18A

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