SONY

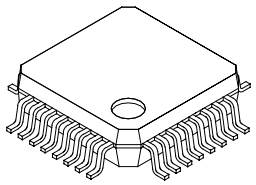
CXB1577R

Post-Amplifier for Optical Fiber Communication Receiver

Description

The CXB1577R achieves the 2R optical-fiber communication receiver functions (Reshaping and Regenerating) on a single chip. This IC is equipped with the signal detection function, which is used to enable TTL/ECL outputs. Also, the output disable function performs the output shutdown.

32 pin LQFP (Plastic)



Features

- Output disable function (TTL input)
- Signal detection function (TTL/ECL output)

Applications

- SONET/SDH: 622.08Mbps
- Fibre Channel: 531.25Mbps
  : 1.062Gbps
- Gigabit-Ethernet: 1.25Gbps

Absolute maximum Ratings

• Supply voltage	$V_{CC} - V_{EE}$	–0.3 to +6	V
• Storage temperature	Tstg	–65 to +150	°C
• Input voltage difference $\lvert V_D - V_{\overline{D}} \rvert$	Vdif	0 to +2	V
• SW input voltage	Vi	V_{EE} to V_{CC}	V
• ECL output current	IoQ/SD-ECL	–30 to 0	mA
• TTL output current (High level)	I_{OH} SD-TTL	–20 to 0	mA
• TTL output current (Low level)	I_{OL} SD-TTL	0 to 20	mA
• D/DB input voltage		Vcc – 2 to Vcc	V
• ODIS input voltage		V_{EE} – 0.5 to V_{EE} +5.5	V

Recommended Operating Conditions

• Supply voltage	$V_{CC} - V_{EE}$	5 ± 0.25	V
• Termination voltage (for data)	$V_{CC} - VT_D$	1.8 to 2.2	V
• Termination voltage (for alarm 1,alarm 2)	VTA	V_{EE}	V
• Termination resistance (for data)	RT_D	46 to 56	Ω
• Termination resistance (for alarm 1)	RTA1	240 to 300	Ω
• Termination resistance (for alarm 2)	RTA2	460 to 560	Ω
• Operating temperature	Ta	0 to +70	°C

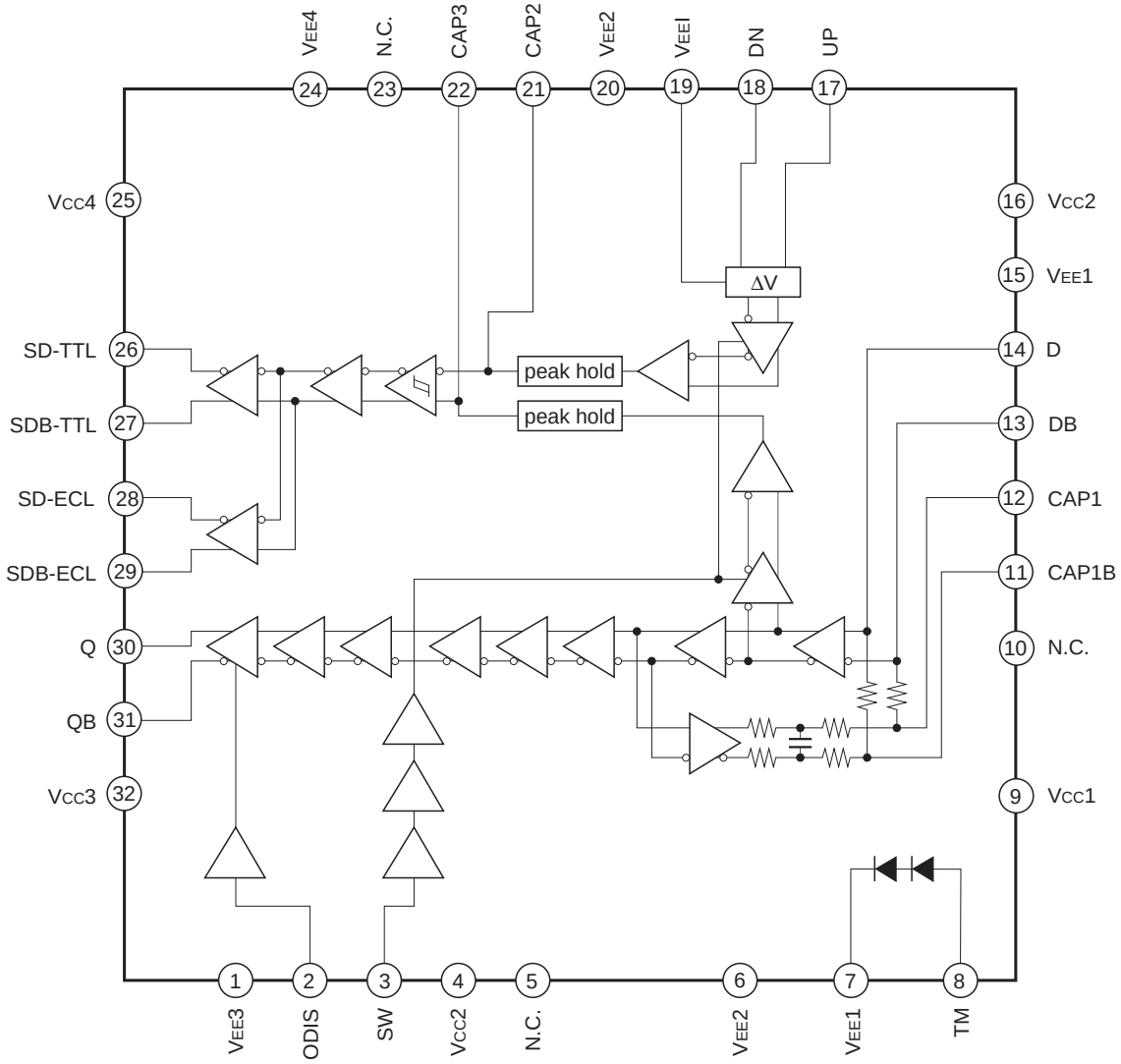
Structure

Bipolar silicon monolithic IC

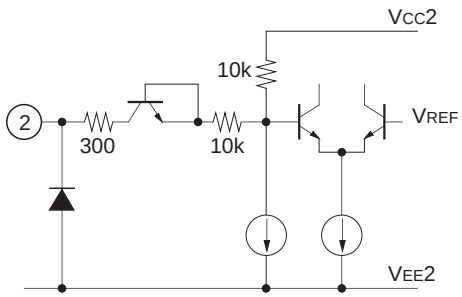
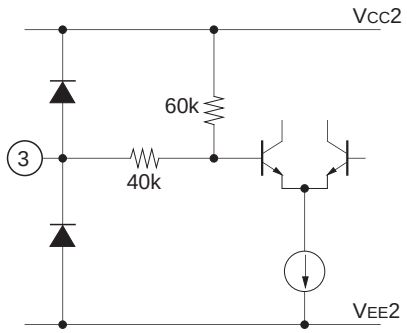
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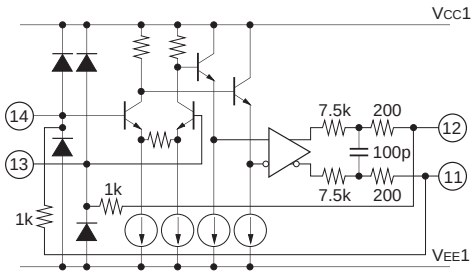
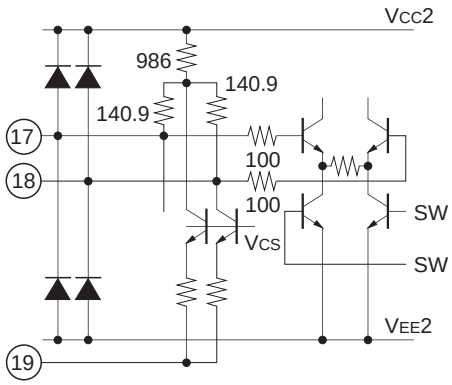
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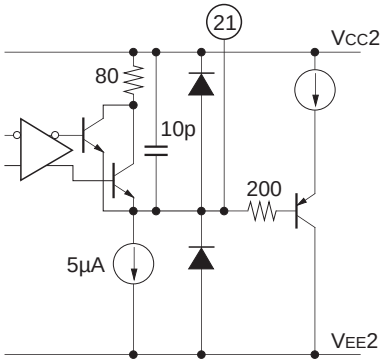
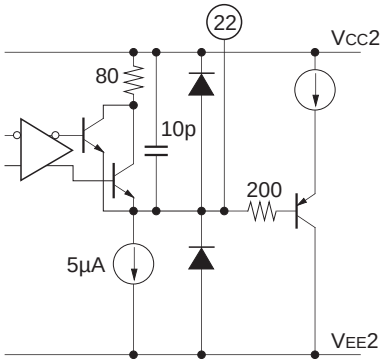
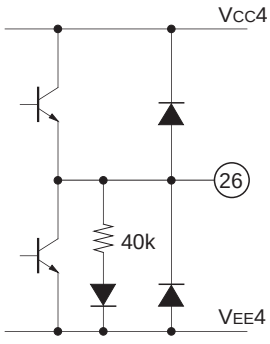
Block Diagram and Pin Configuration

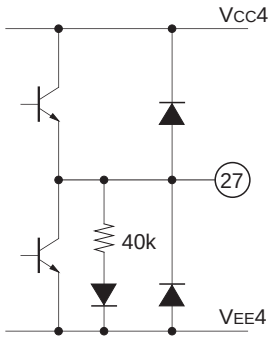
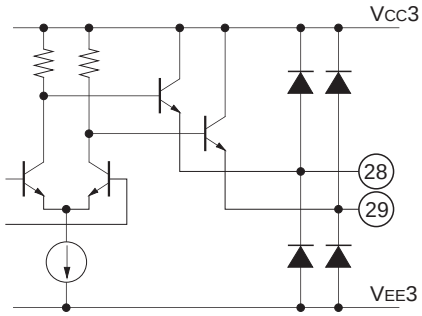
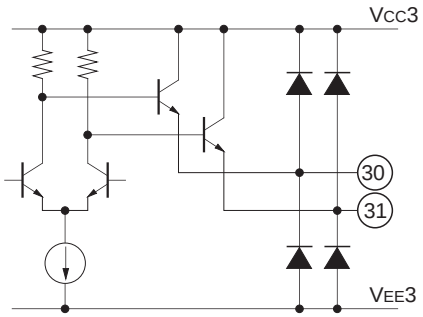


Pin Description

Pin No.	Symbol	Typical pin voltage (V)		Equivalent circuit	Description
		DC	AC		
1	$V_{EE}3$	0			Negative power supply for ECL output buffer.
2	ODIS	0 or 5 (open)			Controls the output shutdown function. High voltage when open; the Q output is fixed to Low. Low voltage when connected to V_{EE}; the D input results in the Q output with ECL level. TTL level is also available.
3	SW	0 or 5 (open)			Switches the identification maximum voltage amplitude. High voltage when open; the identification maximum voltage amplitude becomes 40mVp-p. Low voltage when connected to V_{EE}; the amplitude becomes 20mVp-p.
4	$V_{CC}2$	5			Positive power supply for digital block.
5	N.C.				No connected.
6	$V_{EE}2$	0			Negative power supply for digital block.
7	$V_{EE}1$	0			Negative power supply for analog block.
8	TM	1.6			Chip temperature monitor.
9	$V_{CC}1$	5			Positive power supply for analog block.
10	N.C.				No connected.

Pin No.	Symbol	Typical pin voltage (V)		Equivalent circuit	Description
		DC	AC		
11	CAP1B				Pins 11 and 12 connect a capacitor which determines the cut-off frequency for DC feedback block. Pins 13 and 14 are input pins for limiting amplifier block. Input the signal with AC coupled.
12	CAP1				
13	DB	3.7	3.3 to 4.1		
14	D	3.7	3.3 to 4.1		
15	VEE1	0			Negative power supply for analog block.
16	VCC2	5			Positive power supply for digital block.
17	UP				Connects a resistor for alarm level setting. Default voltage can be generated without an external resistor by shorting the VEEI pin to VEE.
18	DN				
19	VEEI	0			Generates the default voltage between UP and DOWN. The voltage (8.0mV for input conversion) can be generated between UP and DOWN (Pins 17 and 18) as alarm setting level by connecting this pin to VEE.
20	VEE2	0			Negative power supply for digital block.

Pin No.	Symbol	Typical pin voltage (V)		Equivalent circuit	Description
		DC	AC		
21	CAP2	3.2			Connects a peak hold circuit capacitor for alarm block. 470pF should be connected to Vcc each. CAP2 pin connects a peak hold capacitor for alarm level setting block. CAP3 pin connects a peak hold capacitor for limiting amplifier signal.
22	CAP3	3.2			
23	N.C.				No connected.
24	VEE4	0			Negative power supply for TTL output buffer.
25	VCC4	5			Positive power supply for TTL output buffer.
26	SD-TTL		0 or 3		Alarm signal TTL level output.

Pin No.	Symbol	Typical pin voltage (V)		Equivalent circuit	Description
		DC	AC		
27	SDB-TTL		0 or 3		Alarm signal TTL level output.
28	SD-ECL		3.3 or 4.1		Alarm signal ECL level output. Terminate this pin in 510Ω to VEE.
29	SDB-ECL		3.3 or 4.1		
30	Q		3.3 or 4.1		Data signal output. Terminates this pin in 50Ω to VTT = Vcc – 2V.
31	QB		3.3 or 4.1		
32	VCC3	5			Positive power supply for ECL output buffer.

Electrical Characteristics

DC Characteristics

V_{CC} = 5 ± 0.25V, V_{EE} = GND, Ta = 0 to +70°C

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply current	I_{EE}		–74	–51		mA
Q/QB High output voltage	VOH	50Ω to VTT	V_{CC} – 1100		V_{CC} – 860	mV
Q/QB Low output voltage	VOL		V_{CC} –1860		V_{CC} – 1620	
SD-ECL/SDB-ECL High output voltage	VOH-E	510Ω to V_{EE}	V_{CC} –1100		V_{CC} – 860	
SD-ECL/SDB-ECL Low output voltage	VOL-E		V_{CC} –1900		V_{CC} – 1620	
SD-TTL/SDB-TTL High output voltage	VOH-T	IOH = –0.4mA	2.4			V
SD-TTL/SDB-TTL Low output voltage	VOL-T	IOL = 2mA			0.5	
SW High input voltage	VIHSW	at SW pin Open: High	V_{CC} – 0.5		V_{CC}	
SW Low input voltage	VILSW		V_{EE}		0.5	
SW High input current	IIHSW				10	µA
SW Low input current	IILSW		–100			
ODIS High input voltage	VIHOD	at ODIS pin Open: High	2		V_{CC} + 0.5	V
ODIS Low input voltage	VILOD		V_{EE}		0.8	
ODIS High input current	IIHOD	V_{IH} = Vcc			20	µA
ODIS Low input current	IILOD	V_{IL} = V_{EE}	–400			
D/DB input resistance	Rin		765	1020	1275	Ω
TM voltage	VTM	Iin = 1mA	1.2		2	V

AC Characteristics V_{CC} = 5 ± 0.25V, V_{EE} = GND, Ta = 0 to +70°C

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Maximum input voltage amplitude	Vmax	single-ended input	1600			mVp-p
Amplifier gain (excluding the output buffer)	GL		52			dB
Identification maximum voltage amplitude of alarm level	VmaxA1	SW: Low, single-ended input	20			mVp-p
	VmaxA2	SW: Open High, single-ended input	40			
SD/SDB hysteresis width	ΔP1	SW: Low, at default alarm level	3	6	7	dB
	ΔP2	SW: Open High, at default alarm level	3	6	7	
Alarm setting level for default	Vdef	SW: Open High, V_{EE}I = V_{EE}, fin = 100Mbps Differential voltage input	6.6	8.0	9.3	mV
Q/QB rise time	TrQ	20% to 80% 50Ω to VTT		230	350	ps
Q/QB fall time	TfQ			230	350	
SD-TTL/SDB-TTL rise time	TrSDT	0.6V to 2.2V C_L = 10pF			10	ns
SD-TTL/SDB-TTL fall time	TfSDT				10	
SD-ECL/SDB-ECL rise time	TrSDE	20% to 80% 510Ω to V_{EE}			1.6	
SD-ECL/SDB-ECL fall time	TfSDE				1.6	
Propagation delay time	TPD		0.4		1.9	
SD response assert time	Tas	*1	0		100	µs
SD response deassert time	Tdas	*2	2.3		100	
SD response assert time for alarm level default	Tasd	*3	0		100	
SD response deassert time for alarm level default	Tdasd	*4	2.3		100	

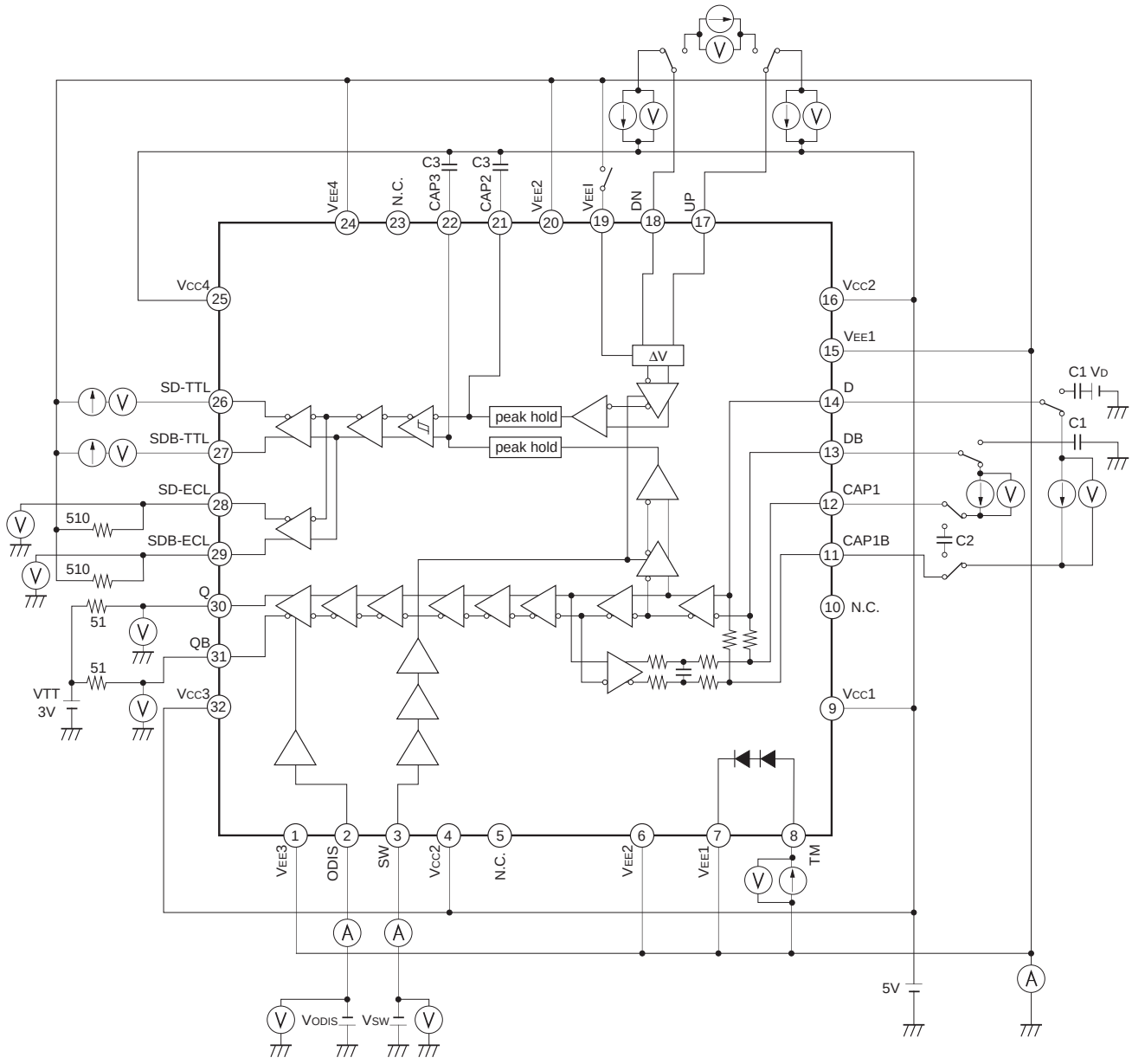
*1 VUP – VDOWN = 100mV, Vin = 100mVp-p (single ended), SW: High, peak hold capacitance (CAP2, CAP3 pins) of 470pF, V_{EE}I: Open.

*2 VUP – VDOWN = 100mV, Vin = 1Vp-p (single ended), SW: High, peak hold capacitance (CAP2, CAP3 pins) of 470pF, connect V_{EE}I: Open.

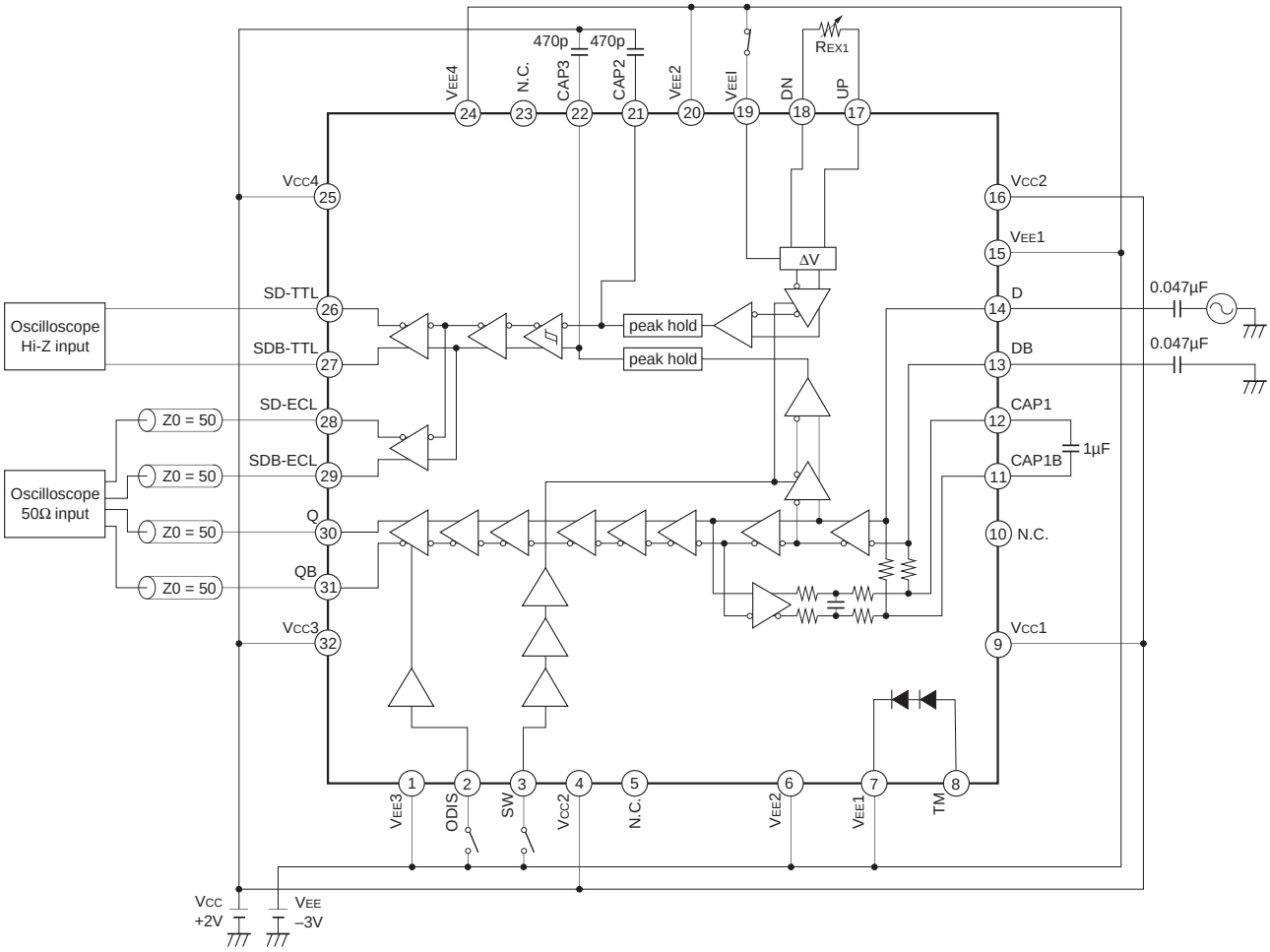
*3 Vin = 50mVp-p (single ended), SW: Low, peak hold capacitance of 470pF, connect V_{EE}I to V_{EE}.

*4 Vin = 1Vp-p (single ended), SW: Low, peak hold capacitance of 470pF, connect V_{EE}I to V_{EE}.

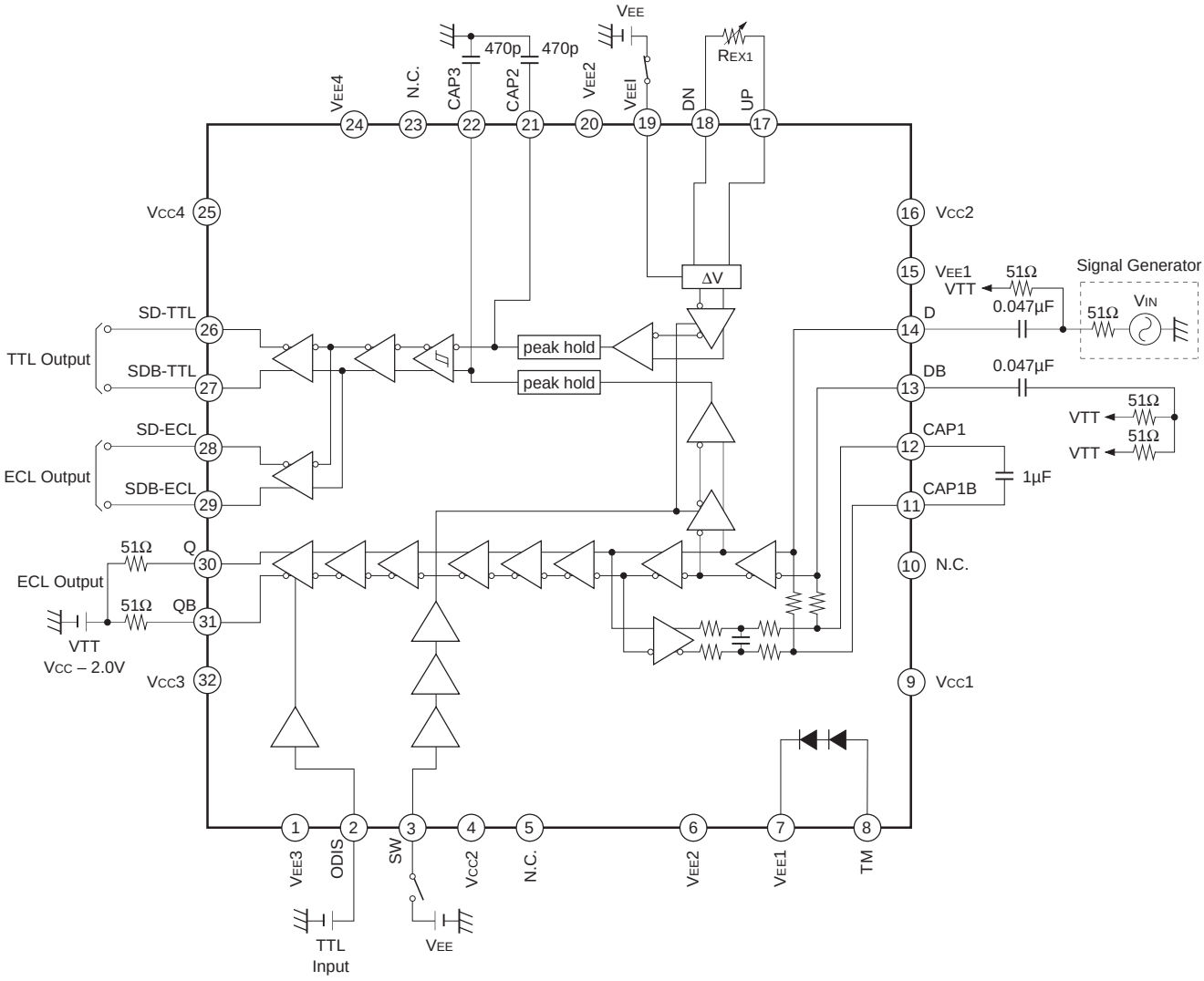
DC Electrical Characteristics Measurement Circuit



AC Electrical Characteristics Measurement Circuit



Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Notes on Operation

1. Limiting amplifier block

The limiting amplifier block is equipped with the auto-offset canceler circuit. When external capacitors C1 and C2 are connected as shown in Fig. 1, the DC bias is set automatically in this block. External capacitor C1 and IC internal resistor R1 determine the low input cut-off frequency f2 as shown in Fig. 2. Similarly, external capacitor C2 and IC internal resistor R2 determine the high cut-off frequency f1 for DC bias feedback. Since peaking characteristics may occur in the low frequency area of the amplifier gain characteristics depending on the f1/f2 combination, set the C1 and C2 values so as to avoid the occurrence of peaking characteristics. The target values of R1 and R2 and the typical values of C1 and C2 are as indicated below. When a single-ended input is used, provide AC grounding by connecting Pin 13 to a capacitor which has the same capacitance as capacitor C1.

R1 (internal): 1kΩ
C1 (external): 0.047µF
f2: 3.4kHz

R2 (internal): 7.5kΩ
C2 (external): 1µF
f1: 21Hz

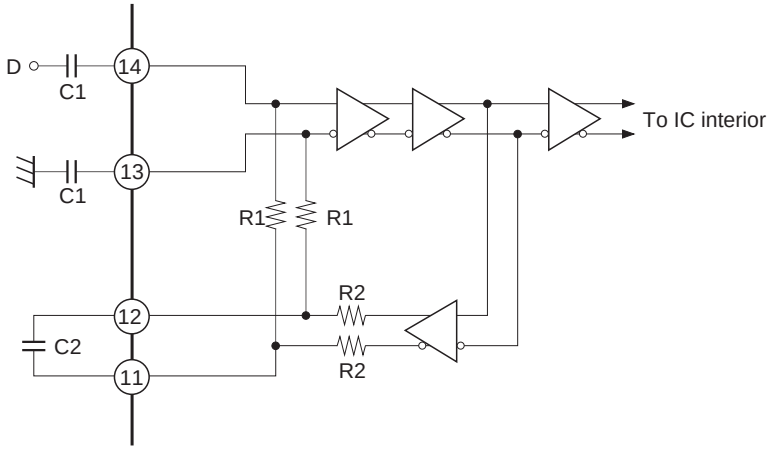


Fig. 1

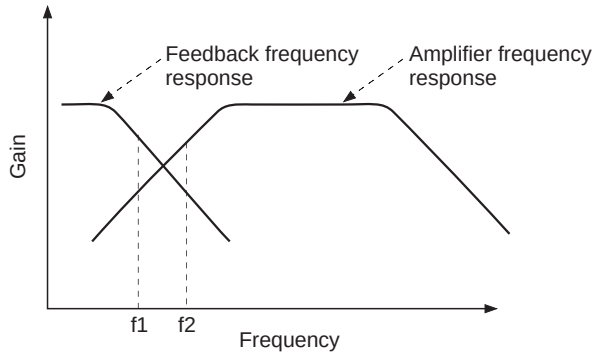


Fig. 2

2. Alarm block

In order to operate the alarm block, give the voltage difference between Pins 17 and 18 to set an alarm level and connect the peak hold capacitor C3 shown in Fig. 3.
This IC has two setting methods of alarm level; one is to connect Pin 19 to V_{EE} and leave Pins 17 and 18 open to set an alarm level default value (8mV for input conversion). The other is to connect Pin 19 to V_{EE} and set a desired alarm level using the external resistors R_{EX1}, R_{EX2} and R_{EX3} shown in Fig. 3. Connect R_{EX1} between Pins 17 and 18 or connect R_{EX3} between Pin 18 and Vcc when less alarm level is desired to be set than its default value; connect R_{EX2} between Pin 17 and Vcc when more alarm level is desired to be set than its default value. However, the Pin 17 voltage must be higher than that of Pin 18.
This IC also features two-level setting of identification maximum voltage amplitude. The amplitude is set to 40mVp-p when Pin 3 is left open (High level) and it is set to 20mVp-p when Pin 3 is Low level. Therefore, the noise margin can be increased by setting Pin 3 to Low level when the small signal is input. The relation of input voltage and peak hold output voltage is shown in Fig. 5.
In the relation between the alarm setting level and hysteresis width, the hysteresis width is designed to maintain a constant gain (design target value: 6dB) as shown in Fig. 4.
This IC is designed to externally have the capacitor C3, and the C3 value should be set so as to obtain desired assert time and deassert time settings for the alarm signal.
The electrical characteristics for the SD response assert and deassert times are guaranteed only when the waveforms are input as shown in the timing chart of Fig. 6.

R_{EX1}: 100Ω (when the alarm level is set to 4mV for input conversion.)
R_{EX2}: 8kΩ (when the alarm level is set to 10mV for input conversion.)
R_{EX3}: 4kΩ (when the alarm level is set to 4mV for input conversion.)
C3: 470pF

The table below shows the alarm logic.

Optical signal input state	SD	$\overline{SD}$
Signal input	High level	Low level
Signal interruption	Low level	High level

The table below shows the output disable function logic.

Optical signal input state	Q	$\overline{Q}$
ODIS: Open High	Fixed Low	Fixed High
ODIS: Low	Data	$\overline{Data}$

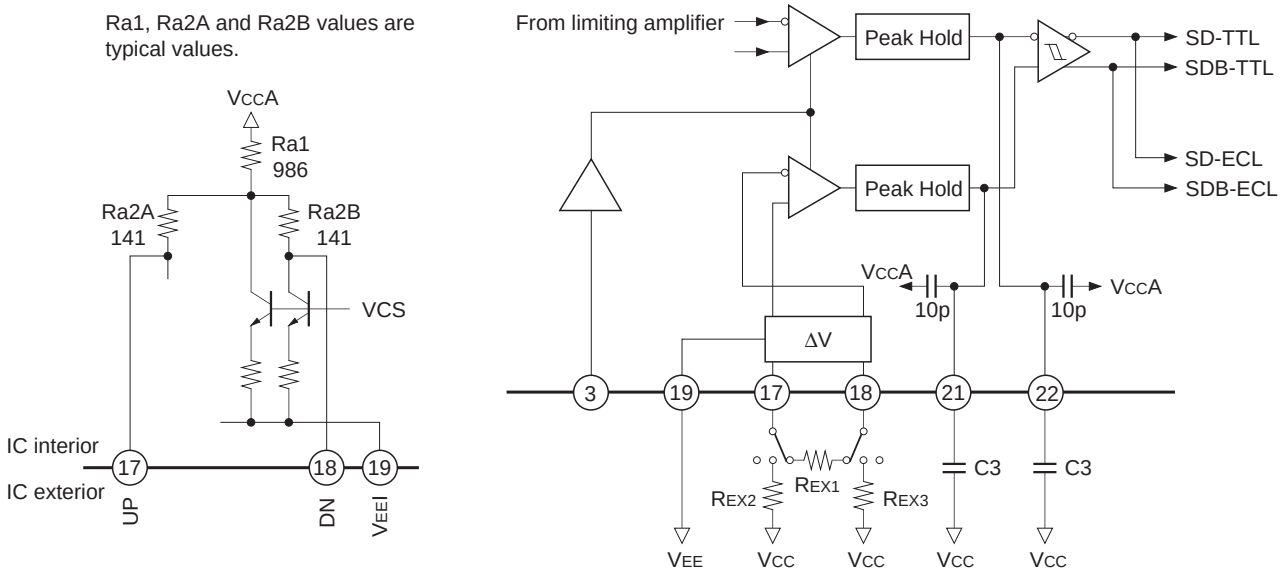


Fig. 3

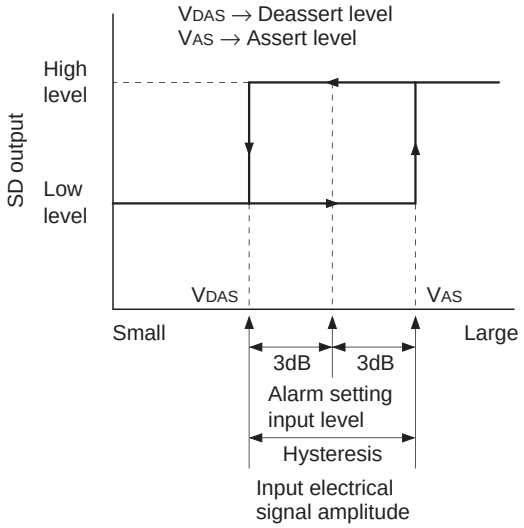


Fig. 4

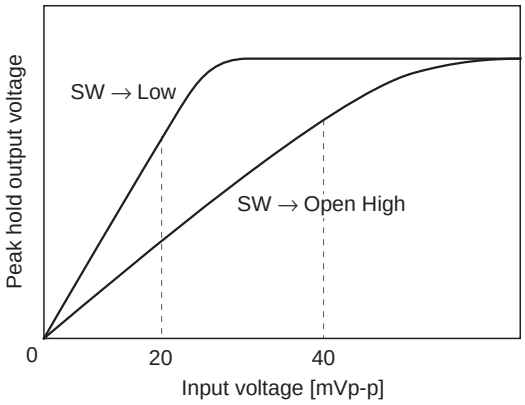


Fig. 5

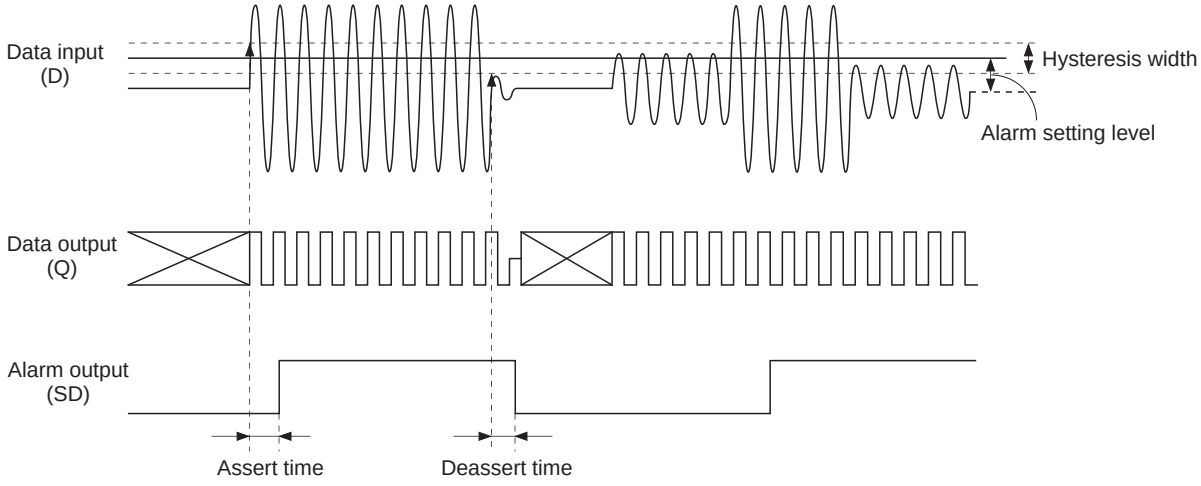
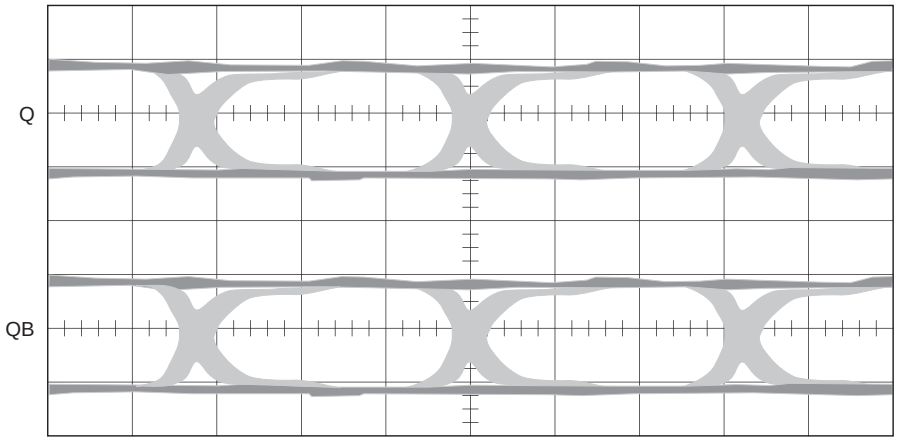


Fig. 6

Example of Representative Characteristics

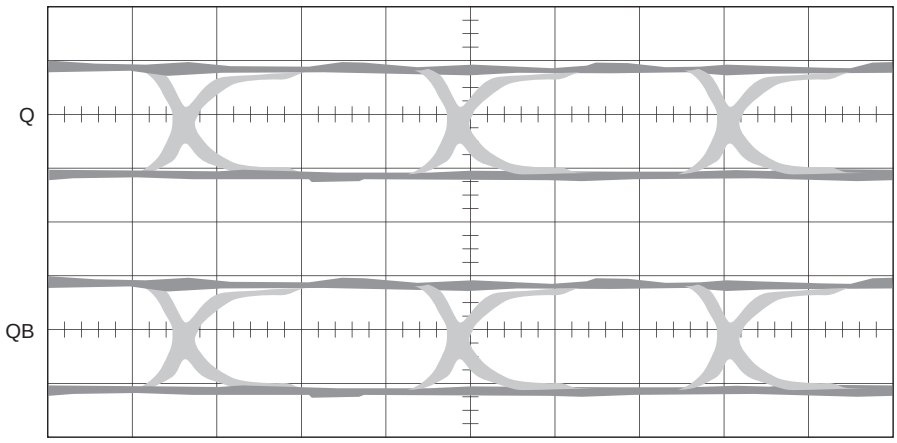
1. Q/QB output waveform



V_{CC} = 5V
V_{EE} = GND
V_{TT} = 3V
Ta = 27°C
D = 622Mbps
Vin = 5mVp-p
Single input
pattern: PRBS2^{23}-1
Q/QB = 50Ω to V_{TT}

Ch. 1 = 400mV/div OFFSET = –1330mV, Ch. 2 = 400mV/div OFFSET = –1330mV, Timebase = 500ps/div

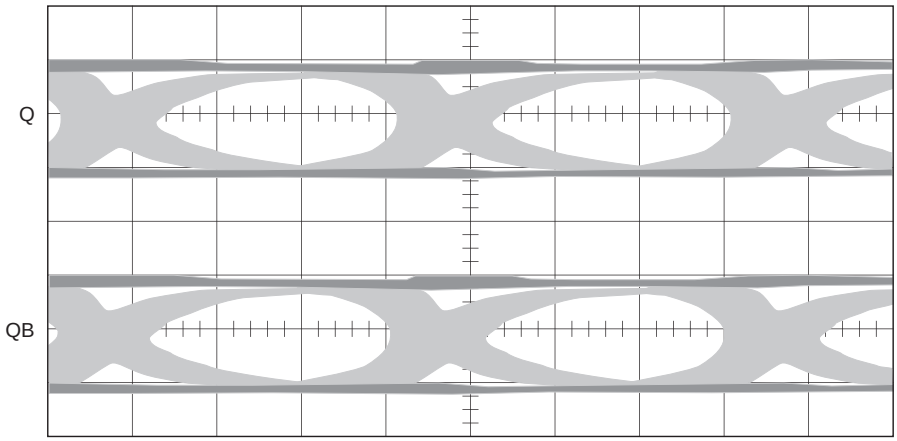
Fig. 7



V_{CC} = 5V
V_{EE} = GND
V_{TT} = 3V
Ta = 27°C
D = 622Mbps
Vin = 10mVp-p
Single input
pattern: PRBS2^{23}-1
Q/QB = 50Ω to V_{TT}

Ch. 1 = 400mV/div OFFSET = –1330mV, Ch. 2 = 400mV/div OFFSET = –1330mV, Timebase = 500ps/div

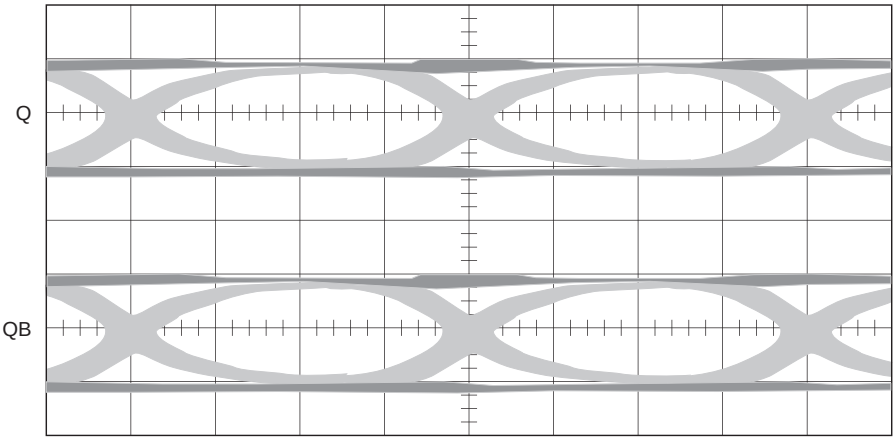
Fig. 8



V_{CC} = 5V
V_{EE} = GND
V_{TT} = 3V
Ta = 27°C
D = 1.25Gbps
Vin = 5mVp-p
Single input
pattern: PRBS2^{23}-1
Q/QB = 50Ω to V_{TT}

Ch. 1 = 400mV/div OFFSET = –1330mV, Ch. 2 = 400mV/div OFFSET = –1330mV, Timebase = 200ps/div

Fig. 9



V_{CC} = 5V
V_{EE} = GND
V_{TT} = 3V
Ta = 27°C
D = 1.25Gbps
Vin = 10mVp-p
Single input
pattern: PRBS2^{23}-1
Q/QB = 50Ω to V_{TT}

Ch. 1 = 400mV/div OFFSET = –1330mV, Ch. 2 = 400mV/div OFFSET = –1330mV, Timebase = 200ps/div

Fig. 10

2. Bit error rate

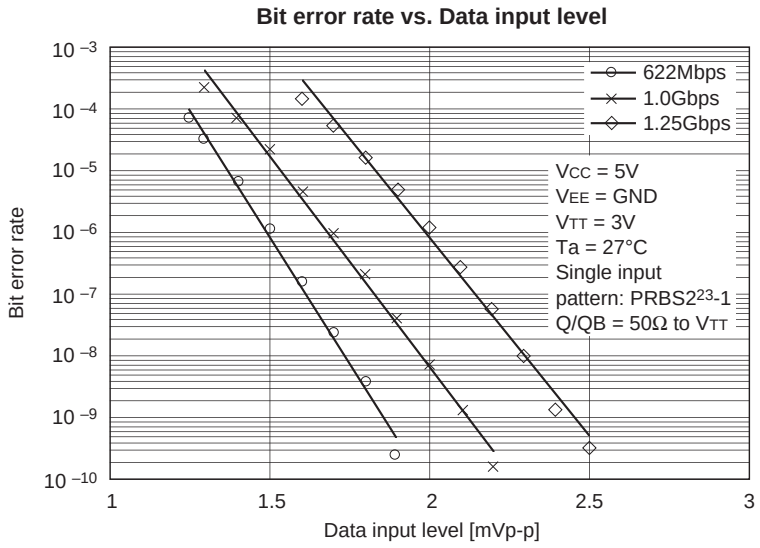


Fig. 11

3. Alarm level

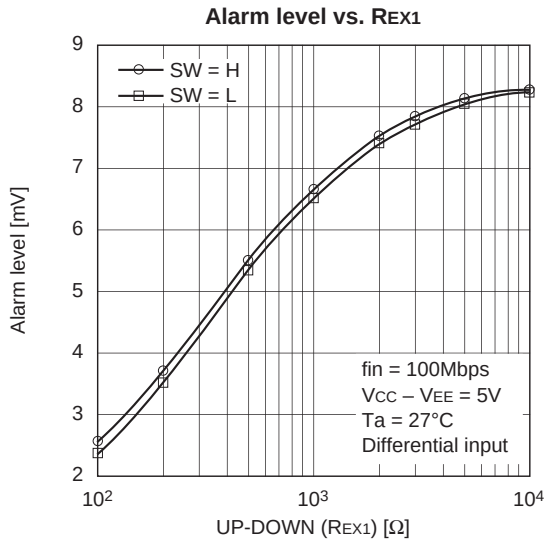


Fig. 12

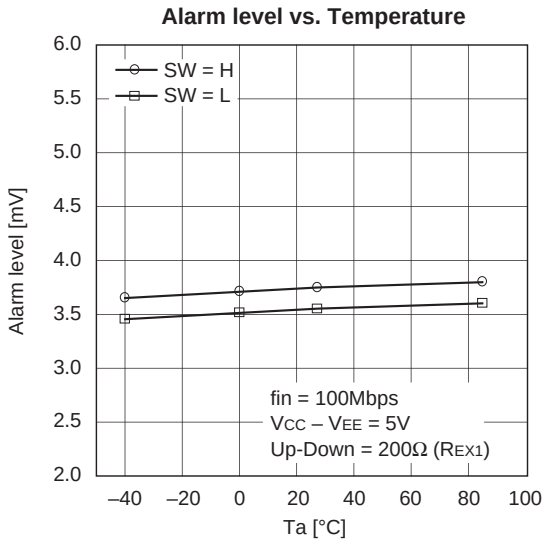


Fig. 13

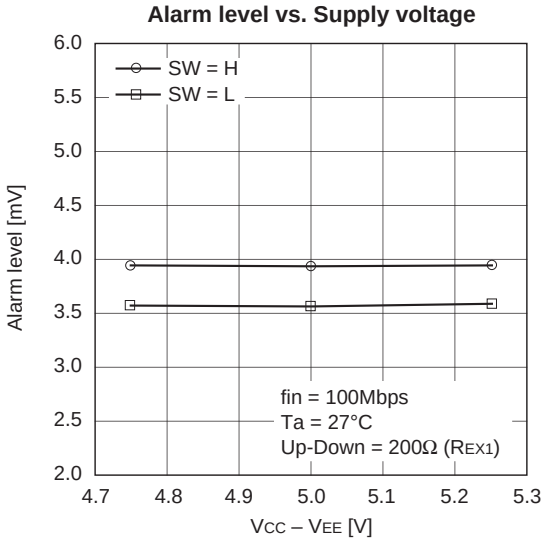


Fig. 14

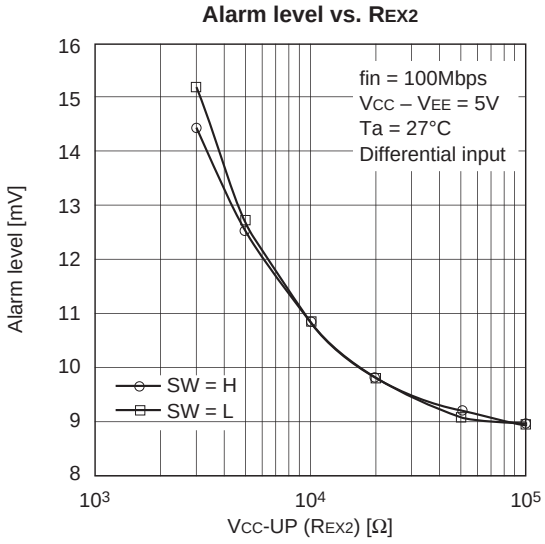


Fig. 15

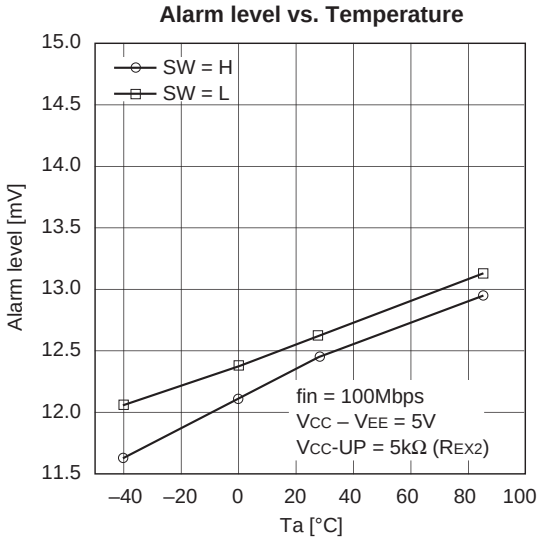


Fig. 16

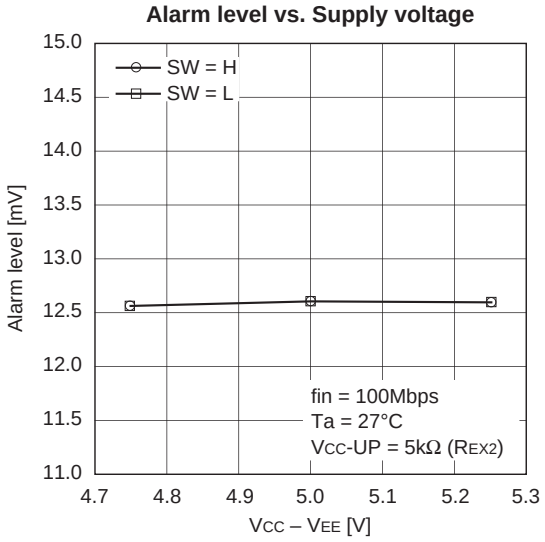


Fig. 17

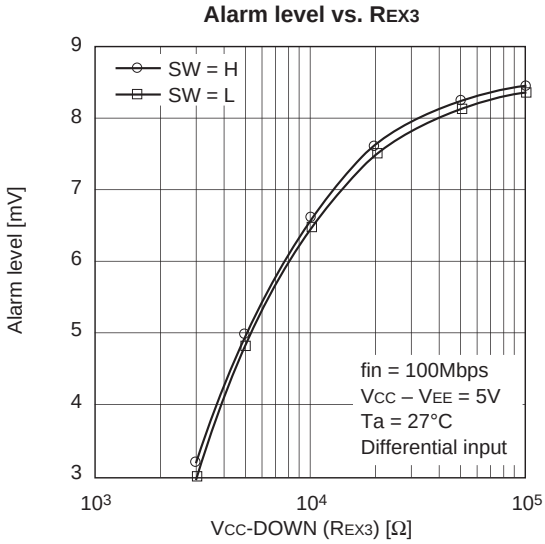


Fig. 18

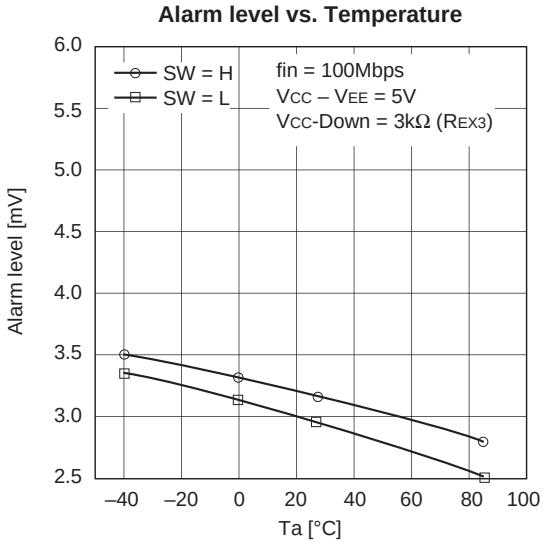


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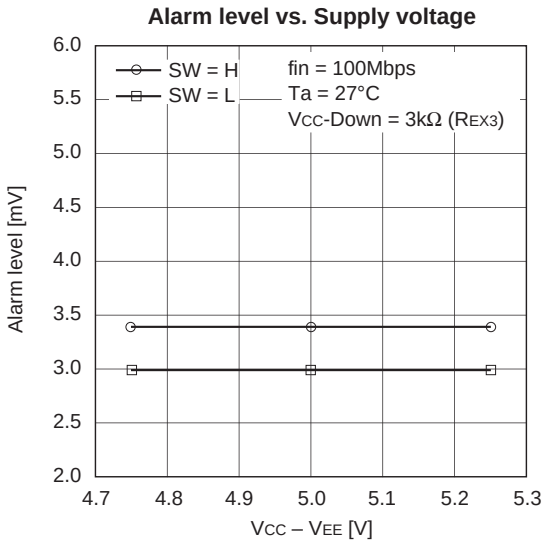


Fig. 20

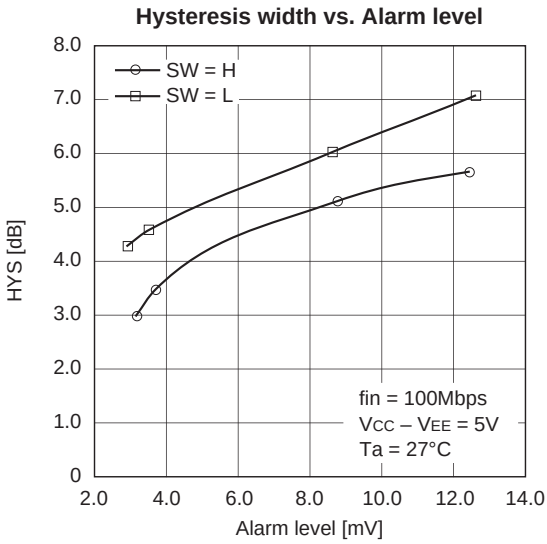


Fig. 21

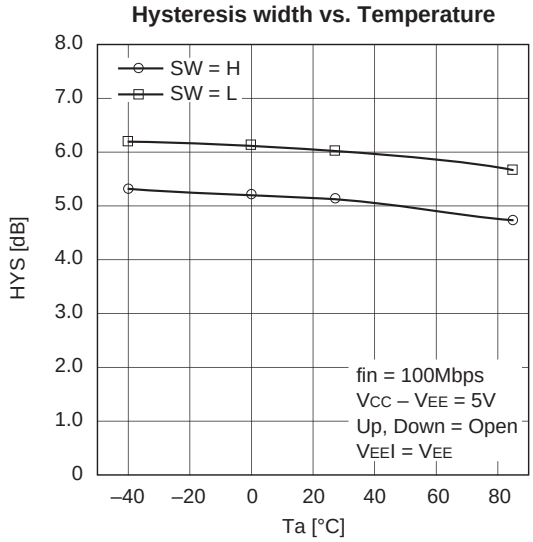


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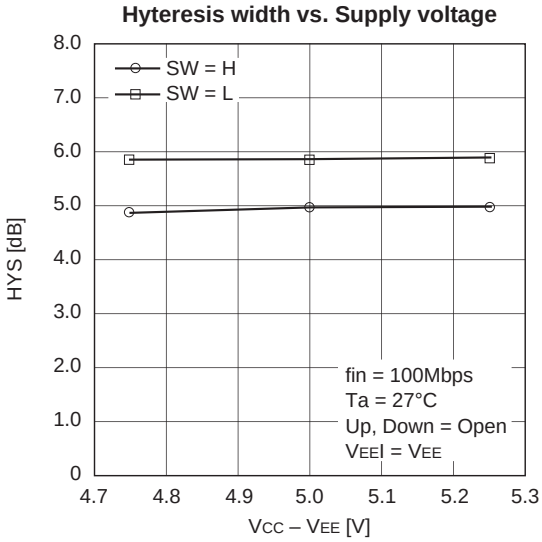


Fig. 23

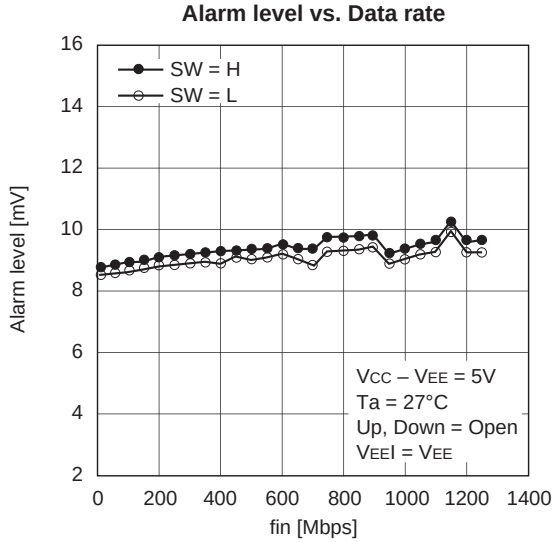


Fig. 24

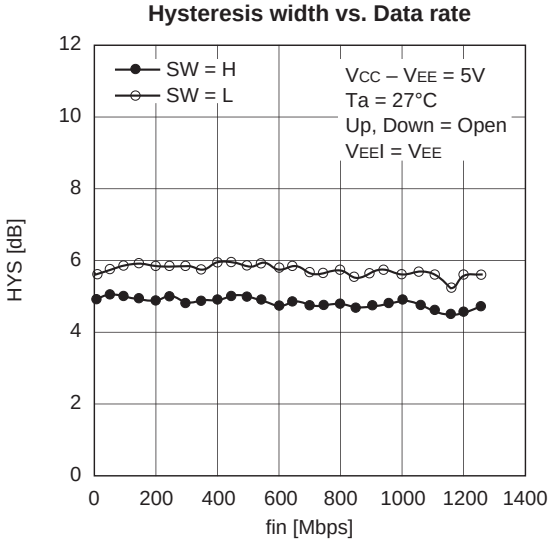


Fig. 25

4. DC voltage

SD-ECL "H" level vs. Supply voltage

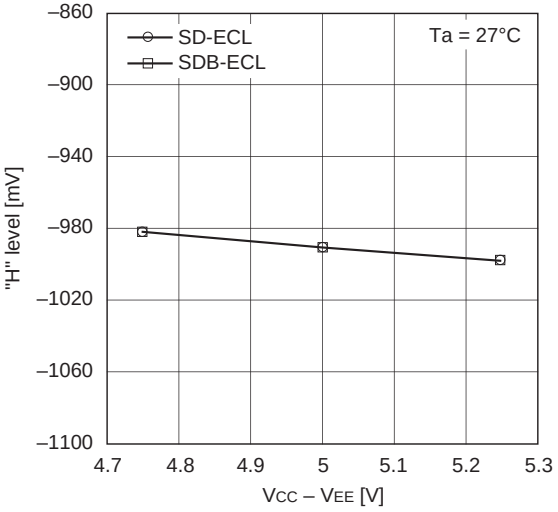


Fig. 26

SD-ECL "H" level vs. Temperature

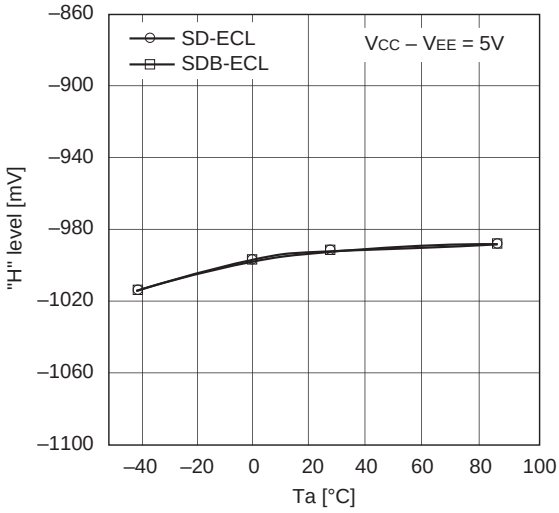


Fig. 27

SD-ECL "L" level vs. Supply voltage

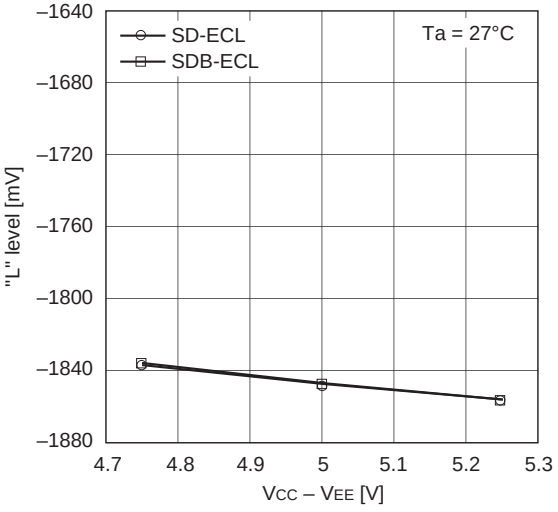


Fig. 28

SD-ECL "L" level vs. Temperature

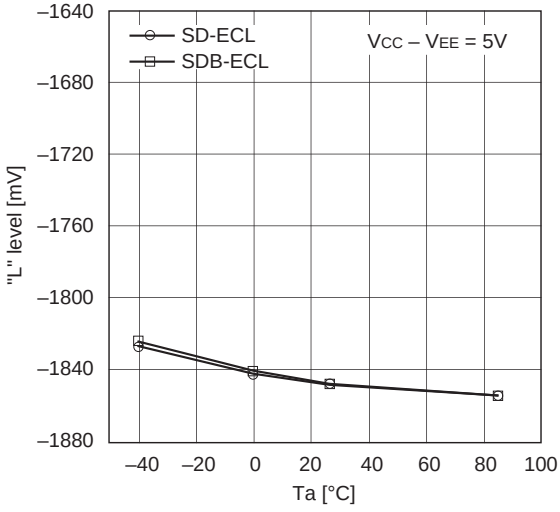


Fig. 29

SD-TTL "H" level vs. Supply voltage

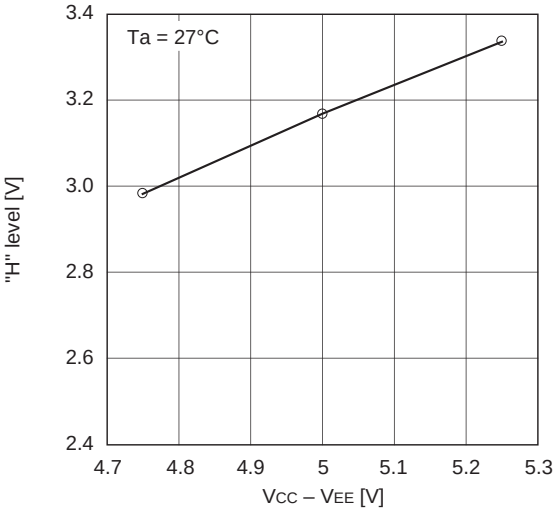


Fig. 30

SD-TTL "H" level vs. Temperature

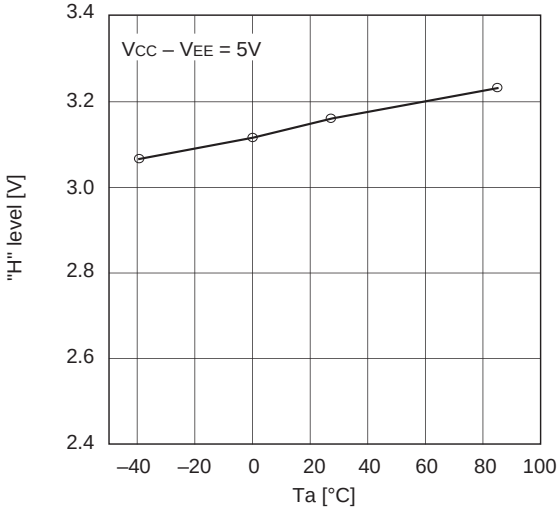


Fig. 31

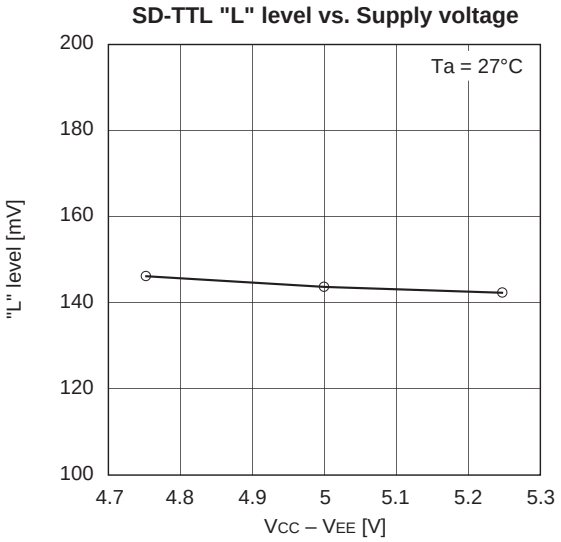


Fig. 32

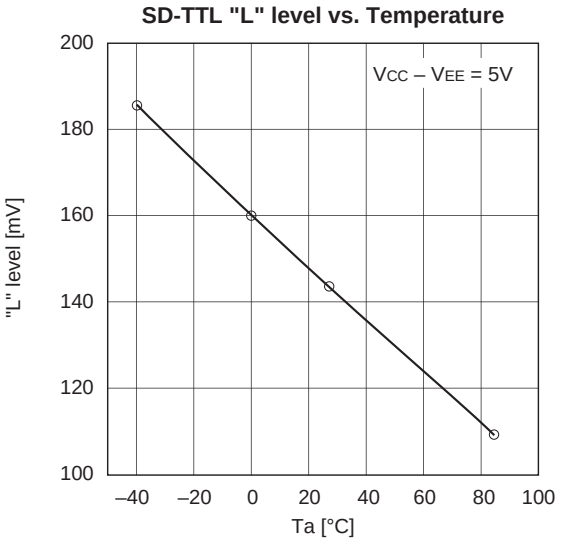


Fig. 33

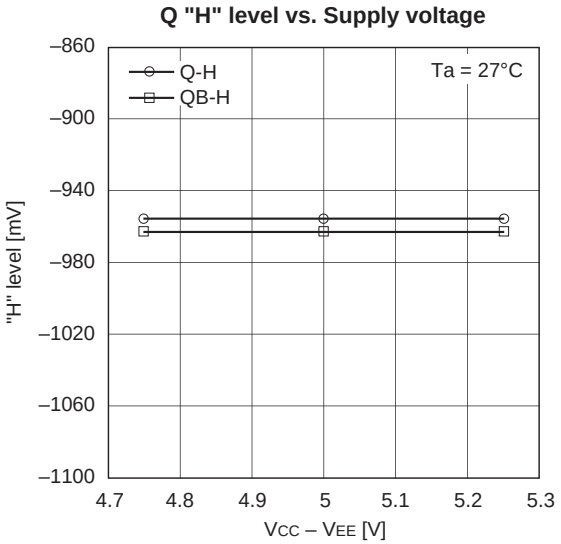


Fig. 34

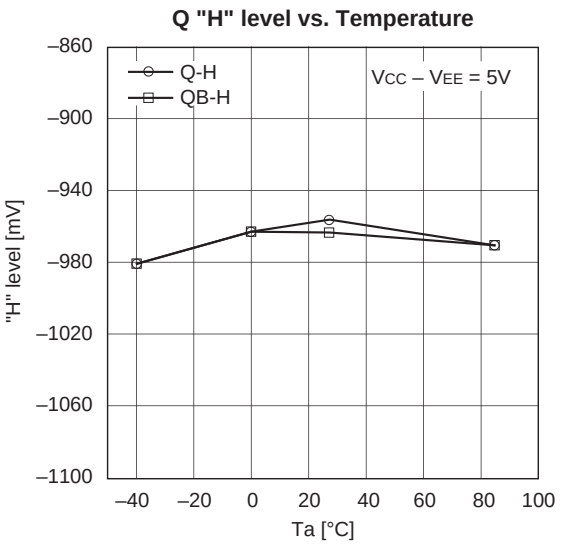


Fig. 35

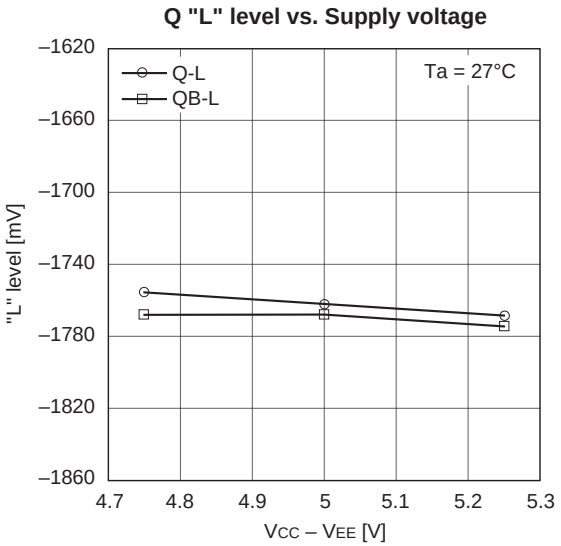


Fig. 36

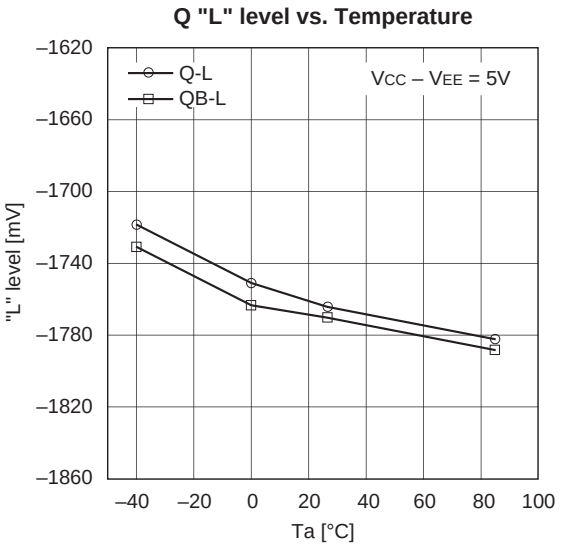
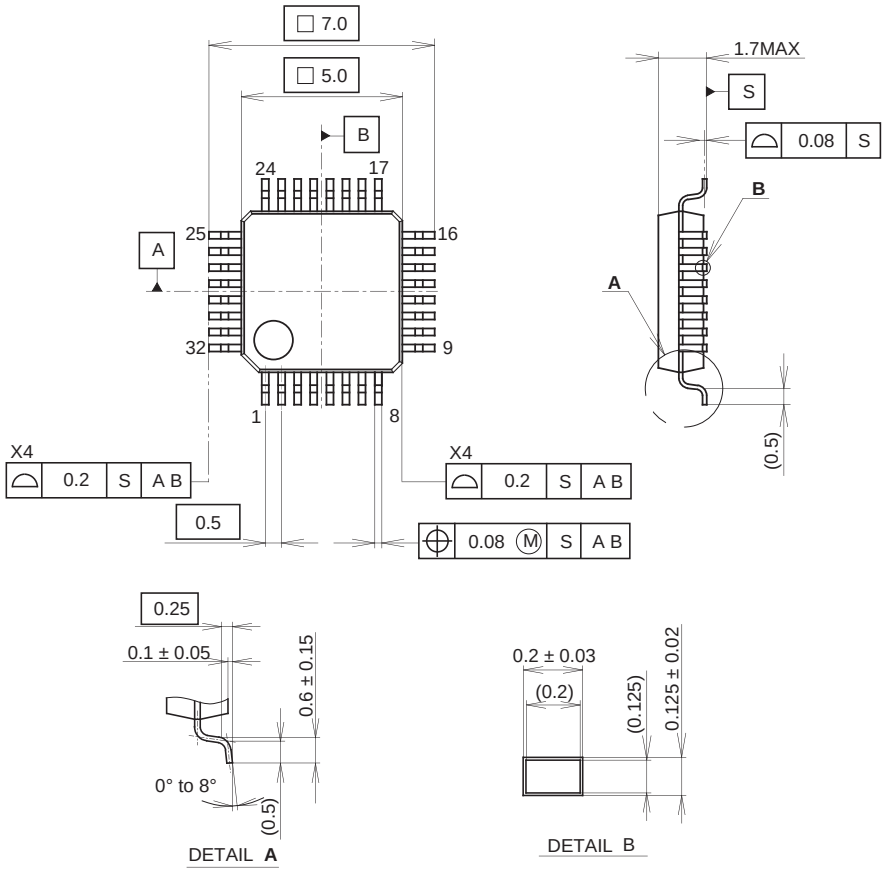


Fig. 37

Package Outline Unit: mm

32PIN LQFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	LQFP-32P-L01
EIAJ CODE	LQFP032-P-0505
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.1g

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).