LMH6554 2.8 GHz Ultra Linear Fully Differential Amplifier

Check for Samples: LMH6554

FEATURES

- **Small Signal Bandwidth 2.8 GHz**
- **2 V_{PP} Large Signal Bandwidth 1.8 GHz**
- **0.1 dB Gain Flatness 830 MHz**
- **OIP3 @ 150 MHz 46.5 dBm**
- **HD2/HD3 @ 75 MHz -96 / -97 dBc**
- **Input Noise Voltage 0.9 nV/√Hz**
- **Input Noise Current 11 pA/√Hz**
- **Slew Rate 6200 V/µs**
- **Power 260mW**
- **Typical Supply Current 52 mA**
- **Package 14 Lead UQFN**

APPLICATIONS

- **Differential ADC Driver**
- **Single-Ended to Differential Converter**
- **High Speed Differential Signaling**
- **IF/RF and Baseband Gain Blocks**
- **SAW Filter Buffer/Driver**
- **Oscilloscope Probes**
- **Automotive Safety Applications**
- **Video Over Twisted Pair**
- **Differential Line Driver**

DESCRIPTION

The LMH6554 is a high performance fully differential amplifier designed to provide the exceptional signal fidelity and wide large-signal bandwidth necessary for driving 8 to 16 bit high speed data acquisition systems. Using TI's proprietary differential current mode input stage architecture, the LMH6554 has unity gain, small-signal bandwidth of 2.8 GHz and allows operation at gains greater than unity without sacrificing response flatness, bandwidth, harmonic distortion, or output noise performance.

The device's low impedance differential output is designed to drive ADC inputs and any intermediate filter stage. The LMH6554 delivers 16-bit linearity up to 75 MHz when driving 2V peak-to-peak into loads as low as 200Ω.

The LMH6554 is fabricated in Texas Instruments' advanced complementary BiCMOS process and is available in a space saving 14 lead UQFN package for higher performance.

Typical Application

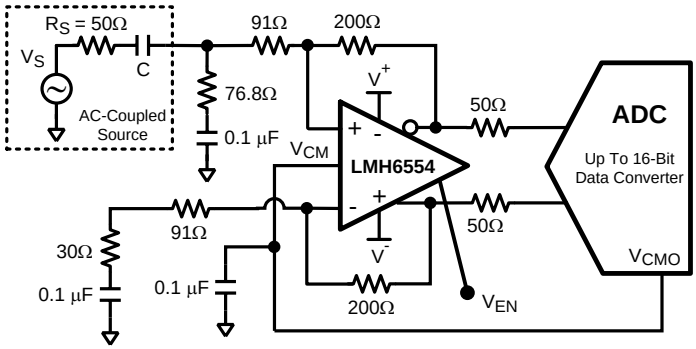


Figure 1. Single to Differential ADC Driver

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

ESD Tolerance (3)	Human Body Model	2000V
	Machine Model	250V
	Charge Device Model	750V
Supply Voltage ($V_S = V^+ - V^-$)		5.5V
Common Mode Input Voltage		From V^- to V^+
Maximum Input Current		30mA
Maximum Output Current (pins 12, 13)		(4)
Soldering Information Infrared or Convection (30 sec)		260°C
For soldering specifications see SNOA549		

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the Electrical Characteristics tables.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human Body Model, applicable std. MIL-STD-883, Method 30157. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC). Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(4) The maximum output current (I_{OUT}) is determined by device power dissipation limitations. See the Power Dissipation section of Application Information for more details.

Operating Ratings (1)

Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Total Supply Voltage Temperature Range	4.7V to 5.25V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the Electrical Characteristics tables.

Thermal Properties

Junction-to-Ambient Thermal Resistance (θ_{JA})	60°C/W
Maximum Operating Junction Temperature	150°C

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+5V Electrical Characteristics (1)

Unless otherwise specified, all limits are ensured for T_A = +25°C, A_V = +2, V^+ = +2.5V, V− = −2.5V, R_L = 200Ω, V_{CM} = (V^++V^-)/2, R_F = 200Ω, for single-ended in, differential out. Boldface Limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
AC Performance (Differential)						
SSBW	Small Signal −3 dB Bandwidth (2)	A_V = 1, V_{OUT} = 0.2 V_{PP}		2800		MHz
		A_V = 2, V_{OUT} = 0.2 V_{PP}		2500		
		A_V = 4, V_{OUT} = 0.2 V_{PP}		1600		
LSBW	Large Signal Bandwidth	A_V = 1, V_{OUT} = 2 V_{PP}		1800		MHz
		A_V = 2, V_{OUT} = 2 V_{PP}		1500		
		A_V = 2, V_{OUT} = 1.5 V_{PP}		1900		
0.1 dBBW	0.1 dB Bandwidth	A_V = 2, V_{OUT} = 0.2 V_{PP}, R_F = 250Ω		830		MHz
SR	Slew Rate	4V Step		6200		V/µs
t_r/t_f	Rise/Fall Time	2V Step, 10–90%		290		ps
		0.4V Step, 10–90%		150		
$T_{s_0.1}$	0.1% Settling Time	2V Step, R_L = 200Ω		4		ns
	Overdrive Recovery Time	V_{IN} = 2V, A_V = 5 V/V		6		ns
Distortion and Noise Response						
HD2	2nd Harmonic Distortion	V_{OUT} = 2 V_{PP}, f = 20 MHz		-102		dBc
		V_{OUT} = 2 V_{PP}, f = 75 MHz		-96		
		V_{OUT} = 2 V_{PP}, f = 125 MHz		-87		
		V_{OUT} = 2 V_{PP}, f = 250 MHz		−79		
		V_{OUT} = 1.5 V_{PP}, f = 250 MHz		−81		
HD3	3rd Harmonic Distortion	V_{OUT} = 2 V_{PP}, f = 20 MHz		−110		dBc
		V_{OUT} = 2 V_{PP}, f = 75 MHz		−97		
		V_{OUT} = 2 V_{PP}, f = 125 MHz		−87		
		V_{OUT} = 2 V_{PP}, f = 250 MHz		−70		
		V_{OUT} = 1.5 V_{PP}, f = 250 MHz		−75		
OIP3	Output 3rd-Order Intercept	f = 150 MHz, V_{OUT} = 2V_{PP} Composite		46.5		dBm
IMD3	Two-Tone Intermodulation	f = 150 MHz, V_{OUT} = 2V_{PP} Composite		−97		dBc
e_n	Input Voltage Noise Density	f = 10 MHz		0.9		nV/√Hz
i_{n+}	Input Noise Current	f = 10 MHz		11		pA/√Hz
i_{n-}	Input Noise Current	f = 10 MHz		11		pA/√Hz
NF	Noise Figure (4)	50Ω System, A_V = 7.3, 100 MHz		7.7		dB
Input Characteristics						
I_{BI+} / I_{BI-}			−75	−29	20	µA
TCIbi	Input Bias Current Temperature Drift			8		µA/°C
I_{BID}	Input Bias Current (5)	V_{CM} = 0V, V_{ID} = 0V, $I_{BOFFSET}$ = (I_{B-} - I_{B+})/2	−10	1	10	µA
TCIbo	Input Bias Current Diff Offset Temperature Drift (3)			0.006		µA/°C
CMRR	Common Mode Rejection Ratio	DC, V_{CM} = 0V, V_{ID} = 0V		83		dB

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A. See Application Information for information on temperature de-rating of this device." Min/Max ratings are based on product characterization and simulation. Individual parameters are tested as noted.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) For test schematic, refer to Figure 35.
(5) I_{BI} is referred to a differential output offset voltage by the following relationship: $V_{OD(OFFSET)}$ = I_{BI}*2R_F.

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+5V Electrical Characteristics (1) (continued)

Unless otherwise specified, all limits are ensured for T_A = +25°C, A_V = +2, V^+ = +2.5V, V− = −2.5V, R_L = 200Ω, V_{CM} = (V^++V^-)/2, R_F = 200Ω, for single-ended in, differential out. Boldface Limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
R_{IN}	Differential Input Resistance	Differential		19		Ω
C_{IN}	Differential Input Capacitance	Differential		1		pF
CMVR	Input Common Mode Voltage Range	CMRR > 32 dB	±1.25	±1.3		V
Output Performance						
	Output Voltage Swing (3)	Single-Ended Output	±1.35	±1.42		V
I_{OUT}	Output Current (3)	V_{OUT} = 0V	±120	±150		mA
I_{SC}	Short Circuit Current	One Output Shorted to Ground V_{IN} = 2V Single-Ended (6)		150		mA
	Output Balance Error	ΔVOUT Common Mode /ΔV_{OUT} Differential, ΔV_{OD} = 1V, f < 1 Mhz		−64		dB
Output Common Mode Control Circuit						
	Common Mode Small Signal Bandwidth	V_{IN^+} = V_{IN^-} = 0V		500		MHz
	Slew Rate	V_{IN^+} = V_{IN^-} = 0V		200		V/µs
V_{OSCM}	Input Offset Voltage	Common Mode, V_{ID} = 0, V_{CM} = 0V	−16	−6.5	4	mV
I_{OSCM}	Input Offset Current	(7)		6	18	µA
	Voltage Range		±1.18	±1.25		V
	CMRR	Measure V_{OD}, V_{ID} = 0V		82		dB
	Input Resistance			180		kΩ
	Gain	$\Delta V_{OCM}/\Delta V_{CM}$	0.99	0.995	1.0	V/V
Miscellaneous Performance						
Z_T	Open Loop Transimpedance Gain	Differential		180		kΩ
PSRR	Power Supply Rejection Ratio	DC, ΔV^+ = ΔV^- = 1V	74	95		dB
I_S	Supply Current (8)	R_L = ∞	46	52	57 **60**	mA
	Enable Voltage Threshold	Single 5V Supply (9)		2.5		V
	Disable Voltage Threshold	Single 5V Supply (9)		2.5		V
	Enable/Disable Time			15		ns
I_{SD}	Supply Current, Disabled	Enable=0, Single 5V supply	450	510	570 **600**	µA

(6) Short circuit current should be limited in duration to no more than 10 seconds. See the Power Dissipation section of Application Information for more details.
(7) Negative input current implies current flowing out of the device.
(8) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(9) V_{EN} threshold is typically +/-0.3V centered around (V^+ + V^-) / 2 relative to ground.

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Connection Diagram

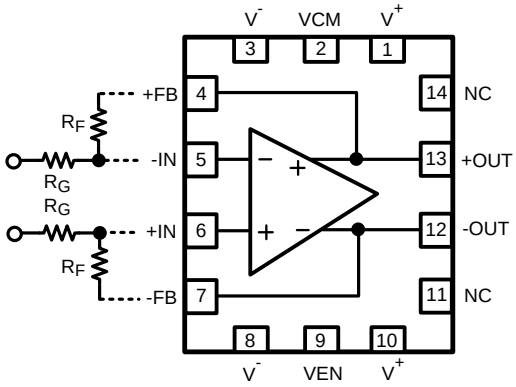


Figure 2. 14 Lead UQFN - Top View
See Package Number NHJ0014A

Typical Performance Characteristics V_S = ±2.5V

(T_A = 25°C, R_F = 200Ω, R_G = 90Ω, R_T = 76.8Ω, R_L = 200Ω, A_V = +2, for single ended in, differential out, unless specified).

Frequency Response vs. R_F

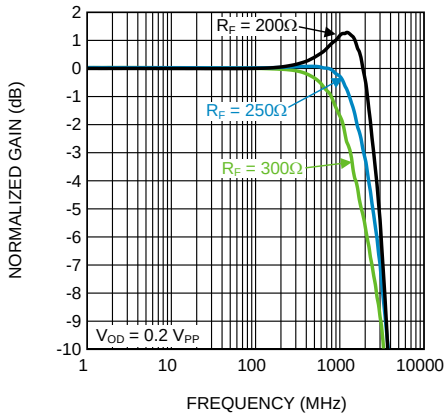


Figure 3.

Frequency Response vs. Gain

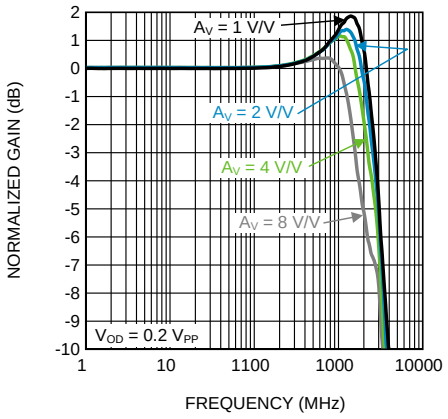


Figure 4.

Frequency Response vs. R_L

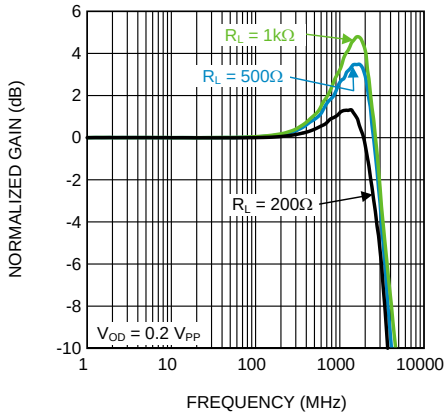


Figure 5.

Frequency Response vs. Output Voltage (V_{OD})

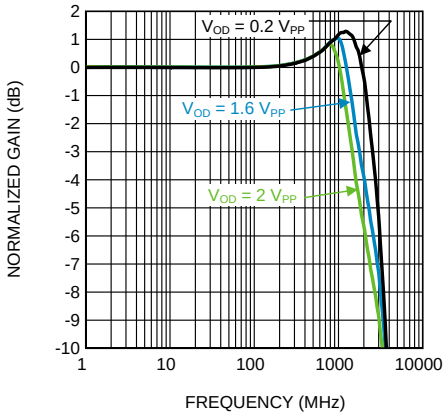


Figure 6.

Frequency Response vs. Capacitive Load

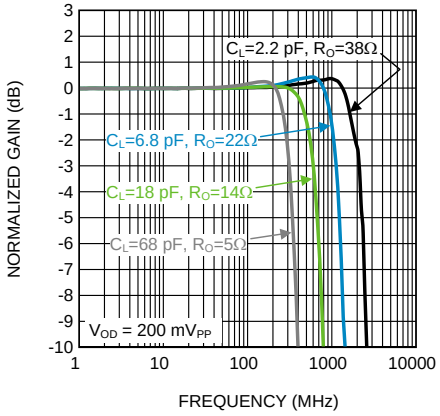


Figure 7.

Suggested R_{OUT} vs. Capacitive Load

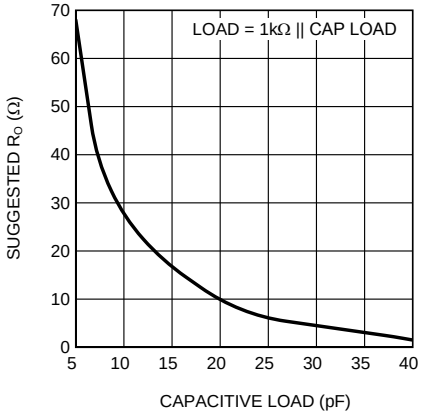


Figure 8.

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Typical Performance Characteristics V_S = ±2.5V (continued)

(T_A = 25°C, R_F = 200Ω, R_G = 90Ω, R_T = 76.8Ω, R_L = 200Ω, A_V = +2, for single ended in, differential out, unless specified).

0.5 V_{PP} Pulse Response Single Ended Input

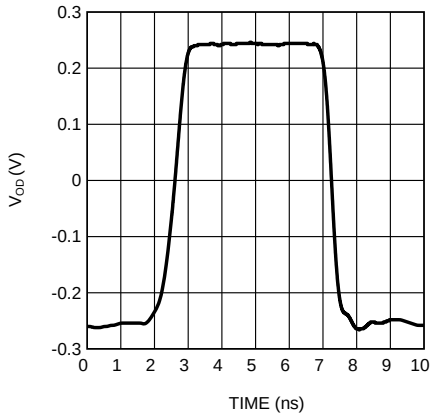


Figure 9.

2 V_{PP} Pulse Response Single Ended Input

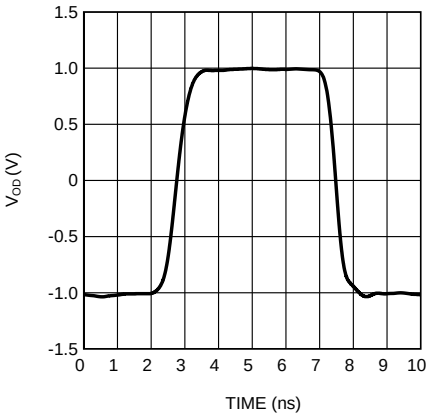


Figure 10.

4 V_{PP} Pulse Response Single Ended Input

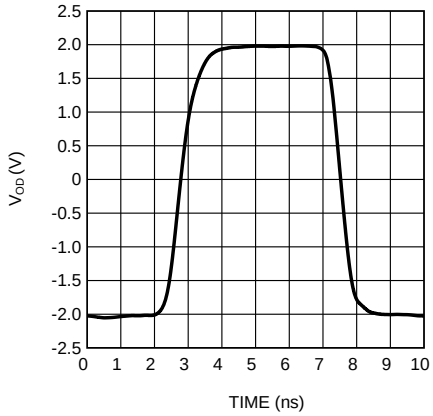


Figure 11.

Distortion vs. Frequency Single Ended Input

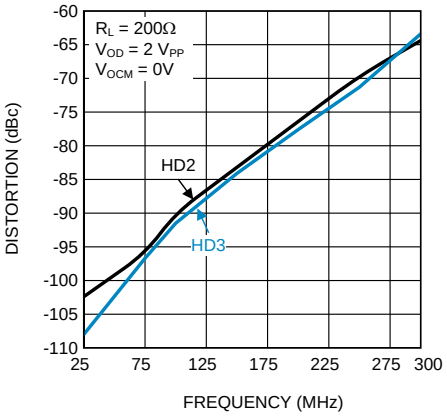


Figure 12.

Distortion vs. Output Common Mode Voltage

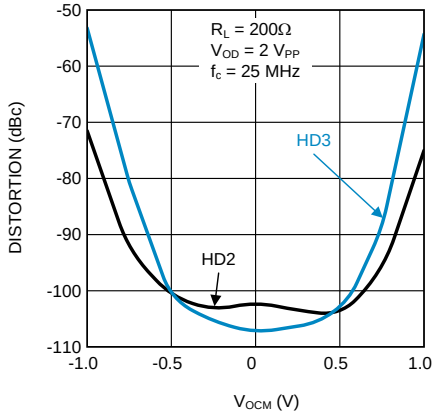


Figure 13.

Distortion vs. Output Common Mode Voltage

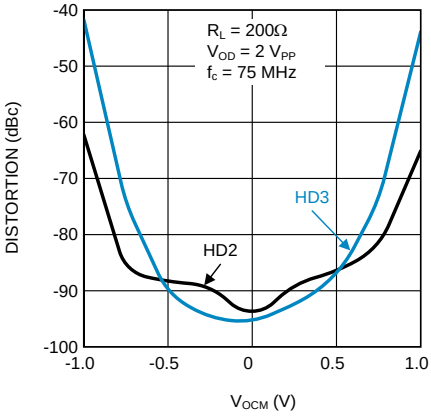


Figure 14.

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Typical Performance Characteristics V_S = ±2.5V (continued)

(T_A = 25°C, R_F = 200Ω, R_G = 90Ω, R_T = 76.8Ω, R_L = 200Ω, A_V = +2, for single ended in, differential out, unless specified).

Distortion vs. Output Common Mode Voltage

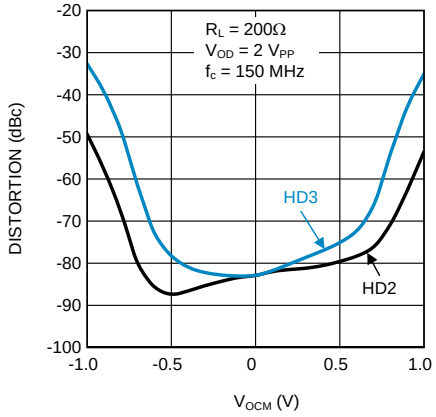


Figure 15.

3rd Order Intermodulation Products vs V_{OUT}

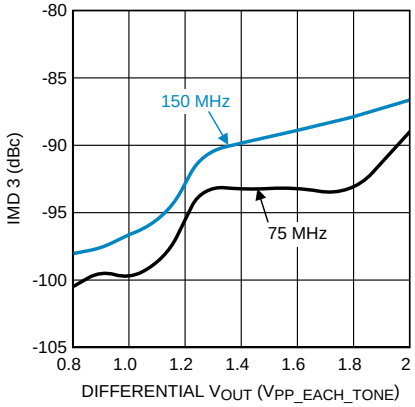


Figure 16.

OIP3 vs Output Power P_{OUT}

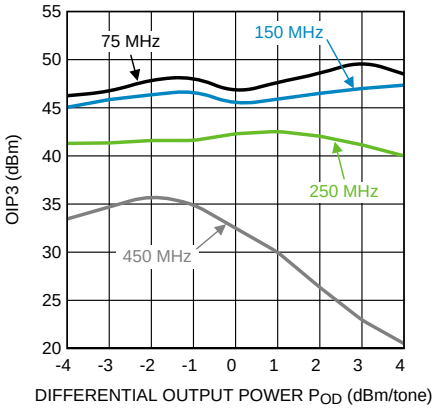


Figure 17.

OIP3 vs Center Frequency

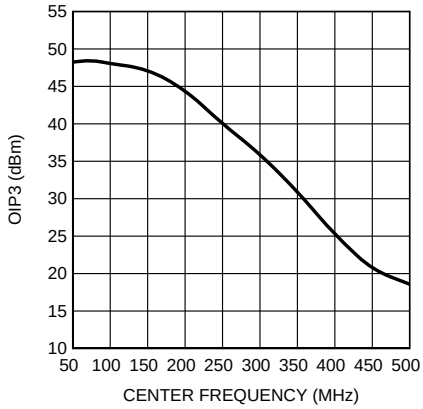


Figure 18.

Noise Figure vs Frequency

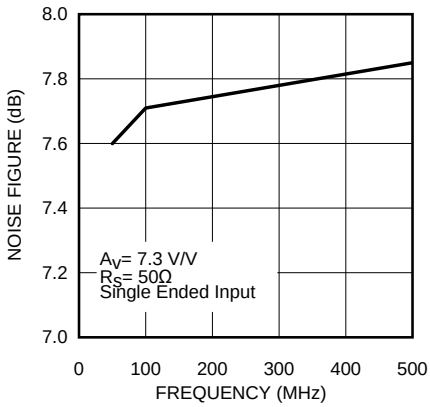


Figure 19.

Maximum V_{OUT} vs. I_{OUT}

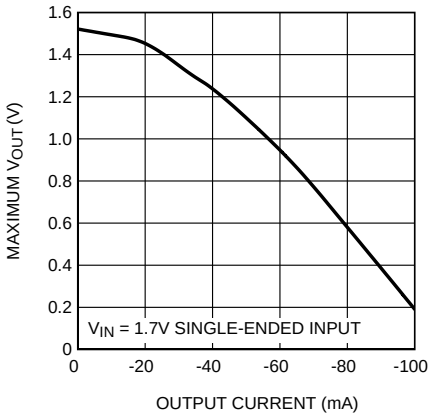


Figure 20.

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Typical Performance Characteristics V_S = ±2.5V (continued)

(T_A = 25°C, R_F = 200Ω, R_G = 90Ω, R_T = 76.8Ω, R_L = 200Ω, A_V = +2, for single ended in, differential out, unless specified).

Minimum V_{OUT} vs. I_{OUT}

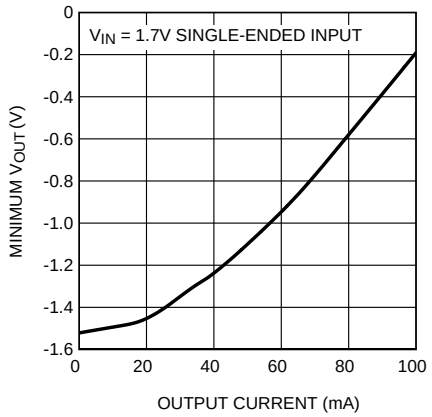


Figure 21.

Overdrive Recovery

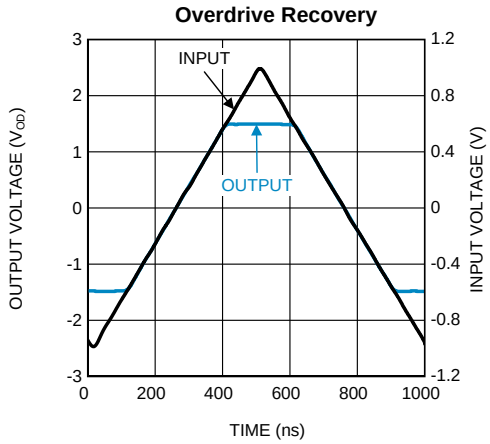


Figure 22.

PSRR

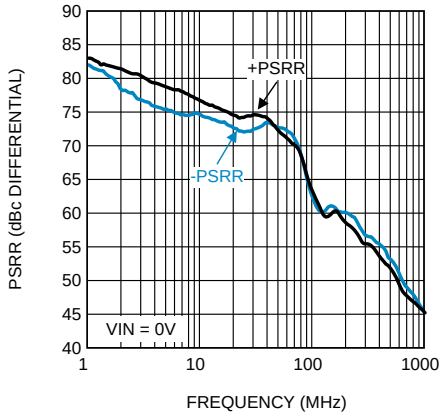


Figure 23.

CMRR

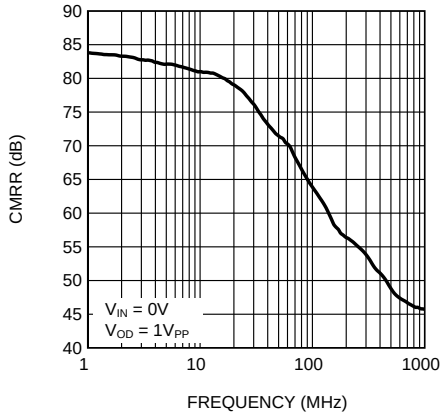


Figure 24.

Balance Error

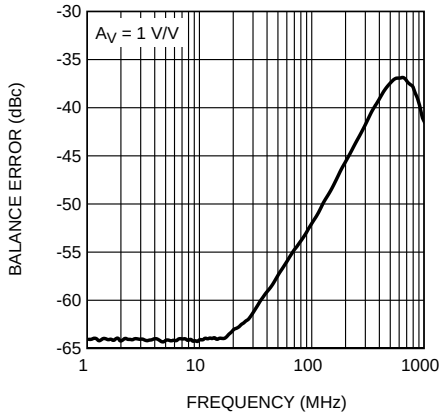


Figure 25.

Open Loop Transimpedance

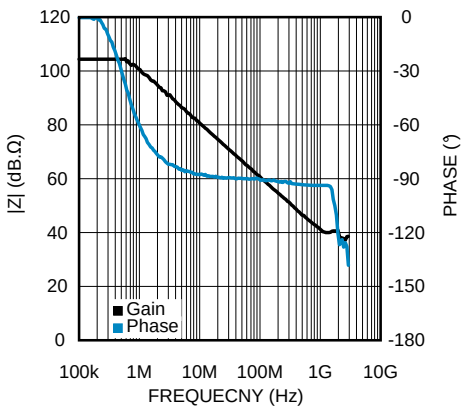


Figure 26.

Typical Performance Characteristics V_S = ±2.5V (continued)

(T_A = 25°C, R_F = 200Ω, R_G = 90Ω, R_T = 76.8Ω, R_L = 200Ω, A_V = +2, for single ended in, differential out, unless specified).

Closed Loop Output Impedance

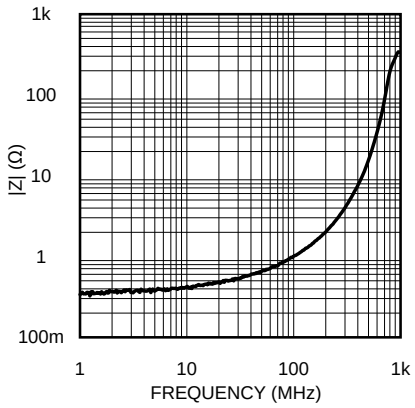


Figure 27.

Differential S-Parameter Magnitude vs. Frequency

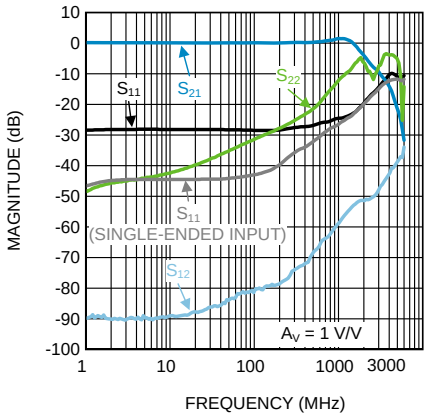


Figure 28.

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APPLICATION INFORMATION

The LMH6554 is a fully differential, current feedback amplifier with integrated output common mode control, designed to provide low distortion amplification to wide bandwidth differential signals. The common mode feedback circuit sets the output common mode voltage independent of the input common mode, as well as forcing the V^+ and V^- outputs to be equal in magnitude and opposite in phase, even when only one of the inputs is driven as in single to differential conversion.

The proprietary current feedback architecture of the LMH6554 offers gain and bandwidth independence with exceptional gain flatness and noise performance, even at high values of gain, simply with the appropriate choice of R_{F1} and R_{F2}. Generally R_{F1} is set equal to R_{F2}, and R_{G1} equal to R_{G2}, so that the gain is set by the ratio R_F/R_G. Matching of these resistors greatly affects CMRR, DC offset error, and output balance. A maximum of 0.1% tolerance resistors are recommended for optimal performance, and the amplifier is internally compensated to operate with optimum gain flatness with R_F value of 200Ω depending on PCB layout, and load resistance.

The output common mode voltage is set by the V_{CM} pin with a fixed gain of 1 V/V. This pin should be driven by a low impedance reference and should be bypassed to ground with a 0.1 µF ceramic capacitor. Any unwanted signal coupling into the V_{CM} pin will be passed along to the outputs, reducing the performance of the amplifier.

The LMH6554 can be configured to operate on a single 5V supply connected to V+ with V- grounded or configured for a split supply operation with V^+ = +2.5V and V^- = −2.5V. Operation on a single 5V supply, depending on gain, is limited by the input common mode range; therefore, AC coupling may be required. Split supplies will allow much less restricted AC and DC coupled operation with optimum distortion performance.

Enable / Disable Operation

The LMH6554 is equipped with an enable pin (V_{EN}) to reduce power consumption when not in use. The V_{EN} pin, when not driven, floats high (on). When the V_{EN} pin is pulled low, the amplifier is disabled and the amplifier output stage goes into a high impedance state so the feedback and gain set resistors determine the output impedance of the circuit. For this reason input to output isolation will be poor in the disabled state and the part is not recommended in multiplexed applications where outputs are all tied together.

With a 5V difference between V^+ and V^-, the V_{EN} threshold is ½ way between the supplies (e.g. 2.5V with 5V single supply) as shown in Figure 29. R2 ensures active (enable) mode with V_{EN} floating, and R1 provides input current limiting. V_{EN} also has ESD diodes to either supply.

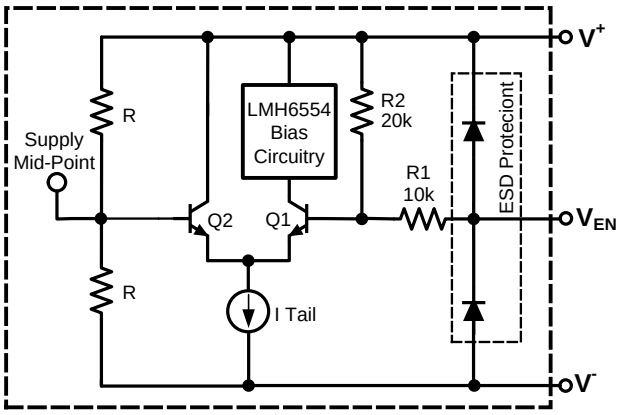


Figure 29. Enable Block Diagram

Fully Differential Operation

The LMH6554 will perform best in a fully differential configuration. The circuit shown in Figure 30 is a typical fully differential application circuit as might be used to drive an analog to digital converter (ADC). In this circuit the closed loop gain is $A_V = V_{OUT} / V_{IN} = R_F / R_G$, where the feedback is symmetric. The series output resistors, R_O, are optional and help keep the amplifier stable when presented with a capacitive load. Refer to the Driving Capacitive Loads section for details.

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Here is the expression for the input impedance, R_{IN}, as defined in Figure 30:

$R_{IN} = 2R_G$

When driven from a differential source, the LMH6554 provides low distortion, excellent balance, and common mode rejection. This is true provided the resistors R_F, R_G and R_O are well matched and strict symmetry is observed in board layout. With an intrinsic device CMRR of greater than 70 dB, using 0.1% resistors will give a worst case CMRR of around 50 dB for most circuits.

The circuit configuration shown in Figure 30 was used to measure differential S-parameters in a 100Ω environment at a gain of 1 V/V. Refer to Figure 28 in Typical Performance Characteristics V_S = ±2.5V for measurement results.

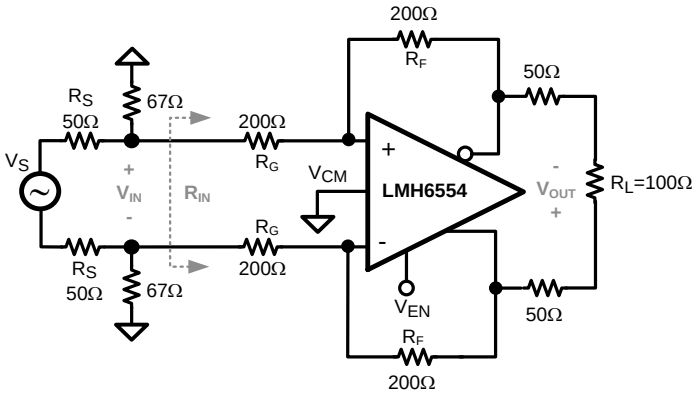
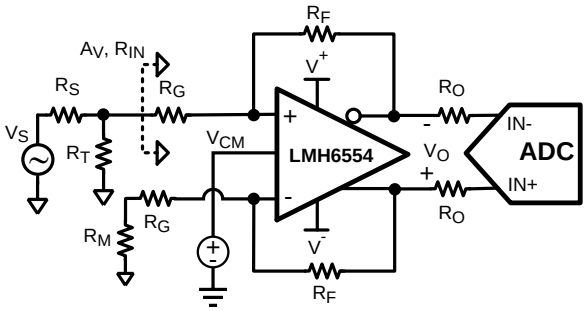


Figure 30. Differential S-Parameter Test Circuit

Single Ended Input To Differential Output Operation

In many applications, it is required to drive a differential input ADC from a single ended source. Traditionally, transformers have been used to provide single to differential conversion, but these are inherently bandpass by nature and cannot be used for DC coupled applications. The LMH6554 provides excellent performance as a single-ended input to differential output converter down to DC. Figure 31 shows a typical application circuit where an LMH6554 is used to produce a balanced differential output signal from a single ended source.



$$A_V = \left(\frac{2(1-\beta_1)}{\beta_1+\beta_2}\right) \qquad \beta_1 = \left(\frac{R_G}{R_G+R_F}\right)$$

$$R_{IN} = \left(\frac{2R_G + R_M(1-\beta_2)}{1+\beta_2}\right) \qquad \beta_2 = \left(\frac{R_G+R_M}{R_G+R_F+R_M}\right)$$

$$R_S = R_T \parallel R_{IN} \qquad R_M = R_T \parallel R_S$$

Figure 31. Single Ended Input with Differential Output

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When using the LMH6554 in single-to-differential mode, the complimentary output is forced to a phase inverted replica of the driven output by the common mode feedback circuit as opposed to being driven by its own complimentary input. Consequently, as the driven input changes, the common mode feedback action results in a varying common mode voltage at the amplifier's inputs, proportional to the driving signal. Due to the non-ideal common mode rejection of the amplifier's input stage, a small common mode signal appears at the outputs which is superimposed on the differential output signal. The ratio of the change in output common mode voltage to output differential voltage is commonly referred to as output balance error. The output balance error response of the LMH6554 over frequency is shown in the Typical Performance Characteristics V_S = ±2.5V.

To match the input impedance of the circuit in Figure 31 to a specified source resistance, R_S, requries that R_T || R_{IN} = R_S. The equations governing R_{IN} and A_V for single-to-differential operation are also provide in Figure 31. These equations, along with the source matching condition, must be solved iteratively to achieve the desired gain with the proper input termination. Component values for several common gain configuration in a 50Ω environment are given in Table 1.

Table 1. Gain Component Values for 50Ω System

Gain	R_F	R_G	R_T	R_M
0dB	200Ω	191Ω	62Ω	27.7Ω
6dB	200Ω	91Ω	76.8Ω	30.3Ω
12dB	200Ω	35.7Ω	147Ω	37.3Ω

Single Supply Operation

Single 5V supply operation is possible: however, as discussed earlier, AC input coupling is recommended due to input common mode limitations. An example of an AC coupled, single supply, single-to-differential circuit is shown in Figure 32. Note that when AC coupling, both inputs need to be AC coupled irrespective of single-to-differential or differential-differential configuration. For higher supply voltages DC coupling of the inputs may be possible provided that the output common mode DC level is set high enough so that the amplifier's inputs and outputs are within their specified operation ranges.

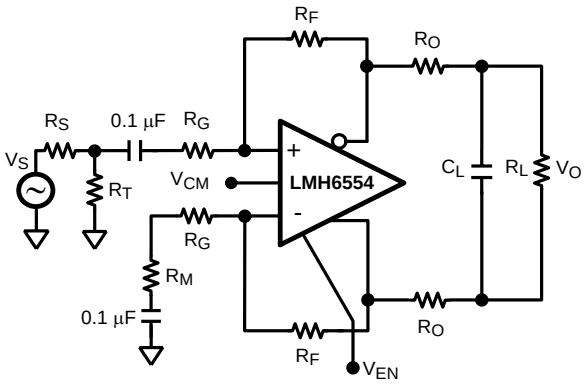


Figure 32. AC Coupled for Single Supply Operation

Split Supply Operation

For optimum performance, split supply operation is recommended using +2.5V and −2.5V supplies; however, operation is possible on split supplies as low as +2.35V and −2.35V and as high as +2.65V and −2.65V. Provided the total supply voltage does not exceed the 4.7V to 5.3V operating specification, non-symmetric supply operation is also possible and in some cases advantageous. For example, if a 5V DC coupled operation is required for low power dissipation but the amplifier input common mode range prevents this operation, it is still possible with split supplies of (V+) and (V-). Where (V+)-(V-) = 5V and V+ and V- are selected to center the amplifier input common mode range to suit the application.

Driving Analog To Digital Converters

Analog-to-digital converters present challenging load conditions. They typically have high impedance inputs with large and often variable capacitive components. Figure 34 shows the LMH6554 driving an ultra-high-speed Gigasample ADC the ADC10D1500. The LMH6554 common mode voltage is set by the ADC10D1500. The circuit in Figure 34 has a 2nd order bandpass LC filter across the differential inputs of the ADC10D1500. The ADC10D1500 is a dual channel 10–bit ADC with maximum sampling rate of 3 GSPS when operating in a single channel mode and 1.5 GSPS in dual channel mode.

Figure 33 shows the SFDR and SNR performance vs. frequency for the LMH6554 and ADC10D1500 combination circuit with the ADC input signal level at −1dBFS. In order to properly match the input impedance seen at the LMH6554 amplifier inputs, R_M is chosen to match Z_S || R_T for proper input balance. The amplifier is configured to provide a gain of 2 V/V in single to differential mode. An external bandpass filter is inserted in series between the input signal source and the amplifier to reduce harmonics and noise from the signal generator.

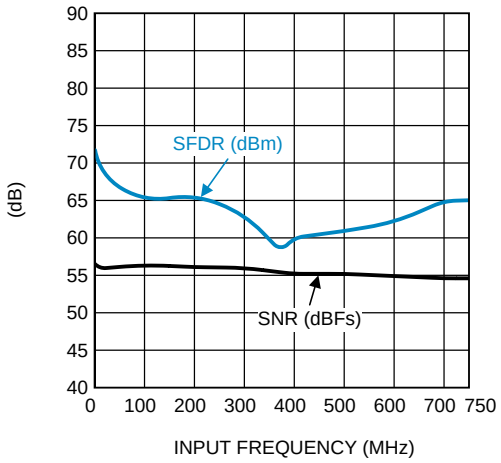


Figure 33. LMH6554 / ADC10D1500 SFDR and SNR Performance vs. Frequency

The amplifier and ADC should be located as close together as possible. Both devices require that the filter components be in close proximity to them. The amplifier needs to have minimal parasitic loading on it's outputs and the ADC is sensitive to high frequency noise that may couple in on its inputs. Some high performance ADCs have an input stage that has a bandwidth of several times its sample rate. The sampling process results in all input signals presented to the input stage mixing down into the first Nyquist zone (DC to Fs/2).

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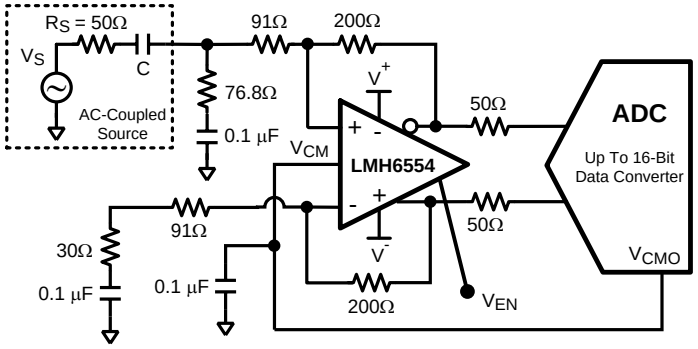


Figure 34. Driving a 10-bit Gigasample ADC

Output Noise Performance and Measurement

Unlike differential amplifiers based on voltage feedback architectures, noise sources internal to the LMH6554 refer to the inputs largely as current sources, hence the low input referred voltage noise and relatively higher input referred current noise. The output noise is therefore more strongly coupled to the value of the feedback resistor and not to the closed loop gain, as would be the case with a voltage feedback differential amplifier. This allows operation of the LMH6554 at much higher gain without incurring a substantial noise performance penalty, simply by choosing a suitable feedback resistor.

Figure 35 shows a circuit configuration used to measure noise figure for the LMH6554 in a 50Ω system. A feedback resistor value of 200Ω is chosen for the UQFN package to minimize output noise while simultaneously allowing both high gain (7 V/V) and proper 50Ω input termination. Refer to Single Ended Input To Differential Output Operation for the calculation of resistor and gain values.

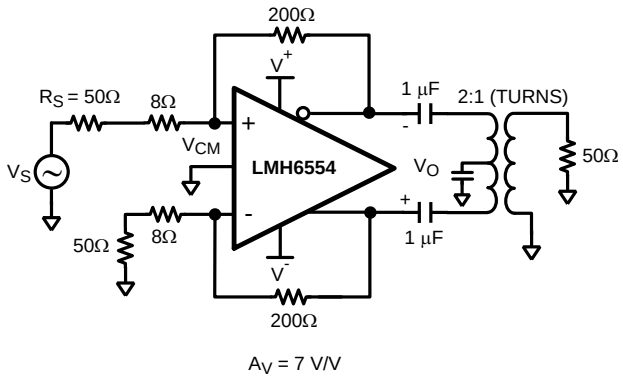


Figure 35. Noise Figure Circuit Configuration

Driving Capacitive Loads

As noted previously, capacitive loads should be isolated from the amplifier output with small valued resistors. This is particularly the case when the load has a resistive component that is 500Ω or higher. A typical ADC has capacitive components of around 10 pF and the resistive component could be 1000Ω or higher. If driving a transmission line, such as 50Ω coaxial or 100Ω twisted pair, using matching resistors will be sufficient to isolate any subsequent capacitance. For other applications see Figure 8 in Typical Performance Characteristics V_S = ±2.5V.

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Balanced Cable Driver

With up to 5.68 V_{PP} differential output voltage swing the LMH6554 can be configured as a cable driver. The LMH6554 is also suitable for driving differential cables from a single ended source as shown in Figure 36.

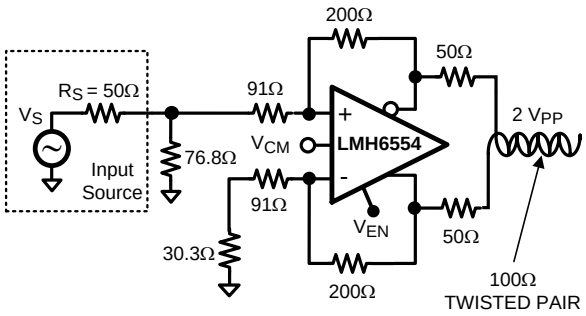


Figure 36. Fully Differential Cable Driver

Power Supply Bypassing

The LMH6554 requires supply bypassing capacitors as shown in Figure 37 and Figure 38. The 0.01 µF and 0.1 µF capacitors should be leadless SMT ceramic capacitors and should be no more than 3 mm from the supply pins. These capacitors should be star routed with a dedicated ground return plane or trace for best harmonic distortion performance. Thin traces or small vias will reduce the effectiveness of bypass capacitors. Also shown in both figures is a capacitor from the VCM and V_{EN} pins to ground. These inputs are high impedance and can provide a coupling path into the amplifier for external noise sources, possibly resulting in loss of dynamic range, degraded CMRR, degraded balance and higher distortion.

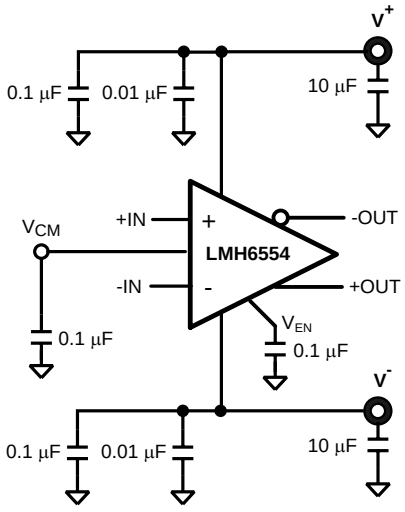


Figure 37. Split Supply Bypassing Capacitors

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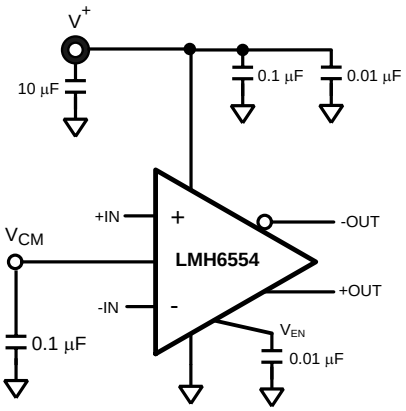


Figure 38. Single Supply Bypassing Capacitors

Power Dissipation

The LMH6554 is optimized for maximum speed and performance in a small form factor 14 lead UQFN package. To ensure maximum output drive and highest performance, thermal shutdown is not provided. Therefore, it is of utmost importance to make sure that the T_{JMAX} is never exceeded due to the overall power dissipation.

Follow these steps to determine the maximum power dissipation for the LMH6554:

1. Calculate the quiescent (no-load) power:

$P_{AMP} = I_{CC} * (V_S)$

where

- $V_S = V^+ - V^-$. (Be sure to include any current through the feedback network if V_{CM} is not mid-rail) (1)

2. Calculate the RMS power dissipated in each of the output stages:

P_D (rms) = rms $((V_S - V+_{OUT}) * I+_{OUT})$ + rms $((V_S - V-_{OUT}) * I-_{OUT})$

where

- V_{OUT} and I_{OUT} are the voltage
- the current measured at the output pins of the differential amplifier as if they were single ended amplifiers
- V_S is the total supply voltage (2)

3. Calculate the total RMS power:

$P_T = P_{AMP} + P_D$ (3)

The maximum power that the LMH6554 package can dissipate at a given temperature can be derived with the following equation:

$P_{MAX} = (150° - T_{AMB})/ \theta_{JA}$

where

- T_{AMB} = Ambient temperature (°C)
- θ_{JA} = Thermal resistance, from junction to ambient, for a given package (°C/W)
- For the 14 lead UQFN package, θ_{JA} is 60°C/W (4)

NOTE

If V_{CM} is not 0V then there will be quiescent current flowing in the feedback network. This current should be included in the thermal calculations and added into the quiescent power dissipation of the amplifier.

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ESD Protection

The LMH6554 is protected against electrostatic discharge (ESD) on all pins. The LMH6554 will survive 2000V Human Body model and 250V Machine model events. Under normal operation the ESD diodes have no affect on circuit performance. There are occasions, however, when the ESD diodes will be evident. If the LMH6554 is driven by a large signal while the device is powered down the ESD diodes will conduct. The current that flows through the ESD diodes will either exit the chip through the supply pins or will flow through the device, hence it is possible to power up a chip with a large signal applied to the input pins. Using the shutdown mode is one way to conserve power and still prevent unexpected operation.

Board Layout

The LMH6554 is a high speed, high performance amplifier. In order to get maximum benefit from the differential circuit architecture board layout and component selection is very critical. The circuit board should have a low inductance ground plane and well bypassed broad supply lines. External components should be leadless surface mount types. The feedback network and output matching resistors should be composed of short traces and precision resistors (0.1%). The output matching resistors should be placed within 3 or 4 mm of the amplifier as should the supply bypass capacitors. Refer to Power Supply Bypassing for recommendations on bypass circuit layout. Evaluation boards are available through the product folder on ti.com.

By design, the LMH6554 is relatively insensitive to parasitic capacitance at its inputs. Nonetheless, ground and power plane metal should be removed from beneath the amplifier and from beneath R_F and R_G for best performance at high frequency.

With any differential signal path, symmetry is very important. Even small amounts of asymmetry can contribute to distortion and balance errors.

Evaluation Board

See LMH6554 Product Folder for evaluation board availability and ordering information.

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REVISION HISTORY

Changes from Revision N (March 2013) to Revision O	Page
• Changed layout of National Data Sheet to TI format	18

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMH6554LE/NOPB	ACTIVE	UQFN	NHJ	14	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	AJA	Samples
LMH6554LEE/NOPB	ACTIVE	UQFN	NHJ	14	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	AJA	Samples
LMH6554LEX/NOPB	ACTIVE	UQFN	NHJ	14	4500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	AJA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

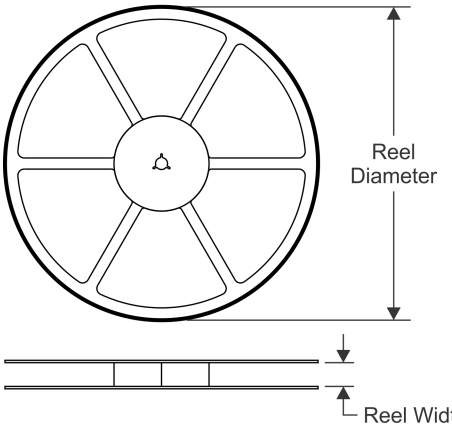
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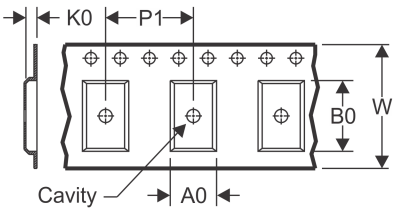
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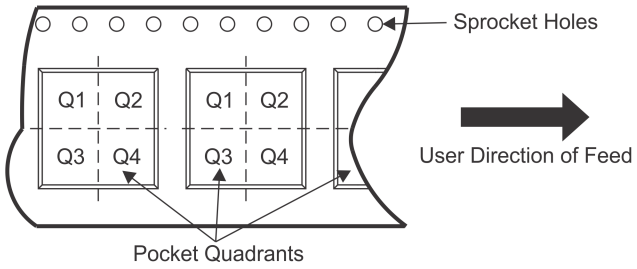


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

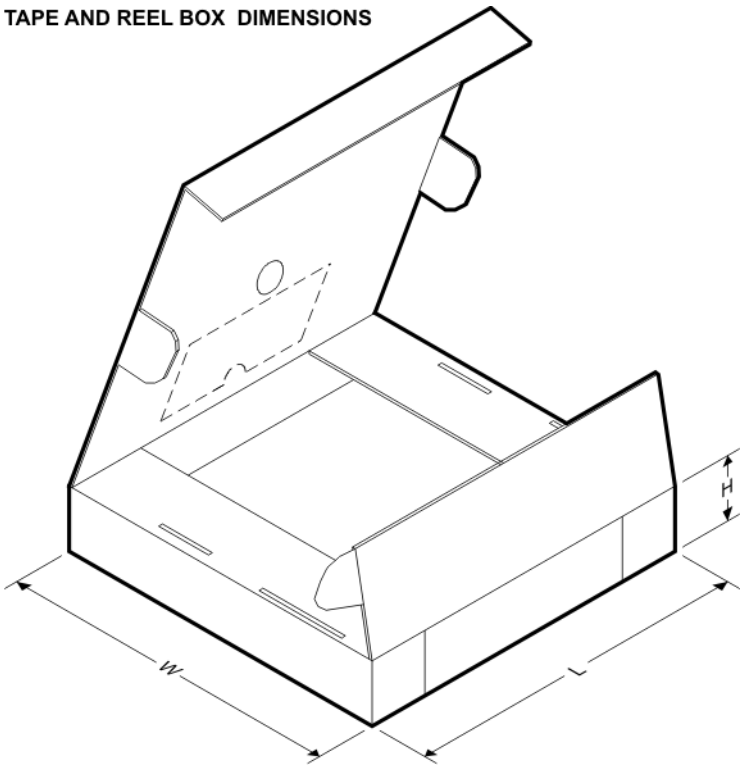
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6554LE/NOPB	UQFN	NHJ	14	1000	178.0	12.4	2.8	2.8	1.0	8.0	12.0	Q1
LMH6554LEE/NOPB	UQFN	NHJ	14	250	178.0	12.4	2.8	2.8	1.0	8.0	12.0	Q1
LMH6554LEX/NOPB	UQFN	NHJ	14	4500	330.0	12.4	2.8	2.8	1.0	8.0	12.0	Q1

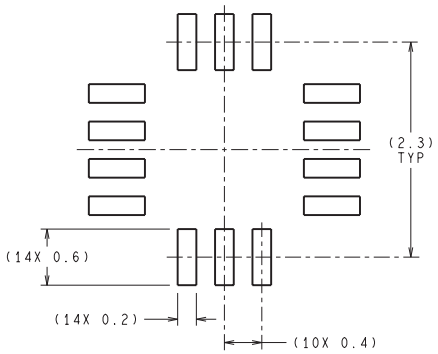
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

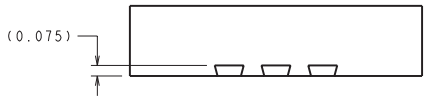
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6554LE/NOPB	UQFN	NHJ	14	1000	213.0	191.0	55.0
LMH6554LEE/NOPB	UQFN	NHJ	14	250	213.0	191.0	55.0
LMH6554LEX/NOPB	UQFN	NHJ	14	4500	367.0	367.0	35.0

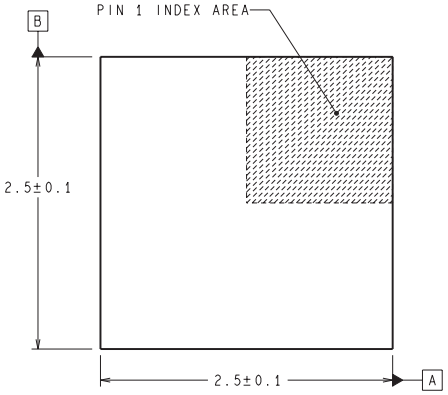
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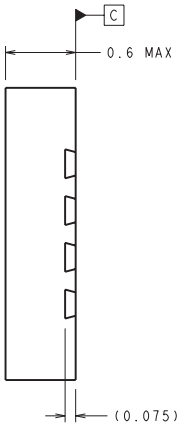


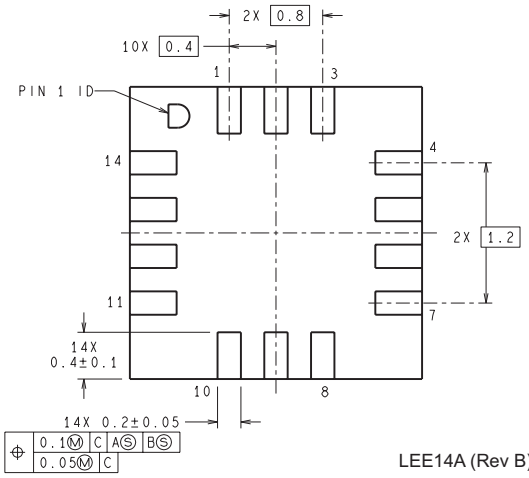
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