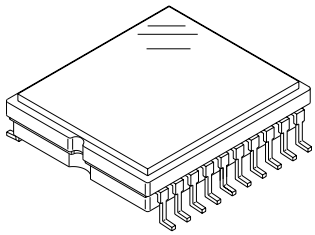
SONY

ICX274AQF

Diagonal 8.923mm (Type 1/1.8) Progressive Scan CCD Image Sensor with Square Pixel for Color Cameras

20 pin SOP (Plastic)



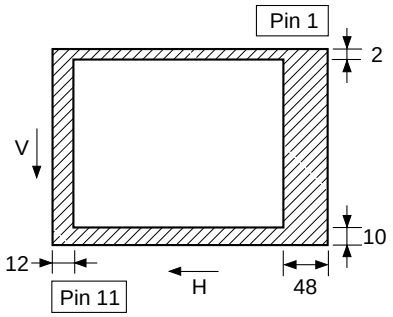
Description

The ICX274AQF is a diagonal 8.923mm (Type 1/1.8) interline CCD solid-state image sensor with a square pixel array and 2.01M effective pixels. Progressive scan allows all pixels' signals to be output independently within approximately 1/15 second, and output is also possible using various addition and pulse elimination methods. This chip features an electronic shutter with variable charge-storage time which makes it possible to realize full-frame still images without a mechanical shutter. High resolution and high color reproductivity are achieved through the use of R, G, B primary color mosaic filters as the color filters. Further, high sensitivity and low dark current are achieved through the adoption of Super HAD CCD technology.

This chip is suitable for applications such as electronic still cameras, PC input cameras, etc.

Features

- High horizontal and vertical resolution
- Supports the following modes
  - Progressive scan mode (with/without mechanical shutter)
  - 2/8-line readout mode
  - 2/4-line readout mode
  - 2-line addition mode
  - Center scan modes (1), (2) and (3)
  - AF modes (1) and (2)
- Square pixel
- Horizontal drive frequency: 28.6364MHz (typ.), 36.0MHz (max.)
- Reset gate bias are not adjusted
- R, G, B primary color mosaic filters on chip
- High sensitivity, low dark current
- Continuous variable-speed shutter function
- Excellent anti-blooming characteristics
- 20-pin high-precision plastic package



Optical black position
(Top View)

Device Structure

- Interline CCD image sensor
- Image size: Diagonal 8.923mm (Type 1/1.8)
- Total number of pixels: 1688 (H) × 1248 (V) approx. 2.11M pixels
- Number of effective pixels: 1628 (H) × 1236 (V) approx. 2.01M pixels
- Number of active pixels: 1620 (H) × 1220 (V) approx. 1.98M pixels
- Recommended number of recording pixels: 1600 (H) × 1200 (V) approx. 1.92M pixels
- Chip size: 8.50mm (H) × 6.80mm (V)
- Unit cell size: 4.40µm (H) × 4.40µm (V)
- Optical black: Horizontal (H) direction: Front 12 pixels, rear 48 pixels
  Vertical (V) direction: Front 10 pixels, rear 2 pixels
- Number of dummy bits: Horizontal 28
  Vertical 1
- Substrate material: Silicon

Wfine CCD™

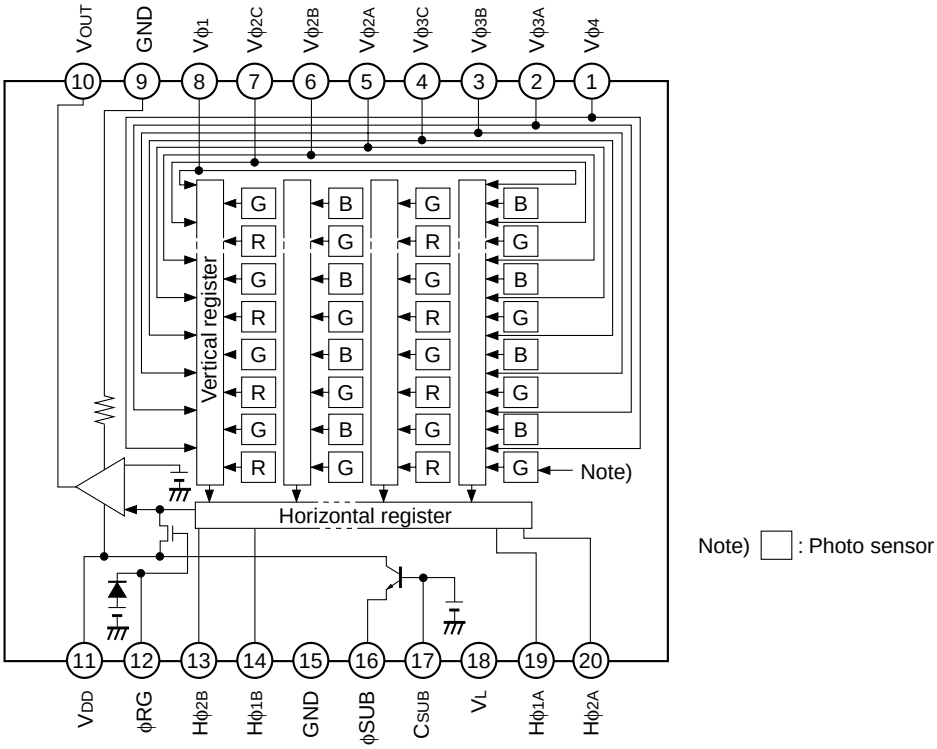
* Wfine CCD is trademark of Sony corporation.
Represents a CCD adopting progressive scan, primary color filter and square pixel.

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E02262

Block Diagram and Pin Configuration

(Top View)



Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	Vφ4	Vertical register transfer clock	11	VDD	Supply voltage
2	Vφ3A	Vertical register transfer clock	12	φRG	Reset gate clock
3	Vφ3B	Vertical register transfer clock	13	Hφ2B	Horizontal register transfer clock
4	Vφ3C	Vertical register transfer clock	14	Hφ1B	Horizontal register transfer clock
5	Vφ2A	Vertical register transfer clock	15	GND	GND
6	Vφ2B	Vertical register transfer clock	16	φSUB	Substrate clock
7	Vφ2C	Vertical register transfer clock	17	CSUB	Substrate bias*1
8	Vφ1	Vertical register transfer clock	18	VL	Protective transistor bias
9	GND	GND	19	Hφ1A	Horizontal register transfer clock
10	VOUT	Signal output	20	Hφ2A	Horizontal register transfer clock

*1 DC bias is generated within the CCD, so that this pin should be grounded externally through a capacitance of 0.1µF.

Absolute Maximum Ratings

Item		Ratings	Unit	Remarks
Against φSUB	V_{DD}, V_{OUT}, φRG – φSUB	–40 to +12	V	
	$V\phi_{2\alpha}$, $V\phi_{3\alpha}$ – φSUB (α = A to C)	–50 to +15	V	
	$V\phi_1$, $V\phi_4$, V_L – φSUB	–50 to +0.3	V	
	$H\phi_{1\beta}$, $H\phi_{2\beta}$, GND – φSUB (β = A, B)	–40 to +0.3	V	
	C_{SUB} – φSUB	–25 to	V	
Against GND	V_{DD}, V_{OUT}, φRG, C_{SUB} – GND	–0.3 to +22	V	
	$V\phi_1$, $V\phi_{2\alpha}$, $V\phi_{3\alpha}$, $V\phi_4$ – GND (α = A to C)	–10 to +18	V	
	$H\phi_{1\beta}$, $H\phi_{2\beta}$ – GND (β = A, B)	–10 to +6.5	V	
Against V_L	$V\phi_{2\alpha}$, $V\phi_{3\alpha}$ – V_L (α = A to C)	–0.3 to +28	V	
	$V\phi_1$, $V\phi_4$, $H\phi_{1\beta}$, $H\phi_{2\beta}$, GND – V_L (β = A, B)	–0.3 to +15	V	
Between input clock pins	Voltage difference between vertical clock input pins	to +15	V	*2
	$H\phi_{1\beta}$ – $H\phi_{2\beta}$ (β = A, B)	–6.5 to +6.5	V	
	$H\phi_{1\beta}$, $H\phi_{2\beta}$ – $V\phi_4$ (β = A, B)	–10 to +16	V	
Storage temperature		–30 to +80	°C	
Guaranteed temperature of performance		–10 to +60	°C	
Operating temperature		–10 to +75	°C	

*2 +24V (Max.) is guaranteed when clock width < 10µs, clock duty factor < 0.1%.
+16V (Max.) is guaranteed during power-on or power-off.

Bias Conditions

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage		V_{DD}	14.55	15.0	15.45	V	
Protective transistor bias		V_L		*3			
Substrate voltage adjustment range	No line addition*1	V_{SUB}	Internally generated value				*4
	2-line addition*2	V_{SUB2}	8.8		14.4	V	
Substrate voltage adjustment accuracy		ΔV_{SUB}	Indicated voltage – 0.2	Indicated voltage	Indicated voltage + 0.2	V	
Reset gate clock		ϕRG		*5		V	

*1 Progressive scan mode, 2/8-line readout mode, 2/4-line readout mode, center scan modes (1) and (3), and AF modes (1) and (2)

*2 2-line addition mode and center scan mode (2)

*3 V_L setting is the V_{VL} voltage of the vertical clock waveform, or the same voltage as the V_L power supply for the V driver should be used.

*4 Substrate voltage (V_{SUB2}) setting value indication
The substrate voltage (V_{SUB}) for modes without line addition is generated internally.
The substrate voltage setting value for use with vertical 2-line addition is indicated by a code on the bottom surface of the image sensor. Adjust the substrate voltage to the indicated voltage.

V_{SUB2} code – 1-digit indication □
↑
V_{SUB2} code

The code and the actual value correspond as follows.

V_{SUB2} code	1	2	3	4	6	7	8	9	A	C	d	E	f	G	h
Actual value	8.8	9.0	9.2	9.4	9.6	9.8	10.0	10.2	10.4	10.6	10.8	11.0	11.2	11.4	11.6

V_{SUB2} code	J	K	L	m	N	P	R	S	U	V	W	X	Y	Z
Actual value	11.8	12.0	12.2	12.4	12.6	12.8	13.0	13.2	13.4	13.6	13.8	14.0	14.2	14.4

[Example] "h" indicates a V_{SUB2} setting of 11.6V.

*5 Do not apply a DC bias to the reset gate clock pin, because a DC bias is generated within the CCD.

DC characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply current	I_{DD}	7.0	10.0	13.0	mA	

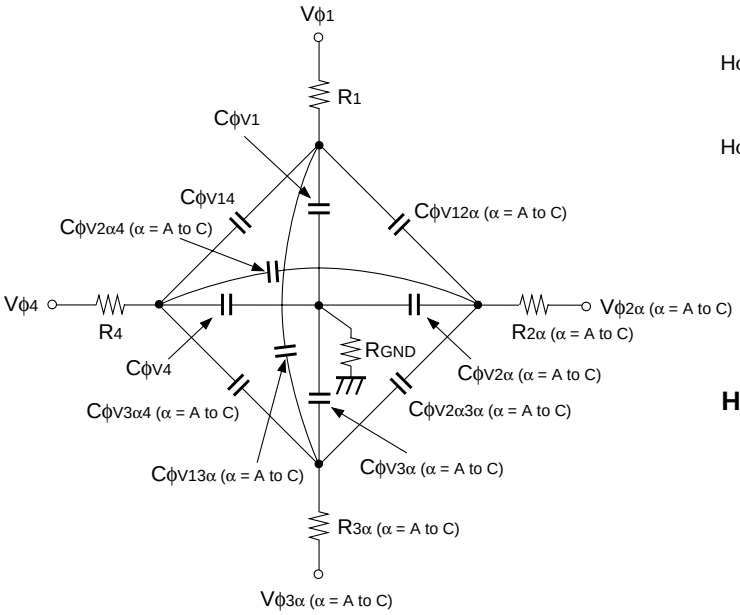
Clock Voltage Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Readout clock voltage	V_{VT}	14.55	15.0	15.45	V	1	
Vertical transfer clock voltage	V_{VH1}, V_{VH2}	–0.05	0	0.05	V	2	$V_{VH} = (V_{VH1} + V_{VH2})/2$
	V_{VH3}, V_{VH4}	–0.2	0	0.05	V	2	
	V_{VL1}, V_{VL2}, V_{VL3}, V_{VL4}	–8.0	–7.5	–7.0	V	2	$V_{VL} = (V_{VL3} + V_{VL4})/2$
	$V\phi_V$	6.8	7.5	8.05	V	2	$V\phi_V = V_{VH}n – V_{VL}n$ (n = 1 to 4)
	$V_{VH3} – V_{VH}$	–0.25		0.1	V	2	
	$V_{VH4} – V_{VH}$	–0.25		0.1	V	2	
	V_{VHH}			0.5	V	2	High-level coupling
	V_{VHL}			0.5	V	2	High-level coupling
	V_{VLH}			0.5	V	2	Low-level coupling
	V_{VLL}			0.5	V	2	Low-level coupling
Horizontal transfer clock voltage	$V\phi_H$	4.75	5.0	5.25	V	3	
	V_{HL}	–0.05	0	0.05	V	3	
	V_{CR}	0.8	2.5		V	3	Cross-point voltage
Reset gate clock voltage	$V\phi_{RG}$	3.0	3.3	5.25	V	4	
	$V_{RGLH} – V_{RGLL}$			0.4	V	4	Low-level coupling
	$V_{RGL} – V_{RGLm}$			0.5	V	4	Low-level coupling
Substrate clock voltage	$V\phi_{SUB}$	21.5	22.5	23.5	V	5	

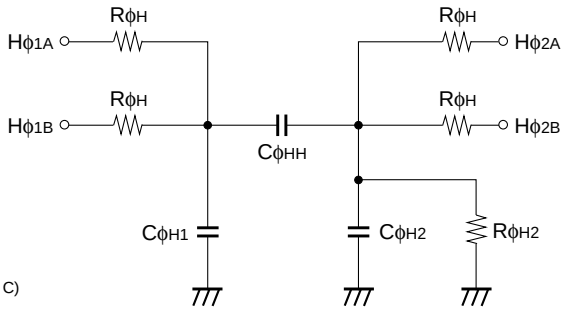
Clock Equivalent Circuit Constants

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C_{\phi V1}$		3300		pF	
	$C_{\phi V2A}$, $C_{\phi V2B}$		1200		pF	
	$C_{\phi V2C}$		2700		pF	
	$C_{\phi V3A}$, $C_{\phi V3B}$		1000		pF	
	$C_{\phi V3C}$		1800		pF	
	$C_{\phi V4}$		6800		pF	
Capacitance between vertical transfer clocks	$C_{\phi V12\ (A, B)}$		120		pF	
	$C_{\phi V12C}$		220		pF	
	$C_{\phi V13\ (A, B)}$		150		pF	
	$C_{\phi V13C}$		270		pF	
	$C_{\phi V14}$		2700		pF	
	$C_{\phi V2\ (A, B),\ 3\ (A, B)}$		470		pF	
	$C_{\phi V2\ (A, B),\ 3C}$		680		pF	
	$C_{\phi V2\ (A, B),\ 4}$		680		pF	
	$C_{\phi V2C,\ 3\ (A, B)}$		1000		pF	
	$C_{\phi V2C,\ 3C}$		820		pF	
	$C_{\phi V2C,\ 4}$		1800		pF	
	$C_{\phi V3\ (A, B),\ 4}$		820		pF	
	$C_{\phi V3C,\ 4}$		1500		pF	
Capacitance between horizontal transfer clock and GND	$C_{\phi H1}$		100		pF	
	$C_{\phi H2}$		100		pF	
Capacitance between horizontal transfer clocks	$C_{\phi HH}$		47		pF	
Capacitance between reset gate clock and GND	$C_{\phi RG}$		2		pF	
Capacitance between substrate clock and GND	$C_{\phi SUB}$		820		pF	
Vertical transfer clock series resistor	R_1, R_4		30		Ω	
	$R_{2\ (A, B, C),\ 3\ (A, B, C)}$		62		Ω	
Vertical transfer clock ground resistor	R_{GND}		15		Ω	
Horizontal transfer clock series resistor	$R_{\phi H}$		7		Ω	
Horizontal transfer clock ground resistor	$R_{\phi H2}$		20		kΩ	
Reset gate clock and series resistor	$R_{\phi RG}$		4.7		Ω	

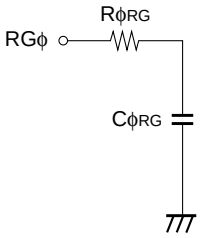
Note 1) Expressions using parentheses such as $C_{\phi V2\ (A,B),\ 3C}$ indicate items which include all combinations of the pins within the parentheses.
For example, $C_{\phi V2\ (A, B),\ 3C}$ indicates [$C_{\phi V2A3C}$, $C_{\phi V2B3C}$].



Vertical transfer clock equivalent circuit



Horizontal transfer clock equivalent circuit

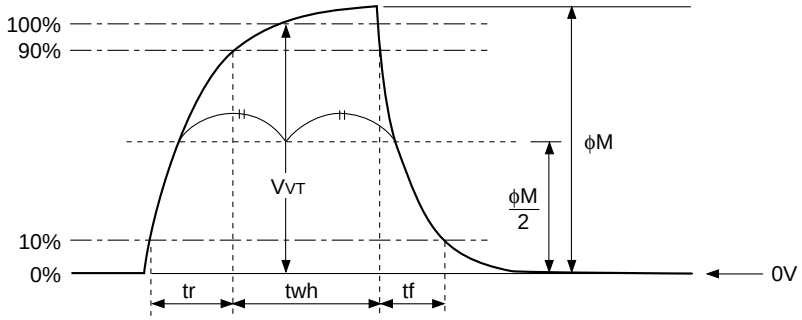


Reset gate clock equivalent circuit

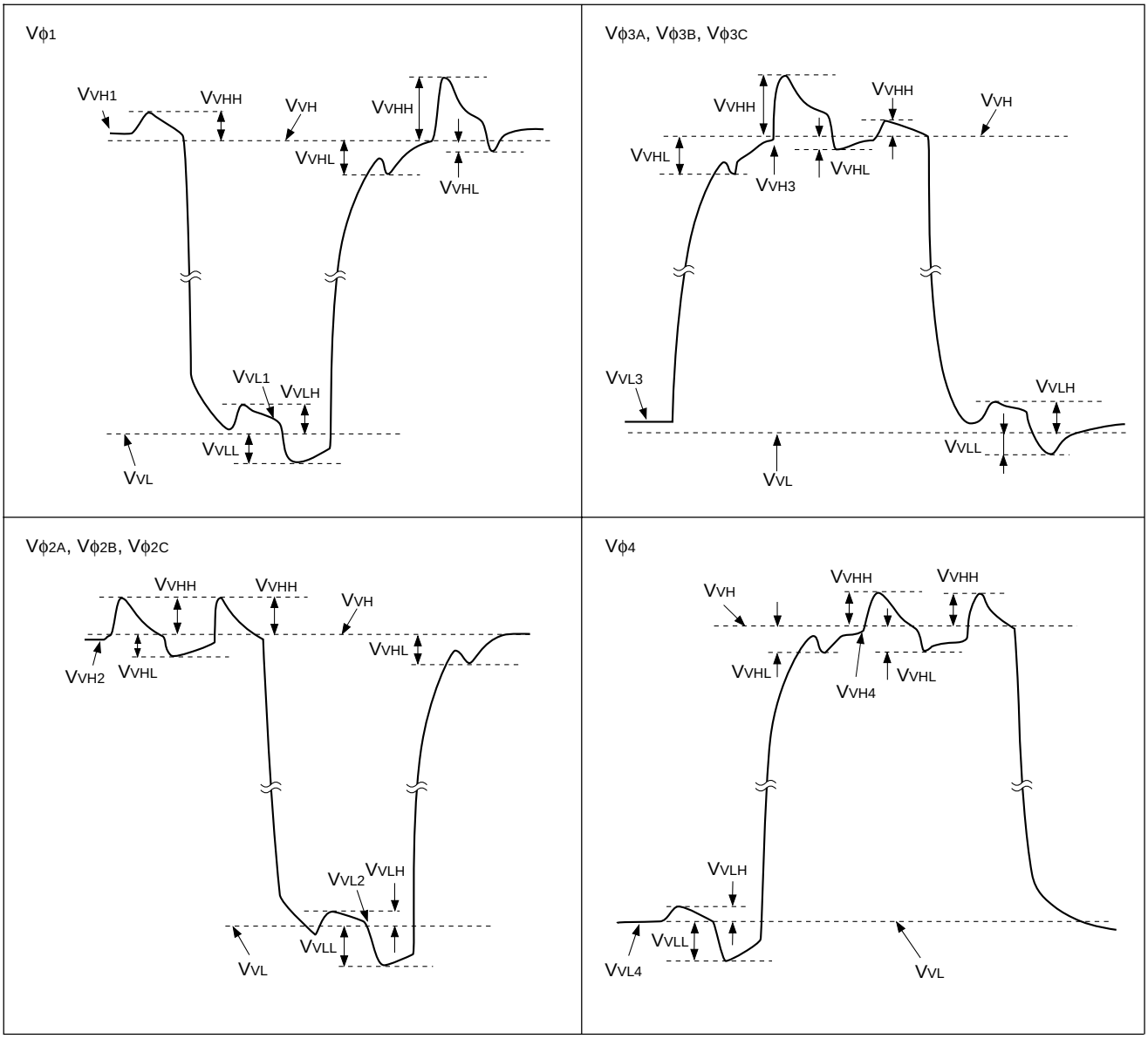
Note 2) Cϕ2α2β and Cϕ3α3β (α = A to C, β = A to C other than α) are sufficiently small relative to other capacitance between other vertical clocks in the equivalent circuit, so these are omitted from the equivalent circuit diagram.

Drive Clock Waveform Conditions

(1) Readout clock waveform



(2) Vertical transfer clock waveform

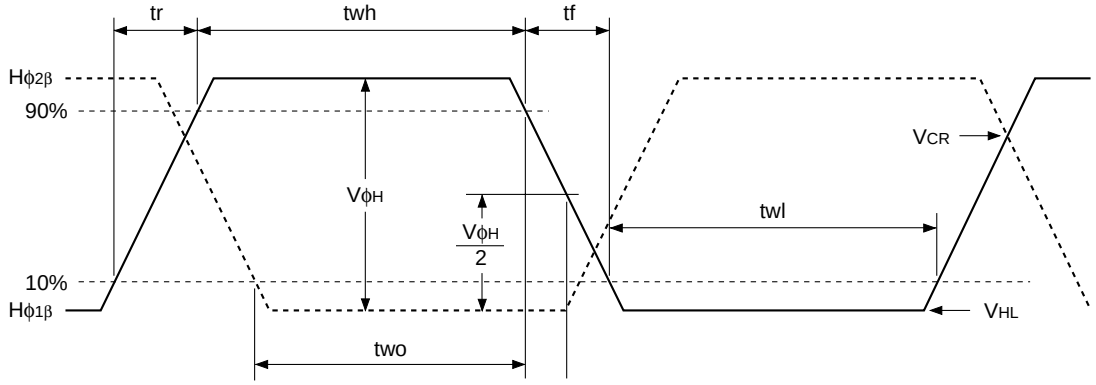


$V_{VH} = (V_{VH1} + V_{VH2})/2$

$V_{VL} = (V_{VL3} + V_{VL4})/2$

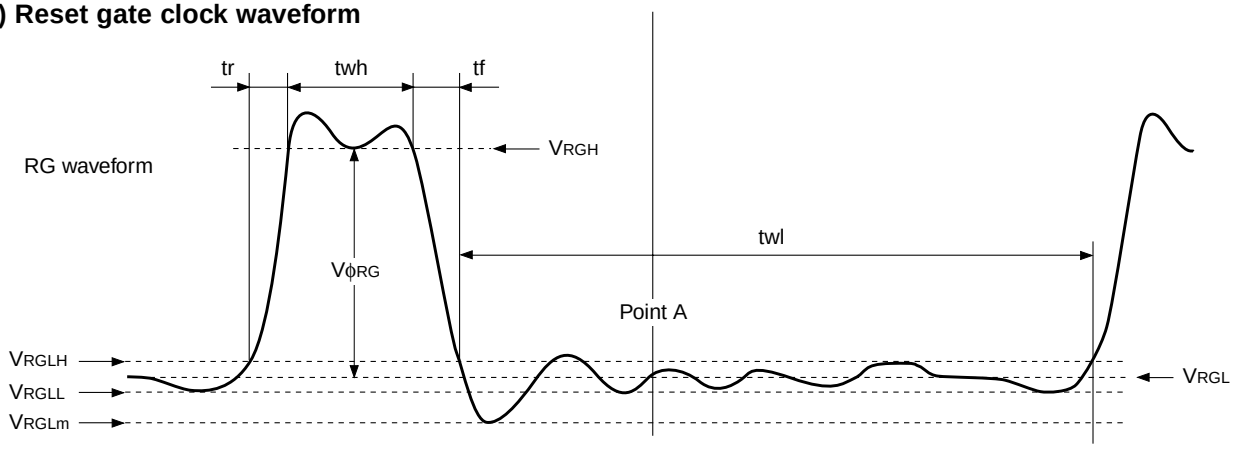
$V_{\phi V} = V_{VHn} – V_{VLn}$ (n = 1 to 4)

(3) Horizontal transfer clock waveform



Cross-point voltage for the Hϕ1β rising side of the horizontal transfer clocks Hϕ1β and Hϕ2β waveforms is VCR.
The overlap period for twh and twl of horizontal transfer clocks Hϕ1β and Hϕ2β is two. (β = A, B)

(4) Reset gate clock waveform



VRGLH is the maximum value and VRGLL is the minimum value of the coupling waveform during the period from Point A in the above diagram until the rising edge of RG.
In addition, VRGL is the average value of VRGLH and VRGLL.

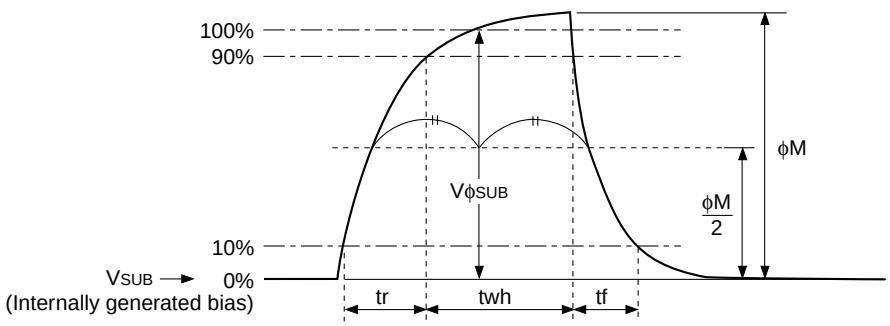
$$V_{RGL} = (V_{RGLH} + V_{RGLL})/2$$

Assuming VRGH is the minimum value during the interval twh, then:

$$V_{\phi RG} = V_{RGH} - V_{RGL}$$

Negative overshoot level during the falling edge of RG is VRGLm.

(5) Substrate clock waveform



Clock Switching Characteristics (Horizontal drive frequency: 28.6364MHz)

Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Readout clock	V_T	3.3	3.5						0.5			0.5		µs	During readout
Vertical transfer clock	Vφ1, Vφ4, Vφ2α, Vφ3α (α = A to C)										15		400	ns	*1
Horizontal transfer clock	Hφ1β (β = A, B)	10	12.5		10	12.5			5	7.5		5	7.5	ns	*2
	Hφ2β (β = A, B)	10	12.5		10	12.5			5	7.5		5	7.5		
Reset gate clock	ϕ_{RG}	4	7			24			2			3		ns	
Substrate clock	ϕ_{SUB}		2.1							0.5			0.5	µs	During drain charge

Item	Symbol	two			Unit	Remarks
		Min.	Typ.	Max.		
Horizontal transfer clock	Hφ1A, Hφ1B, Hφ2A, Hφ2B	8	10		ns	

Clock Switching Characteristics (Horizontal drive frequency: 36MHz)

Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Readout clock	V_T	4.0	4.2						0.5			0.5		µs	During readout
Vertical transfer clock	Vφ1, Vφ4, Vφ2α, Vφ3α (α = A to C)										15		400	ns	*1
Horizontal transfer clock	Hφ1β (β = A, B)	8	9		8	9			5	6		5	6	ns	*2
	Hφ2β (β = A, B)	8	9		8	9			5	6		5	6		
Reset gate clock	ϕ_{RG}	4	5.5			8			2			3		ns	
Substrate clock	ϕ_{SUB}		1.67							0.25			0.25	µs	During drain charge

Item	Symbol	two			Unit	Remarks
		Min.	Typ.	Max.		
Horizontal transfer clock	Hφ1A, Hφ1B, Hφ2A, Hφ2B	8	9		ns	

*1 When two vertical transfer clock drivers CXD3400N are used.

*2 tf ≥ tr – 2ns, and the cross-point voltage (V_{CR}) for the Hφ1β (β = A, B) rising side of the Hφ1β and Hφ2β waveforms must be VφH/2 [V] or more.

Spectral Sensitivity Characteristics (excludes lens characteristics and light source characteristics)

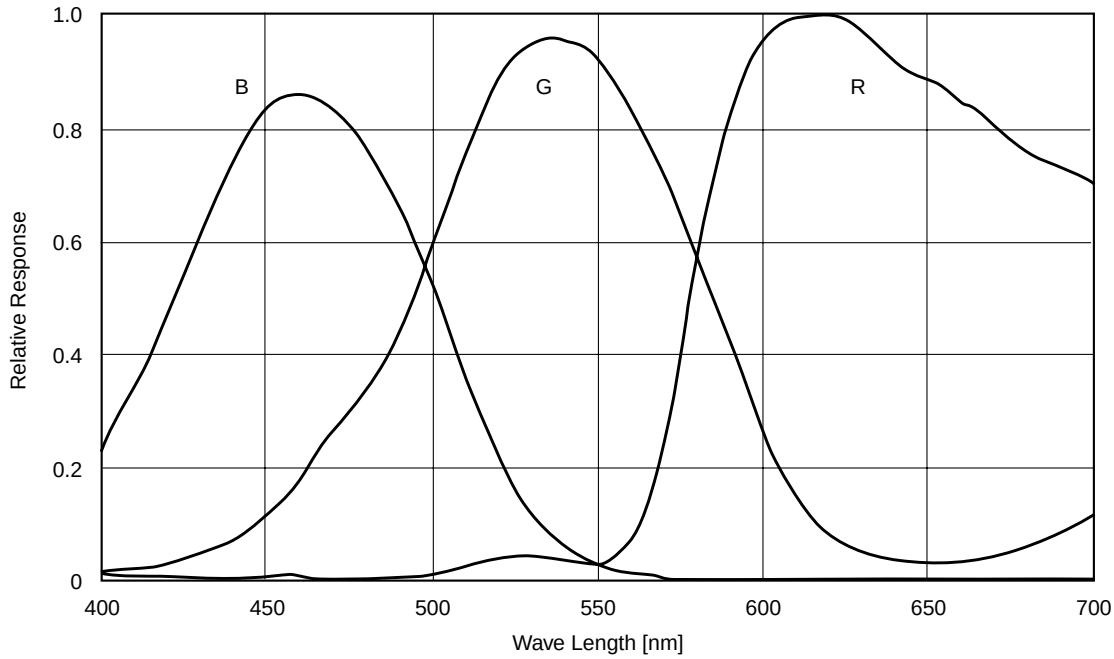


Image Sensor Characteristics (Ta = 25°C)

Item		Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks	
G Sensitivity		Sg	335	420	545	mV	1	1/30s accumulation	
Sensitivity comparison	R	Rr	0.35	0.5	0.65		1		
	B	Rb	0.45	0.6	0.75		1		
Saturation signal		Vsat	400			mV	2	Ta = 60°C	No line addition*2
		Vsat2*1	400						2-line addition*3
Smear		Sm		–100	–92	dB	3	Progressive scan mode*4	
				–94	–86			2/4-line readout mode*5	
				–88	–80			2/8-line readout mode*6	
Video signal shading		SH			20	%	4	Zone 0 and I	
					25			Zone 0 to II'	
Uniformity between video signal channels		ΔSrg			8	%	5		
		ΔSbg			8				
Dark signal		Vdt			8	mV	6	Ta = 60°C, 14.985 frame/s	
Dark signal shading		ΔVdt			2	mV	7	Ta = 60°C, 14.985 frame/s, *7	
Line crawl G		Lcg			3.8	%	8		
Line crawl R		Lcr			3.8	%	8		
Line crawl B		Lcb			3.8	%	8		
Lag		Lag			0.5	%	9		

*1 Vsat2 is the saturation signal level in 2-line addition mode, and is 200mV per pixel.

*2 Progressive scan mode, 2/8-line readout mode, 2/4-line readout mode, and center scan modes (1) and (3).

*3 2-line addition mode and center scan mode (2).

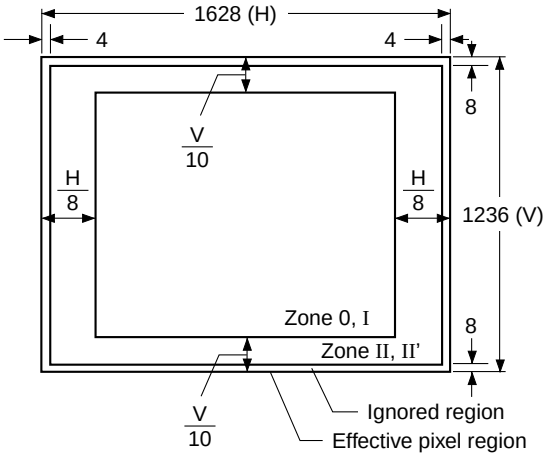
*4 Same for 2-line addition mode and center scan modes (2) and (3).

*5 Same for center scan mode (1).

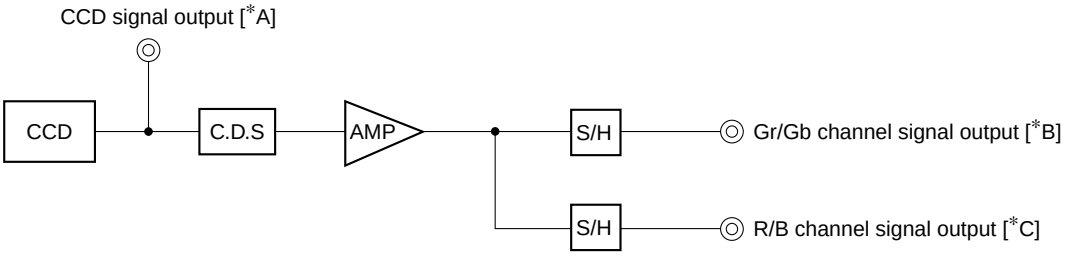
*6 Same for AF modes (1) and (2).

*7 Excludes vertical dark signal shading caused by vertical register high-speed transfer.

Zone Definition of Video Signal Shading



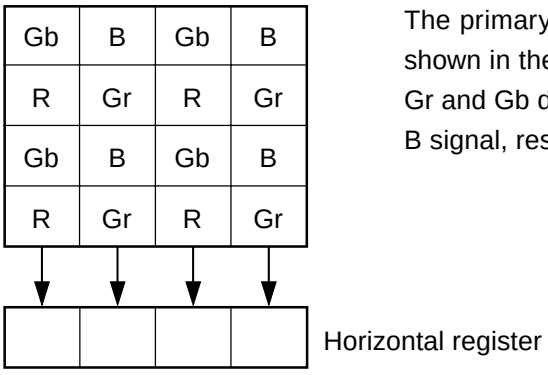
Measurement System



Note) Adjust the amplifier gain so that the gain between [*A] and [*B], and between [*A] and [*C] equals 1.

Image Sensor Characteristics Measurement Method

◎ Color coding of this image sensor & Readout

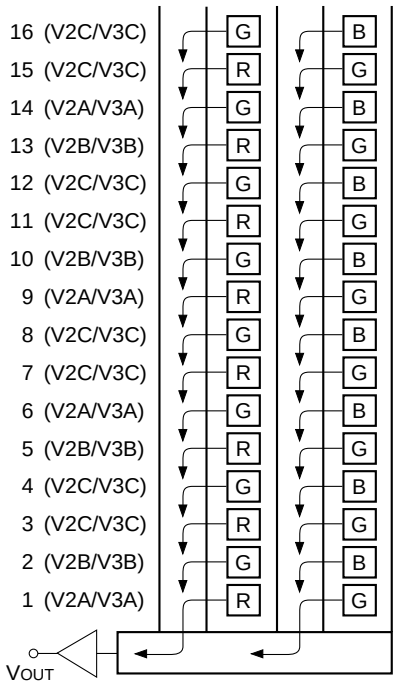
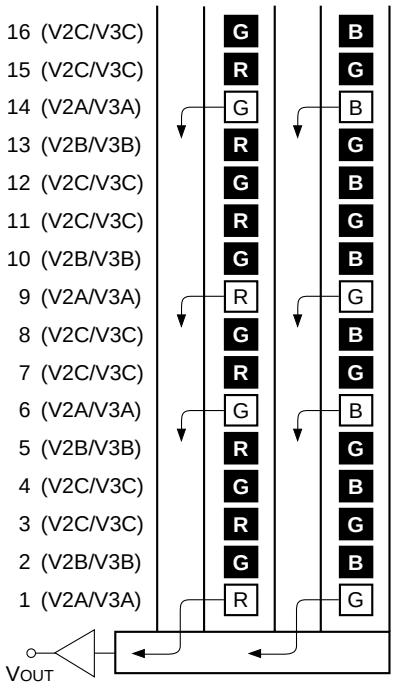
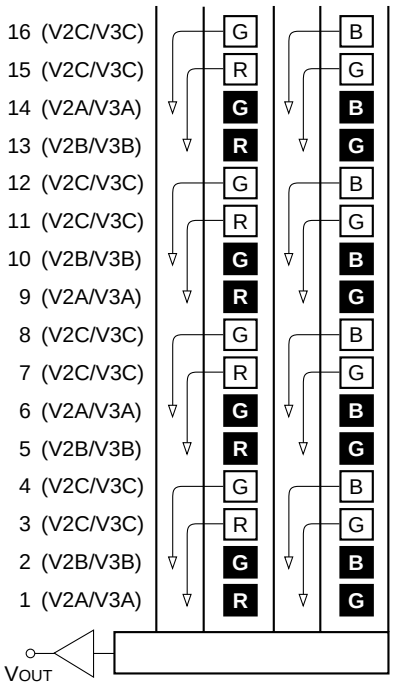


Color Coding Diagram

The primary color filters of this image sensor are arranged in the layout shown in the figure on the left (Bayer arrangement).
Gr and Gb denote the G signals on the same line as the R signal and the B signal, respectively.

◎ Readout modes

The diagrams below and on the following pages show the output methods for the following nine readout modes.

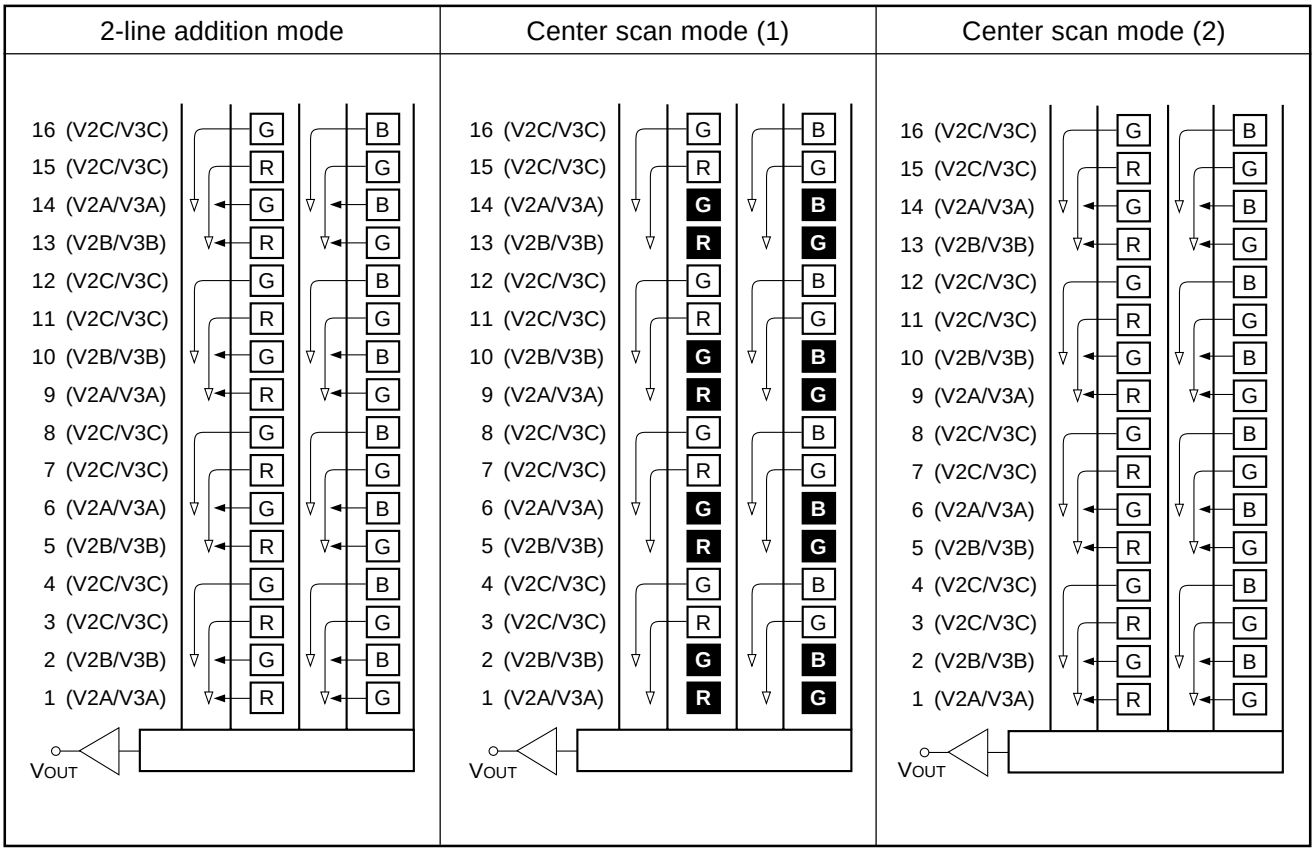
Progressive scan mode	2/8-line readout mode	2/4-line readout mode
		

Note) Blacked out portions in the diagram indicate pixels which are not read out.
Output starts from line 1 in 2/8-line decimation mode.

1. Progressive scan mode
   In this mode, all pixel signals are output in non-interlace format in 1/14.985s.
   All pixel signals within the same exposure period are read out simultaneously, making this mode suitable for high resolution image capturing.

2. 2/8-line readout mode
   All effective area signals are output in approximately 1/30s by reading out the signals for only two out of eight lines (1st and 6th lines, 9th and 14th lines).
   This readout mode emphasizes processing speed over vertical resolution, making it suitable for AE/AF and other control and for checking images on LCD viewfinders.

3. 2/4-line readout mode
   All effective area signals are output in approximately 1/20s by reading out the signals for only two out of four lines (3rd and 4th lines, 7th and 8th lines, and so on).

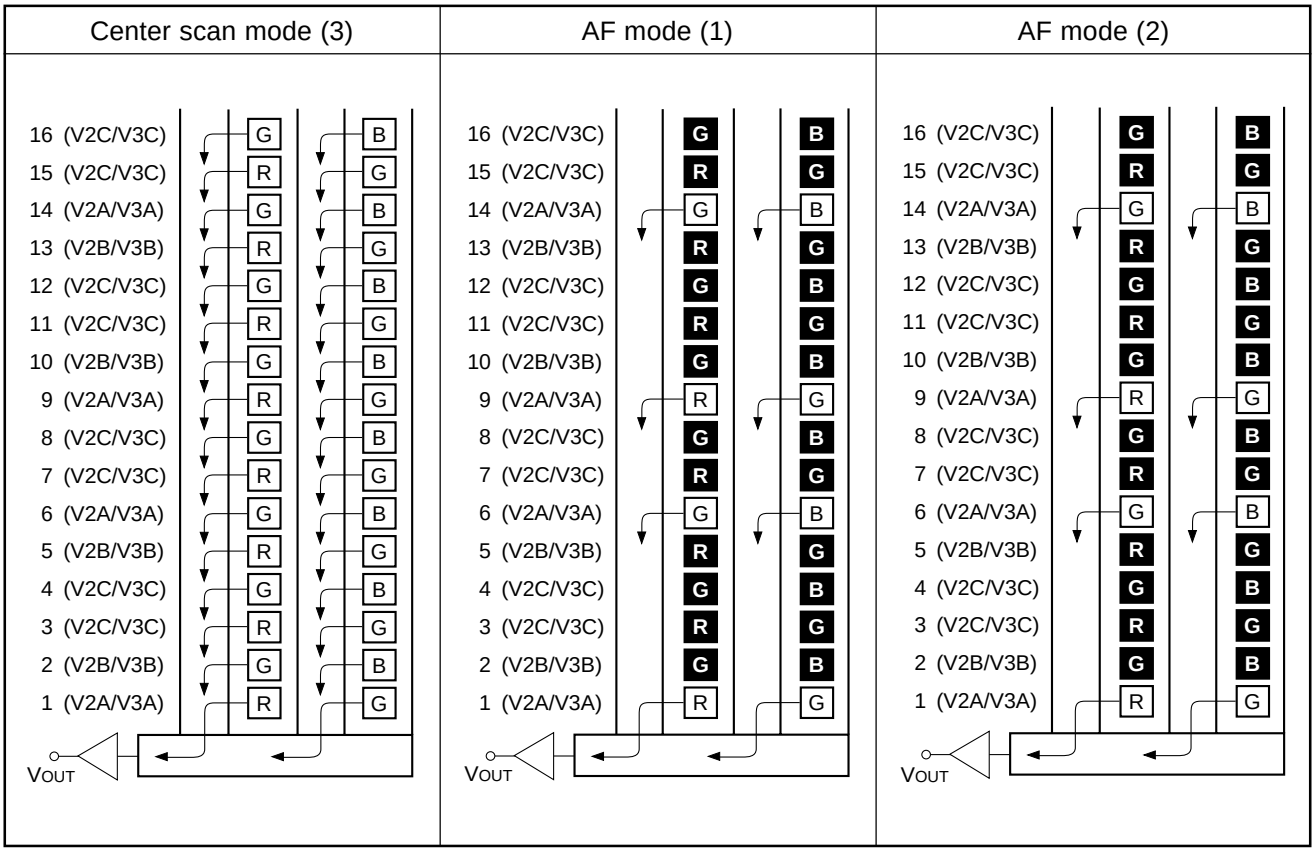


Note) Blacked out portions in the diagram indicate pixels which are not read out.
After reading out the pixels indicated by ⇦ and transferring two lines, the pixels indicated by ← are read out and two pixels of the same color are added by the vertical transfer block.

4. 2-line addition mode
In this mode, the signals for only two out of four lines (3rd and 4th lines, 7th and 8th lines, and so on) are read out, the vertical register is shifted by 2 bits, and then the signals of the remaining two out of the four lines (1st and 2nd lines, 5th and 6th lines, and so on) are read out and added within the vertical register. All effective area signals are output in approximately 1/20s.

5. Center scan mode (1)
In this mode, the signals for only two out of four lines (3rd and 4th lines, 7th and 8th lines, and so on) are read out. The undesired portions are swept by vertical register high-speed transfer, and the vertical 1136-pixel region in the center of the picture is output by the above readout method. The number of output lines is 568 lines at 36MHz, and 434 lines at 28.6364MHz. The frame rate is increased (approximately 30 frames/s) by setting the number of output lines to that of VGA mode, making this mode suitable for VGA moving pictures. (However, the angle of view decreases.)

6. Center scan mode (2)
In this mode, the signals for only two out of four lines (3rd and 4th lines, 7th and 8th lines, and so on) are read out, the vertical register is shifted by 2 bits, and then the signals of the remaining two out of the four lines (1st and 2nd lines, 5th and 6th lines, and so on) are read out and added within the vertical register. The undesired portions are swept by vertical register high-speed transfer, and the vertical 1136-pixel region in the center of the picture is output by the above readout method. The number of output lines is 568 lines at 36MHz, and 434 lines at 28.6364MHz. The frame rate is increased (approximately 30 frames/s) by setting the number of output lines to that of VGA mode, making this mode suitable for VGA moving pictures. (However, the angle of view decreases.)



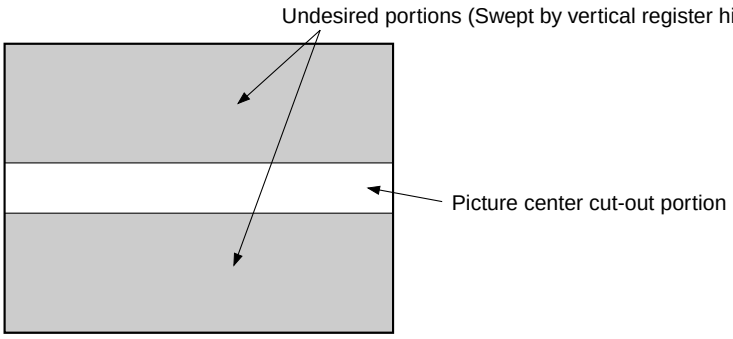
Note) Blacked out portions in the diagram indicate pixels which are not read out.

7. Center scan mode (3)
   This is the center scan mode using the progressive scan method.
   The undesired portions are swept by vertical register high-speed transfer, and the picture center is cut out.
   The number of output lines is 580 lines at 36MHz, and 444 lines at 28.6364MHz.

8. AF mode (1)
   In this mode, the undesired portions are swept by vertical register high-speed transfer, and the vertical 940-pixel region in the center of the picture is output in approximately 1/60s by reading out the signals for only two out of eight lines (1st and 6th lines, 9th and 14th lines). The number of output lines is 235 lines at 36MHz, and 170 lines at 28.6364MHz. This mode aims for even faster AF control than 2/8-line readout mode.

9. AF mode (2)
   In this mode, the undesired portions are swept by vertical register high-speed transfer, and the vertical 300-pixel region in the center of the picture is output in approximately 1/120s by reading out the signals for only two out of eight lines (1st and 6th lines, 9th and 14th lines). The number of output lines is 75 lines at 36MHz, and 43 lines at 28.6364MHz. This mode aims for even faster AF control than 2/8-line readout mode.

◎ Center scan and AF modes



Description of Center Scan and AF Mode Operation

The center scan and AF modes realize high frame rates by sweeping the top and bottom of the picture with high-speed transfer and cutting out the center of the picture.
The various readout modes during center scan and AF operation are described below.

• AF modes
AF mode (1), (2): The output method is the same as readout in 2/8-line readout mode.

• Center scan modes
Center scan mode (1): The output method is the same as 2/4-line readout mode.
Center scan mode (2): The output method consists of 2-line addition readout whereby the signals for only two out of four lines (3rd and 4th lines, 7th and 8th lines, and so on) are read out, the vertical register is shifted by 2 bits, and then the signals of the remaining two out of the four lines (1st and 2nd lines, 5th and 6th lines, and so on) are read out and added within the vertical register.
Center scan mode (3): The output method is the same as progressive scan mode.

The readout method, frame rate, number of output lines and other information for each readout mode are shown in the table below.

Mode	Readout method	Addition method	Frame rate (frame/s)		Number of output effective pixel data lines	
			28.6MHz	36MHz	28.6MHz	36MHz
Progressive scan mode	Progressive scan	None	9.99	14.985	1220	1220
2/8-line readout mode	2/8-line readout	None	29.97	29.97	305	305
2/4-line readout mode	2/4-line readout	None	19.98	19.98	610	610
2-line addition mode	2/4-line readout	Vertical 2-line	19.98	19.98	1220	1220
Center scan mode (1)	2/4-line readout	None	29.97	29.97	434	568
Center scan mode (2)	2-line addition readout	Vertical 2-line	29.97	29.97	434	568
Center scan mode (3)	Progressive scan	None	29.97	29.97	444	580
AF mode (1)	2/8-line readout	None	59.94	59.94	170	235
AF mode (2)	2/8-line readout	None	119.88	119.88	43	75

◎ Measurement conditions

(1) In the following measurements, the device drive conditions are at the typical values of the bias and clock voltage conditions, and the progressive scan readout mode is used.

(2) In the following measurements, spot blemishes are excluded and, unless otherwise specified, the optical black level (OB) is used as the reference for the signal output, which is taken as the value of the Gr/Gb signal output or the R/B signal output of the measurement system.

◎ Definition of standard imaging conditions

(1) Standard imaging condition I:
Use a pattern box (luminance: 706cd/m^2, color temperature of 3200K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter and image at F5.6. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

(2) Standard imaging condition II:
Image a light source (color temperature of 3200K) with a uniformity of brightness within 2% at all angles. Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

1. Sensitivity
Set to the standard imaging condition I. After setting the electronic shutter mode with a shutter speed of 1/100s, measure the signal voltages (V_{Gr}, V_{Gb}) at the center of each Gr and Gb channel screen, and substitute the values into the following formulas.

$$V_G = (V_{Gr} + V_{Gb})/2$$

$$Sg = V_G \times \frac{100}{30} \text{ [mV]}$$

2. Saturation signal
Set to the standard imaging condition II. After adjusting the luminous intensity to 20 times the intensity with the average value of the G channel signal output, 150mV, measure the minimum values of the G, R and B signal outputs.

3. Smear
Set to standard imaging condition II. With the lens diaphragm at F5.6 to F8, first adjust the average value of the Gr signal output to 150mV. Measure the average values of the Gr signal output, Gb signal output, R signal output and B signal output (Gra, Gba, Ra, Ba), and then adjust the luminous intensity to 500 times the intensity with the average value of the Gr signal output, 150mV. After the readout clock is stopped and the charge drain is executed by the electronic shutter at the respective H blankings, measure the maximum value (Vsm [mV]) independent of the Gr, Gb, R and B signal outputs, and substitute the values into the following formula.
Smear in modes other than progressive scan mode is calculated from the storage time and signal addition method. As a result, 2-line addition mode and center scan modes (2) and (3) are the same as progressive scan mode, 2/4-line readout mode and center scan mode (1) are two times progressive scan mode, and 2/8-line readout mode and AF modes (1) and (2) are four times progressive scan mode.

$$Sm = 20 \times \log \left(Vsm \div \frac{Gra + Gba + Ra + Ba}{4} \times \frac{1}{500} \times \frac{1}{10} \right) \text{ [dB] (1/10V method conversion value)}$$

4. Video signal shading
   Set to the standard imaging condition II. With the lens diaphragm at F5.6 to F8, adjusting the luminous intensity so that the average value of the G channel signal output is 150mV. Then measure the maximum value (Gmax [mV]) and minimum value (Gmin [mV]) of the G signal output and substitute the values into the following formula.

   $SH = (Gmax - Gmin)/150 \times 100$ [%]

5. Uniformity between video signal channels
   After measuring 4, measure the maximum (Rmax [mV]) and minimum (Rmin [mV]) values of the R signal and the maximum (Bmax [mV]) and minimum (Bmin [mV]) values of the B signal, and substitute the values into the following formulas.

   $\Delta Srg = (Rmax - Rmin)/150 \times 100$ [%]
   $\Delta Sbg = (Bmax - Bmin)/150 \times 100$ [%]

6. Dark signal
   Measure the average value of the signal output (Vdt [mV]) with the device ambient temperature of 60°C and the device in the light-obstructed state, using the horizontal idle transfer level as a reference.

7. Dark signal shading
   After measuring 6, measure the maximum (Vdmax [mV]) and minimum (Vdmin [mV]) values of the dark signal output and substitute the values into the following formula.

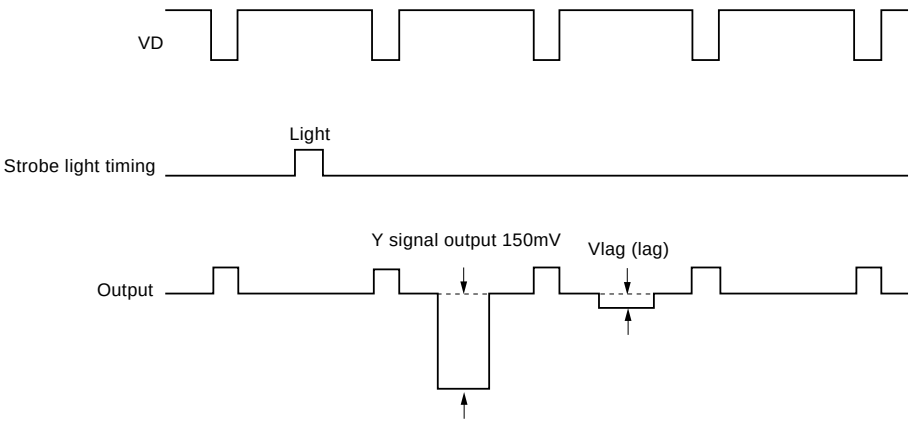
   $\Delta Vdt = Vdmax - Vdmin$ [mV]

8. Line crawl
   Set to the standard imaging condition II. Adjusting the luminous intensity so that the value of the Gr signal output is 150mV, and then insert R, G and B filters and measure the difference between G signal lines (ΔGlr, ΔGlg, ΔGlb [mV]) as well as the value of the G signal output (Gar, Gag, Gab). Substitute the values into the following formula.

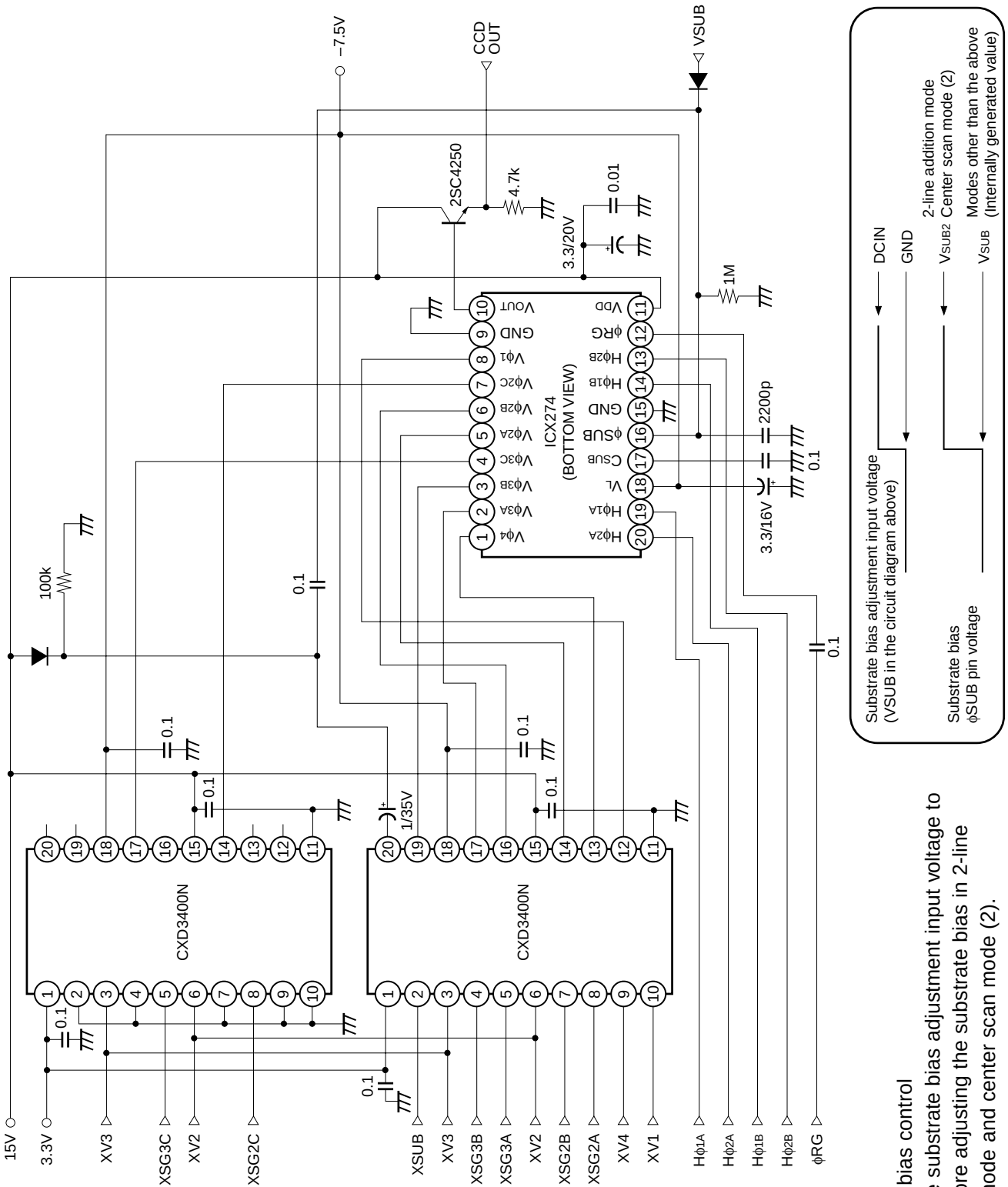
   $$Lci = \frac{\Delta Gli}{Gai} \times 100 \text{ [\%]} \quad (i = r, g, b)$$

9. Lag
   Adjust the Y signal output generated by the strobe light to 150mV. After setting the strobe light so that it strobes with the following timing, measure the residual signal amount (Vlag). Substitute the value into the following formula.

   $Lag = (Vlag/150) \times 100$ [%]

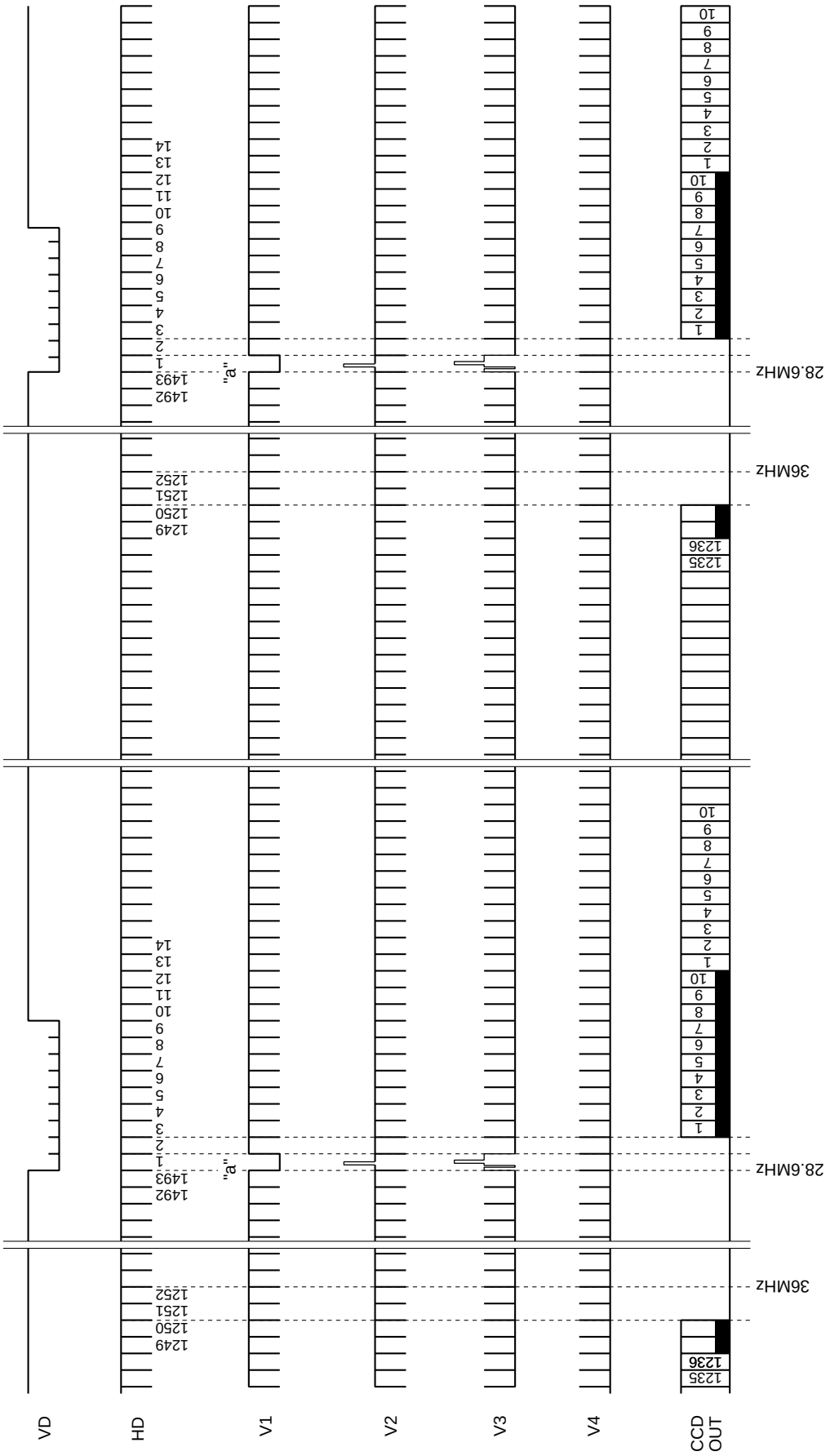


Drive Circuit



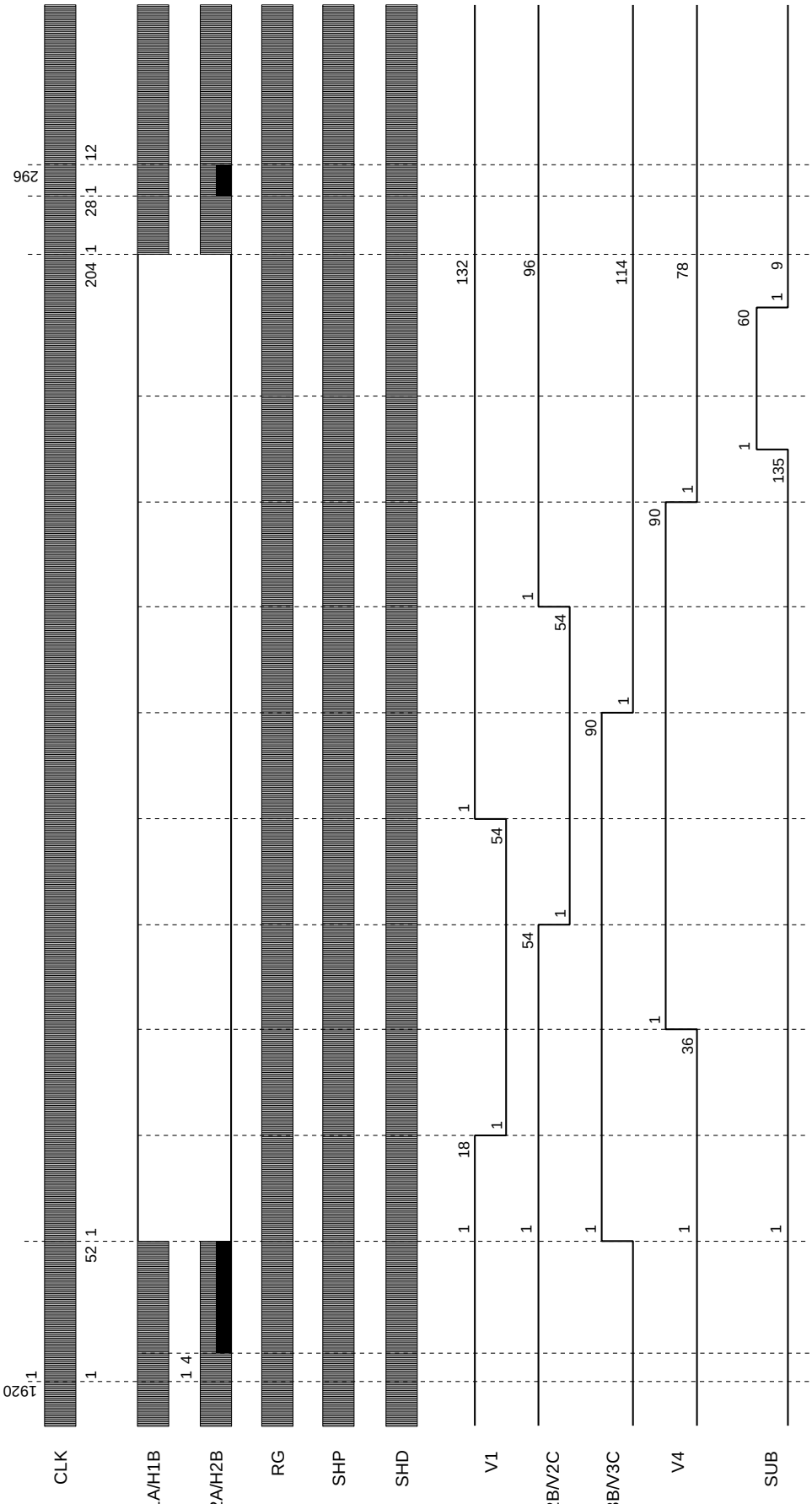
Note) Substrate bias control
Switch the substrate bias adjustment input voltage to DCIN before adjusting the substrate bias in 2-line addition mode and center scan mode (2).

Drive Timing Chart (Vertical Sync) **Progressive Scan Mode**



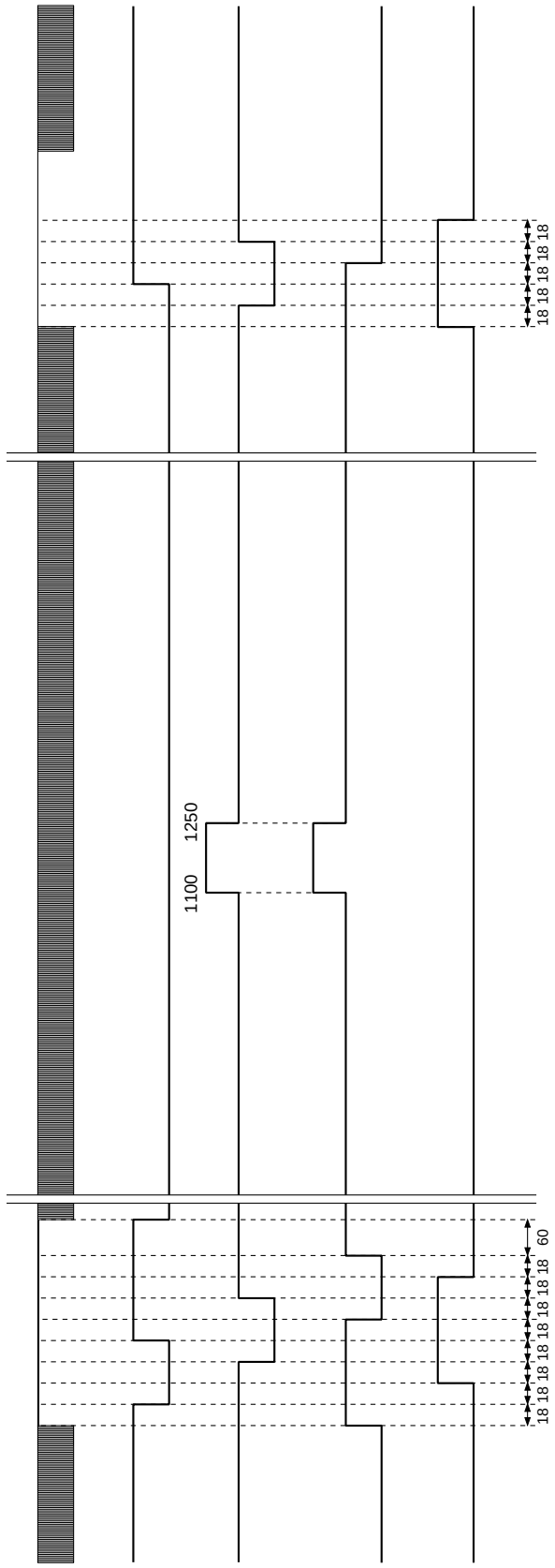
Note) The 1252H horizontal period at 36MHz is 480clk; the 1493H horizontal period at 28MHz is 1860clk.

Drive Timing Chart (Horizontal Sync) **Progressive Scan Mode**

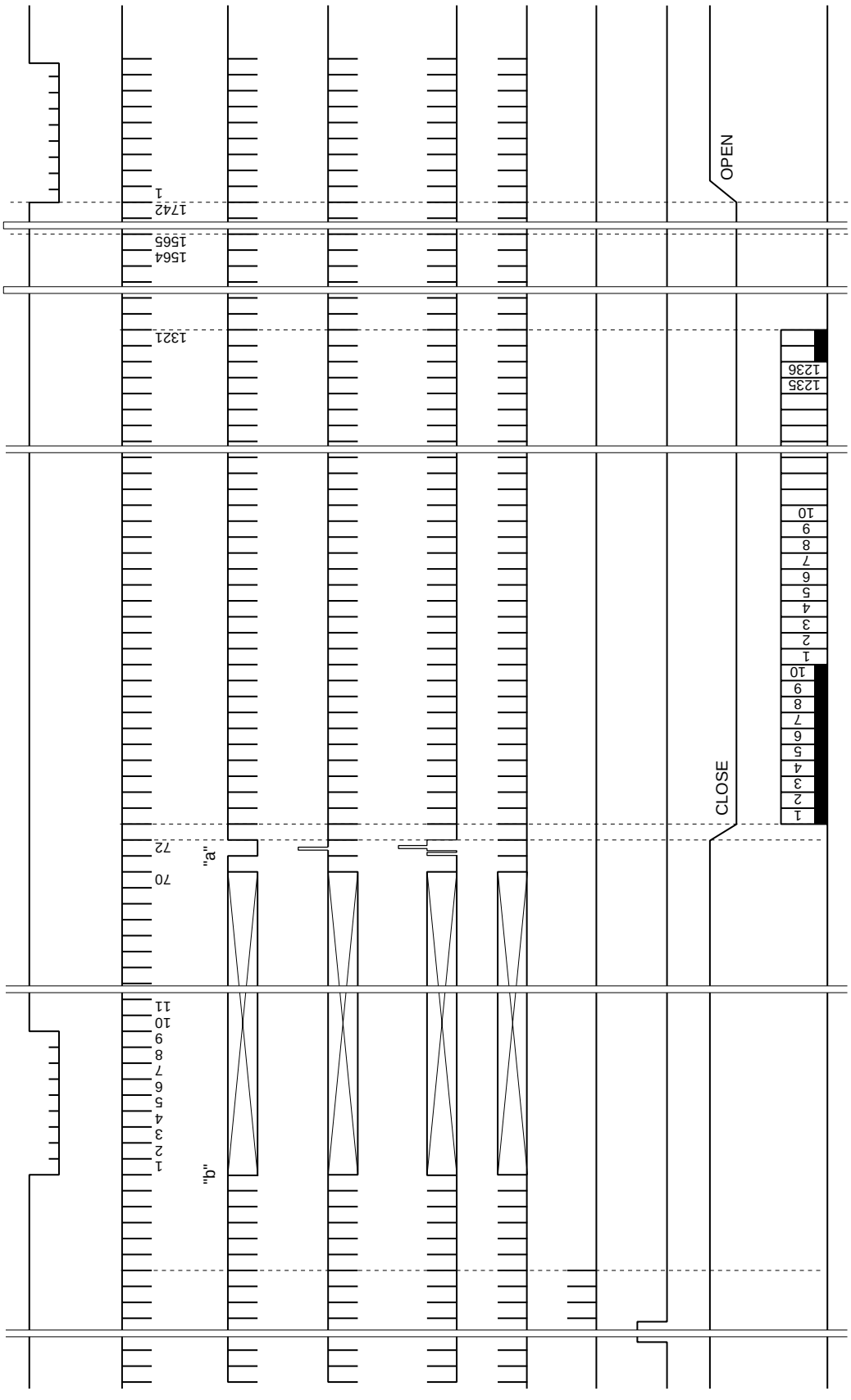


Drive Timing Chart (Vertical Sync) **Progressive Scan Mode**

"a" enlarged



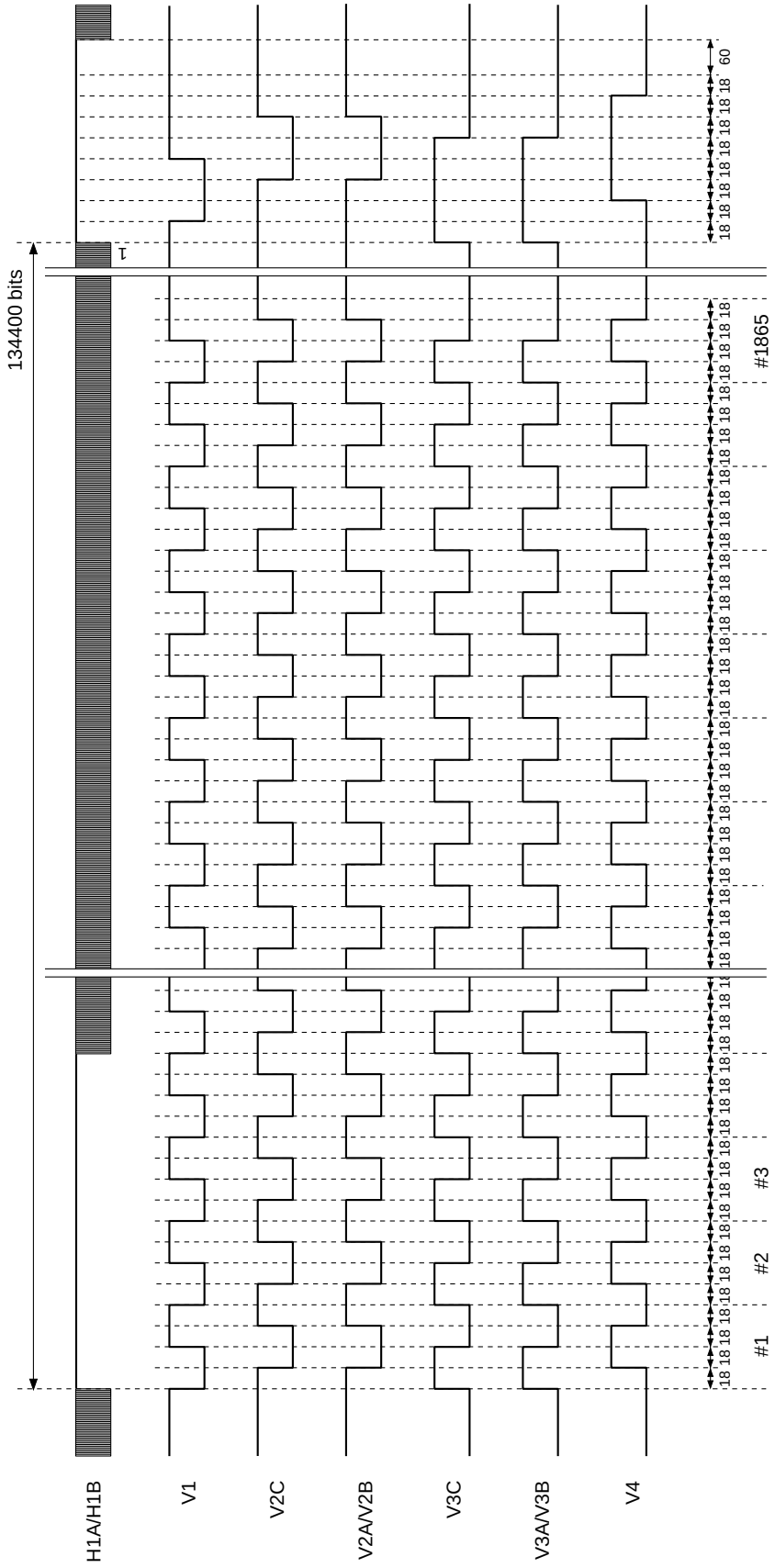
Drive Timing Chart (Vertical Sync) Progressive Scan Mode (With Mechanical Shutter)



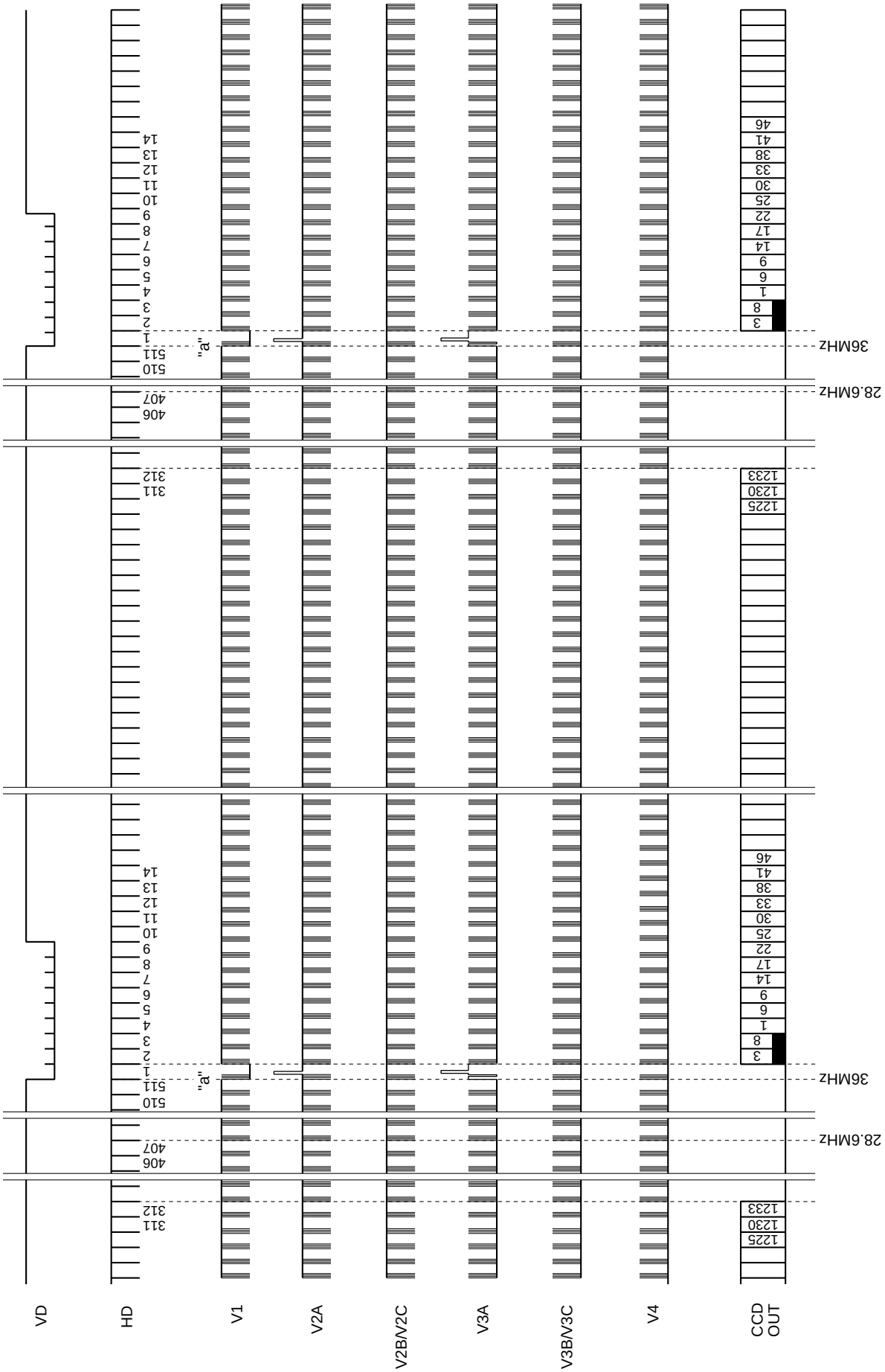
Note) The 1564 and 1565H horizontal periods at 36MHz are 1021clk; the 1742H horizontal period at 28MHz is 1530clk.

Drive Timing Chart (Vertical Sync) **Progressive Scan Mode (With Mechanical Shutter)**

"b" enlarged

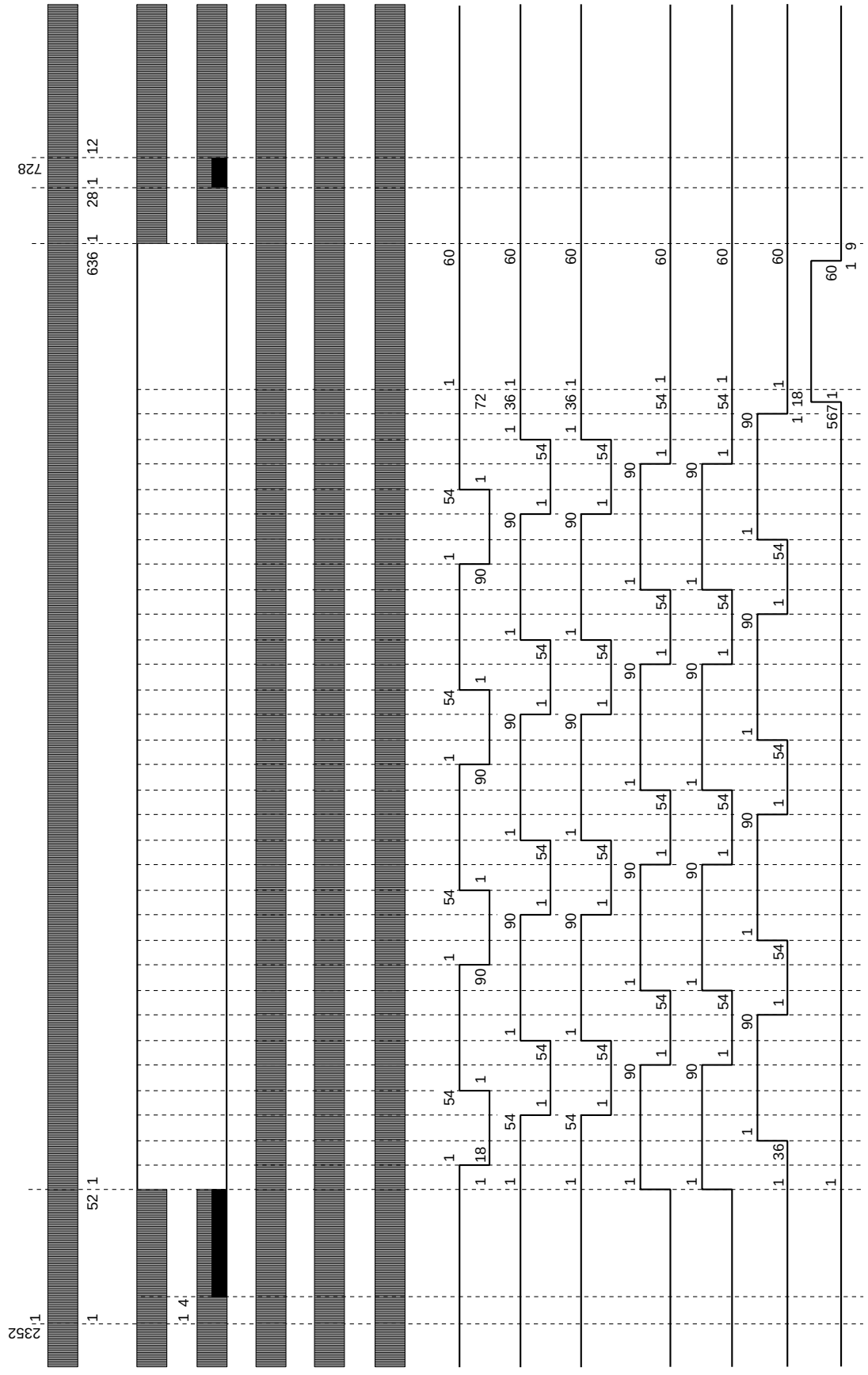


Drive Timing Chart (Vertical Sync) 2/8-line Readout Mode



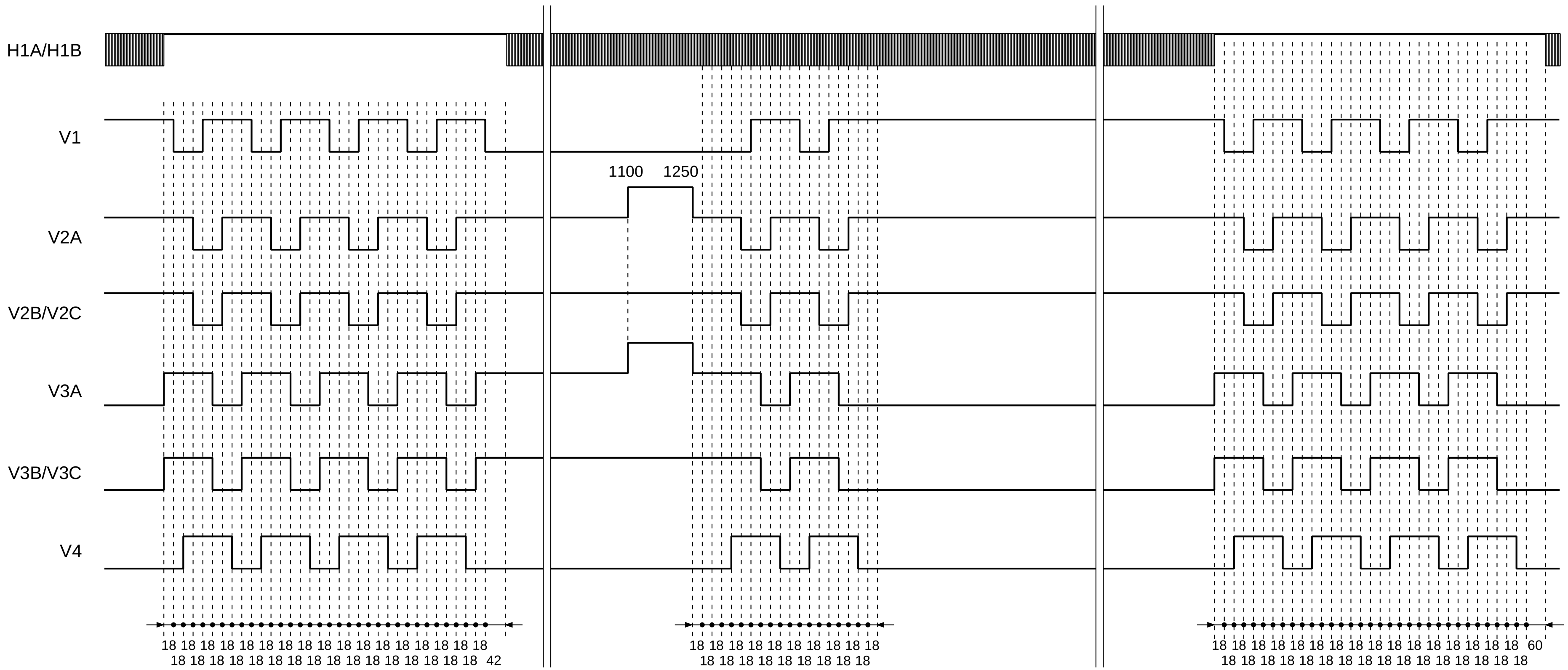
Note) The 511H horizontal period at 36MHz is 1680clk; the 406 and 407H horizontal periods at 28MHz are 1470clk.

Drive Timing Chart (Horizontal Sync) 2/8-line Readout Mode

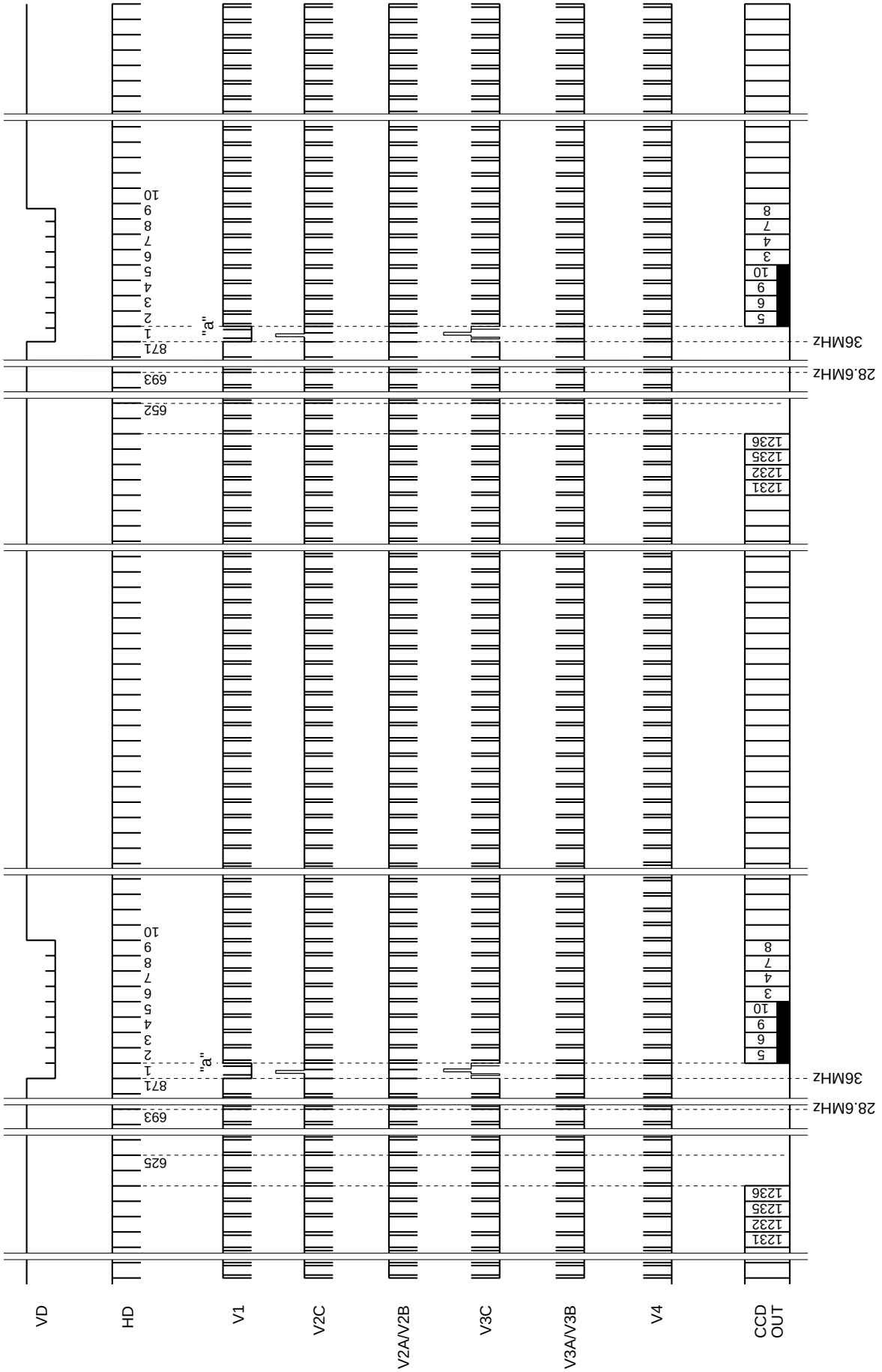


Drive Timing Chart (Vertical Sync) **2/8-line Readout Mode**

"a" enlarged

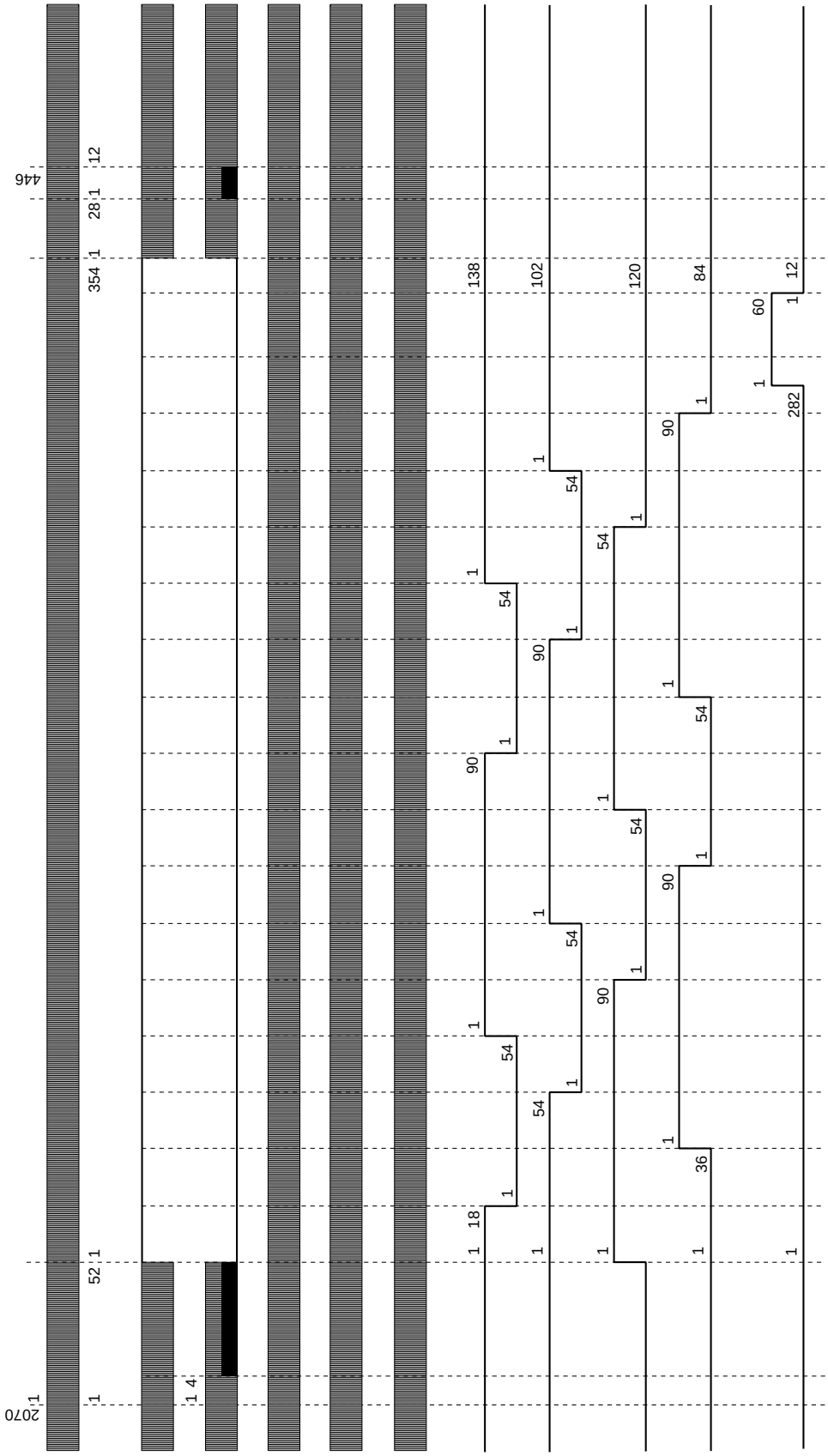


Drive Timing Chart (Vertical Sync) 2/4-line Readout Mode



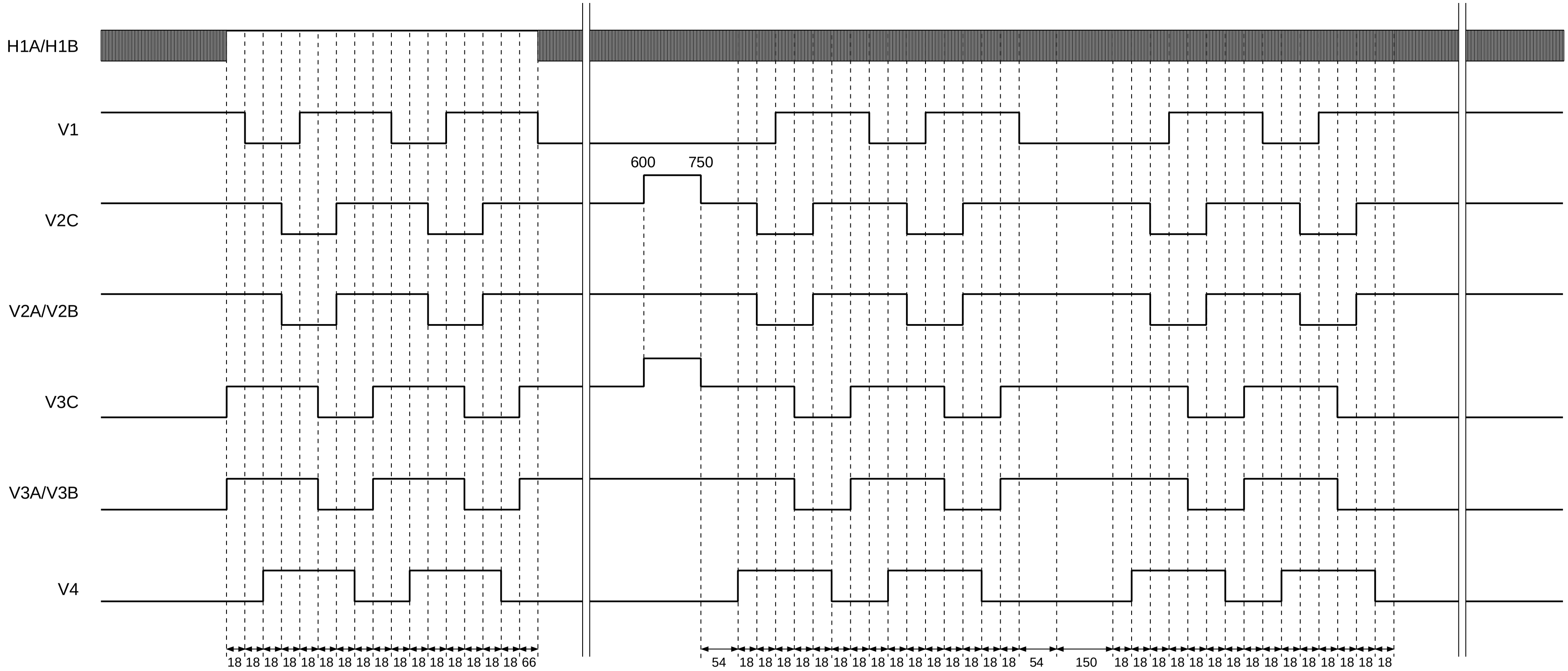
Note) The 871H horizontal period at 36MHz is 900clk; the 693H horizontal period at 28MHz is 810clk.

Drive Timing Chart (Horizontal Sync) **2/4-line Readout Mode**

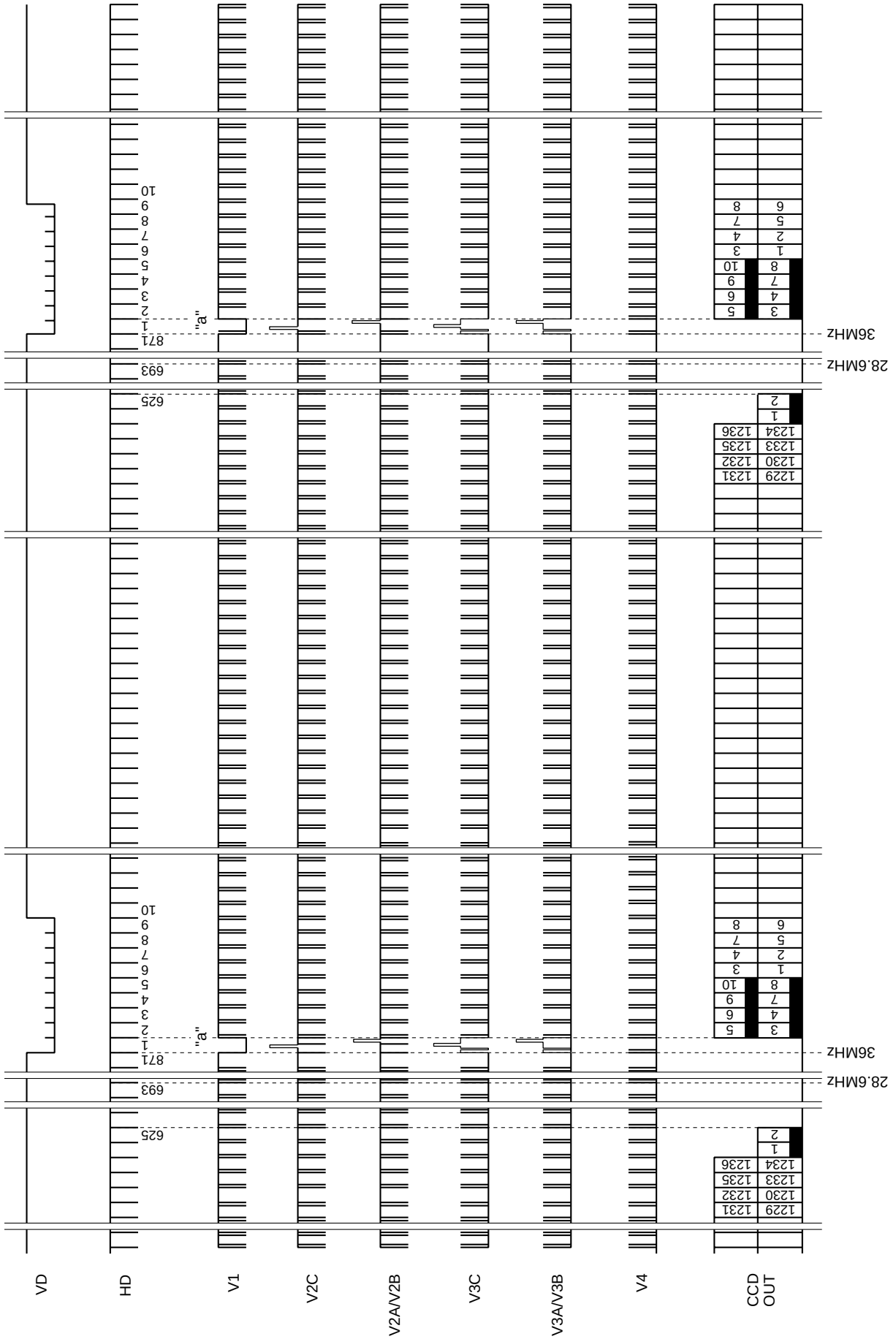


Drive Timing Chart (Vertical Sync) 2/4-line Readout Mode

"a" enlarged

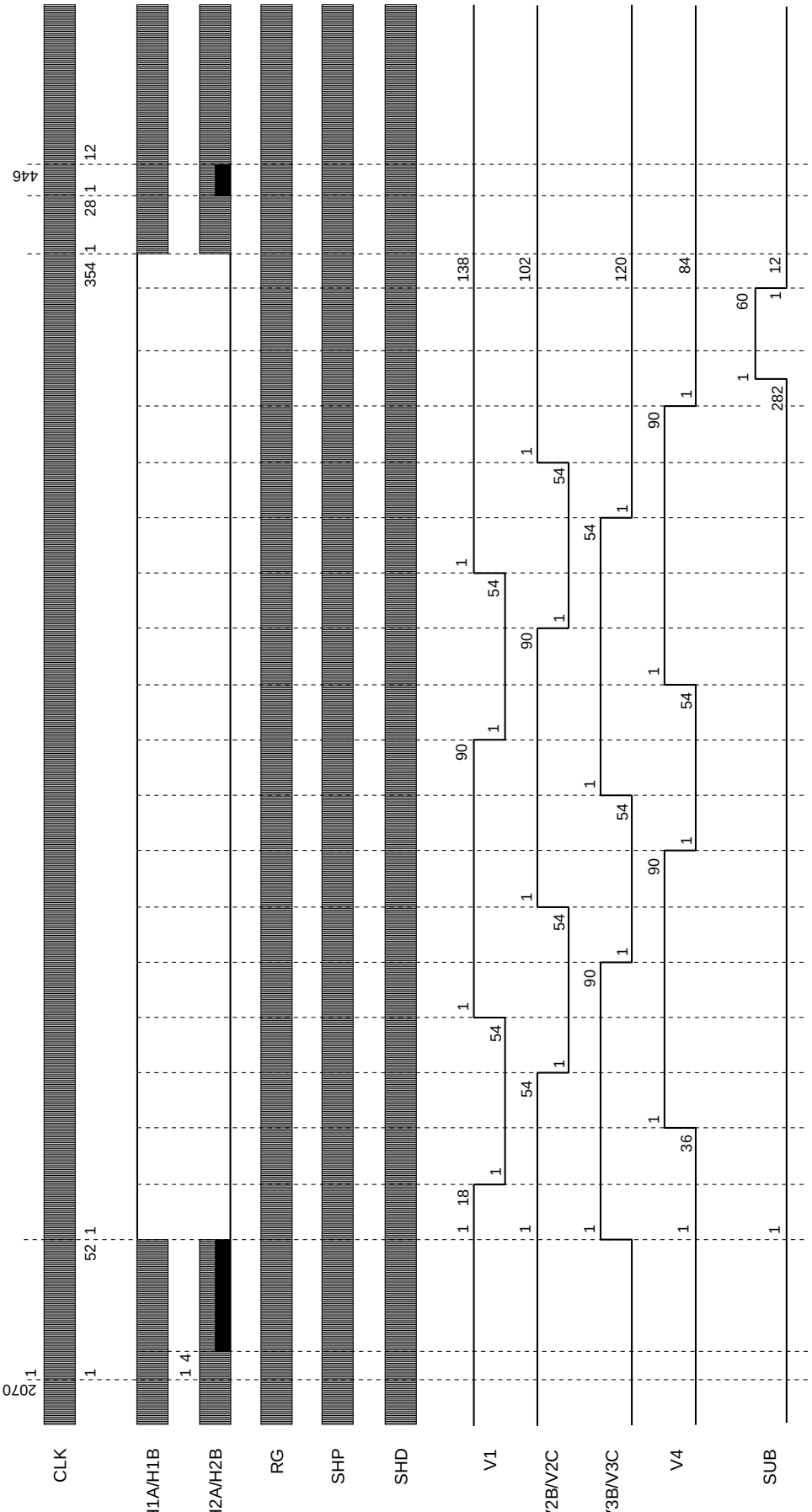


Drive Timing Chart (Vertical Sync) 2-line Addition Mode



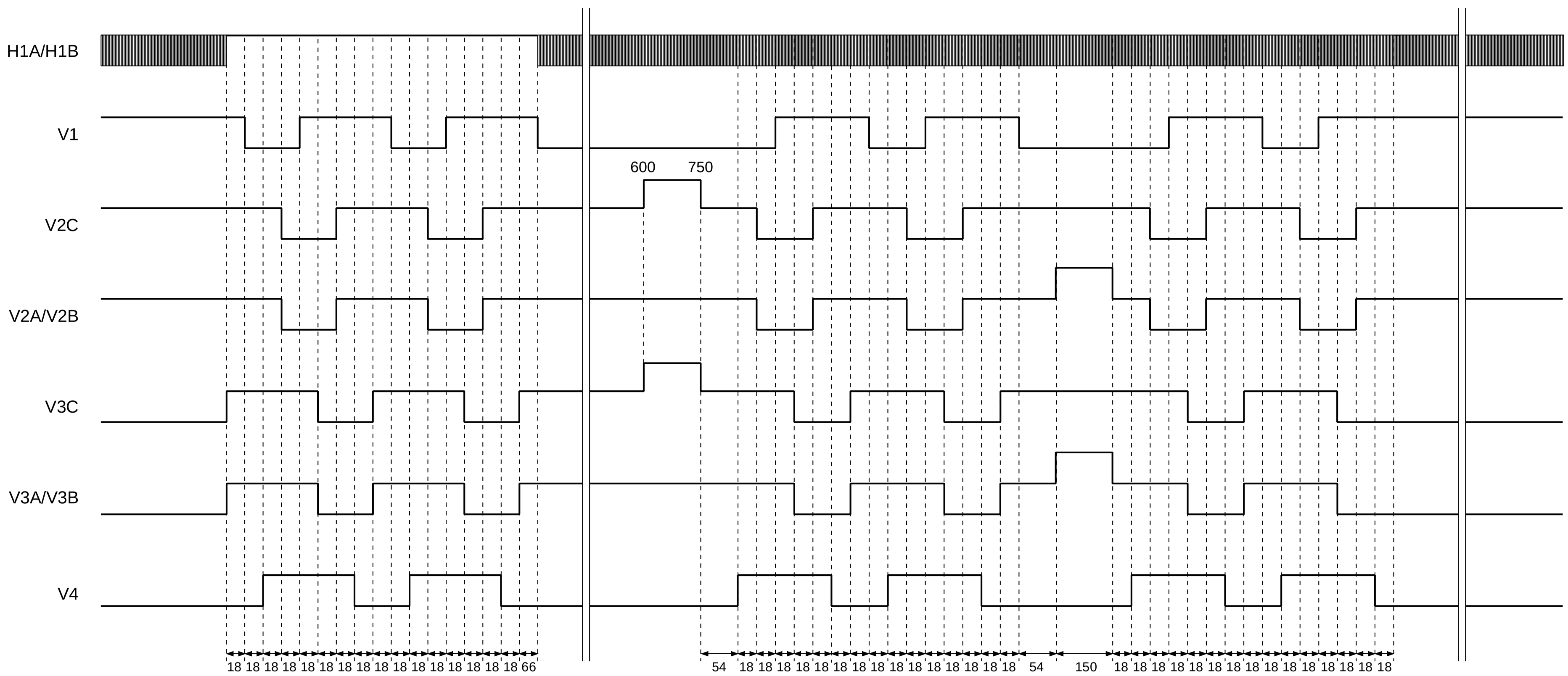
Note) The 871H horizontal period at 36MHz is 900clk; the 693H horizontal period at 28MHz is 810clk.

Drive Timing Chart (Horizontal Sync) 2-line Addition Mode

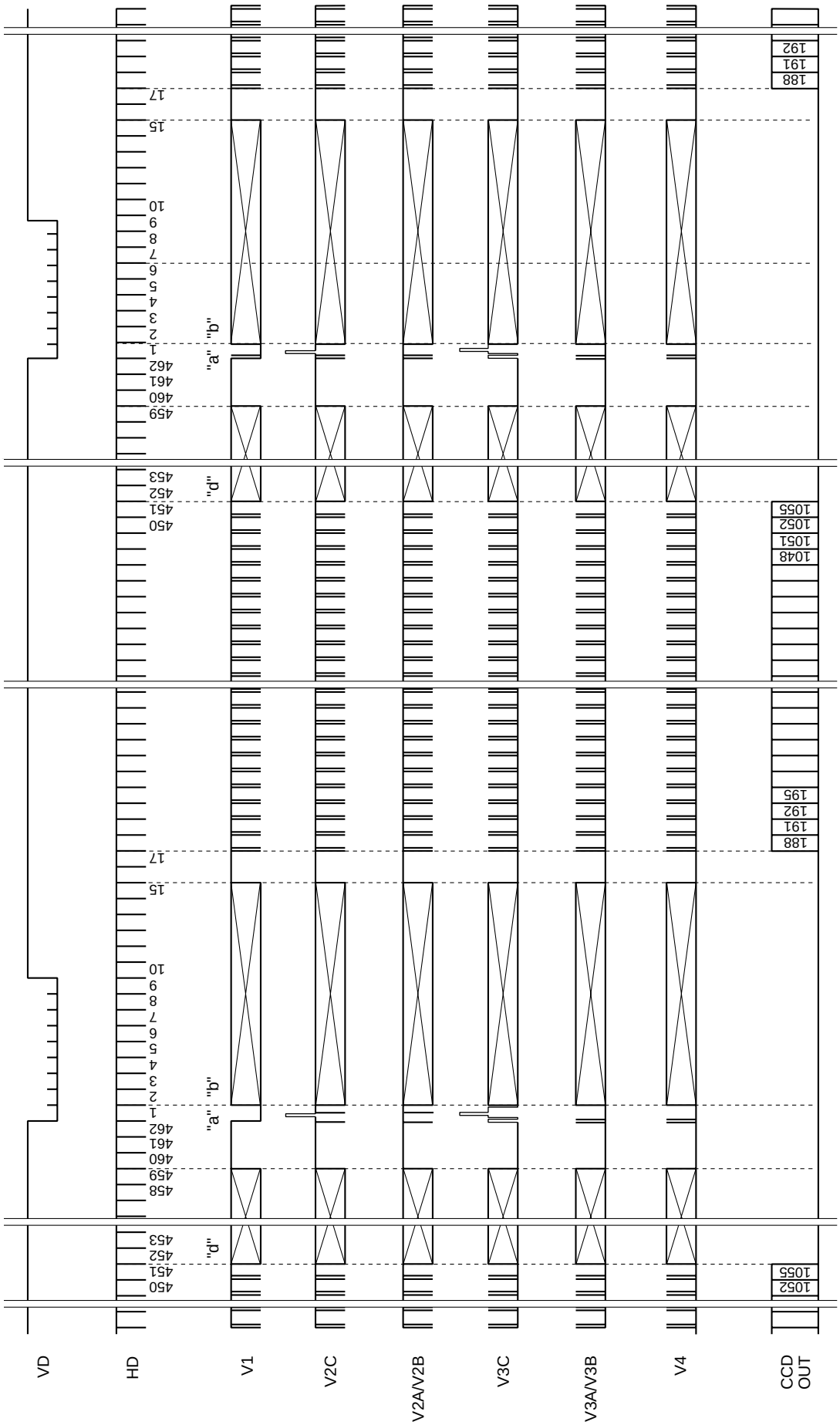


Drive Timing Chart (Vertical Sync) 2-line Addition Mode

"a" enlarged

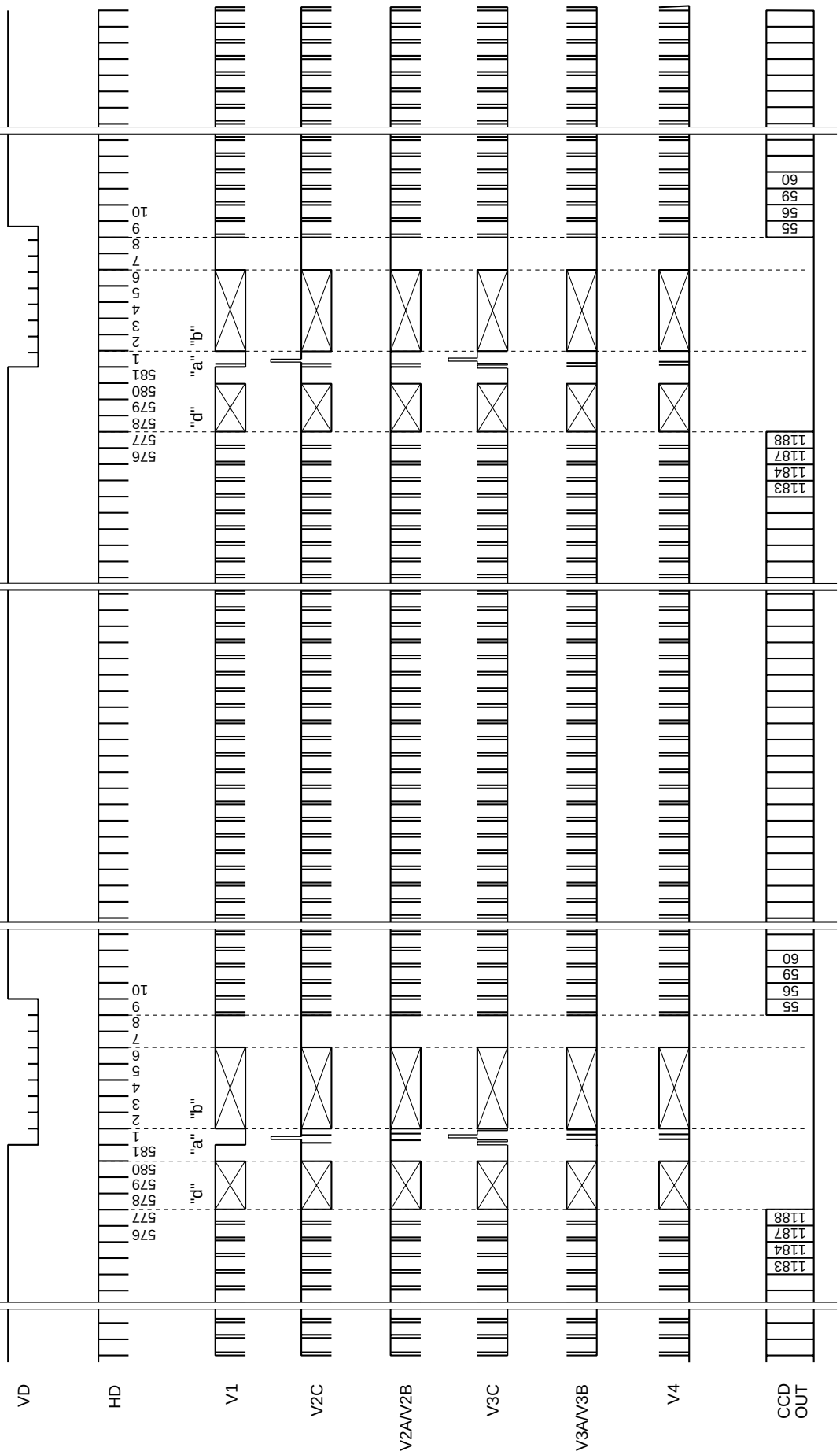


Drive Timing Chart (Vertical Sync) **Center Scan Mode (1)/(28.6MHz)**



Note) The 462H horizontal period is 1230clk.

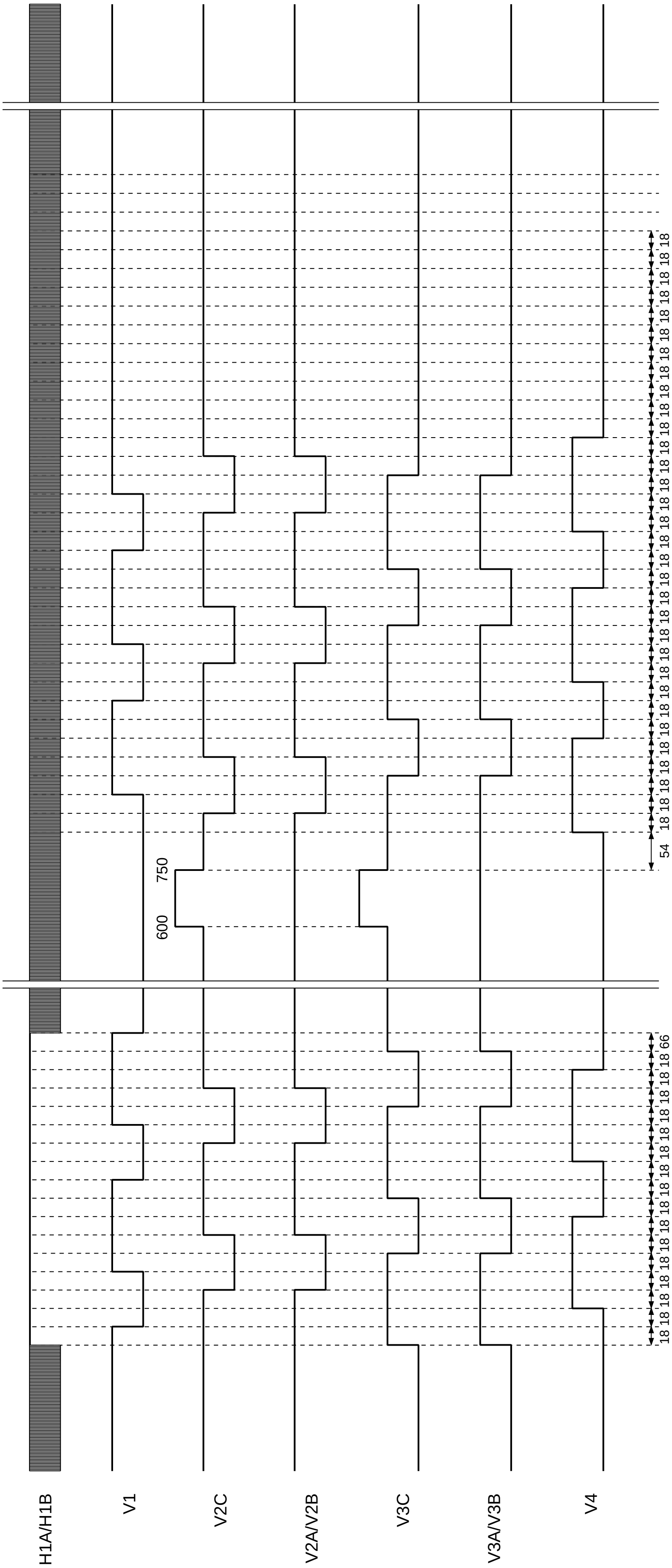
Drive Timing Chart (Vertical Sync) **Center Scan Mode (1)/(36MHz)**



Note) The 581H horizontal period is 601clk.

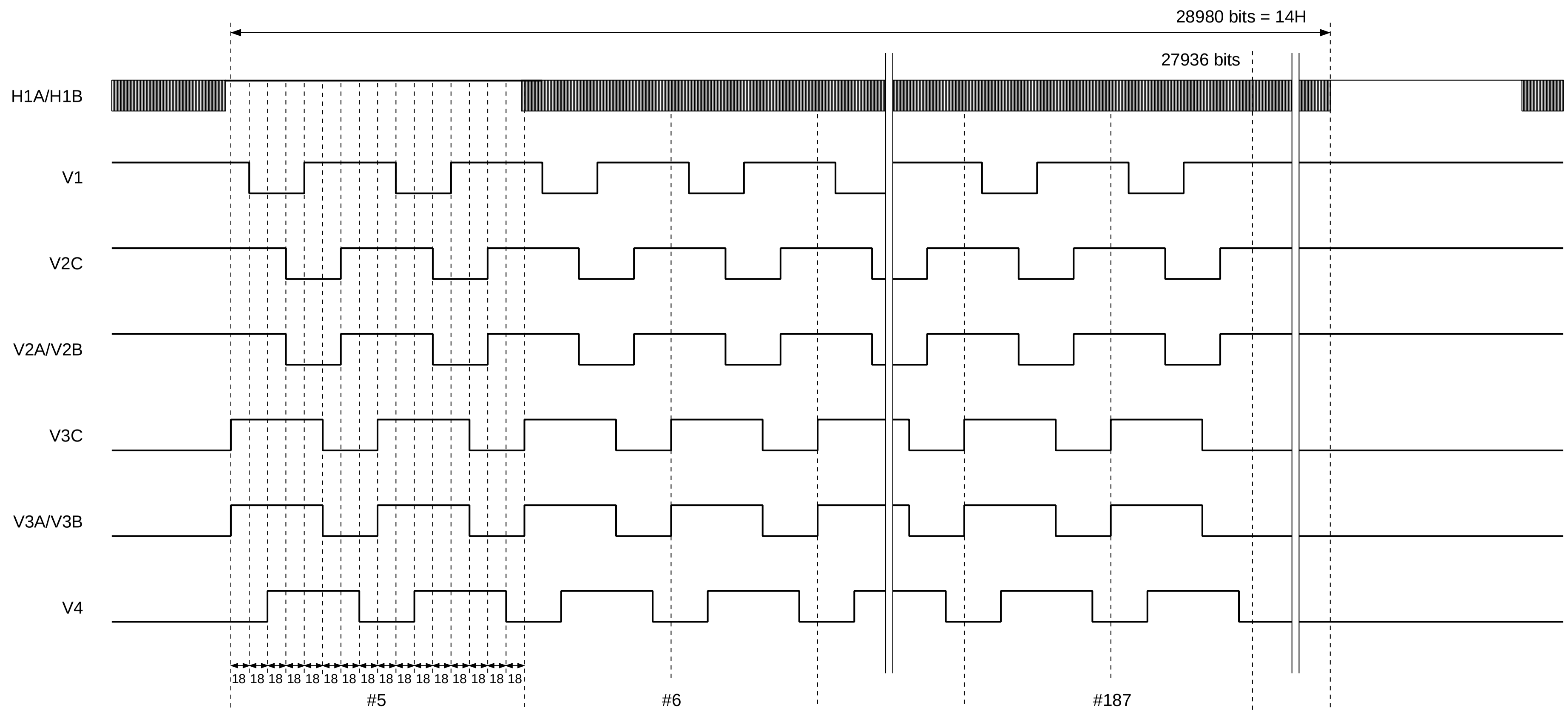
Drive Timing Chart (Vertical Sync) Center Scan Mode (1)

"a" enlarged



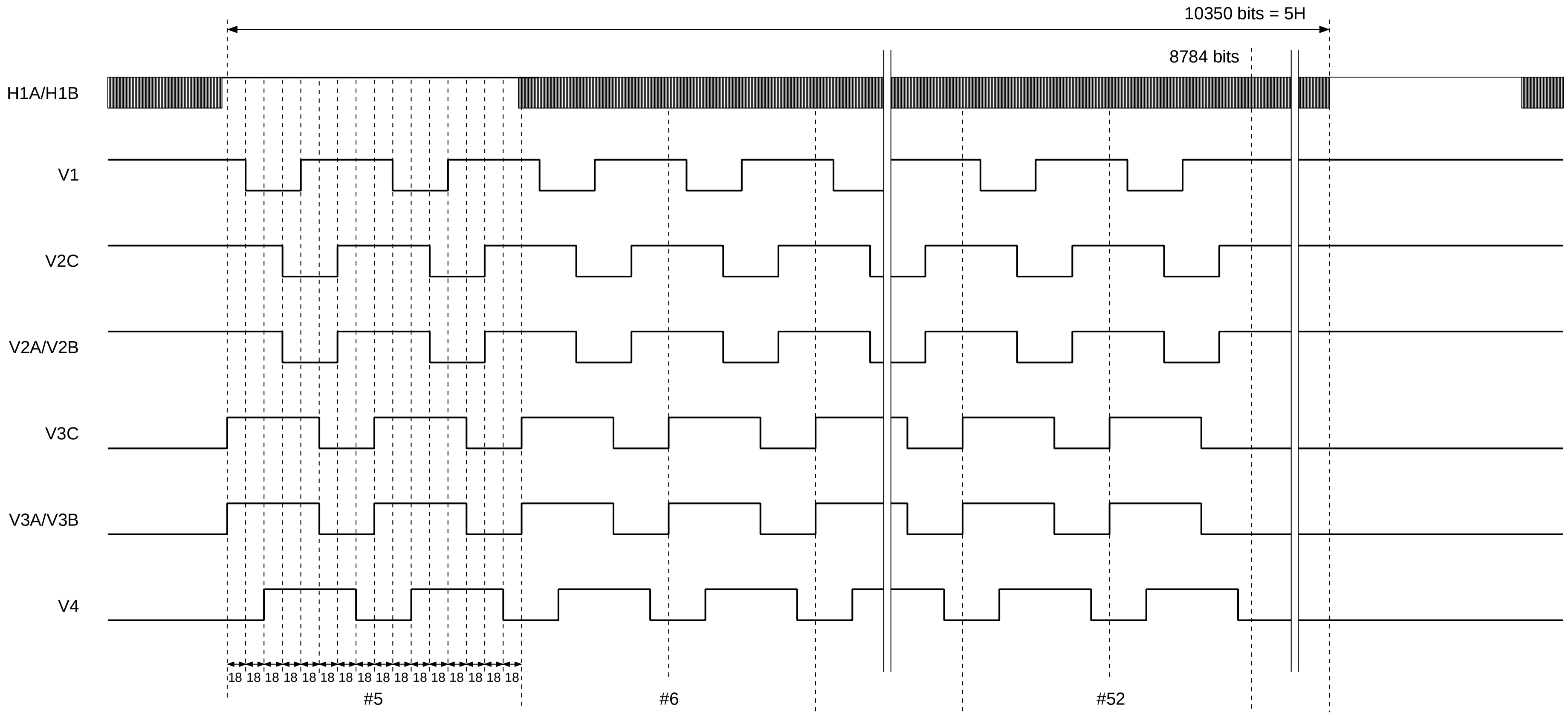
Drive Timing Chart (Vertical Sync) **Center Scan Mode (1)/(28.6MHz)**

"b" enlarged

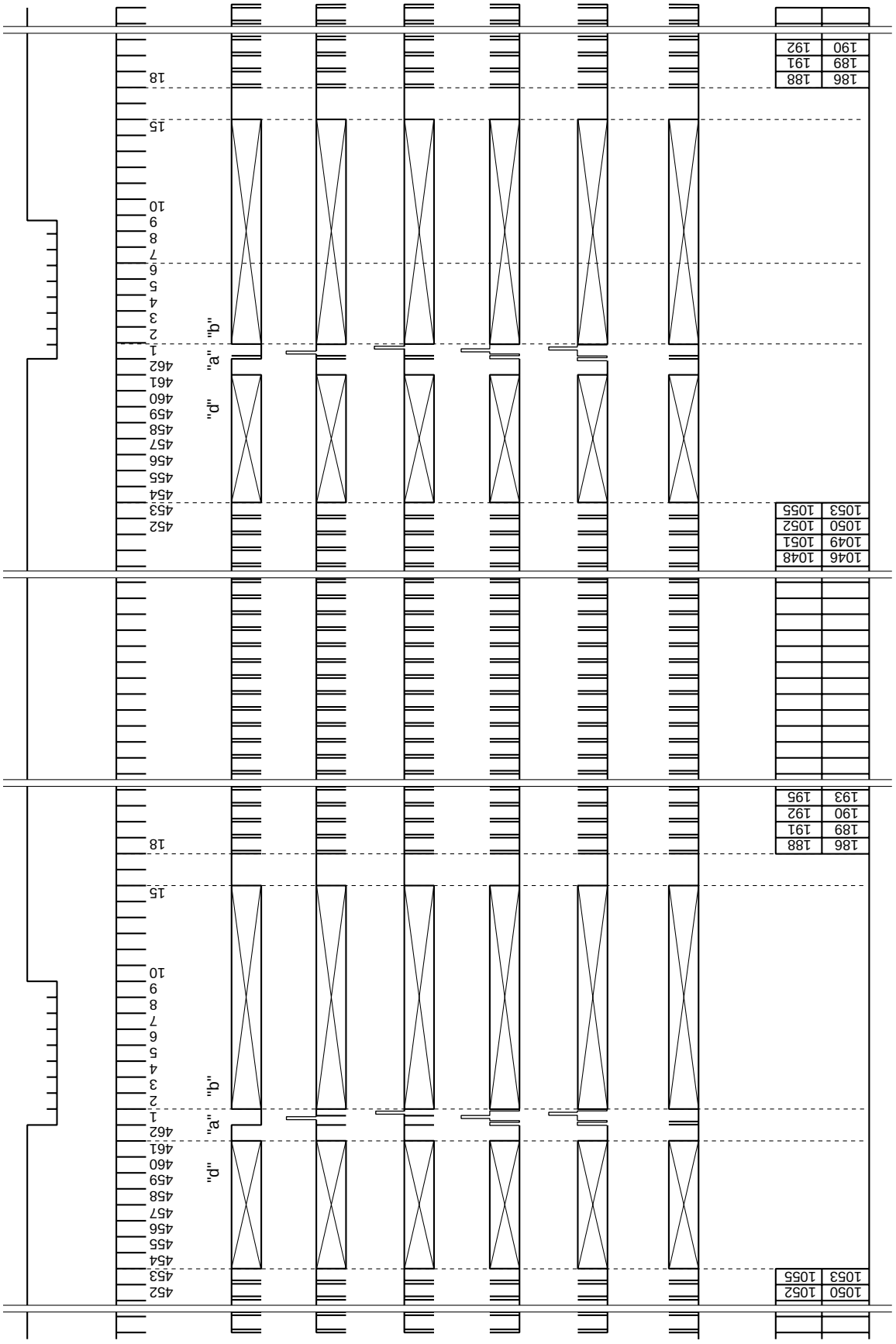


Drive Timing Chart (Vertical Sync) **Center Scan Mode (1)/(36MHz)**

"b" enlarged

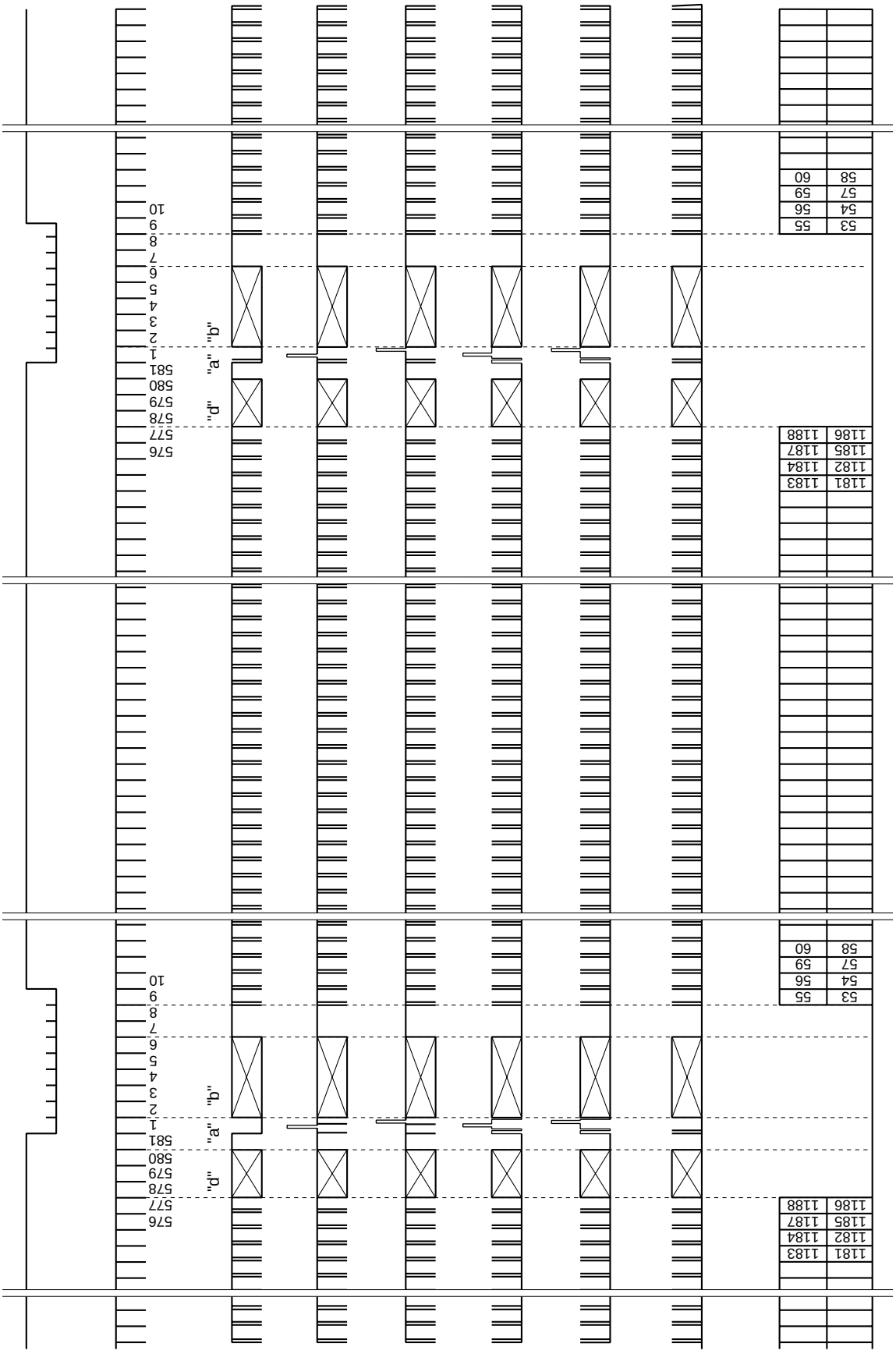


Drive Timing Chart (Vertical Sync) Center Scan Mode (2)/(28.6MHz)



Note) The 462H horizontal period is 1230clk.

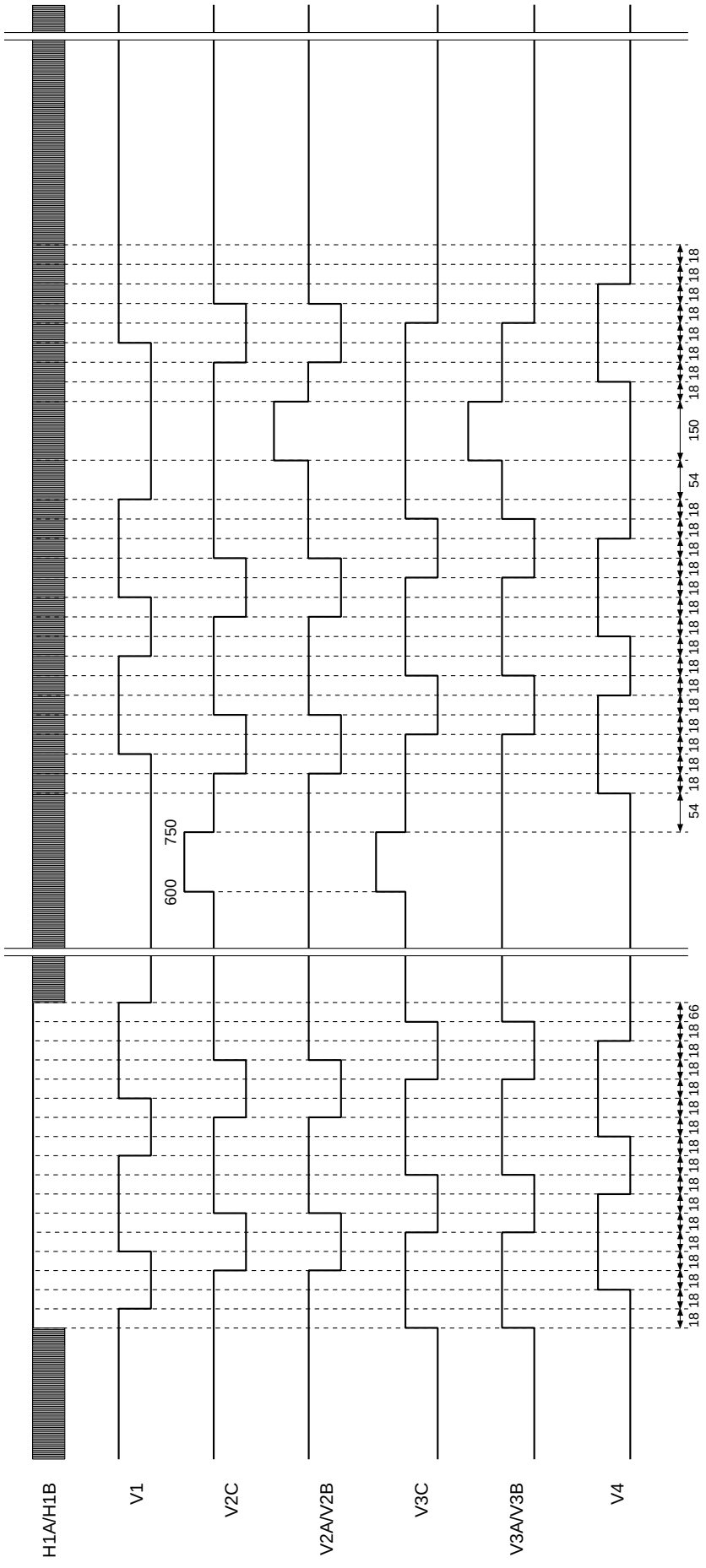
Drive Timing Chart (Vertical Sync) **Center Scan Mode (2)/(36MHz)**



Note) The 581H horizontal period is 601clk.

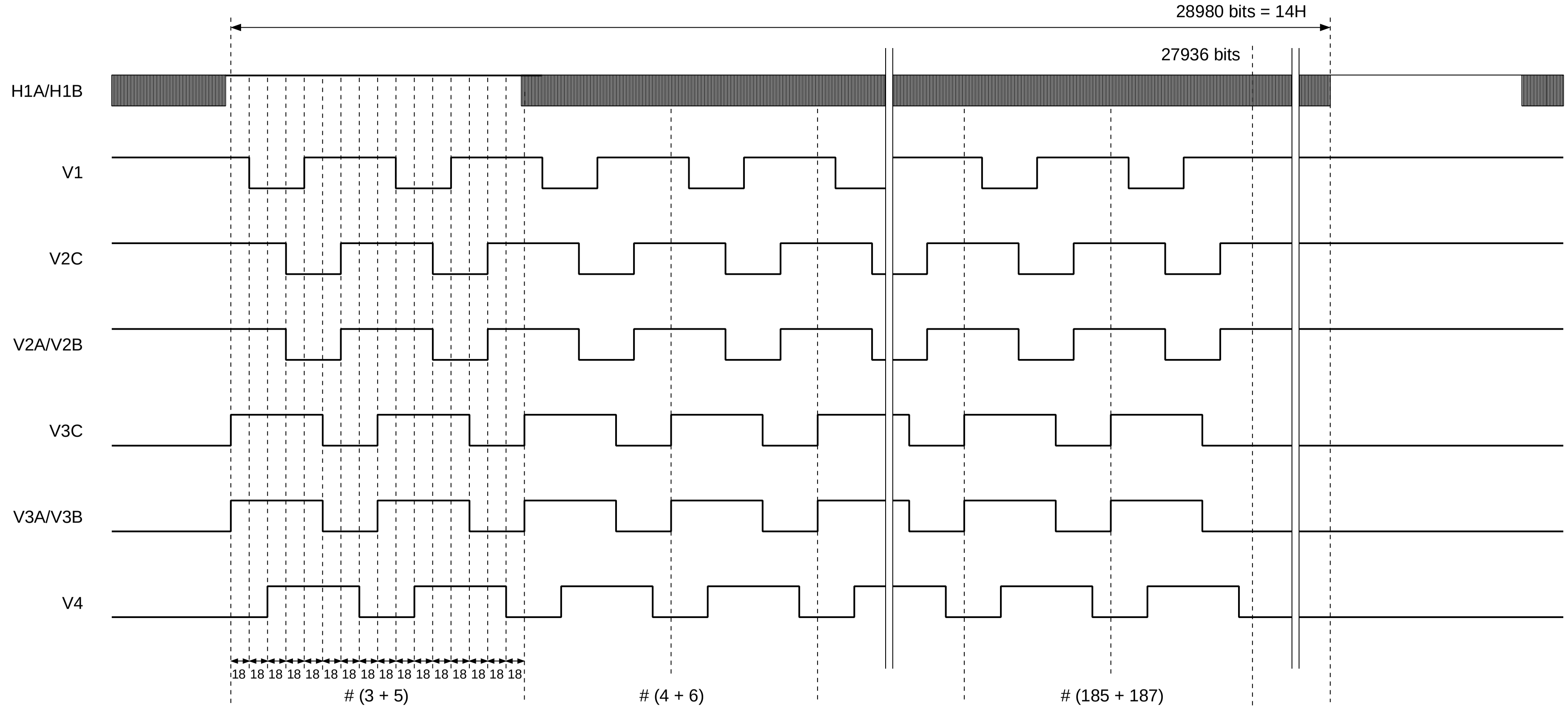
Drive Timing Chart (Vertical Sync) Center Scan Mode (2)

"a" enlarged



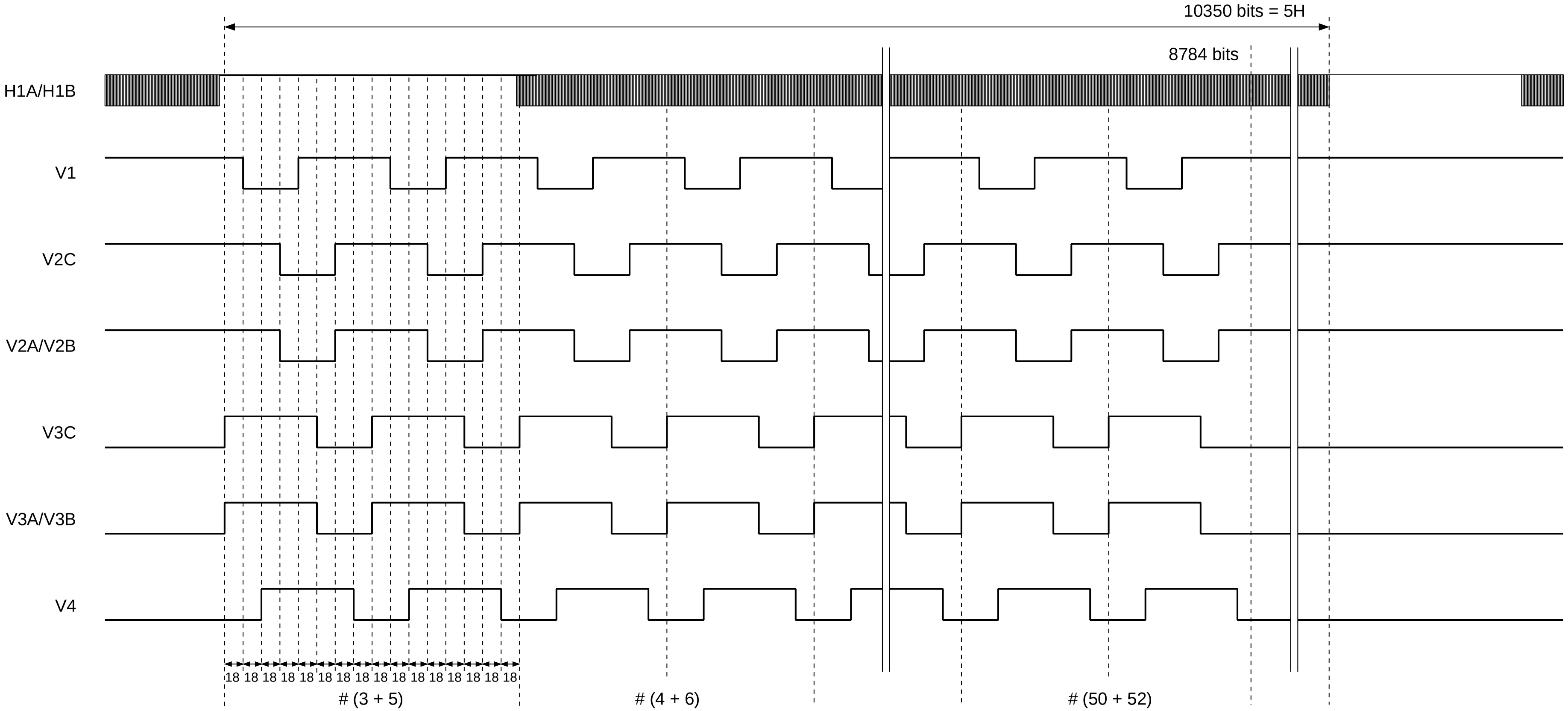
Drive Timing Chart (Vertical Sync)   Center Scan Mode (2)/(28.6MHz)

"b" enlarged

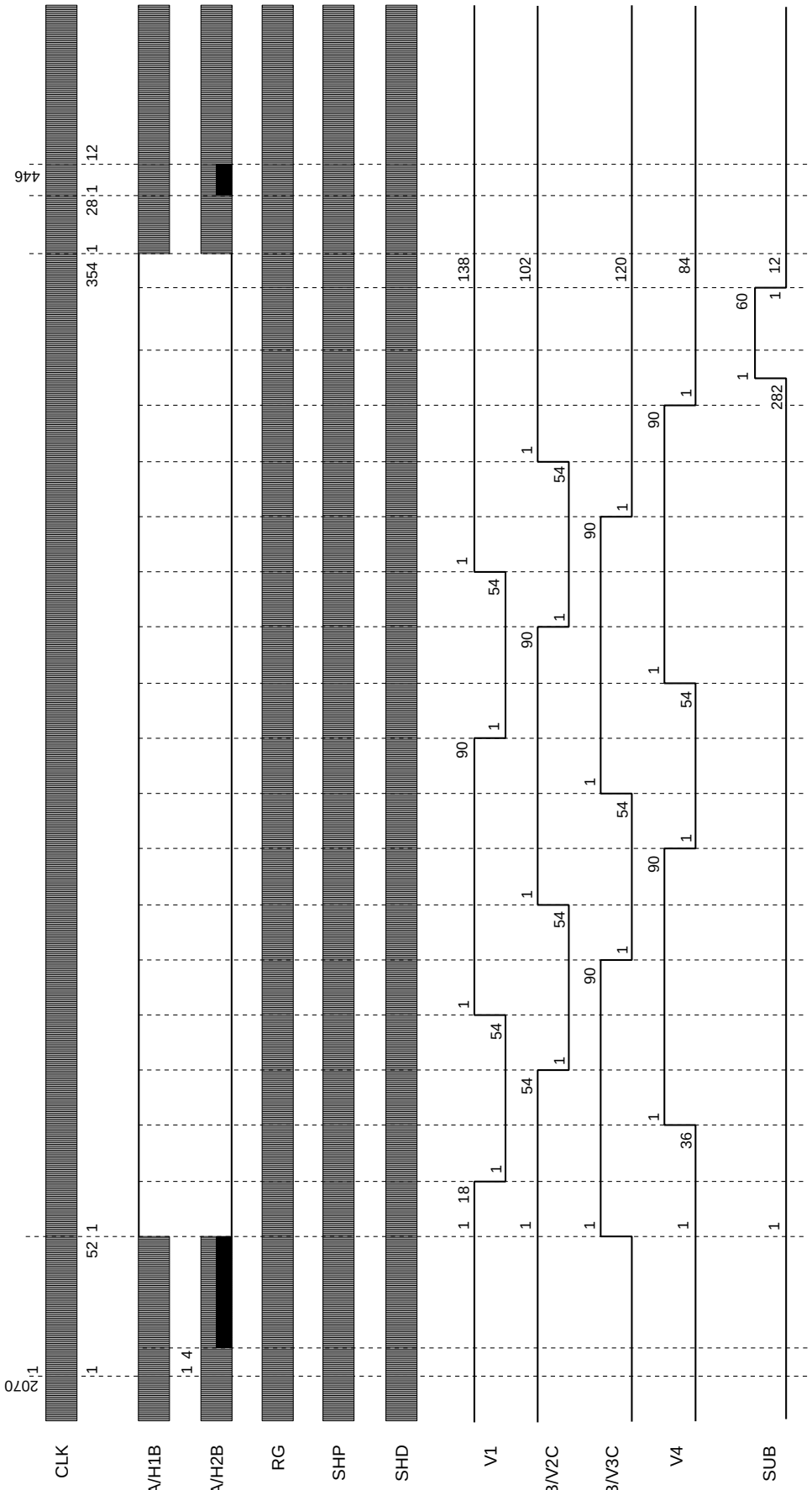


Drive Timing Chart (Vertical Sync) **Center Scan Mode (2)/(36MHz)**

"b" enlarged

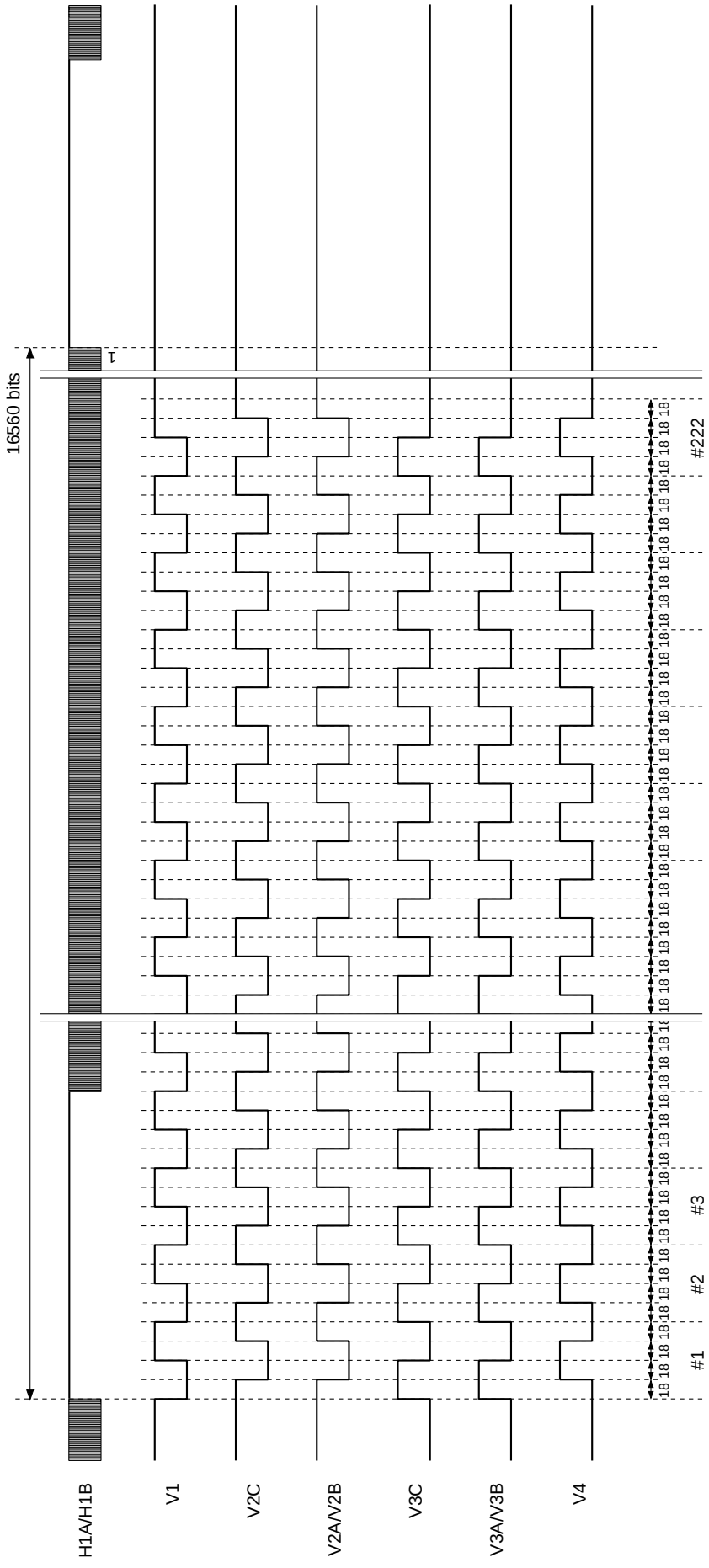


Drive Timing Chart (Horizontal Sync) **Center Scan Modes (1) and (2)**



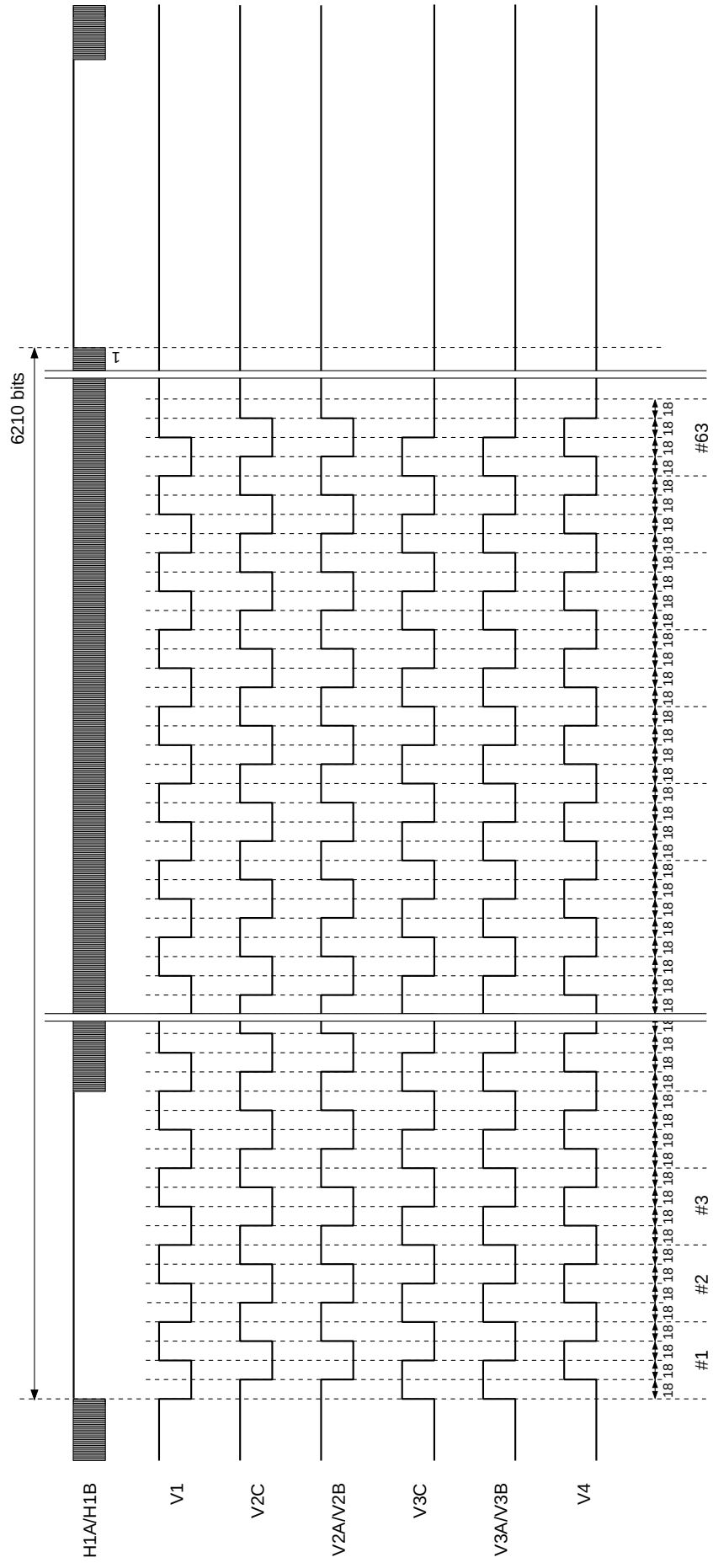
Drive Timing Chart (Vertical Sync) **Center Scan Modes (1) and (2)/(28.6MHz)**

"d" enlarged

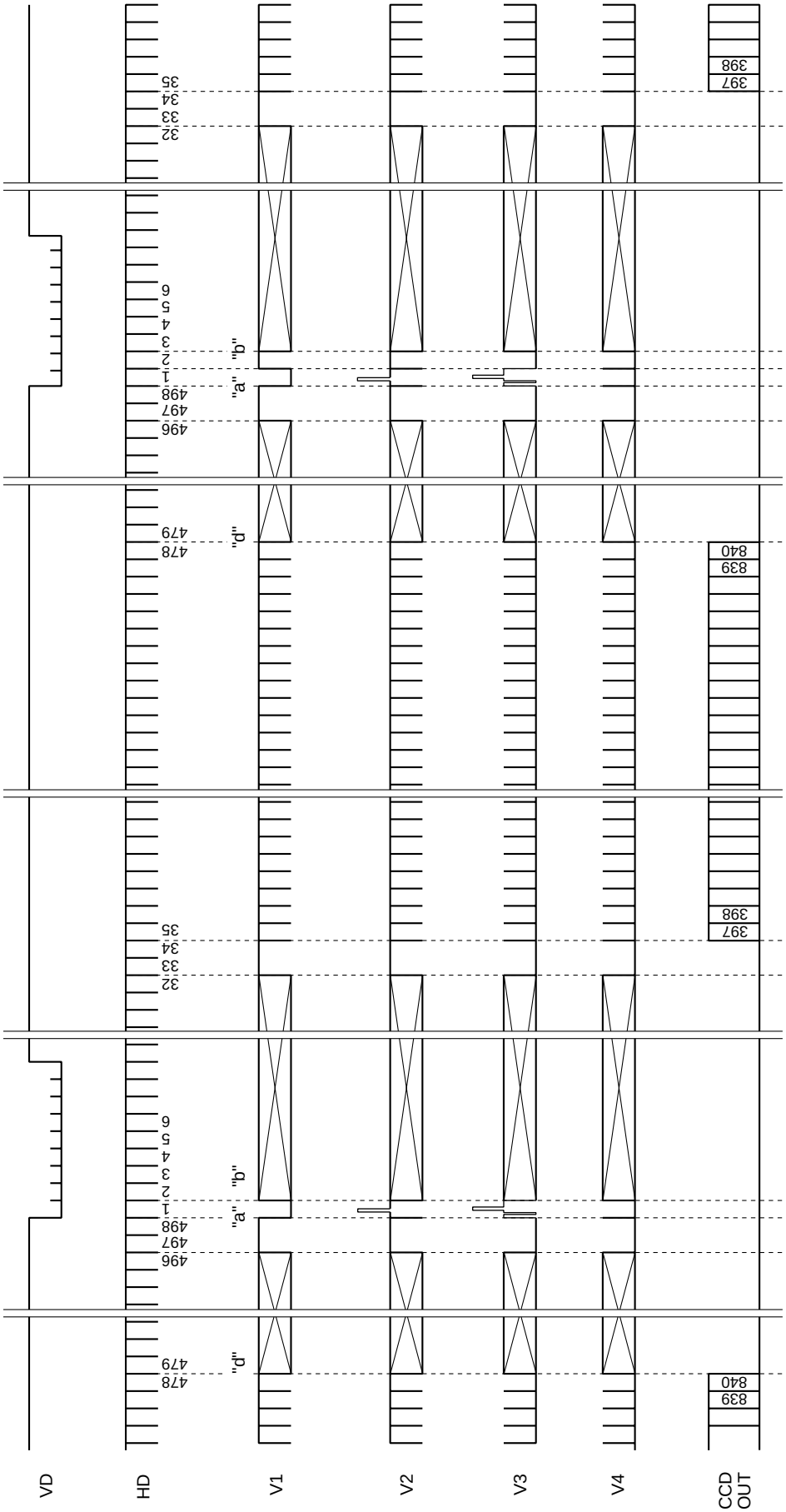


Drive Timing Chart (Vertical Sync) **Center Scan Modes (1) and (2)/(36MHz)**

"d" enlarged

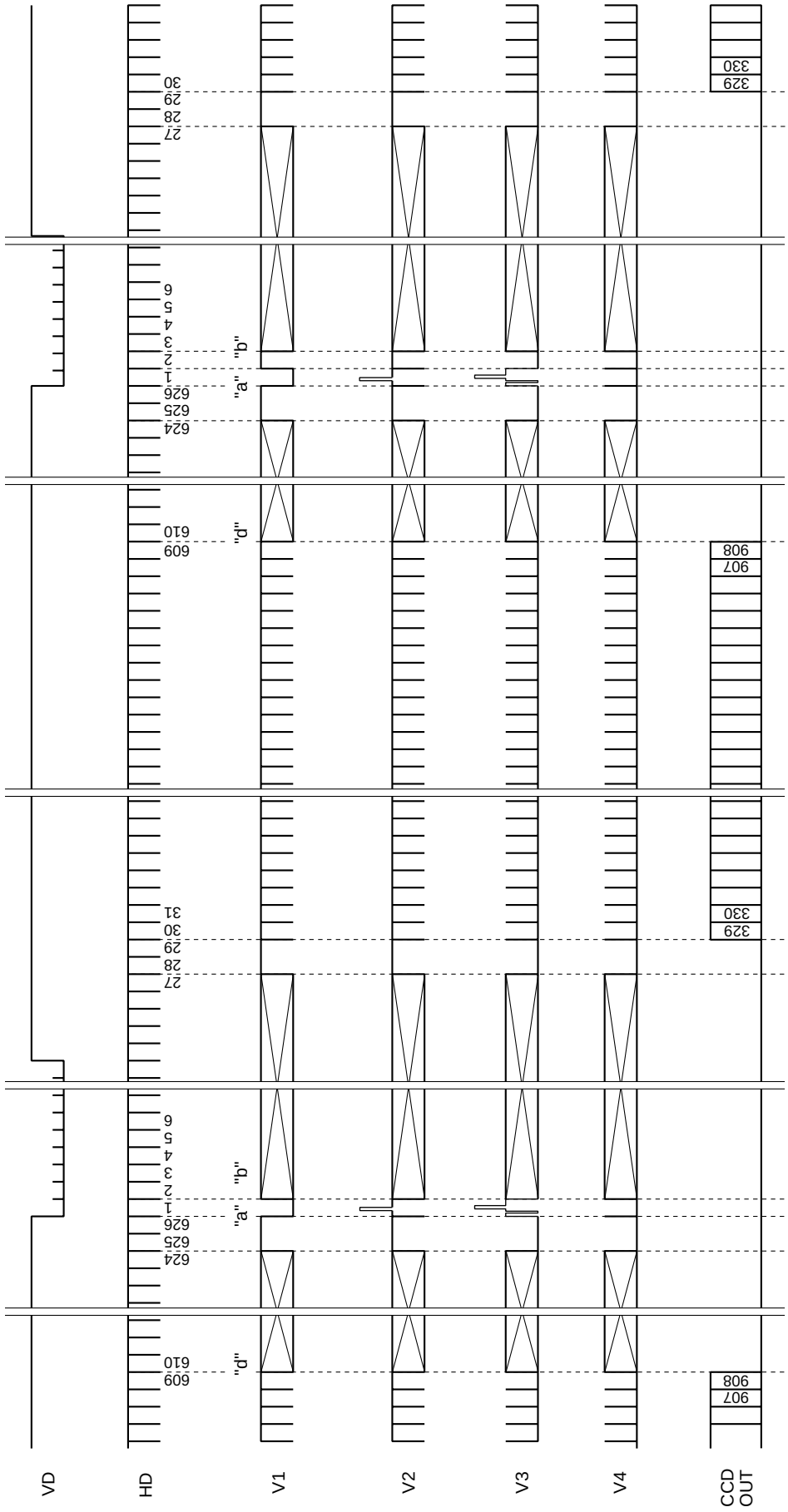


Drive Timing Chart (Vertical Sync) **Center Scan Mode (3)/(28.6MHz)**



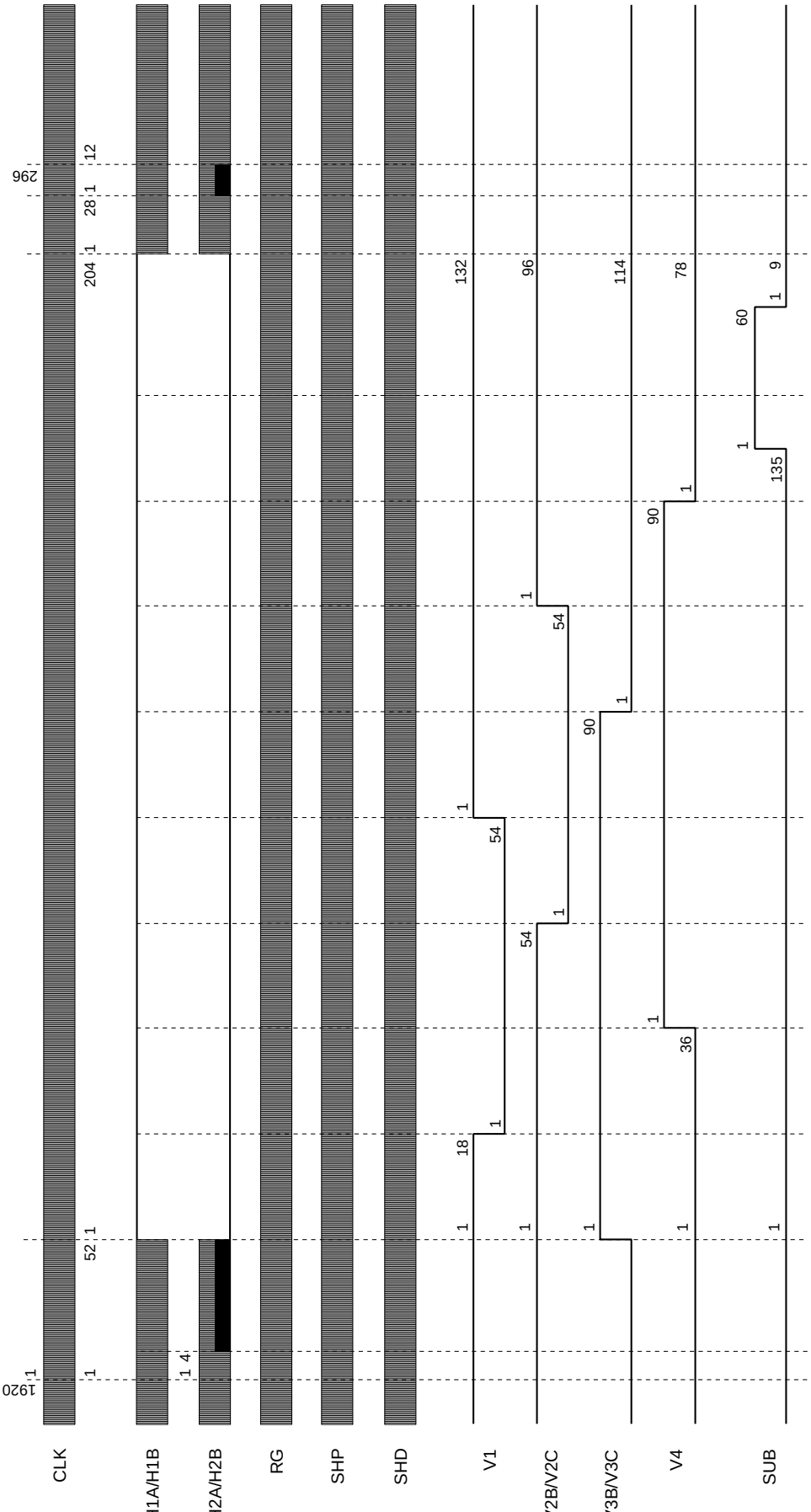
Note) The 498H horizontal period is 1260clk.

Drive Timing Chart (Vertical Sync) **Center Scan Mode (3)/(36MHz)**



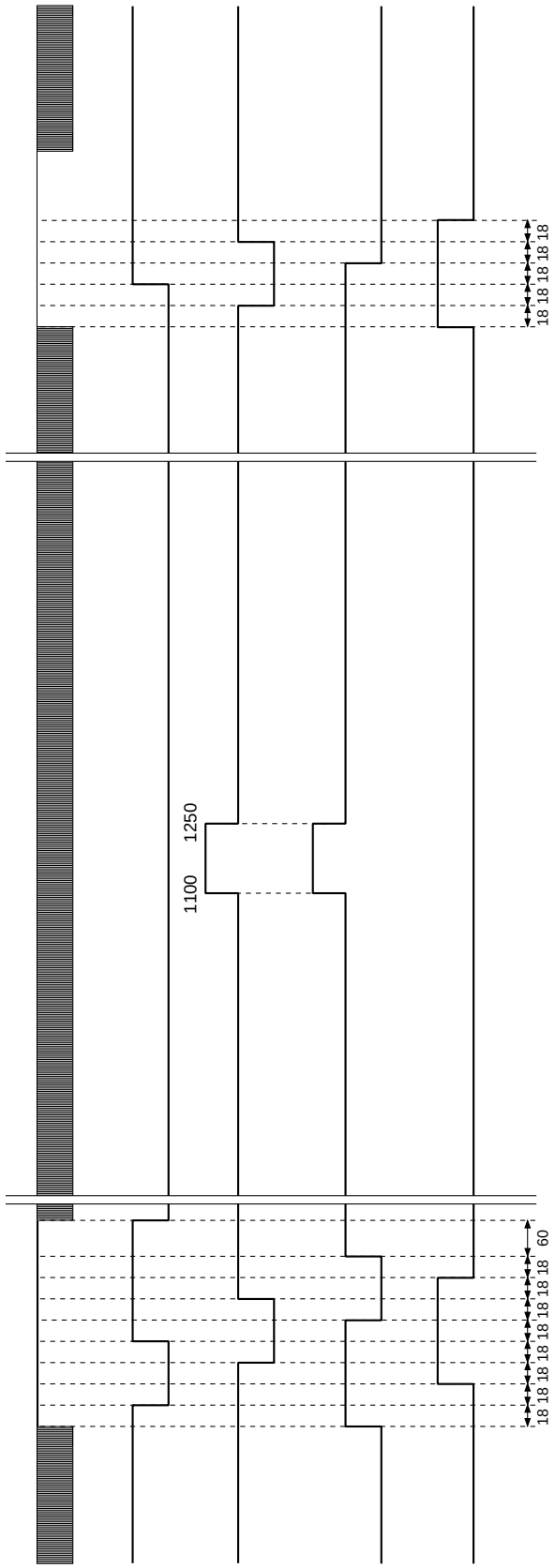
Note) The 626H horizontal period is 1200clk.

Drive Timing Chart (Horizontal Sync) **Center Scan Mode (3)**



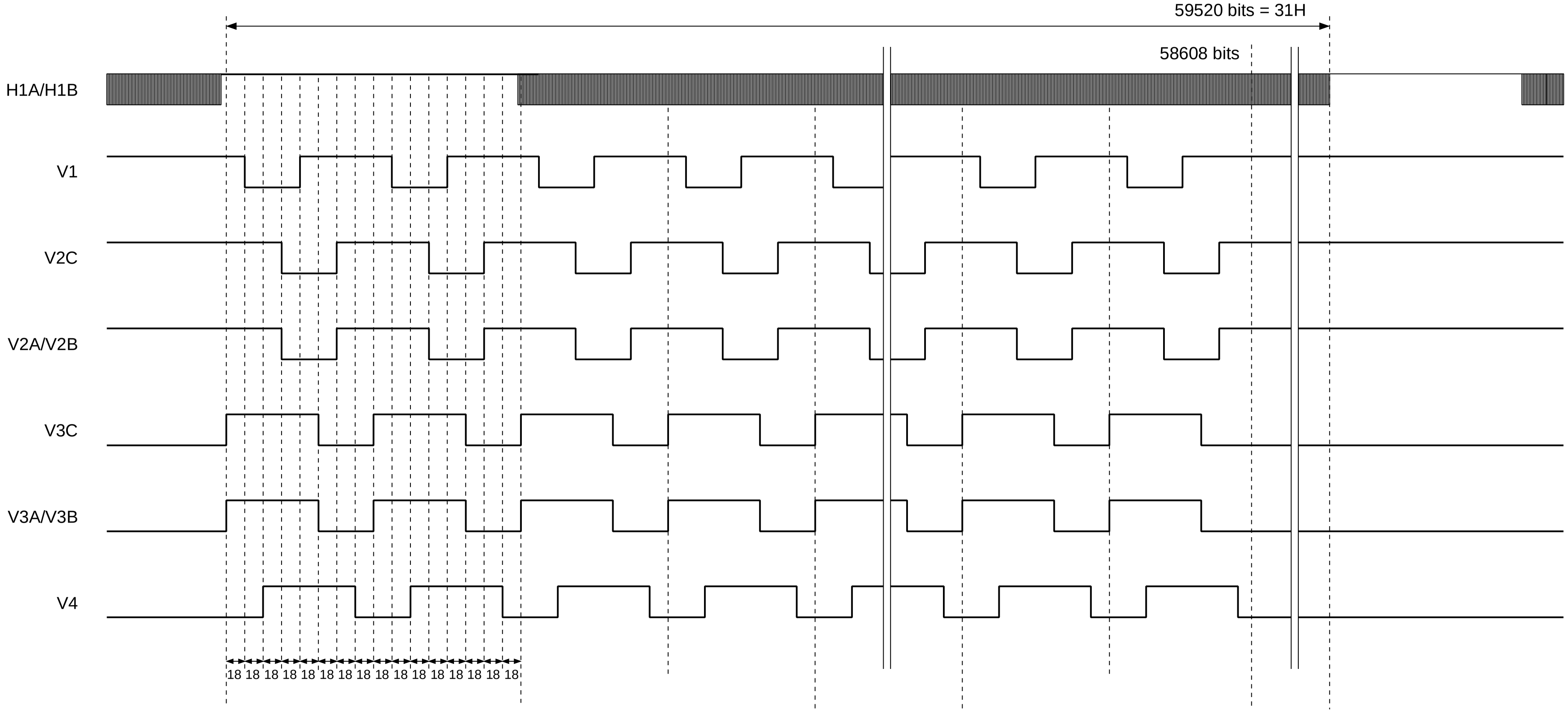
Drive Timing Chart (Vertical Sync) **Center Scan Mode (3)**

"a" enlarged



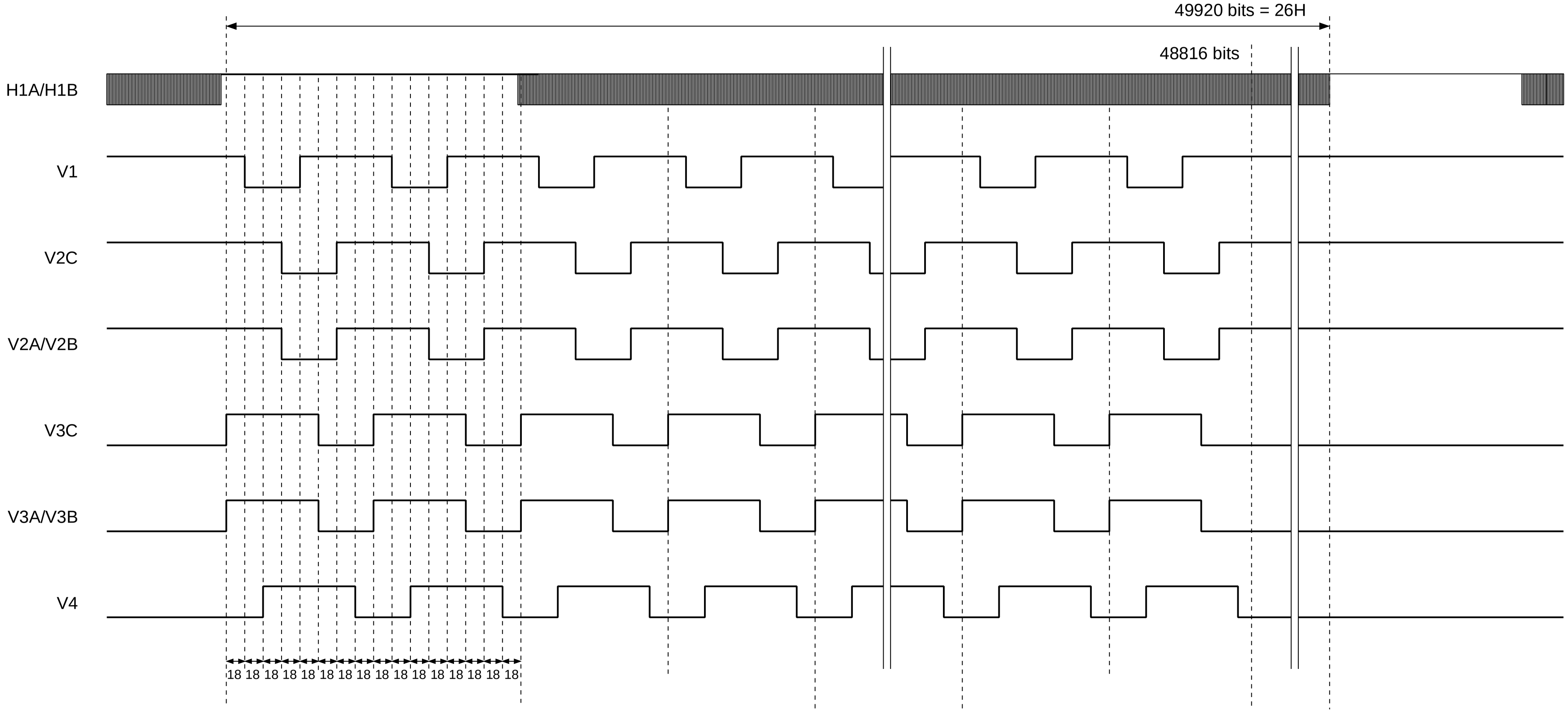
Drive Timing Chart (Vertical Sync) Center Scan Mode (3)/(28.6MHz)

"b" enlarged



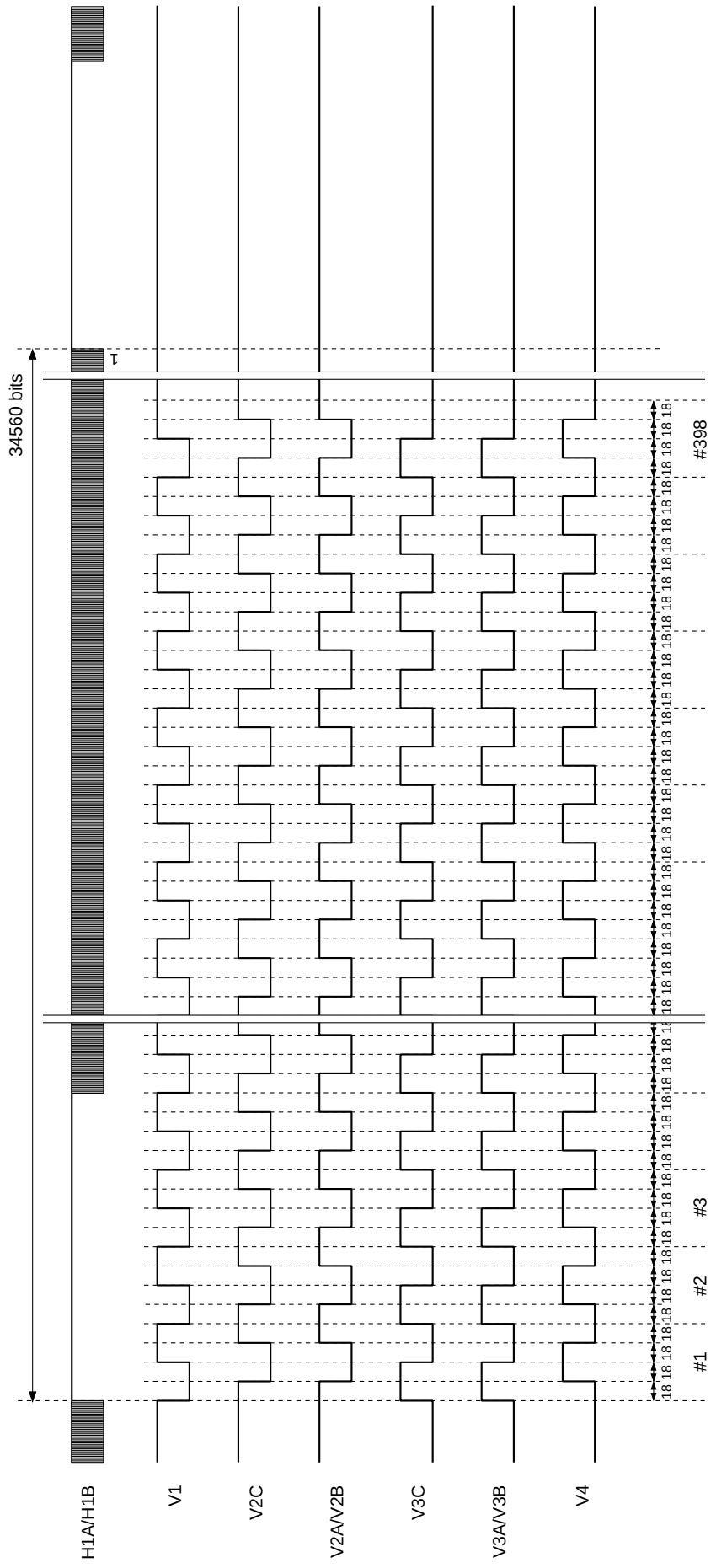
Drive Timing Chart (Vertical Sync) Center Scan Mode (3)/(36MHz)

"b" enlarged



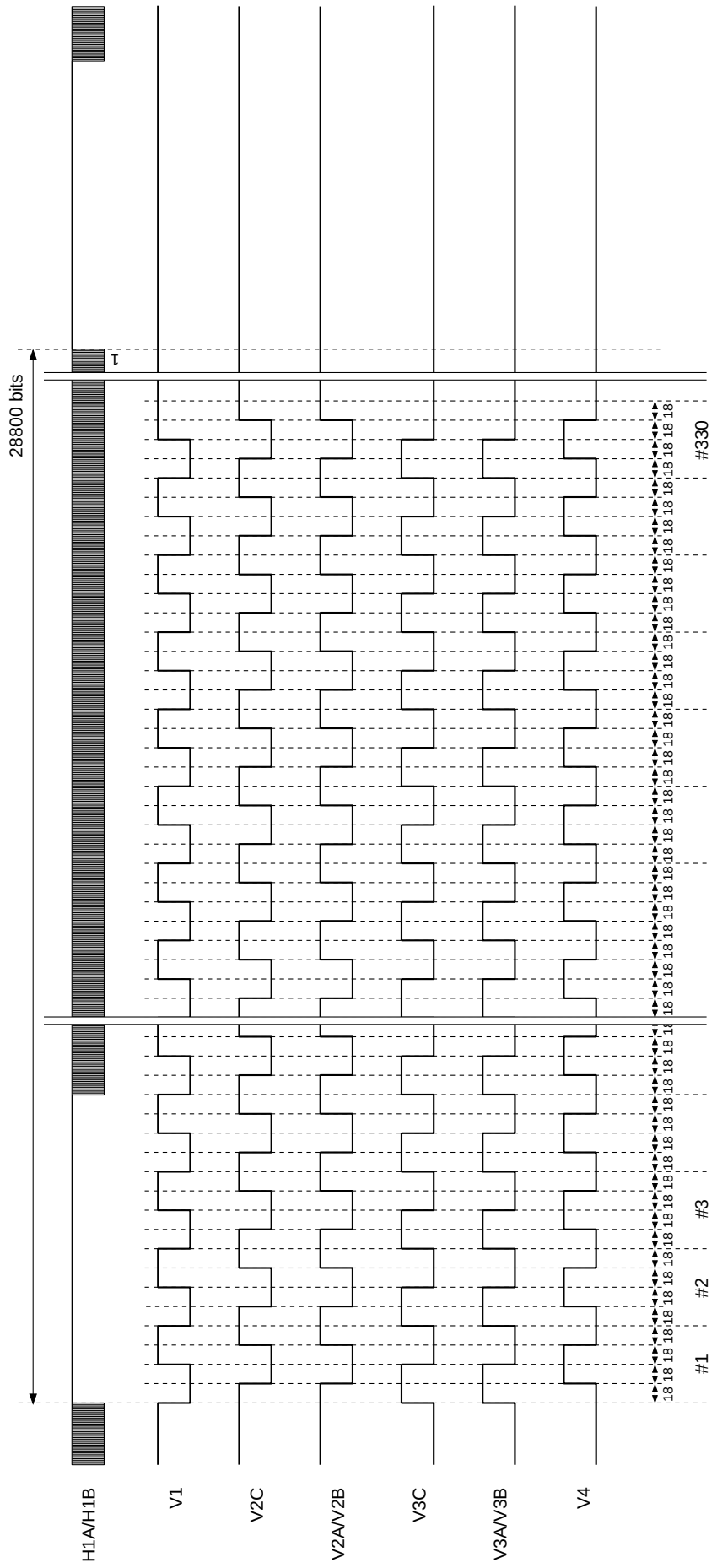
Drive Timing Chart (Vertical Sync) **Center Scan Mode (3)/(28.6MHz)**

"d" enlarged

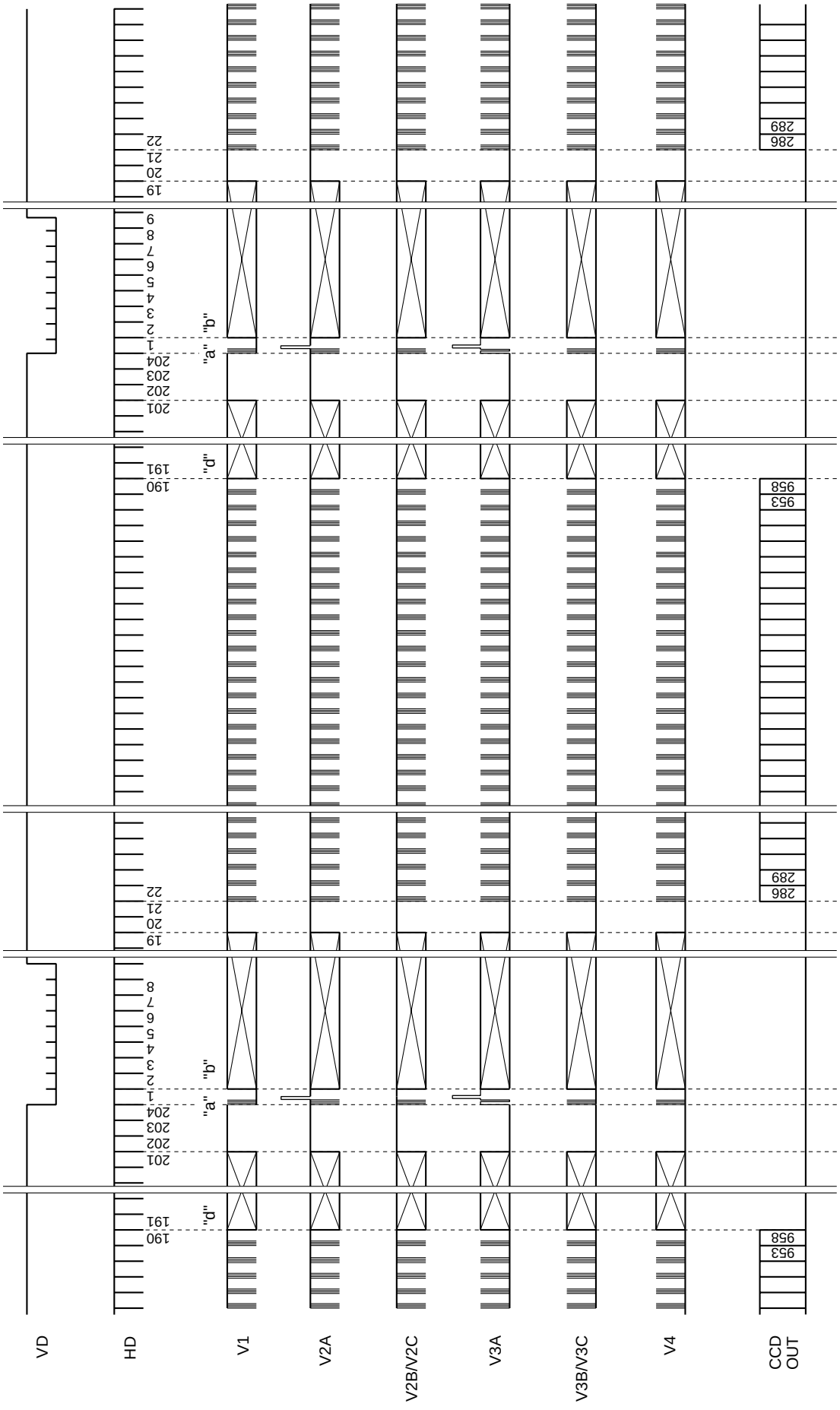


Drive Timing Chart (Vertical Sync) **Center Scan Mode (3)/(36MHz)**

"d" enlarged

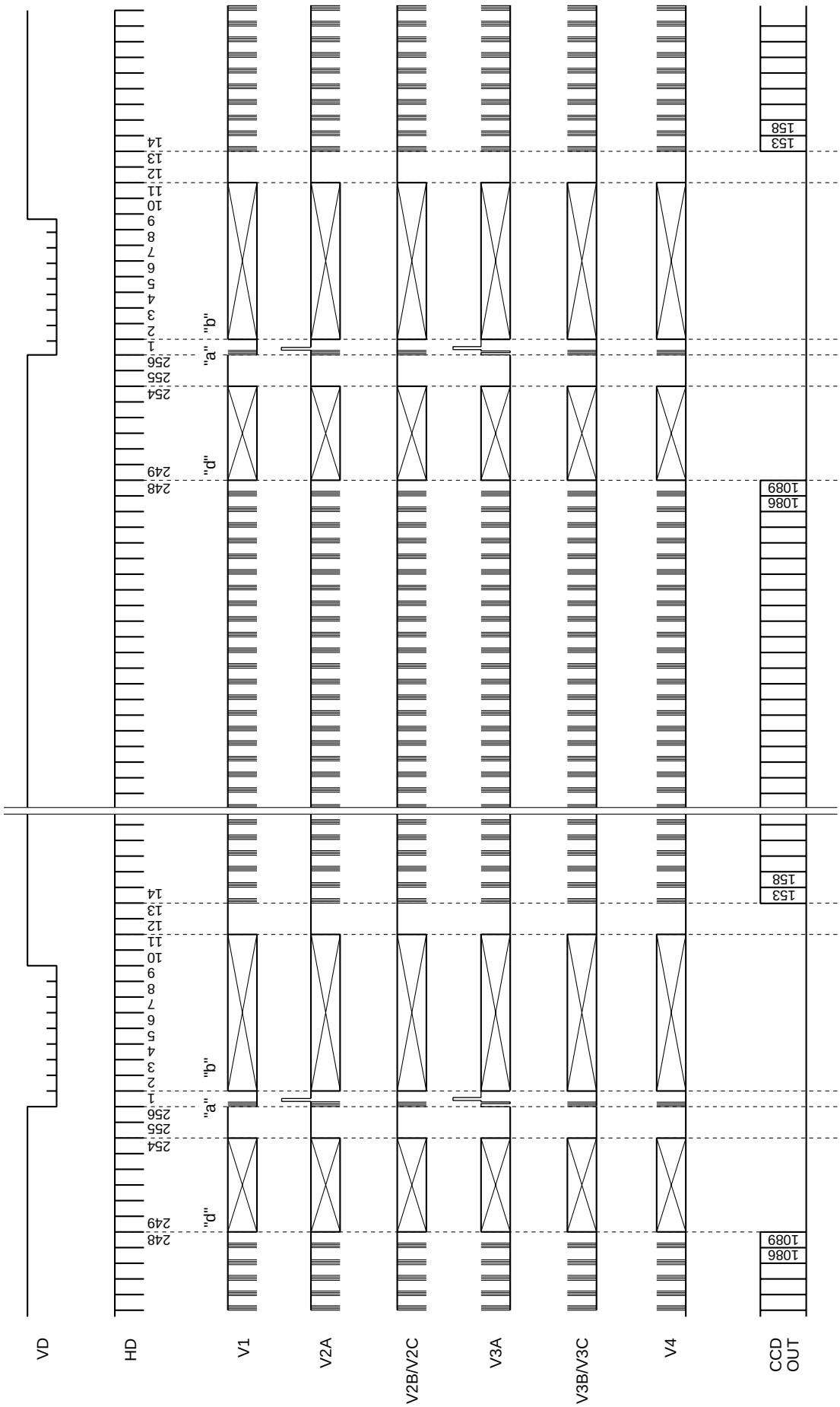


Drive Timing Chart (Vertical Sync) **AF Mode (1)/(28.6MHz)**



Note) The 203 and 204H horizontal periods are 1323clk.

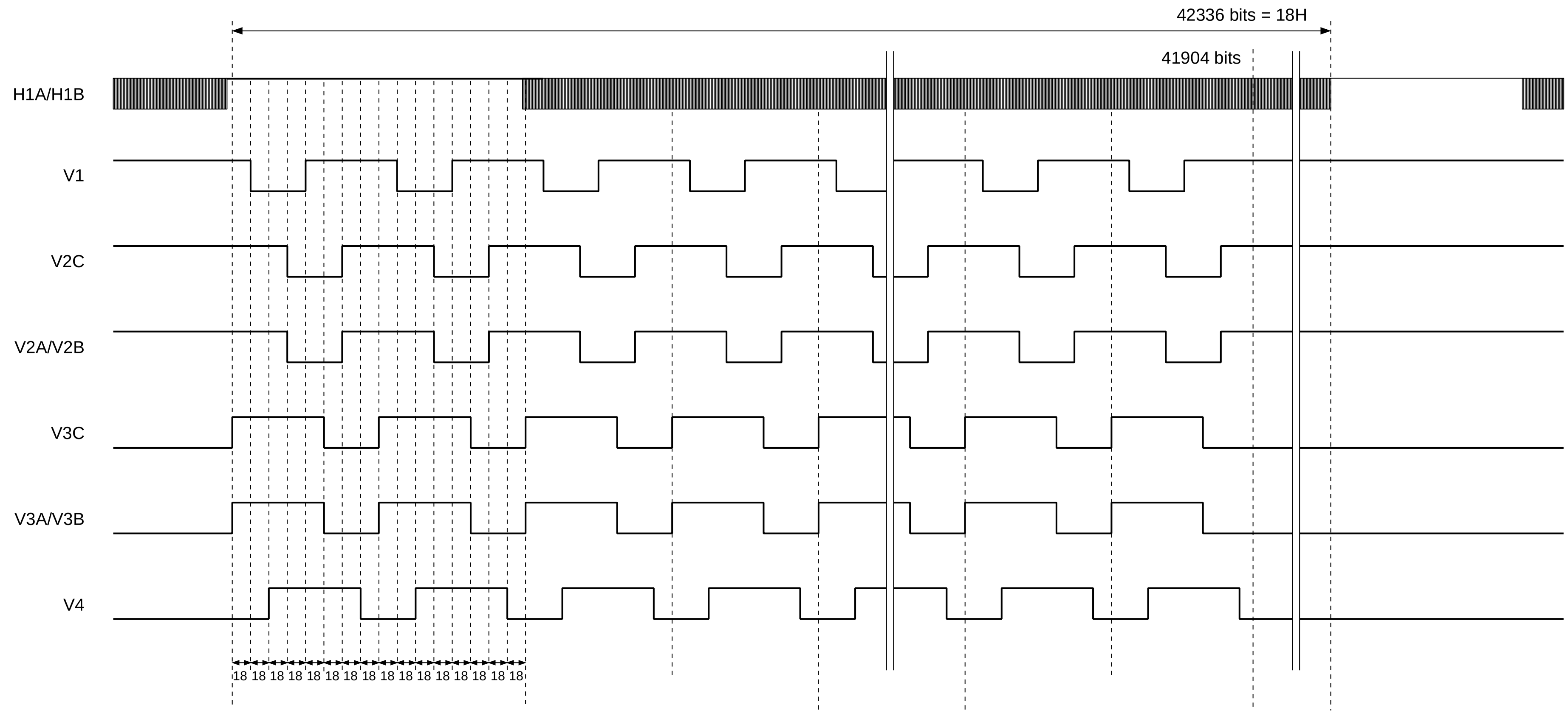
Drive Timing Chart (Vertical Sync) **AF Mode (1)/(36MHz)**



Note) The 256H horizontal period is 840clk.

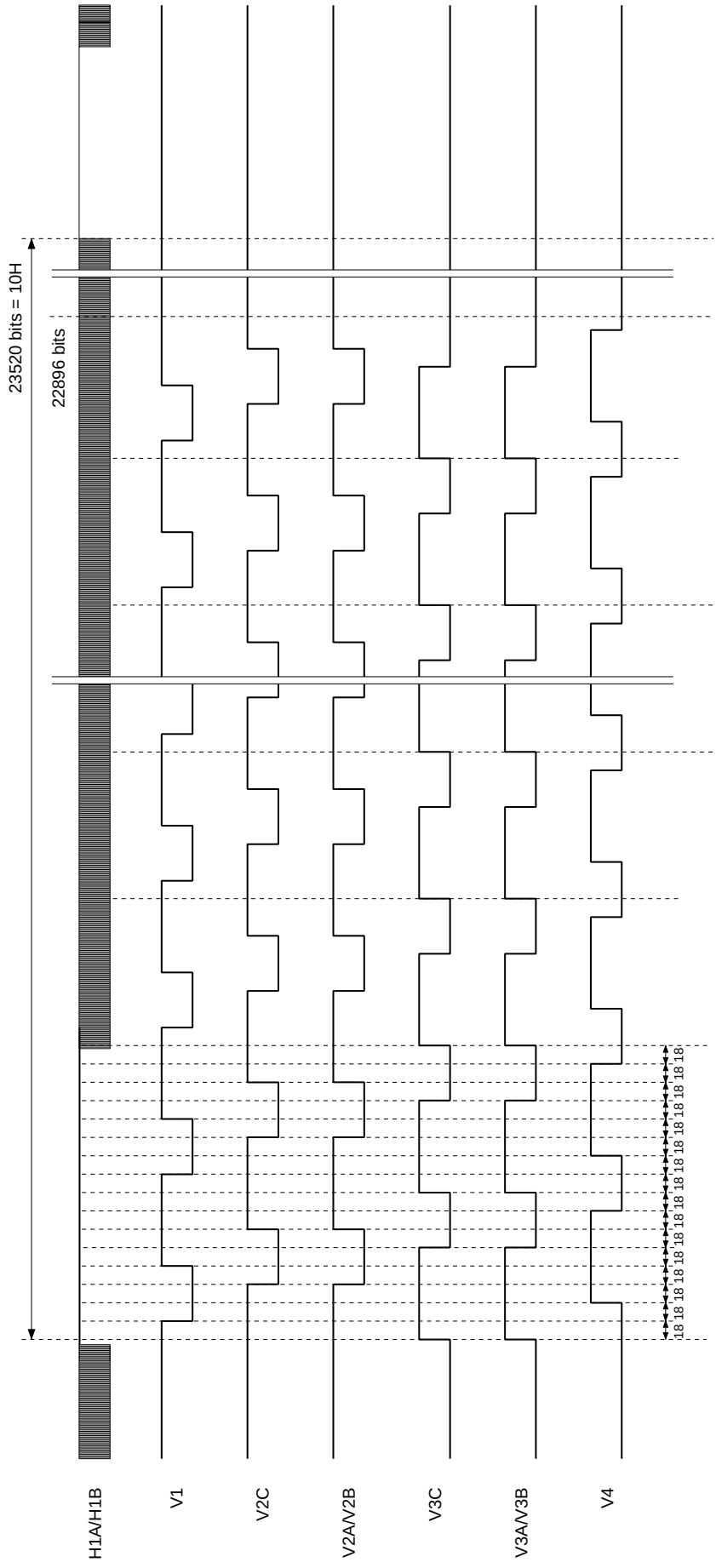
Drive Timing Chart (Vertical Sync) AF Mode (1)/(28.6MHz)

"b" enlarged



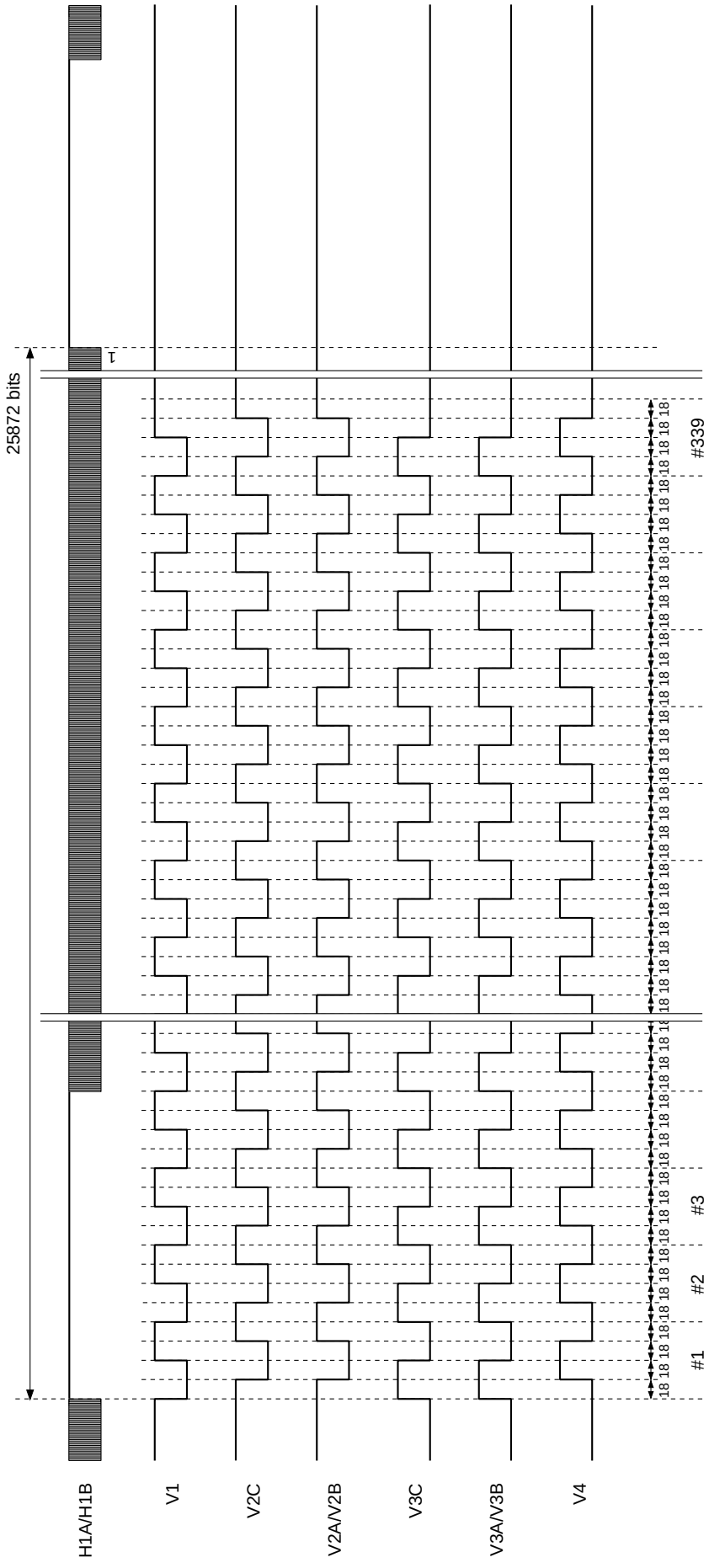
Drive Timing Chart (Vertical Sync) **AF Mode (1)/(36MHz)**

"b" enlarged



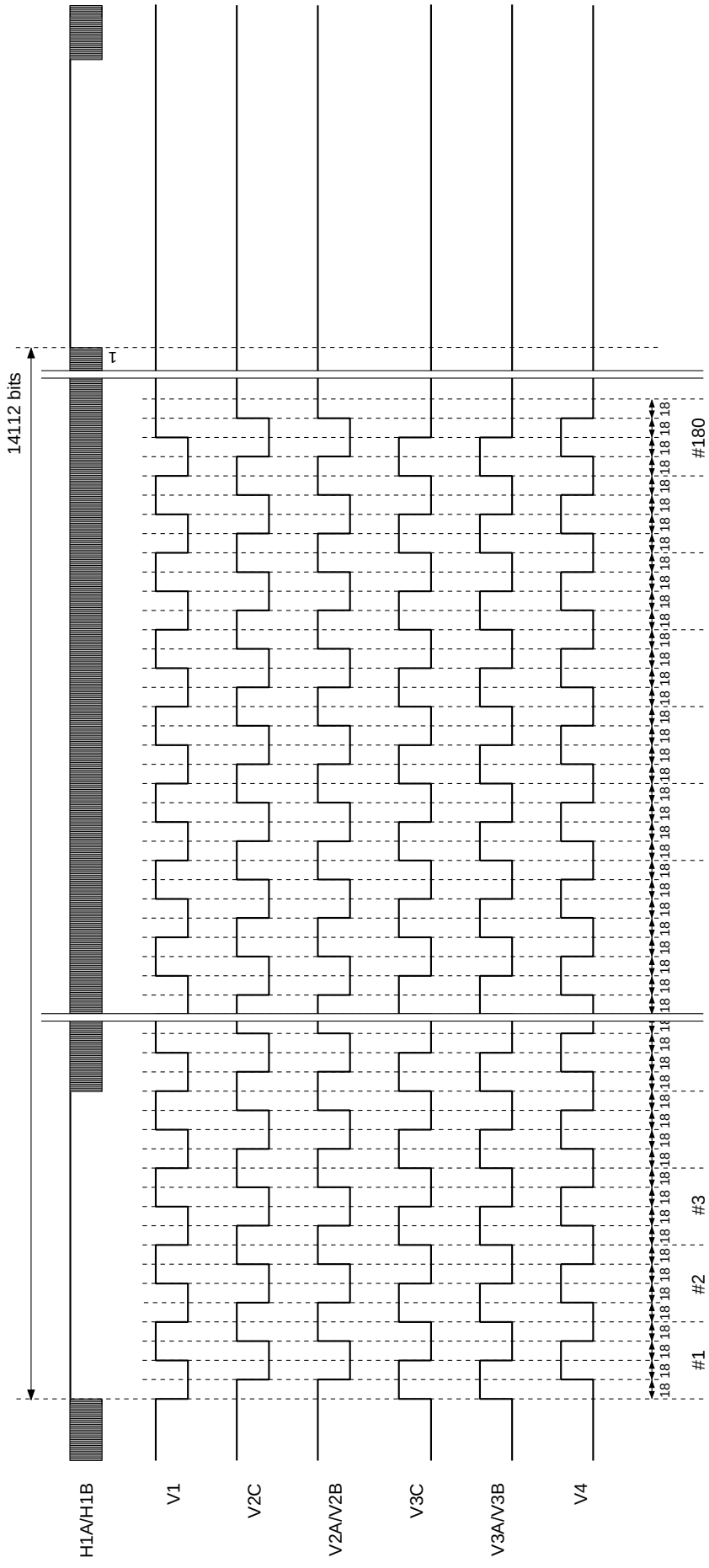
Drive Timing Chart (Vertical Sync) **AF Mode (1)/(28.6MHz)**

"d" enlarged

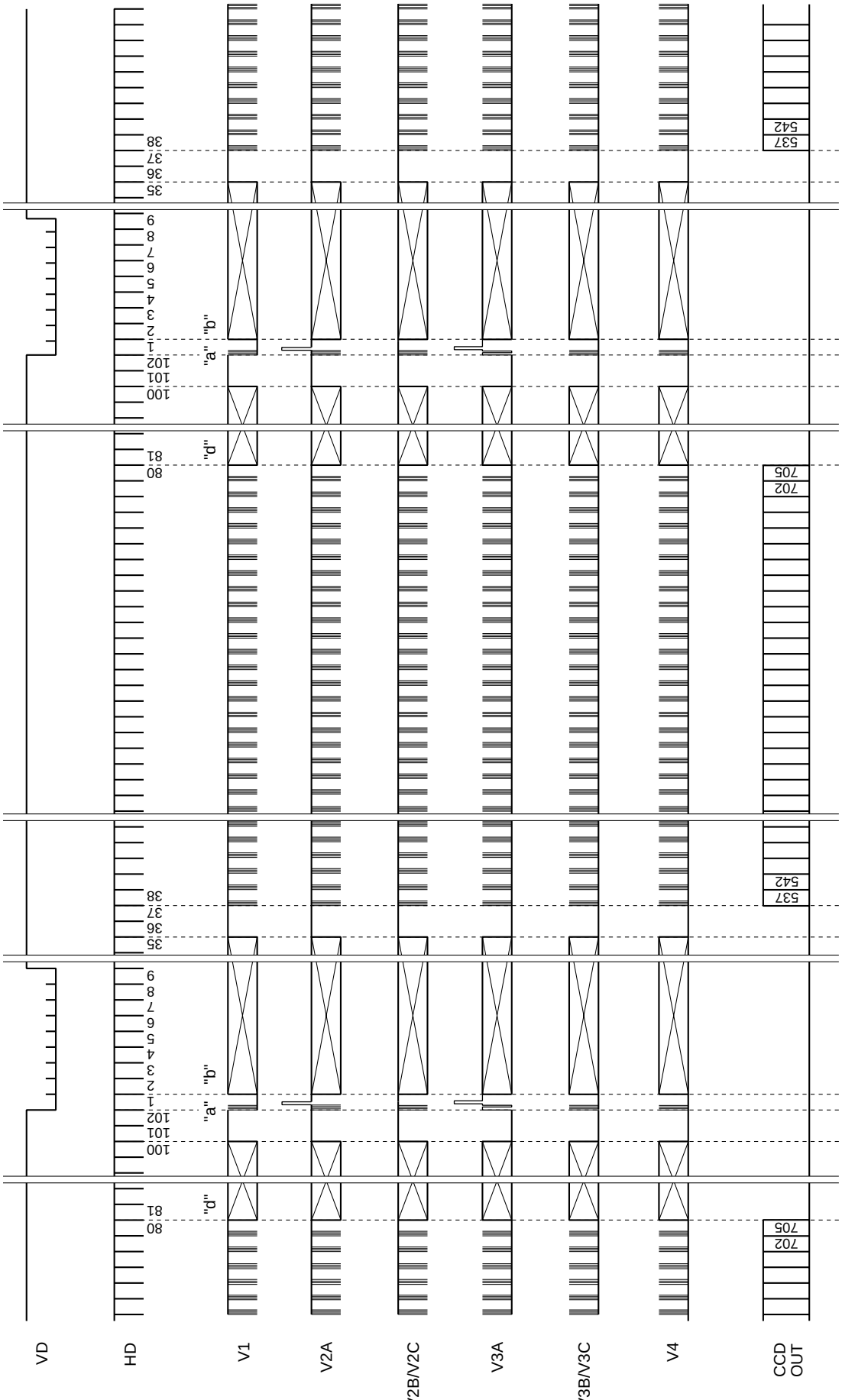


Drive Timing Chart (Vertical Sync) **AF Mode (1)/(36MHz)**

"d" enlarged

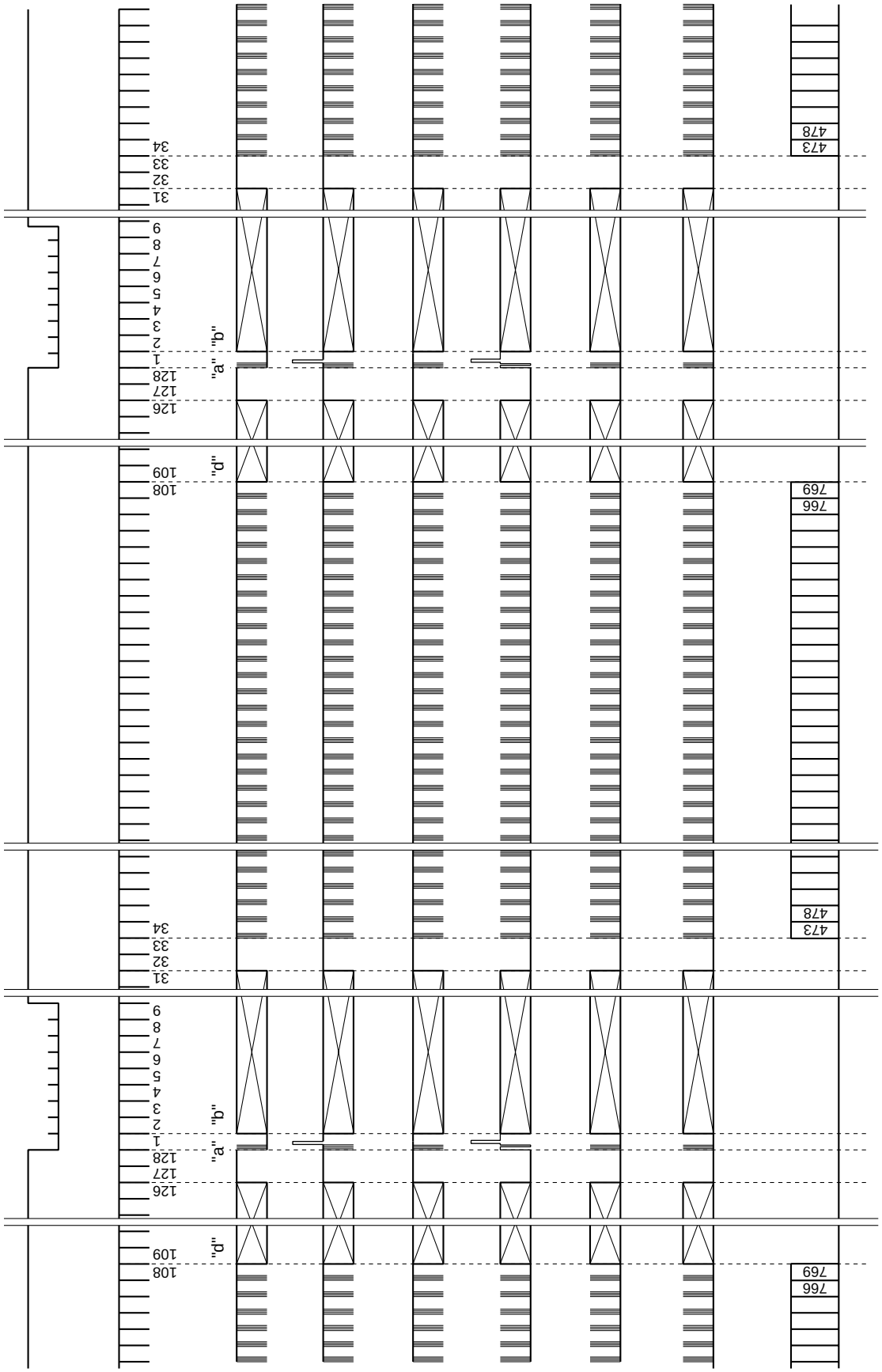


Drive Timing Chart (Vertical Sync) **AF Mode (2)/(28.6MHz)**



Note) The 102H horizontal period is 1323clk.

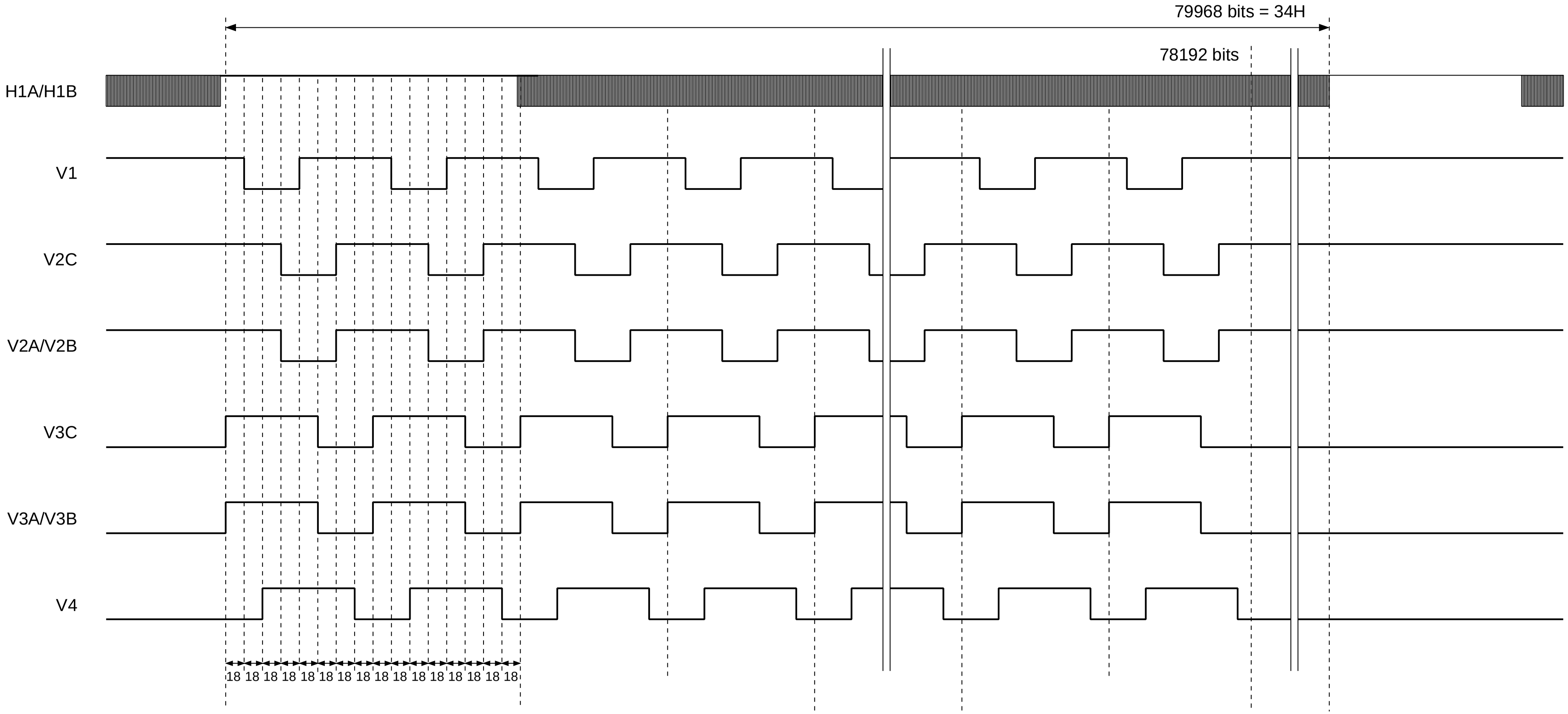
Drive Timing Chart (Vertical Sync) **AF Mode (2)/(36MHz)**



Note) The 128H horizontal period is 1596clk.

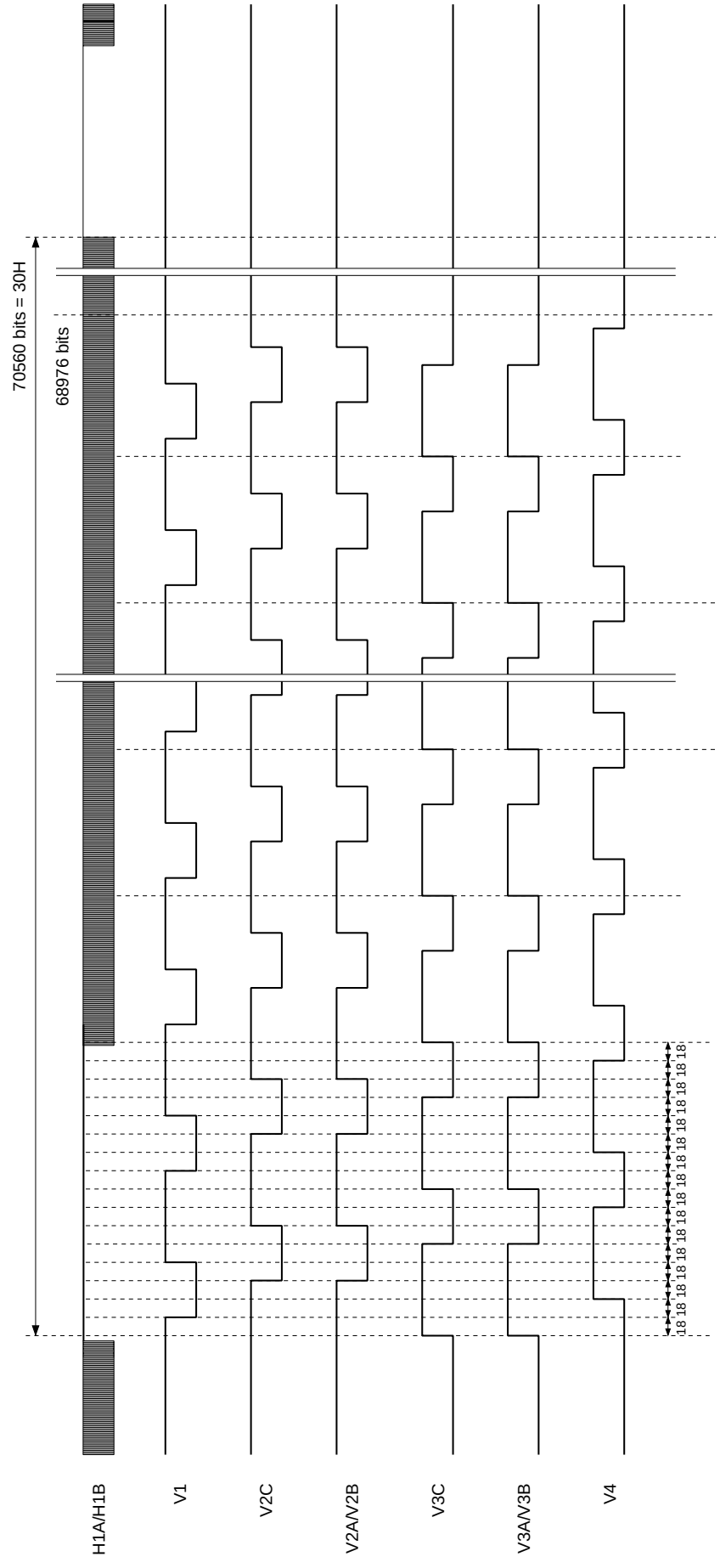
Drive Timing Chart (Vertical Sync) AF Mode (2)/(28.6MHz)

"b" enlarged



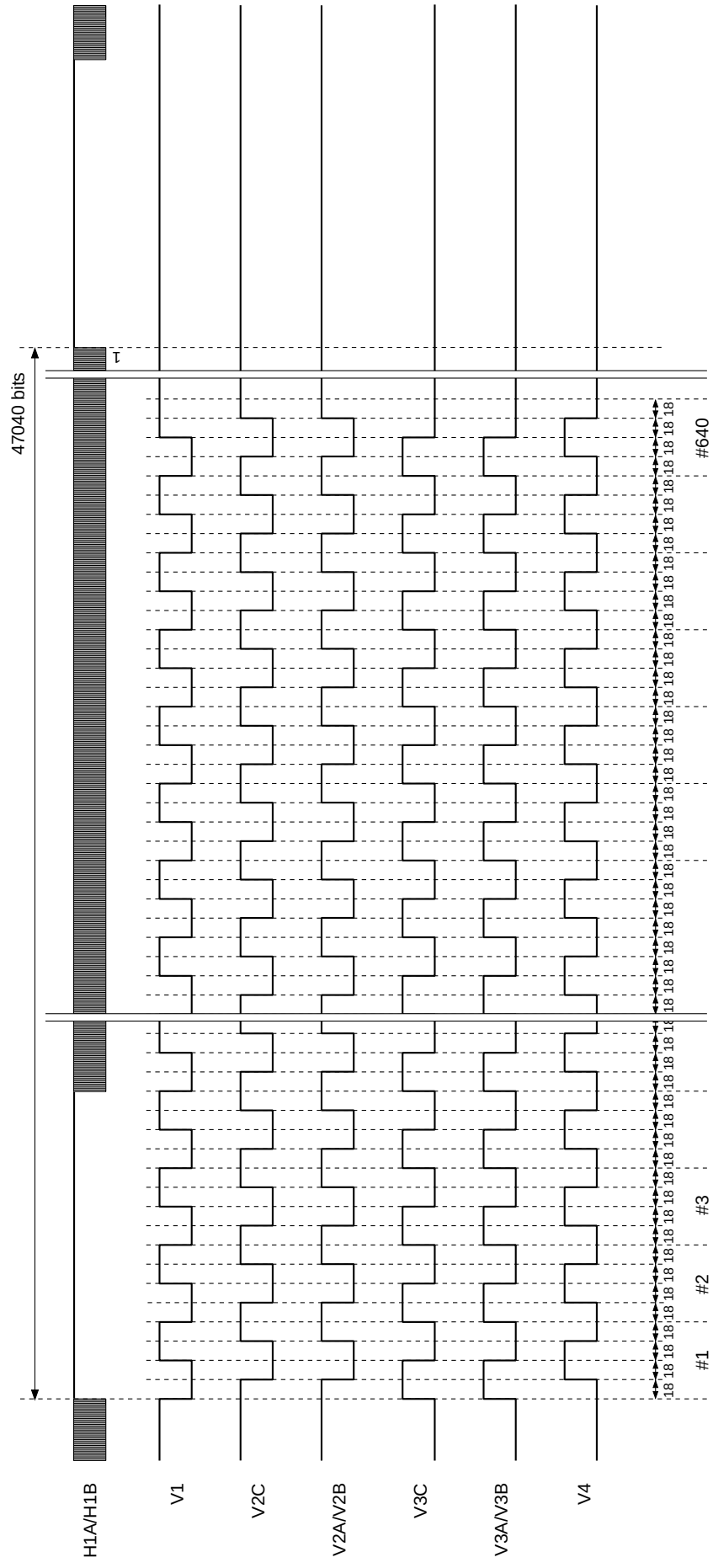
Drive Timing Chart (Vertical Sync) **AF Mode (2)/(36MHz)**

"b" enlarged



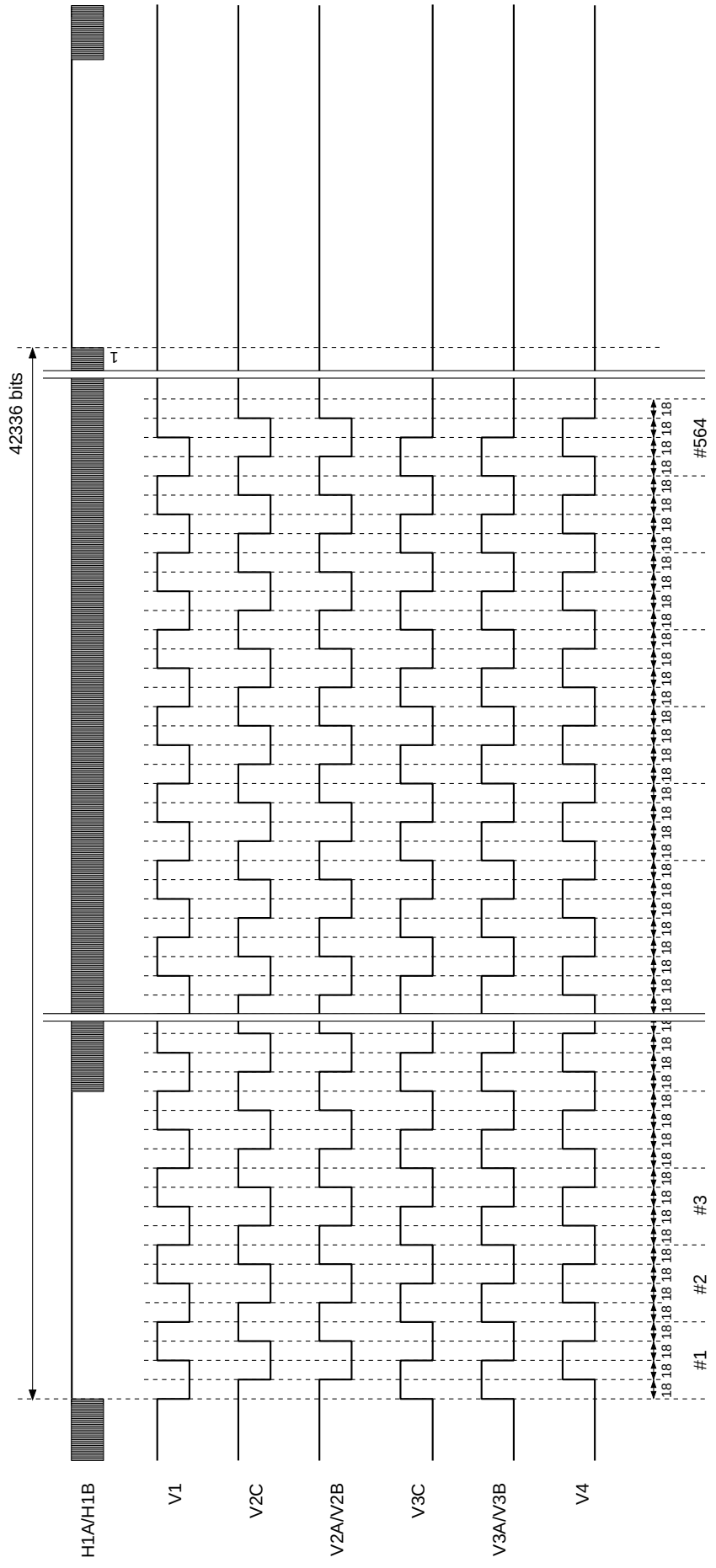
Drive Timing Chart (Vertical Sync) **AF Mode (2)/(28.6MHz)**

"d" enlarged

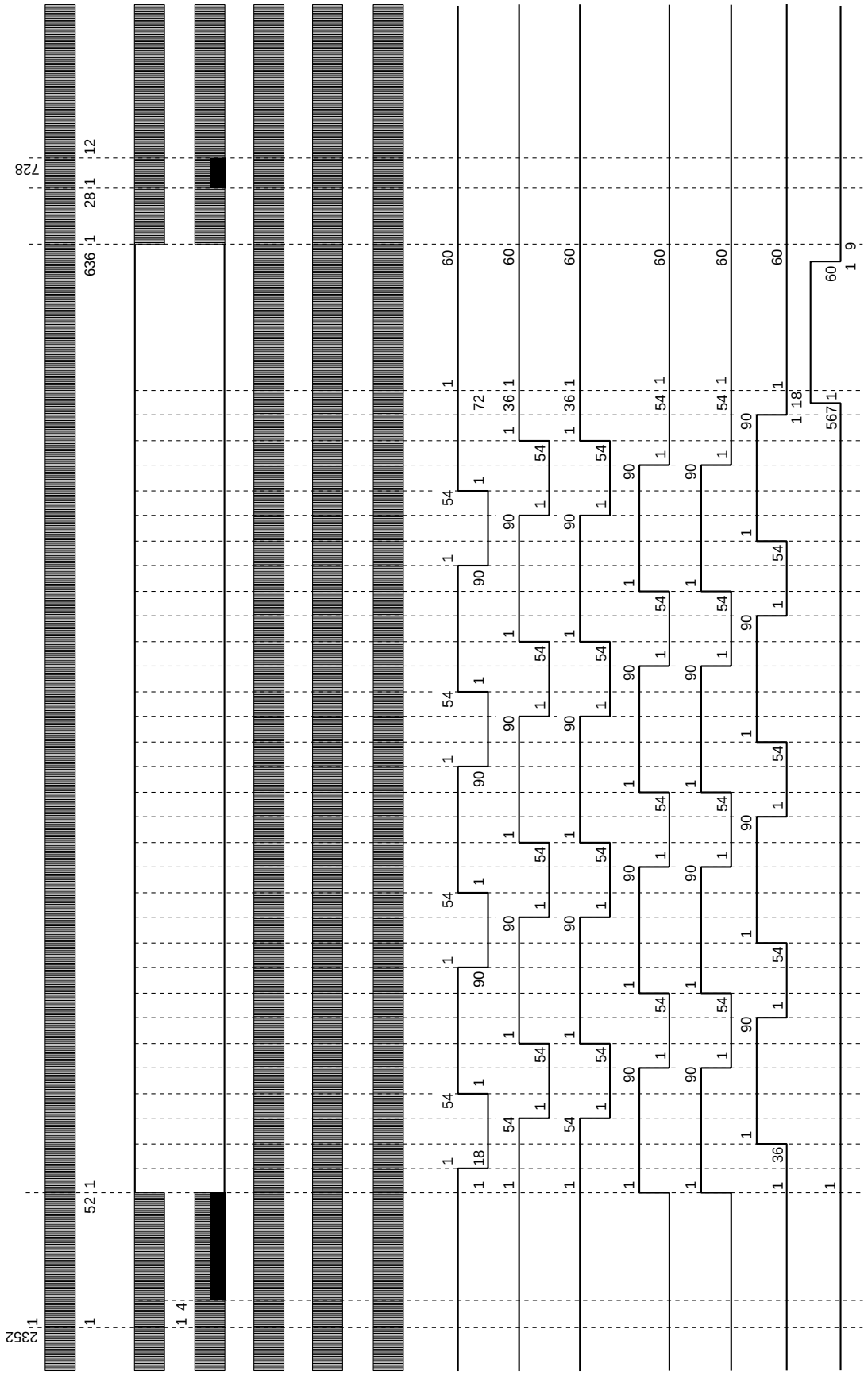


Drive Timing Chart (Vertical Sync) **AF Mode (2)/(36MHz)**

"d" enlarged

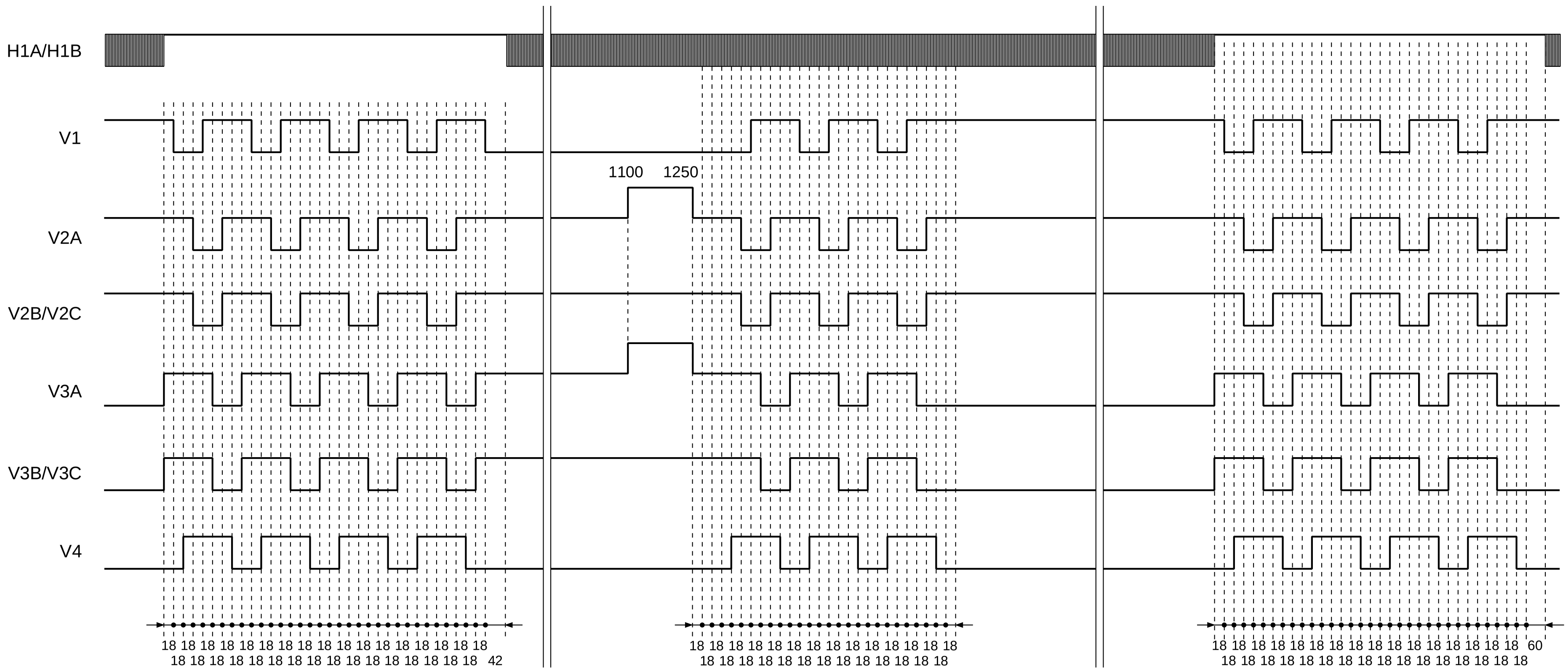


Drive Timing Chart (Horizontal Sync) AF Modes (1) and (2)



Drive Timing Chart (Vertical Sync) AF Modes (1) and (2)

"a" enlarged



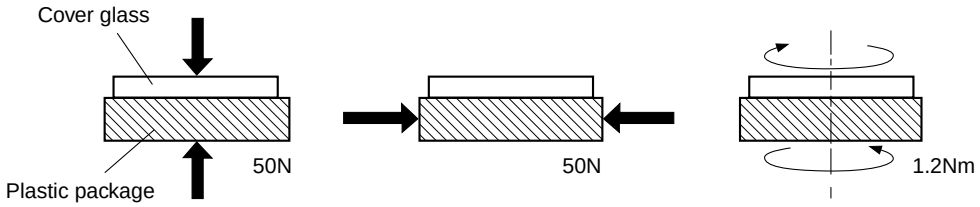
Notes of Handling

1) Static charge prevention
   CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.
   a) Either handle bare handed or use non-chargeable gloves, clothes or material.
      Also use conductive shoes.
   b) When handling directly use an earth band.
   c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
   d) Ionized air is recommended for discharge when handling CCD image sensors.
   e) For the shipment of mounted substrates, use boxes treated for the prevention of static charges.

2) Soldering
   a) Make sure the package temperature does not exceed 80°C.
   b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a ground 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
   c) To dismount an image sensor, do not use a solder suction equipment. When using an electric desoldering tool, use a thermal controller of the zero-cross On/Off type and connect it to ground.

3) Dust and dirt protection
   Image sensors are packed and delivered by taking care of protecting its glass plates from harmful dust and dirt. Clean glass plates with the following operations as required, and use them.
   a) Perform all assembly operations in a clean room (class 1000 or less).
   b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
   c) Clean with a cotton bud and ethyl alcohol if grease stained. Be careful not to scratch the glass.
   d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
   e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Installing (attaching)
   a) Remain within the following limits when applying a static load to the package. Do not apply any load more than 0.7mm inside the outer perimeter of the glass portion, and do not apply any load or impact to limited portions. (This may cause cracks in the package.)

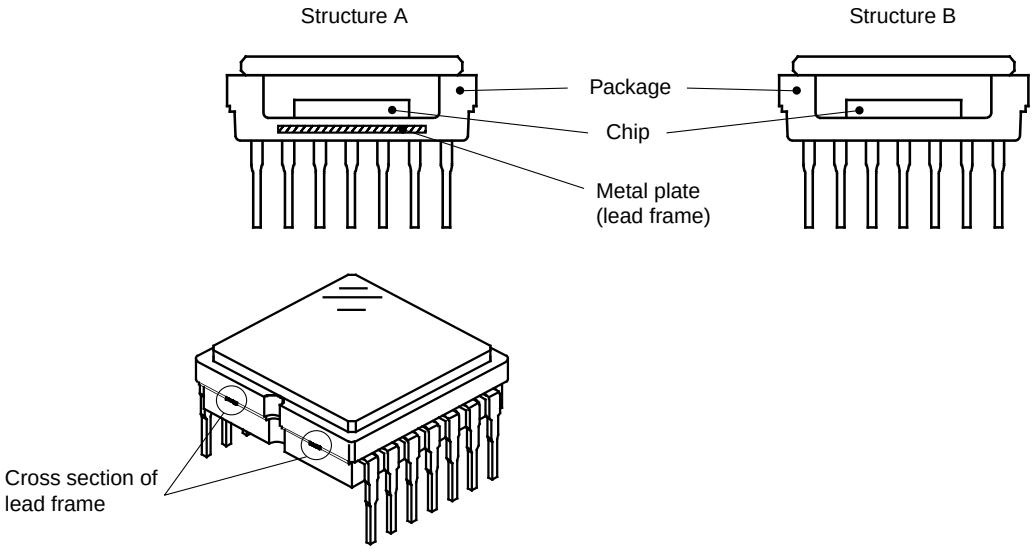


Compressive strength **Torsional strength**

   b) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.

c) The adhesive may cause the marking on the rear surface to disappear, especially in case the regulated voltage value is indicated on the rear surface. Therefore, the adhesive should not be applied to this area, and indicated values should be transferred to other locations as a precaution.
d) The notch of the package is used for directional index, and that can not be used for reference of fixing. In addition, the cover glass and seal resin may overlap with the notch of the package.
e) If the leads are bent repeatedly and metal, etc., clash or rub against the package, the dust may be generated by the fragments of resin.
f) Acrylate anaerobic adhesives are generally used to attach CCD image sensors. In addition, cyano-acrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives. (reference)

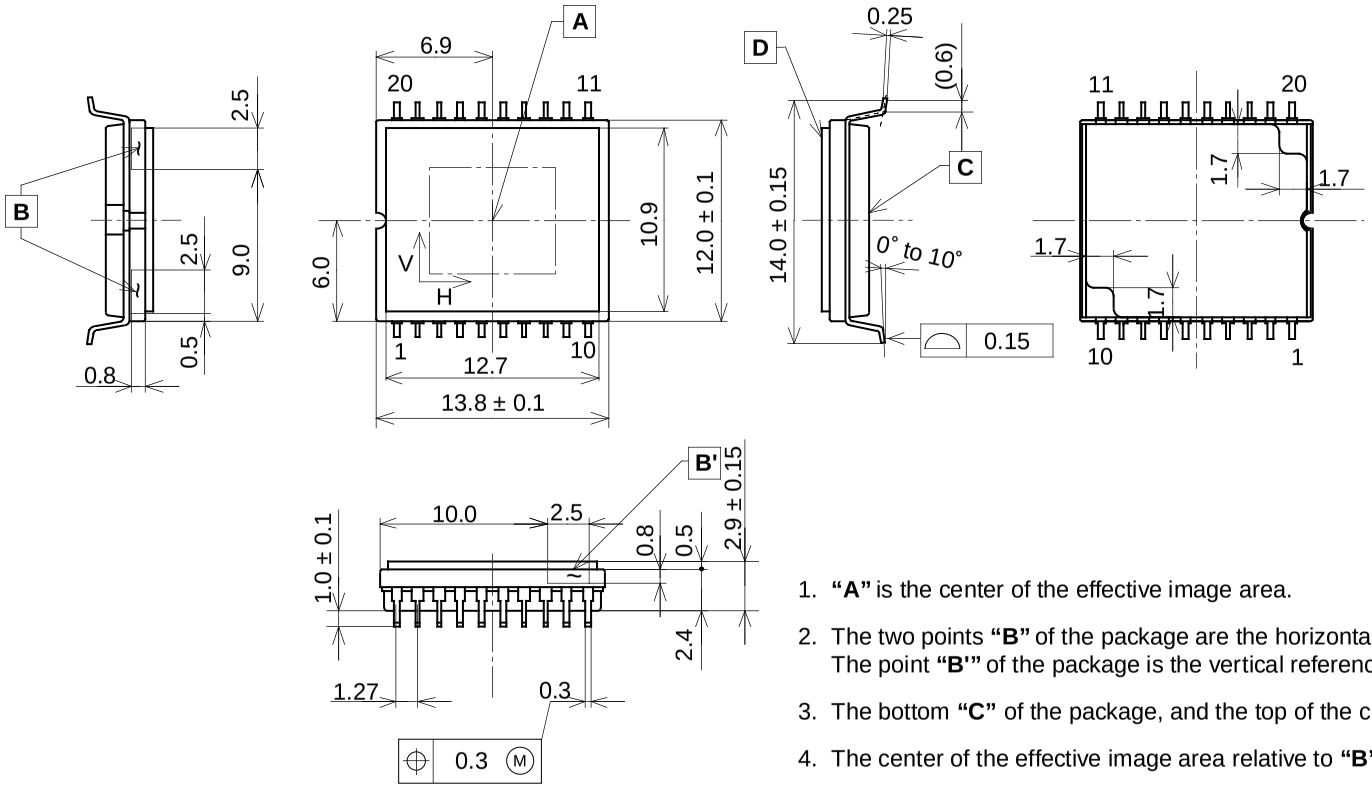
5) Others
a) Do not expose to strong light (sun rays) for long periods, as color filters will be discolored. When high luminous objects are imaged with the exposure level controlled by the electronic iris, the luminance of the image-plane may become excessive and discoloring of the color filter will possibly be accelerated. In such a case, it is advisable that taking-lens with the automatic-iris and closing of the shutter during the power-off mode should be properly arranged. For continuous using under cruel condition exceeding the normal using condition, consult our company.
b) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.
c) Brown stains may be seen on the bottom or side of the package. But this does not affect the CCD characteristics.
d) This package has 2 kinds of internal structure. However, their package outline, optical size, and strength are the same.



The cross section of lead frame can be seen on the side of the package for structure A.

Package Outline Unit: mm

20 pin SOP



PACKAGE STRUCTURE

PACKAGE MATERIAL	Plastic
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.95g
DRAWING NUMBER	AS-B7-03(E)

1. **"A"** is the center of the effective image area.
2. The two points **"B"** of the package are the horizontal reference.
   The point **"B'"** of the package is the vertical reference.
3. The bottom **"C"** of the package, and the top of the cover glass **"D"** are the height reference.
4. The center of the effective image area relative to **"B"** and **"B'"** is (H, V) = (6.9, 6.0) ± 0.075mm.
5. The rotation angle of the effective image area relative to H and V is ±0.7°.
6. The height from the bottom **"C"** to the effective image area is 1.41 ± 0.10mm.
   The height from the top of the cover glass **"D"** to the effective image area is 1.49 ± 0.15mm.
7. The tilt of the effective image area relative to the bottom **"C"** is less than 50µm.
   The tilt of the effective image area relative to the top **"D"** of the cover glass is less than 50µm.
8. The thickness of the cover glass is 0.5mm, and the refractive index is 1.5.
9. The notches on the bottom of the package are used only for directional index, they must not be used for reference of fixing.