

HYS64T256020HU-[3/3S]-A  
HYS72T256020HU-[3/3S]-A  
HYS64T256020HU-[3.7/5]-A  
HYS72T256020HU-[3.7/5]-A

*240-Pin Unbuffered DDR2 SDRAM Modules  
UDIMM  
DDR2 SDRAM  
RoHS Compliant*



## Internet Data Sheet

*Rev. 1.32*

HYS[64/72]T256xxxHU-[3/.../5]-A  
Unbuffered DDR2 SDRAM Modules

<b>HYS64T256020HU-[3/3S]-A, HYS72T256020HU-[3/3S]-A, HYS64T256020HU-[3.7/5]-A, HYS72T256020HU-[3.7/5]-A</b>	
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<b>5</b>	In Ordering Information Table: Corrected " <b>Compliance Code</b> ", " <b>PC2-5300</b> " for -3S; corrected " <b>Footnote</b> ".
<b>16</b>	Corrected Cross-reference to Table 14.
<b>58</b>	Updated Product Type Nomenclature
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<b>5</b>	Added PC2-5300 product types
<b>3</b>	Added performance tables
<b>18</b>	Added speed grade definitions
<b>21</b>	Updated AC Timing parameter
<b>41</b>	Added tables for $I_{DD}$ test conditions
<b>33</b>	Updated $I_{DD}$ currents
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# 1 Overview

This chapter gives an overview of the 240-Pin Unbuffered DDR2 SDRAM Modules product family and describes its main characteristics.

## 1.1 Features

- 240-Pin PC2-5300, PC2-4200 and PC2-DDR2 SDRAM memory modules
- 256M × 64 non-ECC and 256M × 72 ECC module organization, and 128M × 8 chip organization
- 2GByte modules built with 1-Gbit DDR2 SDRAMs in P-TFBGA-68 chipsize packages
- All Speed grades faster than DDR2-400 comply with DDR2-400 timing specifications.
- Standard Double-Data-Rate-Two Synchronous DRAMs (DDR2 SDRAM) with a single + 1.8 V (± 0.1 V) power supply
- Programmable CAS Latencies (3, 4 and 5), Burst Length (8 & 4) and Burst Type
- Auto Refresh (CBR) and Self Refresh
- Average Refresh Period 7.8 μs at a  $T_{CASE}$  lower than 85°C, 3.9μs between 85°C and 95°C.
- All inputs and outputs SSTL\_1.8 compatible
- Off-Chip Driver Impedance Adjustment (OCD) and On-Die Termination (ODT)
- Serial Presence Detect with E<sup>2</sup>PROM
- Dimensions (nominal): 30 mm high, 133.35 mm wide
- Based on standard reference layouts Raw Card “B”, “E” and “G”
- RoHS compliant products<sup>1)</sup>

### Performance tables

- **Table 1** “Performance table for -3(S)” on Page 3
- **Table 2** “Performance table for -3.7” on Page 4
- **Table 3** “Performance table for -5” on Page 4

**TABLE 1**  
Performance table for -3(S)

Product Type Speed Code			-3	-3S	Unit
Speed Grade			PC2-5300 4-4-4	PC2-5300 5-5-5	—
Max. Clock Frequency	@CL5	$f_{CK5}$	333	333	MHz
	@CL4	$f_{CK4}$	333	266	MHz
	@CL3	$f_{CK3}$	200	200	MHz
Min. RAS-CAS-Delay		$t_{RCD}$	12	15	ns
Min. Row Precharge Time		$t_{RP}$	12	15	ns
Min. Row Active Time		$t_{RAS}$	45	45	ns
Min. Row Cycle Time		$t_{RC}$	57	60	ns

1) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.

HYS[64/72]T256xxxHU-[3/.../5]-A  
Unbuffered DDR2 SDRAM Modules**TABLE 2**  
Performance table for -3.7

Product Type Speed Code			-3.7	Unit
Speed Grade			PC2-4200 4-4-4	—
Max. Clock Frequency	@CL5	$f_{CK5}$	266	MHz
	@CL4	$f_{CK4}$	266	MHz
	@CL3	$f_{CK3}$	200	MHz
Min. RAS-CAS-Delay		$t_{RCD}$	15	ns
Min. Row Precharge Time		$t_{RP}$	15	ns
Min. Row Active Time		$t_{RAS}$	45	ns
Min. Row Cycle Time		$t_{RC}$	60	ns

**TABLE 3**  
Performance table for -5

Product Type Speed Code			-5	Unit
Speed Grade			PC2-3200 3-3-3	—
max. Clock Frequency	@CL5	$f_{CK5}$	200	MHz
	@CL4	$f_{CK4}$	200	MHz
	@CL3	$f_{CK3}$	200	MHz
min. RAS-CAS-Delay		$t_{RCD}$	15	ns
min. Row Precharge Time		$t_{RP}$	15	ns
min. Row Active Time		$t_{RAS}$	40	ns
min. Row Cycle Time		$t_{RC}$	55	ns



HYS[64/72]T256xxxHU-[3/.../5]-A  
Unbuffered DDR2 SDRAM Modules

## 1.2 Description

The Qimonda HYS[64/72]T256xxxHU-[3/.../5]-A module family are unbuffered DIMM modules "UDIMMs with 30,0 mm height based on DDR2 technology. DIMMs are available as non-ECC modules in 256M × 64 (2 GB), and as ECC modules in 256M × 72 (2 GB) organization and density, intended for mounting into 240-pin connector sockets.

The memory array is designed with 1-Gbit Double-Data-Rate-Two (DDR2) Synchronous DRAMs. Decoupling capacitors

are mounted on the PCB board. The DIMMs feature serial presence detect based on a serial E<sup>2</sup>PROM device using the 2-pin I<sup>2</sup>C protocol. The first 128 bytes are programmed with configuration data and are write protected; the second 128 bytes are available to the customer.



**TABLE 4**  
Ordering Information for RoHS Compliant Products

Product Type <sup>1)</sup>	Compliance Code <sup>2)</sup>	Description	SDRAM Technology
<b>PC2-5300</b>			
HYS64T256020HU-3-A	2GB 2R×8 PC2-5300U-444-11-E0	2 Ranks, Non-ECC	1 Gbit (×8)
HYS72T256020HU-3-A	2GB 2R×8 PC2-5300U-444-11-G0	2 Ranks, ECC	1 Gbit (×8)
<b>PC2-5300</b>			
HYS64T256020HU-3S-A	2GB 2R×8 PC2-5300U-555-12-E0	2 Ranks, Non-ECC	1 Gbit (×8)
HYS72T256020HU-3S-A	2GB 2R×8 PC2-5300U-555-12-G0	2 Ranks, ECC	1 Gbit (×8)
<b>PC2-4200</b>			
HYS64T256020HU-3.7-A	2GB 2R×8 PC2-4200U-444-11-B1	2 Ranks, Non-ECC	1 Gbit (×8)
HYS72T256020HU-3.7-A	2GB 2R×8 PC2-4200U-444-11-B1	2 Ranks, ECC	1 Gbit (×8)
<b>PC2-3200</b>			
HYS64T256020HU-5-A	2GB 2R×8 PC2-3200U-333-11-B1	2 Ranks, Non-ECC	1 Gbit (×8)
HYS72T256020HU-5-A	2GB 2R×8 PC2-3200U-333-11-B1	2 Ranks, ECC	1 Gbit (×8)

- 1) All part numbers end with a place code, designating the silicon die revision. Example: HYS64T256020HU-3.7-A, indicating Rev. "A" dies are used for DDR2 SDRAM components. For all Qimonda DDR2 module and component nomenclature see [Chapter 6](#) of this data sheet.
- 2) The Compliance Code is printed on the module label and describes the speed grade, for example "PC2-4200U-444-11-B1", where 4200U means Unbuffered DIMM modules with 4.26 GB/sec Module Bandwidth and "444-11" means Column Address Strobe (CAS) latency = 4, Row Column Delay (RCD) latency = 4 and Row Precharge (RP) latency = 4 using the latest JEDEC SPD Revision 1.1 and produced on the Raw Card "B".

HYS[64/72]T256xxxHU-[3/.../5]-A  
Unbuffered DDR2 SDRAM Modules**TABLE 5**  
Address Format

DIMM Density	Module Organization	Memory Ranks	ECC/ Non-ECC	# of SDRAMs	# of row/bank/column bits	Raw Card
2 GByte	256M ×64	2	Non-ECC	16	14/3/10	E,B
2 GByte	256M ×72	2	ECC	18	14/3/10	G,B

**TABLE 6**  
Components on Modules

Product Type <sup>1)</sup>	DRAM Components <sup>1)</sup>	DRAM Density	DRAM Organisation	Note
HYS64T256020HU	HYB18T1G800AF	1 Gbit	128M × 8	2)
HYS72T256020HU	HYB18T1G800AF	1 Gbit	128M × 8	2)

1) Green Product

2) For a detailed description of all functionalities of the DRAM components on these modules see the component data sheet.



## 2 Pin Configurations

### 2.1 Pin Configuration

The pin configuration of the Unbuffered DDR2 SDRAM DIMM is listed by function in **Table 7** (240 pins). The abbreviations used in columns Pin and Buffer Type are explained in **Table 8** and **Table 9** respectively. The pin numbering is depicted in **Figure 1** for non-ECC modules ( $\times 64$ ) and **Figure 2** for ECC modules ( $\times 72$ ).

**TABLE 7**  
Pin Configuration of UDIMM

Ball No.	Name	Pin Type	Buffer Type	Function
<b>Clock Signals</b>				
185	CK0	I	SSTL	<b>Clock Signals 2:0, Complement Clock Signals 2:0</b>
137	CK1	I	SSTL	
220	CK2	I	SSTL	
186	CK0	I	SSTL	
138	CK1	I	SSTL	
221	CK2	I	SSTL	
52	CKE0	I	SSTL	<b>Clock Enable Rank 1:0</b>
171	CKE1	I	SSTL	<i>Note: 2 Ranks module</i>
	NC	NC	—	<b>Not Connected</b> <i>Note: 1 Rank module</i>
<b>Control Signals</b>				
193	S0#	I	SSTL	<b>Chip Select Rank 1:0</b>
76	S1#	I	SSTL	<i>Note: 2 Ranks module</i>
	NC	NC	—	<b>Not Connected</b> <i>Note: 1 Rank module</i>
192	RAS	I	SSTL	<b>Row Address Strobe</b>
74	$\overline{\text{CAS}}$	I	SSTL	<b>Column Address Strobe</b>
73	$\overline{\text{WE}}$	I	SSTL	<b>Write Enable</b>
<b>Address Signals</b>				
71	BA0	I	SSTL	<b>Bank Address Bus 1:0</b>
190	BA1	I	SSTL	
54	BA2	I	SSTL	<b>Bank Address Bus 2</b>
	NC	NC	—	<b>Not Connected</b>



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Unbuffered DDR2 SDRAM Modules

Ball No.	Name	Pin Type	Buffer Type	Function
188	A0	I	SSTL	<b>Address Bus 12:0</b>
183	A1	I	SSTL	
63	A2	I	SSTL	
182	A3	I	SSTL	
61	A4	I	SSTL	
60	A5	I	SSTL	
180	A6	I	SSTL	
58	A7	I	SSTL	
179	A8	I	SSTL	
177	A9	I	SSTL	
70	A10	I	SSTL	
	AP	I	SSTL	
57	A11	I	SSTL	
176	A12	I	SSTL	
196	A13	I	SSTL	<b>Address Signal 13</b> <i>Note: 1 Gbit based module and 512M x4/x8</i>
	NC	NC	—	<b>Not Connected</b> <i>Note: Module based on 1 Gbit x16</i> <i>Module based on 512 Mbit x16 or smaller</i>
174	A14	I	SSTL	<b>Address Signal 14</b> <i>Note: Modules based on 2 Gbit</i>
	NC	NC	—	<b>Not Connected</b> <i>Note: Modules based on 1 Gbit or smaller</i>
<b>Data Signals</b>				
3	DQ0	I/O	SSTL	<b>Data Bus 63:0</b>
4	DQ1	I/O	SSTL	
9	DQ2	I/O	SSTL	
10	DQ3	I/O	SSTL	
122	DQ4	I/O	SSTL	
123	DQ5	I/O	SSTL	
128	DQ6	I/O	SSTL	
129	DQ7	I/O	SSTL	





HYS[64/72]T256xxxHU-[3/.../5]-A  
Unbuffered DDR2 SDRAM Modules

Ball No.	Name	Pin Type	Buffer Type	Function
12	DQ8	I/O	SSTL	<b>Data Bus 63:0</b>
13	DQ9	I/O	SSTL	
21	DQ10	I/O	SSTL	
22	DQ11	I/O	SSTL	
131	DQ12	I/O	SSTL	
132	DQ13	I/O	SSTL	
140	DQ14	I/O	SSTL	
141	DQ15	I/O	SSTL	
24	DQ16	I/O	SSTL	
25	DQ17	I/O	SSTL	
30	DQ18	I/O	SSTL	
31	DQ19	I/O	SSTL	
143	DQ20	I/O	SSTL	
144	DQ21	I/O	SSTL	
149	DQ22	I/O	SSTL	
150	DQ23	I/O	SSTL	
33	DQ24	I/O	SSTL	
34	DQ25	I/O	SSTL	
39	DQ26	I/O	SSTL	
40	DQ27	I/O	SSTL	
152	DQ28	I/O	SSTL	
153	DQ29	I/O	SSTL	
158	DQ30	I/O	SSTL	
159	DQ31	I/O	SSTL	
80	DQ32	I/O	SSTL	
81	DQ33	I/O	SSTL	
86	DQ34	I/O	SSTL	
87	DQ35	I/O	SSTL	
199	DQ36	I/O	SSTL	
200	DQ37	I/O	SSTL	
205	DQ38	I/O	SSTL	
206	DQ39	I/O	SSTL	
89	DQ40	I/O	SSTL	
90	DQ41	I/O	SSTL	
95	DQ42	I/O	SSTL	
96	DQ43	I/O	SSTL	
208	DQ44	I/O	SSTL	
209	DQ45	I/O	SSTL	
214	DQ46	I/O	SSTL	
215	DQ47	I/O	SSTL	



HYS[64/72]T256xxxHU-[3/.../5]-A  
Unbuffered DDR2 SDRAM Modules

Ball No.	Name	Pin Type	Buffer Type	Function
98	DQ48	I/O	SSTL	<b>Data Bus 63:0</b>
99	DQ49	I/O	SSTL	
107	DQ50	I/O	SSTL	
108	DQ51	I/O	SSTL	
217	DQ52	I/O	SSTL	
218	DQ53	I/O	SSTL	
226	DQ54	I/O	SSTL	
227	DQ55	I/O	SSTL	
110	DQ56	I/O	SSTL	
111	DQ57	I/O	SSTL	
116	DQ58	I/O	SSTL	
117	DQ59	I/O	SSTL	
229	DQ60	I/O	SSTL	
230	DQ61	I/O	SSTL	
235	DQ62	I/O	SSTL	
236	DQ63	I/O	SSTL	
<b>Check Bit Signals</b>				
42	CB0	I/O	SSTL	<b>Check Bit 0</b>
	NC	NC	—	<b>Not Connected</b>
43	CB1	I/O	SSTL	<b>Check Bit 1</b>
	NC	NC	—	<b>Not Connected</b>
48	CB2	I/O	SSTL	<b>Check Bit 2</b>
	NC	NC	—	<b>Not Connected</b>
49	CB3	I/O	SSTL	<b>Check Bit 3</b>
	NC	NC	—	<b>Not Connected</b>
161	CB4	I/O	SSTL	<b>Check Bit 4</b>
	NC	NC	—	<b>Not Connected</b>
162	CB5	I/O	SSTL	<b>Check Bit 5</b>
	NC	NC	—	<b>Not Connected</b>
167	CB6	I/O	SSTL	<b>Check Bit 6</b>
	NC	NC	—	<b>Not Connected</b>
168	CB7	I/O	SSTL	<b>Check Bit 7</b>
	NC	NC	—	<b>Not Connected</b>



Ball No.	Name	Pin Type	Buffer Type	Function
<b>Data Strobe Bus</b>				
7	DQS0	I/O	SSTL	<b>Data Strobe Bus 8:0</b>
16	DQS1	I/O	SSTL	
28	DQS2	I/O	SSTL	
37	DQS3	I/O	SSTL	
84	DQS4	I/O	SSTL	
93	DQS5	I/O	SSTL	
105	DQS6	I/O	SSTL	
114	DQS7	I/O	SSTL	
46	DQS8	I/O	SSTL	
6	$\overline{\text{DQS0}}$	I/O	SSTL	<b>Complement Data Strobe Bus 8:0</b>
15	$\overline{\text{DQS1}}$	I/O	SSTL	
27	$\overline{\text{DQS2}}$	I/O	SSTL	
36	$\overline{\text{DQS3}}$	I/O	SSTL	
83	$\overline{\text{DQS4}}$	I/O	SSTL	
92	$\overline{\text{DQS5}}$	I/O	SSTL	
104	$\overline{\text{DQS6}}$	I/O	SSTL	
113	$\overline{\text{DQS7}}$	I/O	SSTL	
45	$\overline{\text{DQS8}}$	I/O	SSTL	
<b>Data Mask Signals</b>				
125	DM0	I	SSTL	<b>Data Mask Bus 8:0</b>
134	DM1	I	SSTL	
146	DM2	I	SSTL	
155	DM3	I	SSTL	
202	DM4	I	SSTL	
211	DM5	I	SSTL	
223	DM6	I	SSTL	
232	DM7	I	SSTL	
164	DM8	I	SSTL	
<b>EEPROM</b>				
120	SCL	I	CMOS	<b>Serial Bus Clock</b>
119	SDA	I/O	OD	<b>Serial Bus Data</b>
239	SA0	I	CMOS	<b>Serial Address Select Bus 2:0</b>
240	SA1	I	CMOS	
101	SA2	I	CMOS	
<b>Power Supplies</b>				
1	$V_{\text{REF}}$	AI	—	<b>I/O Reference Voltage</b>
238	$V_{\text{DDSPD}}$	PWR	—	<b>EEPROM Power Supply</b>



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Ball No.	Name	Pin Type	Buffer Type	Function
51,56,62,72,75,, 78,170,175,181,, 191,194	$V_{DDQ}$	PWR	—	<b>I/O Driver Power Supply</b>
53,59,64,67,69,, 172,178,184,187, 189,197	$V_{DD}$	PWR	—	<b>Power Supply</b>
2,5,8,11,14,17,, 20,23,26,29,32, 35,38,41,44,47,, 50,65,66,79,82, 85,88,91,94,97,, 100,103,106, 109,112,115,118, 121,124,127,, 130,133,136,139, 142,145,148,, 151,154,157,160, 163,166,169, 198,201,204,207, 210,213,216,, 219,222,225,228, 231,234,237	$V_{SS}$	GND	—	<b>Ground Plane</b>
<b>Other Pins</b>				
195	ODT0	I	SSTL	<b>On-Die Termination Control 0</b>
77	ODT1	I	SSTL	<b>On-Die Termination Control 1</b> <i>Note: 2 Rank modules</i>
	NC	NC	—	<b>Not Connected</b> <i>Note: 1 Rank modules</i>
18,19,55,68,102,1 26,135,147, 156,165,173,203, 212, 224,233	NC	NC	—	<b>Not connected</b>

HYS[64/72]T256xxxHU-[3/.../5]-A  
Unbuffered DDR2 SDRAM Modules**TABLE 8**  
Abbreviations for Pin Type

Abbreviation	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
PWR	Power
GND	Ground
NC	Not Connected

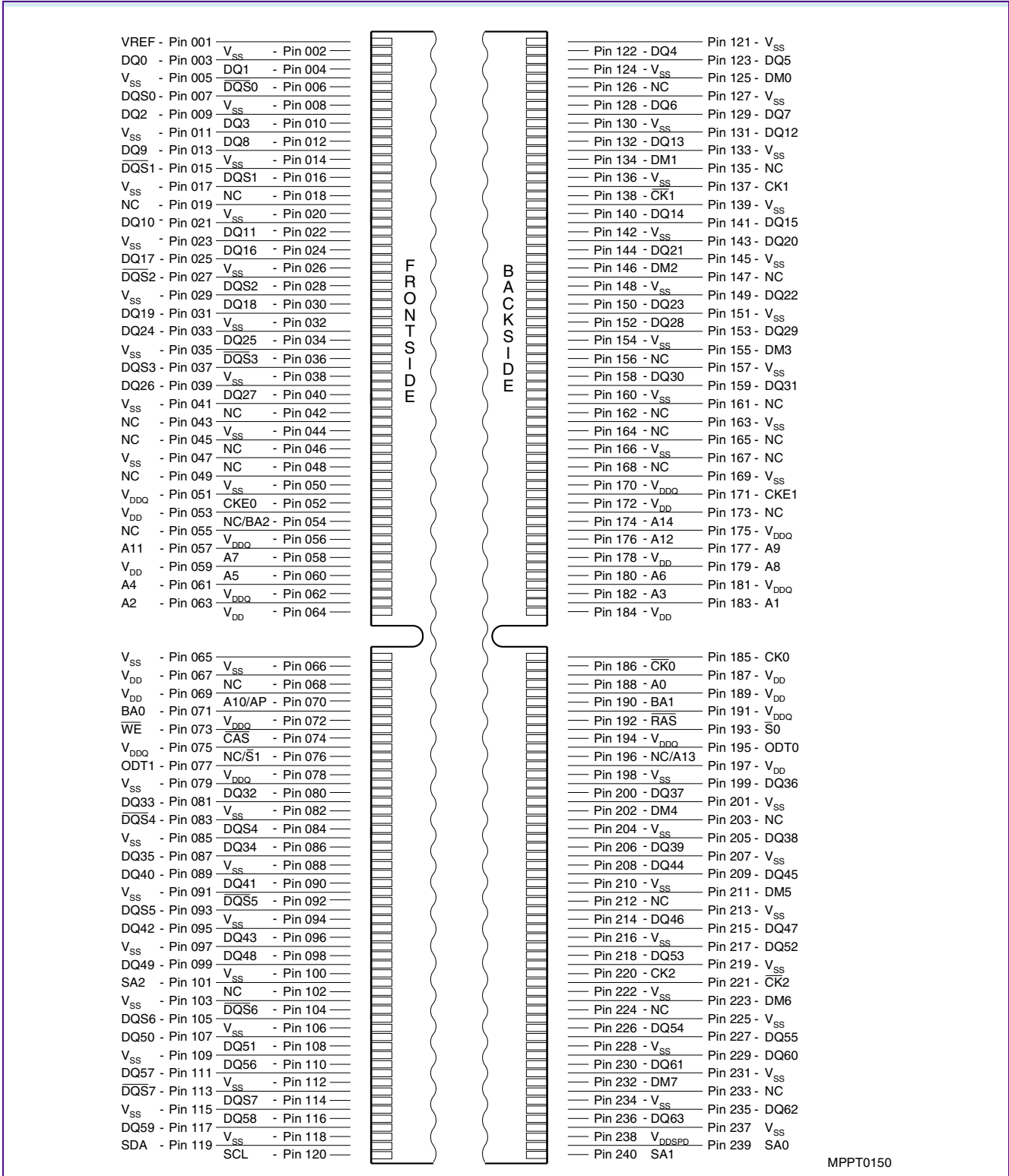
**TABLE 9**  
Abbreviations for Buffer Type

Abbreviation	Description
SSTL	Serial Stub Terminated Logic (SSTL_18)
LV-CMOS	Low Voltage CMOS
CMOS	CMOS Levels
OD	Open Drain. The corresponding pin has 2 operational states, active low and tri-state, and allows multiple devices to share as a wire-OR.



HYS[64/72]T256xxxHU-[3/.../5]-A  
Unbuffered DDR2 SDRAM Modules

**FIGURE 1**  
**Pin Configuration UDIMM ×64 (240 Pin)**

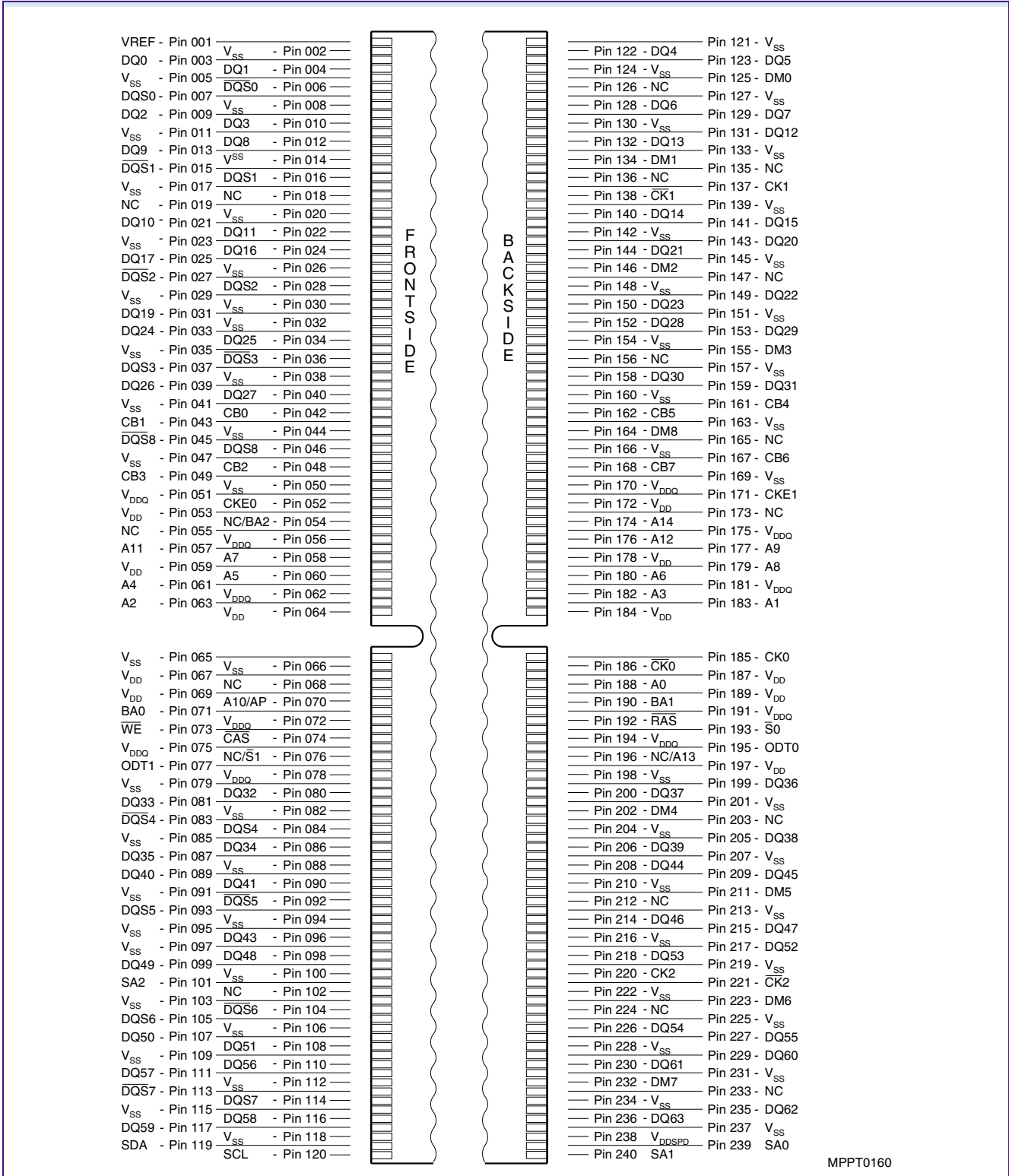


MPPT0150



HYS[64/72]T256xxxHU-[3/.../5]-A  
Unbuffered DDR2 SDRAM Modules

**FIGURE 2**  
**Pin Configuration UDIMM ×72 (240 Pin)**



MPPT0160



## 3 Electrical Characteristics

### 3.1 Absolute Maximum Ratings

Caution is needed not to exceed absolute maximum ratings of the DRAM device listed in **Table 10** at any time.

**TABLE 10**  
Absolute Maximum Ratings

Symbol	Parameter	Rating		Unit	Note
		Min.	Max.		
$V_{DD}$	Voltage on $V_{DD}$ pin relative to $V_{SS}$	-1.0	+2.3	V	1)
$V_{DDQ}$	Voltage on $V_{DDQ}$ pin relative to $V_{SS}$	-0.5	+2.3	V	1)2)
$V_{DDL}$	Voltage on $V_{DDL}$ pin relative to $V_{SS}$	-0.5	+2.3	V	1)2)
$V_{IN}, V_{OUT}$	Voltage on any pin relative to $V_{SS}$	-0.5	+2.3	V	1)
$T_{STG}$	Storage Temperature	-55	+100	°C	1)2)

1) When  $V_{DD}$  and  $V_{DDQ}$  and  $V_{DDL}$  are less than 500 mV;  $V_{REF}$  may be equal to or less than 300 mV.

2) Storage Temperature is the case surface temperature on the center/top side of the DRAM.

**Attention: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.**

**TABLE 11**  
DRAM Component Operating Temperature Range

Symbol	Parameter	Rating		Unit	Note
		Min.	Max.		
$T_{OPER}$	Operating Temperature	0	95	°C	1)2)3)4)

1) Operating Temperature is the case surface temperature on the center / top side of the DRAM.

2) The operating temperature range are the temperatures where all DRAM specification will be supported. During operation, the DRAM case temperature must be maintained between 0 - 95 °C under all other specification parameters.

3) Above 85 °C the Auto-Refresh command interval has to be reduced to  $t_{REFI} = 3.9 \mu s$

4) When operating this product in the 85 °C to 95 °C TCASE temperature range, the High Temperature Self Refresh has to be enabled by setting EMR(2) bit A7 to “1”. When the High Temperature Self Refresh is enabled there is an increase of  $I_{DD6}$  by approximately 50%





### 3.2 DC Operating Conditions

**TABLE 12**  
Operating Conditions

Parameter	Symbol	Values		Unit	Note
		Min.	Max.		
Operating temperature (ambient)	$T_{OPR}$	0	+65	°C	
DRAM Case Temperature	$T_{CASE}$	0	+95	°C	1)2)3)4)
Storage Temperature	$T_{STG}$	- 50	+100	°C	
Barometric Pressure (operating & storage)	PBar	+69	+105	kPa	5)
Operating Humidity (relative)	$H_{OPR}$	10	90	%	

- 1) DRAM Component Case Temperature is the surface temperature in the center on the top side of any of the DRAMs.
- 2) Within the DRAM Component Case Temperature Range all DRAM specifications will be supported
- 3) Above 85 °C DRAM Case Temperature the Auto-Refresh command interval has to be reduced to  $t_{REFI} = 3.9 \mu s$
- 4) Self-Refresh period is hard-coded in the DRAMs and therefore it is imperative that the system ensures the DRAM is below 85 °C Case Temperature before initiating Self-Refresh operation.
- 5) Up to 3000 m.

**TABLE 13**  
Supply Voltage Levels and DC Operating Conditions

Parameter	Symbol	Values			Unit	Note
		Min.	Nom.	Max.		
Device Supply Voltage	VDD	1.7	1.8	1.9	V	
Output Supply Voltage	VDDQ	1.7	1.8	1.9	V	1)
Input Reference Voltage	VREF	0.49 x VDDQ	0.5 x VDDQ	0.51 x VDDQ	V	2)
SPD Supply Voltage	VDDSPD	1.7	—	3.6	V	
DC Input Logic High	VIH (DC)	VREF + 0.125	—	VDDQ + 0.3	V	
DC Input Logic Low	VIL (DC)	- 0.30	—	VREF - 0.125	V	
In / Output Leakage Current	$I_L$	- 5	—	5	μA	3)

- 1) Under all conditions,  $V_{DDQ}$  must be less than or equal to  $V_{DD}$
- 2) Peak to peak AC noise on  $V_{REF}$  may not exceed  $\pm 2\% V_{REF(DC)}$ .  $V_{REF}$  is also expected to track noise in  $V_{DDQ}$ .
- 3) Input voltage for any connector pin under test of  $0 V \leq V_{IN} \leq V_{DDQ} + 0.3 V$ ; all other pins at 0 V. Current is per pin



### 3.3 AC Characteristics

#### 3.3.1 Speed Grade Definitions

List of speed grade definition tables.

- Table 14 “Speed Grade Definition Speed Bins for DDR2-667” on Page 18
- Table 15 “Speed Grade Definition Speed Bins for DDR2-533C” on Page 19
- Table 16 “Speed Grade Definition Speed Bins for DDR2-400B” on Page 20

**TABLE 14**

**Speed Grade Definition Speed Bins for DDR2-667**

Speed Grade		DDR2-667C		DDR2-667D		Unit	Note	
QAG Sort Name		-3		-3S				
CAS-RCD-RP latencies		4-4-4		5-5-5		$t_{CK}$		
Parameter	Symbol	Min.	Max.	Min.	Max.	—		
Clock Frequency	@ CL = 3	$t_{CK}$	5	8	5	8	ns	1)2)3)4)
	@ CL = 4	$t_{CK}$	3	8	3.75	8	ns	1)2)3)4)
	@ CL = 5	$t_{CK}$	3	8	3	8	ns	1)2)3)4)
Row Active Time	$t_{RAS}$	45	70000	45	70000	ns	1)2)3)4)5)	
Row Cycle Time	$t_{RC}$	57	—	60	—	ns	1)2)3)4)	
RAS-CAS-Delay	$t_{RCD}$	12	—	15	—	ns	1)2)3)4)	
Row Precharge Time	$t_{RP}$	12	—	15	—	ns	1)2)3)4)	

- 1) Timings are guaranteed with CK/ $\overline{CK}$  differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. Timings are further guaranteed for normal OCD drive strength (EMRS(1) A1 = 0) .
- 2) The CK/ $\overline{CK}$  input reference level (for timing reference to CK/ $\overline{CK}$ ) is the point at which CK and  $\overline{CK}$  cross. The DQS /  $\overline{DQS}$ , RDQS /  $\overline{RDQS}$ , input reference level is the crosspoint when in differential strobe mode
- 3) Inputs are not recognized as valid until  $V_{REF}$  stabilizes. During the period before  $V_{REF}$  stabilizes,  $CKE = 0.2 \times V_{DDQ}$  is recognized as low.
- 4) The output timing reference voltage level is  $V_{TT}$ .
- 5)  $t_{RAS,MAX}$  is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to  $9 \times t_{REFI}$ .



**TABLE 15**  
**Speed Grade Definition Speed Bins for DDR2-533C**

Speed Grade		DDR2-533C		Unit	Note	
QAG Sort Name		-3.7				
CAS-RCD-RP latencies		4-4-4		$t_{CK}$		
Parameter	Symbol	Min.	Max.	—		
Clock Frequency	@ CL = 3	$t_{CK}$	5	8	ns	1)2)3)4)
	@ CL = 4	$t_{CK}$	3.75	8	ns	1)2)3)4)
	@ CL = 5	$t_{CK}$	3.75	8	ns	1)2)3)4)
Row Active Time	$t_{RAS}$	45	70000	ns	1)2)3)4)5)	
Row Cycle Time	$t_{RC}$	60	—	ns	1)2)3)4)	
RAS-CAS-Delay	$t_{RCD}$	15	—	ns	1)2)3)4)	
Row Precharge Time	$t_{RP}$	15	—	ns	1)2)3)4)	

- 1) Timings are guaranteed with CK/ $\overline{CK}$  differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. Timings are further guaranteed for normal OCD drive strength (EMRS(1) A1 = 0)
- 2) The CK/ $\overline{CK}$  input reference level (for timing reference to CK/ $\overline{CK}$ ) is the point at which CK and  $\overline{CK}$  cross. The DQS /  $\overline{DQS}$ , RDQS /  $\overline{RDQS}$ , input reference level is the crosspoint when in differential strobe mode.
- 3) Inputs are not recognized as valid until  $V_{REF}$  stabilizes. During the period before  $V_{REF}$  stabilizes,  $CKE = 0.2 \times V_{DDQ}$  is recognized as low.
- 4) The output timing reference voltage level is  $V_{TT}$ .
- 5)  $t_{RAS,MAX}$  is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to  $9 \times t_{REFI}$ .



**TABLE 16**

**Speed Grade Definition Speed Bins for DDR2-400B**

Speed Grade		DDR2-400B		Unit	Note	
IFX Sort Name		-5				
CAS-RCD-RP latencies		3-3-3		$t_{CK}$		
Parameter	Symbol	Min.	Max.	—		
Clock Frequency	@ CL = 3	$t_{CK}$	5	8	ns	1)2)3)4)
	@ CL = 4	$t_{CK}$	5	8	ns	1)2)3)4)
	@ CL = 5	$t_{CK}$	5	8	ns	1)2)3)4)
Row Active Time	$t_{RAS}$	40	70000	ns	1)2)3)4)5)	
Row Cycle Time	$t_{RC}$	55	—	ns	1)2)3)4)	
RAS-CAS-Delay	$t_{RCD}$	15	—	ns	1)2)3)4)	
Row Precharge Time	$t_{RP}$	15	—	ns	1)2)3)4)	

- 1) Timings are guaranteed with CK/ $\overline{CK}$  differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. Timings are further guaranteed for normal OCD drive strength (EMRS(1) A1 = 0) only.
- 2) The CK/ $\overline{CK}$  input reference level (for timing reference to CK/ $\overline{CK}$ ) is the point at which CK and  $\overline{CK}$  cross. The DQS /  $\overline{DQS}$ , RDQS /  $\overline{RDQS}$ , input reference level is the crosspoint when in differential strobe mode
- 3) Inputs are not recognized as valid until  $V_{REF}$  stabilizes. During the period before  $V_{REF}$  stabilizes,  $CKE = 0.2 \times V_{DDQ}$  is recognized as low.
- 4) The output timing reference voltage level is  $V_{TT}$ .
- 5)  $t_{RAS,MAX}$  is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to  $9 \times t_{REFI}$ .



### 3.3.2 AC Timing Parameters

List of AC timing parameter tables.

- **Table 17** “Timing Parameter by Speed Grade - DDR2-667” on Page 21
- **Table 18** “Timing Parameter by Speed Grade - DDR2-533” on Page 26
- **Table 19** “Timing Parameter by Speed Grade - DDR2-400” on Page 29

**TABLE 17**

**Timing Parameter by Speed Grade - DDR2-667**

Parameter	Symbol	DDR2-667		Unit	Note <sup>1)2)3)4)5)6)7)8)</sup>
		Min.	Max.		
DQ output access time from CK / $\overline{\text{CK}}$	$t_{AC}$	-450	+450	ps	9)
DQS output access time from CK / $\overline{\text{CK}}$	$t_{DQ\text{SCK}}$	-400	+400	ps	9)
Average clock high pulse width	$t_{CH.AVG}$	0.48	0.52	$t_{CK.AVG}$	10)11)
Average clock low pulse width	$t_{CL.AVG}$	0.48	0.52	$t_{CK.AVG}$	10)11)
Average clock period	$t_{CK.AVG}$	3000	8000	ps	
DQ and DM input setup time	$t_{DS.BASE}$	100	—	ps	12)13)14)
DQ and DM input hold time	$t_{DH.BASE}$	175	—	ps	13)14)15)
Control & address input pulse width for each input	$t_{IPW}$	0.6	—	$t_{CK.AVG}$	
DQ and DM input pulse width for each input	$t_{DIPW}$	0.35	—	$t_{CK.AVG}$	
Data-out high-impedance time from CK / $\overline{\text{CK}}$	$t_{HZ}$	—	$t_{AC.MAX}$	ps	9)16)
DQS/DQS low-impedance time from CK / $\overline{\text{CK}}$	$t_{LZ.DQS}$	$t_{AC.MIN}$	$t_{AC.MAX}$	ps	9)16)
DQ low impedance time from CK/ $\overline{\text{CK}}$	$t_{LZ.DQ}$	$2 \times t_{AC.MIN}$	$t_{AC.MAX}$	ps	9)16)
DQS-DQ skew for DQS & associated DQ signals	$t_{DQSQ}$	—	240	ps	17)
CK half pulse width	$t_{HP}$	$\text{Min}(t_{CH.ABS}, t_{CL.ABS})$	—	ps	18)
DQ hold skew factor	$t_{QHS}$	—	340	ps	19)
DQ/DQS output hold time from DQS	$t_{QH}$	$t_{HP} - t_{QHS}$	—	ps	20)
Write command to DQS associated clock edges	WL	RL-1		nCK	
DQS latching rising transition to associated clock edges	$t_{DQSS}$	- 0.25	+ 0.25	$t_{CK.AVG}$	21)
DQS input high pulse width	$t_{DQSH}$	0.35	—	$t_{CK.AVG}$	
DQS input low pulse width	$t_{DQSL}$	0.35	—	$t_{CK.AVG}$	
DQS falling edge to CK setup time	$t_{DSS}$	0.2	—	$t_{CK.AVG}$	21)
DQS falling edge hold time from CK	$t_{DSH}$	0.2	—	$t_{CK.AVG}$	21)
Write postamble	$t_{WPST}$	0.4	0.6	$t_{CK.AVG}$	
Write preamble	$t_{WPRE}$	0.35	—	$t_{CK.AVG}$	
Address and control input setup time	$t_{LS.BASE}$	200	—	ps	22)23)
Address and control input hold time	$t_{LH.BASE}$	275	—	ps	23)24)
Read preamble	$t_{RPRE}$	0.9	1.1	$t_{CK.AVG}$	25)26)
Read postamble	$t_{RPST}$	0.4	0.6	$t_{CK.AVG}$	25)27)
Active to precharge command	$t_{RAS}$	45	70000	ns	28)



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Parameter	Symbol	DDR2-667		Unit	Note 1)2)3)4)5)6)7)8)
		Min.	Max.		
Active to active command period for 1KB page size products	$t_{RRD}$	7.5	—	ns	28)
Active to active command period for 2KB page size products	$t_{RRD}$	10	—	ns	28)
Four Activate Window for 1KB page size products	$t_{FAW}$	37.5	—	ns	28)
Four Activate Window for 2KB page size products	$t_{FAW}$	50	—	ns	28)
CAS to CAS command delay	$t_{CCD}$	2	—	nCK	
Write recovery time	$t_{WR}$	15	—	ns	28)
Auto-Precharge write recovery + precharge time	$t_{DAL}$	$WR + t_{nRP}$	—	nCK	29)30)
Internal write to read command delay	$t_{WTR}$	7.5	—	ns	28)31)
Internal Read to Precharge command delay	$t_{RTP}$	7.5	—	ns	28)
Exit self-refresh to a non-read command	$t_{XSNR}$	$t_{RFC} + 10$	—	ns	28)
Exit self-refresh to read command	$t_{XSRD}$	200	—	nCK	
Exit precharge power-down to any valid command (other than NOP or Deselect)	$t_{XP}$	2	—	nCK	
Exit power down to read command	$t_{XARD}$	2	—	nCK	
Exit active power-down mode to read command (slow exit, lower power)	$t_{XARDS}$	7 – AL	—	nCK	
CKE minimum pulse width ( high and low pulse width)	$t_{CKE}$	3	—	nCK	32)
ODT turn-on delay	$t_{AOND}$	2	2	nCK	
ODT turn-on	$t_{AON}$	$t_{AC,MIN}$	$t_{AC,MAX} + 0.7$	ns	9)33)
ODT turn-on (Power down mode)	$t_{AONPD}$	$t_{AC,MIN} + 2$	$2 \times t_{CK,AVG} + t_{AC,MAX} + 1$	ns	
ODT turn-off delay	$t_{AOFD}$	2.5	2.5	nCK	
ODT turn-off	$t_{AOF}$	$t_{AC,MIN}$	$t_{AC,MAX} + 0.6$	ns	34)35)
ODT turn-off (Power down mode)	$t_{AOFPD}$	$t_{AC,MIN} + 2$	$2.5 \times t_{CK,AVG} + t_{AC,MAX} + 1$	ns	
ODT to power down entry latency	$t_{ANPD}$	3	—	nCK	
ODT to power down exit latency	$t_{AXPD}$	8	—	nCK	
Mode register set command cycle time	$t_{MRD}$	2	—	nCK	
MRS command to ODT update delay	$t_{MOD}$	0	12	ns	28)
OCD drive mode output delay	$t_{OIT}$	0	12	ns	28)
Minimum time clocks remain ON after CKE asynchronously drops LOW	$t_{DELAY}$	$t_{LS} + t_{CK,AVG} + t_{LH}$	—	ns	

- 1) For details and notes see the relevant Qimonda component data sheet
- 2)  $V_{DDQ} = 1.8 V \pm 0.1 V$ ;  $V_{DD} = 1.8 V \pm 0.1 V$ . See notes 5)6)7)8)
- 3) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
- 4) Timings are guaranteed with  $\overline{CK}/\overline{CK}$  differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.
- 5) The  $\overline{CK} / \overline{CK}$  input reference level (for timing reference to  $\overline{CK} / \overline{CK}$ ) is the point at which  $\overline{CK}$  and  $\overline{CK}$  cross. The  $\overline{DQS} / \overline{DQS}$ ,  $\overline{RDQS} / \overline{RDQS}$ , input reference level is the crosspoint when in differential strobe mode.

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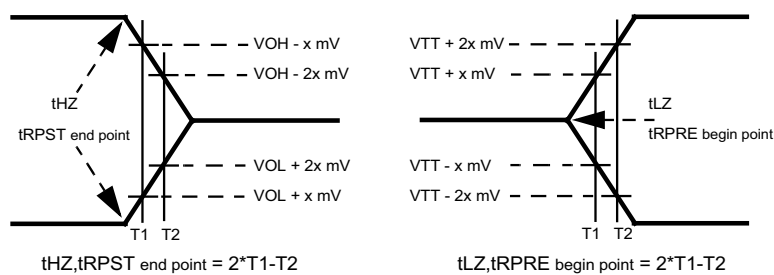
- 6) Inputs are not recognized as valid until  $V_{REF}$  stabilizes. During the period before  $V_{REF}$  stabilizes,  $CKE = 0.2 \times V_{DDQ}$  is recognized as low.
- 7) The output timing reference voltage level is  $V_{TT}$ .
- 8) New units, ' $t_{CK,AVG}$ ' and ' $nCK$ ', are introduced in DDR2-667 and DDR2-800. Unit ' $t_{CK,AVG}$ ' represents the actual  $t_{CK,AVG}$  of the input clock under operation. Unit ' $nCK$ ' represents one clock cycle of the input clock, counting the actual clock edges. Note that in DDR2-400 and DDR2-533, ' $t_{CK}$ ' is used for both concepts. Example:  $t_{XP} = 2 [nCK]$  means; if Power Down exit is registered at  $T_m$ , an Active command may be registered at  $T_m + 2$ , even if  $(T_m + 2 - T_m)$  is  $2 \times t_{CK,AVG} + t_{ERR,2PER(MIN)}$ .
- 9) When the device is operated with input clock jitter, this parameter needs to be derated by the actual  $t_{ERR(6-10PER)}$  of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2-667 SDRAM has  $t_{ERR(6-10PER),MIN} = -293$  ps and  $t_{ERR(6-10PER),MAX} = +293$  ps, then  $t_{DQSCK,MIN(DERATED)} = t_{DQSCK,MIN} - t_{ERR(6-10PER),MAX} = -400$  ps - 293 ps = -693 ps and  $t_{DQSCK,MAX(DERATED)} = t_{DQSCK,MAX} - t_{ERR(6-10PER),MIN} = 400$  ps + 272 ps = +672 ps. Similarly,  $t_{LZ,DQ}$  for DDR2-667 derates to  $t_{LZ,DQ,MIN(DERATED)} = -900$  ps - 293 ps = -1193 ps and  $t_{LZ,DQ,MAX(DERATED)} = 450$  ps + 272 ps = +722 ps. (Caution on the MIN/MAX usage!)
- 10) Input clock jitter spec parameter. These parameters are referred to as 'input clock jitter spec parameters' and these parameters apply to DDR2-667 and DDR2-800 only. The jitter specified is a random jitter meeting a Gaussian distribution.
- 11) These parameters are specified per their average values, however it is understood that the relationship between the average timing and the absolute instantaneous timing holds all the times (min. and max of SPEC values are to be used for calculations).
- 12) Input waveform timing  $t_{DS}$  with differential data strobe enabled  $MR[bit10] = 0$ , is referenced from the input signal crossing at the  $V_{IH,AC}$  level to the differential data strobe crosspoint for a rising signal, and from the input signal crossing at the  $V_{IL,AC}$  level to the differential data strobe crosspoint for a falling signal applied to the device under test. DQS,  $\overline{DQS}$  signals must be monotonic between  $V_{i(DC),MAX}$  and  $V_{i(DC),MIN}$ . See **Figure 4**.
- 13) If  $t_{DS}$  or  $t_{DH}$  is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.
- 14) These parameters are measured from a data signal ((L/U)DM, (L/U)DQ0, (L/U)DQ1, etc.) transition edge to its respective data strobe signal ((L/U/R)DQS /  $\overline{DQS}$ ) crossing.
- 15) Input waveform timing  $t_{DH}$  with differential data strobe enabled  $MR[bit10] = 0$ , is referenced from the differential data strobe crosspoint to the input signal crossing at the  $V_{IH,DC}$  level for a falling signal and from the differential data strobe crosspoint to the input signal crossing at the  $V_{IL,DC}$  level for a rising signal applied to the device under test. DQS,  $\overline{DQS}$  signals must be monotonic between  $V_{IL,DC,MAX}$  and  $V_{IH,DC,MIN}$ . See **Figure 4**.
- 16)  $t_{HZ}$  and  $t_{LZ}$  transitions occur in the same access time as valid data transitions. These parameters are referenced to a specific voltage level which specifies when the device output is no longer driving ( $t_{HZ}$ ), or begins driving ( $t_{LZ}$ ).
- 17)  $t_{DQSQ}$ : Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output slew rate mismatch between DQS /  $\overline{DQS}$  and associated DQ in any given cycle.
- 18)  $t_{HP}$  is the minimum of the absolute half period of the actual input clock.  $t_{HP}$  is an input parameter but not an input specification parameter. It is used in conjunction with  $t_{QHS}$  to derive the DRAM output timing  $t_{QH}$ . The value to be used for  $t_{QH}$  calculation is determined by the following equation;  $t_{HP} = \text{MIN}(t_{CH,ABS}, t_{CL,ABS})$ , where,  $t_{CH,ABS}$  is the minimum of the actual instantaneous clock high time;  $t_{CL,ABS}$  is the minimum of the actual instantaneous clock low time.
- 19)  $t_{QHS}$  accounts for: 1) The pulse duration distortion of on-chip clock circuits, which represents how well the actual  $t_{HP}$  at the input is transferred to the output; and 2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are independent of each other, due to data pin skew, output pattern effects, and pchannel to n-channel variation of the output drivers.
- 20)  $t_{QH} = t_{HP} - t_{QHS}$ , where:  $t_{HP}$  is the minimum of the absolute half period of the actual input clock; and  $t_{QHS}$  is the specification value under the max column. {The less half-pulse width distortion present, the larger the  $t_{QH}$  value is; and the larger the valid data eye will be.} Examples: 1) If the system provides  $t_{HP}$  of 1315 ps into a DDR2-667 SDRAM, the DRAM provides  $t_{QH}$  of 975 ps minimum. 2) If the system provides  $t_{HP}$  of 1420 ps into a DDR2-667 SDRAM, the DRAM provides  $t_{QH}$  of 1080 ps minimum.
- 21) These parameters are measured from a data strobe signal ((L/U/R)DQS /  $\overline{DQS}$ ) crossing to its respective clock signal (CK /  $\overline{CK}$ ) crossing. The spec values are not affected by the amount of clock jitter applied (i.e.  $t_{JIT,PER}$ ,  $t_{JIT,CC}$ , etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.
- 22) Input waveform timing is referenced from the input signal crossing at the  $V_{IH,AC}$  level for a rising signal and  $V_{IL,AC}$  for a falling signal applied to the device under test. See **Figure 5**.
- 23) These parameters are measured from a command/address signal (CKE, CS, RAS, CAS, WE, ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CK /  $\overline{CK}$ ) crossing. The spec values are not affected by the amount of clock jitter applied (i.e.  $t_{JIT,PER}$ ;  $t_{JIT,CC}$ , etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.
- 24) Input waveform timing is referenced from the input signal crossing at the  $V_{IL,DC}$  level for a rising signal and  $V_{IH,DC}$  for a falling signal applied to the device under test. See **Figure 5**.
- 25)  $t_{RPST}$  end point and  $t_{RPRE}$  begin point are not referenced to a specific voltage level but specify when the device output is no longer driving ( $t_{RPST}$ ), or begins driving ( $t_{RPRE}$ ). **Figure 3** shows a method to calculate these points when the device is no longer driving ( $t_{RPST}$ ), or begins driving ( $t_{RPRE}$ ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.



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- 26) When the device is operated with input clock jitter, this parameter needs to be derated by the actual  $t_{JIT.PER}$  of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2-667 SDRAM has  $t_{JIT.PER.MIN} = -72$  ps and  $t_{JIT.PER.MAX} = +93$  ps, then  $t_{RPRE.MIN(DERATED)} = t_{RPRE.MIN} + t_{JIT.PER.MIN} = 0.9 \times t_{CK.AVG} - 72$  ps = + 2178 ps and  $t_{RPRE.MAX(DERATED)} = t_{RPRE.MAX} + t_{JIT.PER.MAX} = 1.1 \times t_{CK.AVG} + 93$  ps = + 2843 ps. (Caution on the MIN/MAX usage!).
- 27) When the device is operated with input clock jitter, this parameter needs to be derated by the actual  $t_{JIT.DUTY}$  of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2-667 SDRAM has  $t_{JIT.DUTY.MIN} = -72$  ps and  $t_{JIT.DUTY.MAX} = +93$  ps, then  $t_{RPST.MIN(DERATED)} = t_{RPST.MIN} + t_{JIT.DUTY.MIN} = 0.4 \times t_{CK.AVG} - 72$  ps = + 928 ps and  $t_{RPST.MAX(DERATED)} = t_{RPST.MAX} + t_{JIT.DUTY.MAX} = 0.6 \times t_{CK.AVG} + 93$  ps = + 1592 ps. (Caution on the MIN/MAX usage!).
- 28) For these parameters, the DDR2 SDRAM device is characterized and verified to support  $t_{nPARAM} = RU\{t_{PARAM} / t_{CK.AVG}\}$ , which is in clock cycles, assuming all input clock jitter specifications are satisfied. For example, the device will support  $t_{nRP} = RU\{t_{RP} / t_{CK.AVG}\}$ , which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR2-667 5-5-5, of which  $t_{RP} = 15$  ns, the device will support  $t_{nRP} = RU\{t_{RP} / t_{CK.AVG}\} = 5$ , i.e. as long as the input clock jitter specifications are met, Precharge command at  $T_m$  and Active command at  $T_m + 5$  is valid even if  $(T_m + 5 - T_m)$  is less than 15 ns due to input clock jitter.
- 29)  $DAL = WR + RU\{t_{RP}(ns) / t_{CK}(ns)\}$ , where RU stands for round up. WR refers to the tWR parameter stored in the MRS. For  $t_{RP}$ , if the result of the division is not already an integer, round up to the next highest integer.  $t_{CK}$  refers to the application clock period. Example: For DDR2-533 at  $t_{CK} = 3.75$  ns with  $t_{WR}$  programmed to 4 clocks.  $t_{DAL} = 4 + (15 \text{ ns} / 3.75 \text{ ns})$  clocks = 4 + (4) clocks = 8 clocks.
- 30)  $t_{DAL.nCK} = WR [nCK] + t_{nRP.nCK} = WR + RU\{t_{RP} [ps] / t_{CK.AVG} [ps]\}$ , where WR is the value programmed in the EMR.
- 31)  $t_{WTR}$  is at least two clocks ( $2 \times t_{CK}$ ) independent of operation frequency.
- 32)  $t_{CKE.MIN}$  of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of  $t_{IS} + 2 \times t_{CK} + t_{IH}$ .
- 33) ODT turn on time min is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measured from  $t_{AOND}$ .
- 34) ODT turn off time min is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from  $t_{AOFD}$ .
- 35) When the device is operated with input clock jitter, this parameter needs to be derated by  $\{-t_{JIT.DUTY.MAX} - t_{ERR(6-10PER).MAX}\}$  and  $\{-t_{JIT.DUTY.MIN} - t_{ERR(6-10PER).MIN}\}$  of the actual input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2-667 SDRAM has  $t_{ERR(6-10PER).MIN} = -272$  ps,  $t_{ERR(6-10PER).MAX} = +293$  ps,  $t_{JIT.DUTY.MIN} = -106$  ps and  $t_{JIT.DUTY.MAX} = +94$  ps, then  $t_{AOF.MIN(DERATED)} = t_{AOF.MIN} + \{-t_{JIT.DUTY.MAX} - t_{ERR(6-10PER).MAX}\} = -450$  ps +  $\{-94 \text{ ps} - 293 \text{ ps}\} = -837$  ps and  $t_{AOF.MAX(DERATED)} = t_{AOF.MAX} + \{-t_{JIT.DUTY.MIN} - t_{ERR(6-10PER).MIN}\} = 1050$  ps +  $\{106 \text{ ps} + 272 \text{ ps}\} = +1428$  ps. (Caution on the MIN/MAX usage!).

**FIGURE 3**  
Method for calculating transitions and endpoint

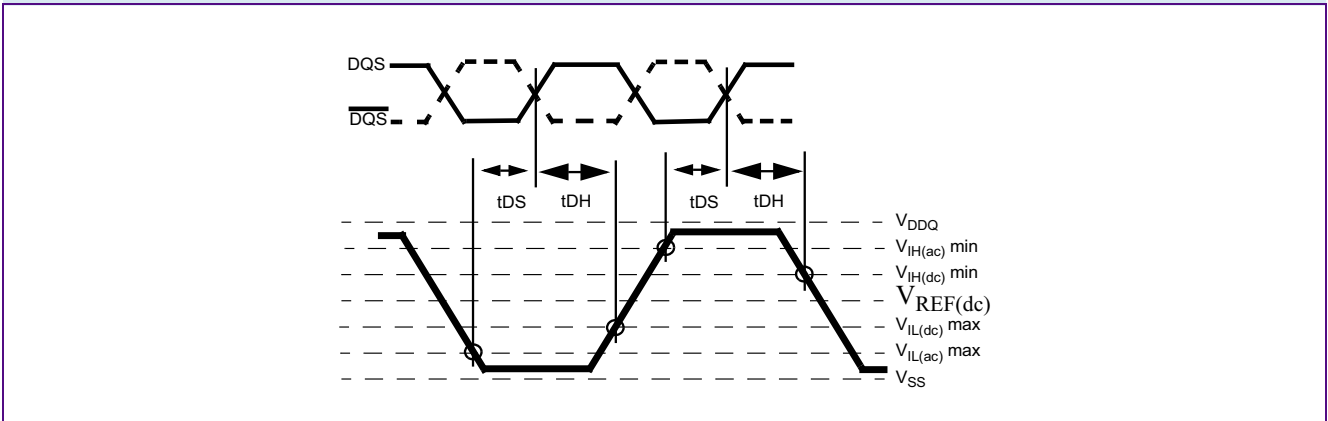






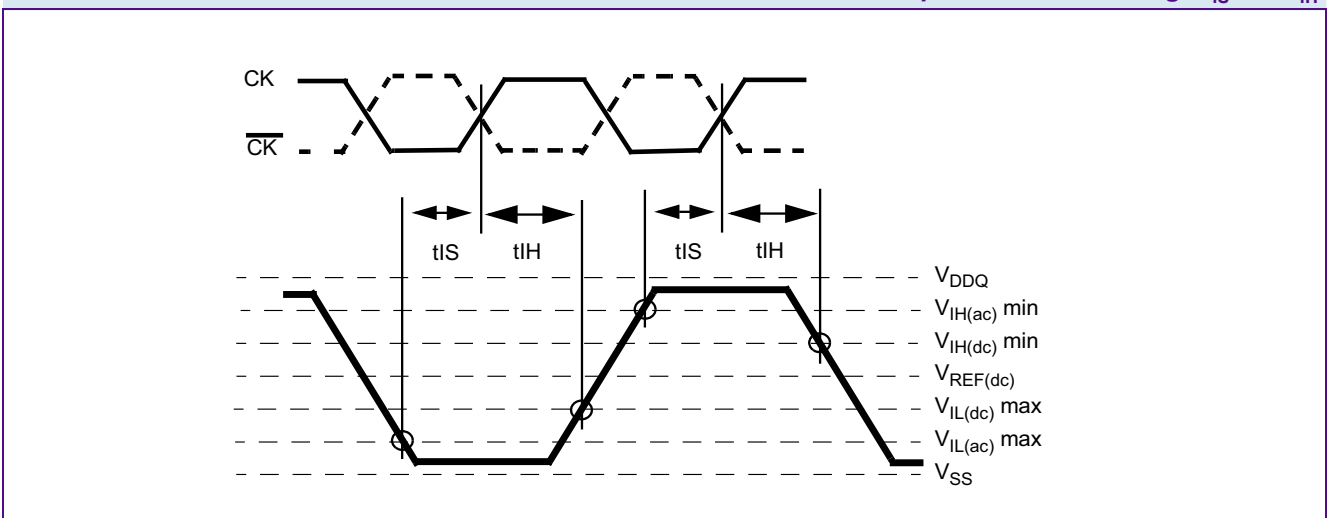
**FIGURE 4**

Differential input waveform timing -  $t_{DS}$  and  $t_{DH}$



**FIGURE 5**

Differential input waveform timing -  $t_{IS}$  and  $t_{IH}$





**TABLE 18**  
**Timing Parameter by Speed Grade - DDR2-533**

Parameter	Symbol	DDR2-533		Unit	Note <sup>1)2)3)4)5)6)7)</sup>
		Min.	Max.		
DQ output access time from CK / $\overline{\text{CK}}$	$t_{AC}$	-500	+500	ps	
CAS A to $\overline{\text{CAS}}$ B command period	$t_{CCD}$	2	—	$t_{CK}$	
CK, $\overline{\text{CK}}$ high-level width	$t_{CH}$	0.45	0.55	$t_{CK}$	
CKE minimum high and low pulse width	$t_{CKE}$	3	—	$t_{CK}$	
CK, $\overline{\text{CK}}$ low-level width	$t_{CL}$	0.45	0.55	$t_{CK}$	
Auto-Precharge write recovery + precharge time	$t_{DAL}$	WR + $t_{RP}$	—	$t_{CK}$	8)18)
Minimum time clocks remain ON after CKE asynchronously drops LOW	$t_{DELAY}$	$t_{IS} + t_{CK} + t_{IH}$	—	ns	9)
DQ and DM input hold time (differential data strobe)	$t_{DH}(\text{base})$	225	—	ps	10)
DQ and DM input hold time (single ended data strobe)	$t_{DH1}(\text{base})$	-25	—	ps	11)
DQ and DM input pulse width (each input)	$t_{DIPW}$	0.35	—	$t_{CK}$	
DQS output access time from CK / $\overline{\text{CK}}$	$t_{DQSCK}$	-450	+450	ps	
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	$t_{CK}$	
DQS-DQ skew (for DQS & associated DQ signals)	$t_{DQSQ}$	—	300	ps	11)
Write command to 1st DQS latching transition	$t_{DQSS}$	- 0.25	+ 0.25	$t_{CK}$	
DQ and DM input setup time (differential data strobe)	$t_{DS}(\text{base})$	100	—	ps	11)
DQ and DM input setup time (single ended data strobe)	$t_{DS1}(\text{base})$	-25	—	ps	11)
DQS falling edge hold time from CK (write cycle)	$t_{DSH}$	0.2	—	$t_{CK}$	
DQS falling edge to CK setup time (write cycle)	$t_{DSS}$	0.2	—	$t_{CK}$	
Four Activate Window period	$t_{FAW}$	37.5	—	ns	13)
		50	—	ns	
Clock half period	$t_{HP}$	MIN. ( $t_{CL}, t_{CH}$ )			12)
Data-out high-impedance time from CK / $\overline{\text{CK}}$	$t_{HZ}$	—	$t_{AC,MAX}$	ps	13)
Address and control input hold time	$t_{IH}(\text{base})$	375	—	ps	11)
Address and control input pulse width (each input)	$t_{IPW}$	0.6	—	$t_{CK}$	
Address and control input setup time	$t_{IS}(\text{base})$	250	—	ps	11)
DQ low-impedance time from CK / $\overline{\text{CK}}$	$t_{LZ(DQ)}$	$2 \times t_{AC,MIN}$	$t_{AC,MAX}$	ps	14)
DQS low-impedance from CK / $\overline{\text{CK}}$	$t_{LZ(DQS)}$	$t_{AC,MIN}$	$t_{AC,MAX}$	ps	14)
Mode register set command cycle time	$t_{MRD}$	2	—	$t_{CK}$	
OCD drive mode output delay	$t_{OIT}$	0	12	ns	
Data output hold time from DQS	$t_{QH}$	$t_{HP} - t_{QHS}$	—		



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Parameter	Symbol	DDR2-533		Unit	Note <sup>1)2)3)4)5)6)7)</sup>
		Min.	Max.		
Data hold skew factor	$t_{QHS}$	—	400	ps	
Average periodic refresh Interval	$t_{REFI}$	—	7.8	$\mu$ s	14)15)
		—	3.9	$\mu$ s	16)18)
Auto-Refresh to Active/Auto-Refresh command period	$t_{RFC}$	127.5	—	ns	17)
Precharge-All (4 banks) command period	$t_{RP}$	$t_{RP} + 1t_{CK}$	—	ns	
Precharge-All (8 banks) command period	$t_{RP}$	$15 + 1t_{CK}$	—	ns	
Read preamble	$t_{RPRE}$	0.9	1.1	$t_{CK}$	14)
Read postamble	$t_{RPST}$	0.40	0.60	$t_{CK}$	14)
Active bank A to Active bank B command period	$t_{RRD}$	7.5	—	ns	14)18)
		10	—	ns	16)20)
Internal Read to Precharge command delay	$t_{RTP}$	7.5	—	ns	
Write preamble	$t_{WPRE}$	$0.25 \times t_{CK}$	—	$t_{CK}$	
Write postamble	$t_{WPST}$	0.40	0.60	$t_{CK}$	19)
Write recovery time for write without Auto-Precharge	$t_{WR}$	15	—	ns	
Write recovery time for write with Auto-Precharge	WR	$t_{WR}/t_{CK}$	—	$t_{CK}$	20)
Internal Write to Read command delay	$t_{WTR}$	7.5	—	ns	21)
Exit power down to any valid command (other than NOP or Deselect)	$t_{XARD}$	2	—	$t_{CK}$	22)
Exit active power-down mode to Read command (slow exit, lower power)	$t_{XARDS}$	6 – AL	—	$t_{CK}$	22)
Exit precharge power-down to any valid command (other than NOP or Deselect)	$t_{XP}$	2	—	$t_{CK}$	
Exit Self-Refresh to non-Read command	$t_{XSNR}$	$t_{RFC} + 10$	—	ns	
Exit Self-Refresh to Read command	$t_{XSRD}$	200	—	$t_{CK}$	

- 1) For details and notes see the relevant Qimonda component data sheet
- 2)  $V_{DDQ} = 1.8 V \pm 0.1 V$ ;  $V_{DD} = 1.8 V \pm 0.1 V$ . See notes <sup>5)6)7)8)</sup>
- 3) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
- 4) Timings are guaranteed with  $CK/\overline{CK}$  differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.
- 5) The  $CK / \overline{CK}$  input reference level (for timing reference to  $CK / \overline{CK}$ ) is the point at which  $CK$  and  $\overline{CK}$  cross. The  $DQS / \overline{DQS}$ ,  $RDQS / \overline{RDQS}$ , input reference level is the crosspoint when in differential strobe mode.
- 6) Inputs are not recognized as valid until  $V_{REF}$  stabilizes. During the period before  $V_{REF}$  stabilizes,  $CKE = 0.2 \times V_{DDQ}$  is recognized as low.
- 7) The output timing reference voltage level is  $V_{TT}$ .
- 8) For each of the terms, if not already an integer, round to the next highest integer.  $t_{CK}$  refers to the application clock period. WR refers to the WR parameter stored in the MR.
- 9) The clock frequency is allowed to change during self-refresh mode or precharge power-down mode.
- 10) For timing definition, refer to the Component data sheet.
- 11) Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output Slew Rate mis-match between  $DQS / \overline{DQS}$  and associated DQ in any given cycle.
- 12) MIN ( $t_{CL}$ ,  $t_{CH}$ ) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for  $t_{CL}$  and  $t_{CH}$ ).

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- 13) The  $t_{HZ}$ ,  $t_{RPST}$  and  $t_{LZ}$ ,  $t_{RPRE}$  parameters are referenced to a specific voltage level, which specify when the device output is no longer driving ( $t_{HZ}$ ,  $t_{RPST}$ ), or begins driving ( $t_{LZ}$ ,  $t_{RPRE}$ ).  $t_{HZ}$  and  $t_{LZ}$  transitions occur in the same access time windows as valid data transitions. These parameters are verified by design and characterization, but not subject to production test.
- 14) The Auto-Refresh command interval has been reduced to 3.9  $\mu$ s when operating the DDR2 DRAM in a temperature range between 85 °C and 95 °C.
- 15)  $0\text{ }^{\circ}\text{C} \leq T_{CASE} \leq 85\text{ }^{\circ}\text{C}$
- 16)  $85\text{ }^{\circ}\text{C} < T_{CASE} \leq 95\text{ }^{\circ}\text{C}$
- 17) A maximum of eight Auto-Refresh commands can be posted to any given DDR2 SDRAM device.
- 18) The  $t_{RRD}$  timing parameter depends on the page size of the DRAM organization. See **Table 4 “Ordering Information for RoHS Compliant Products” on Page 5**.
- 19) The maximum limit for the  $t_{WPST}$  parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
- 20) WR must be programmed to fulfill the minimum requirement for the  $t_{WR}$  timing parameter, where  $WR_{MIN}[\text{cycles}] = t_{WR}(\text{ns})/t_{CK}(\text{ns})$  rounded up to the next integer value.  $t_{DAL} = WR + (t_{RP}/t_{CK})$ . For each of the terms, if not already an integer, round to the next highest integer.  $t_{CK}$  refers to the application clock period. WR refers to the WR parameter stored in the MRS.
- 21) Minimum  $t_{WTR}$  is two clocks when operating the DDR2-SDRAM at frequencies  $\leq 200$  MHz.
- 22) User can choose two different active power-down modes for additional power saving via MRS address bit A12. In “standard active power-down mode” (MR, A12 = “0”) a fast power-down exit timing  $t_{XARD}$  can be used. In “low active power-down mode” (MR, A12 = “1”) a slow power-down exit timing  $t_{XARDS}$  has to be satisfied.



**TABLE 19**  
**Timing Parameter by Speed Grade - DDR2-400**

Parameter	Symbol	DDR2-400		Unit	Note <sup>1)2)3)4)5)6)7)</sup>
		Min.	Max.		
DQ output access time from CK / $\overline{\text{CK}}$	$t_{AC}$	-600	+600	ps	
CAS A to $\overline{\text{CAS}}$ B command period	$t_{CCD}$	2	—	$t_{CK}$	
CK, $\overline{\text{CK}}$ high-level width	$t_{CH}$	0.45	0.55	$t_{CK}$	
CKE minimum high and low pulse width	$t_{CKE}$	3	—	$t_{CK}$	
CK, $\overline{\text{CK}}$ low-level width	$t_{CL}$	0.45	0.55	$t_{CK}$	
Auto-Precharge write recovery + precharge time	$t_{DAL}$	WR + $t_{RP}$	—	$t_{CK}$	8)22)
Minimum time clocks remain ON after CKE asynchronously drops LOW	$t_{DELAY}$	$t_{IS} + t_{CK} + t_{IH}$	—	ns	9)
DQ and DM input hold time (differential data strobe)	$t_{DH}(\text{base})$	275	—	ps	10)
DQ and DM input hold time (single ended data strobe)	$t_{DH1}(\text{base})$	-25	—	ps	11)
DQ and DM input pulse width (each input)	$t_{DIPW}$	0.35	—	$t_{CK}$	
DQS output access time from CK / $\overline{\text{CK}}$	$t_{DQSCK}$	-500	+500	ps	
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	$t_{CK}$	
DQS-DQ skew (for DQS & associated DQ signals)	$t_{DQSQ}$	—	350	ps	11)
Write command to 1st DQS latching transition	$t_{DQSS}$	- 0.25	+ 0.25	$t_{CK}$	
DQ and DM input setup time (differential data strobe)	$t_{DS}(\text{base})$	150	—	ps	11)
DQ and DM input setup time (single ended data strobe)	$t_{DS1}(\text{base})$	-25	—	ps	11)
DQS falling edge hold time from CK (write cycle)	$t_{DSH}$	0.2	—	$t_{CK}$	
DQS falling edge to CK setup time (write cycle)	$t_{DSS}$	0.2	—	$t_{CK}$	
Four Activate Window period	$t_{FAW}$	37.5	—	ns	13)
		50	—	ns	
Clock half period	$t_{HP}$	MIN. ( $t_{CL}, t_{CH}$ )			12)
Data-out high-impedance time from CK / $\overline{\text{CK}}$	$t_{HZ}$	—	$t_{AC,MAX}$	ps	13)
Address and control input hold time	$t_{IH}(\text{base})$	475	—	ps	11)
Address and control input pulse width (each input)	$t_{IPW}$	0.6	—	$t_{CK}$	
Address and control input setup time	$t_{IS}(\text{base})$	350	—	ps	11)
DQ low-impedance time from CK / $\overline{\text{CK}}$	$t_{LZ(DQ)}$	$2 \times t_{AC,MIN}$	$t_{AC,MAX}$	ps	14)
DQS low-impedance from CK / $\overline{\text{CK}}$	$t_{LZ(DQS)}$	$t_{AC,MIN}$	$t_{AC,MAX}$	ps	14)
Mode register set command cycle time	$t_{MRD}$	2	—	$t_{CK}$	
OCD drive mode output delay	$t_{OIT}$	0	12	ns	
Data output hold time from DQS	$t_{QH}$	$t_{HP} - t_{QHS}$	—		



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Parameter	Symbol	DDR2-400		Unit	Note <sup>1)2)3)4)5)6)7)</sup>
		Min.	Max.		
Data hold skew factor	$t_{QHS}$	—	450	ps	
Average periodic refresh Interval	$t_{REFI}$	—	7.8	$\mu$ s	14)15)
		—	3.9	$\mu$ s	16)18)
Auto-Refresh to Active/Auto-Refresh command period		127.5	—	ns	17)
Precharge-All (4 banks) command period	$t_{RP}$	$t_{RP} + 1t_{CK}$	—	ns	
Precharge-All (8 banks) command period	$t_{RP}$	$15 + 1t_{CK}$	—	ns	
Read preamble	$t_{RPRE}$	0.9	1.1	$t_{CK}$	14)
Read postamble	$t_{RPST}$	0.40	0.60	$t_{CK}$	14)
Active bank A to Active bank B command period	$t_{RRD}$	7.5	—	ns	14)18)
		10	—	ns	16)20)
Internal Read to Precharge command delay	$t_{RTP}$	7.5	—	ns	
Write preamble	$t_{WPRE}$	$0.25 \times t_{CK}$	—	$t_{CK}$	
Write postamble	$t_{WPST}$	0.40	0.60	$t_{CK}$	19)
Write recovery time for write without Auto-Precharge	$t_{WR}$	15	—	ns	
Write recovery time for write with Auto-Precharge	WR	$t_{WR}/t_{CK}$	—	$t_{CK}$	20)
Internal Write to Read command delay	$t_{WTR}$	10	—	ns	21)
Exit power down to any valid command (other than NOP or Deselect)	$t_{XARD}$	2	—	$t_{CK}$	22)
Exit active power-down mode to Read command (slow exit, lower power)	$t_{XARDS}$	6 – AL	—	$t_{CK}$	22)
Exit precharge power-down to any valid command (other than NOP or Deselect)	$t_{XP}$	2	—	$t_{CK}$	
Exit Self-Refresh to non-Read command	$t_{XSNR}$	$t_{RFC} + 10$	—	ns	
Exit Self-Refresh to Read command	$t_{XSRD}$	200	—	$t_{CK}$	

- 1) For details and notes see the relevant Qimonda component data sheet
- 2)  $V_{DDQ} = 1.8 \text{ V} \pm 0.1 \text{ V}$ ;  $V_{DD} = 1.8 \text{ V} \pm 0.1 \text{ V}$ . See notes <sup>5)6)7)8)</sup>
- 3) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
- 4) Timings are guaranteed with  $\overline{CK}/\overline{CK}$  differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.
- 5) The  $\overline{CK} / \overline{CK}$  input reference level (for timing reference to  $\overline{CK} / \overline{CK}$ ) is the point at which  $\overline{CK}$  and  $\overline{CK}$  cross. The  $\overline{DQS} / \overline{DQS}$ ,  $\overline{RDQS} / \overline{RDQS}$ , input reference level is the crosspoint when in differential strobe mode.
- 6) Inputs are not recognized as valid until  $V_{REF}$  stabilizes. During the period before  $V_{REF}$  stabilizes,  $\overline{CKE} = 0.2 \times V_{DDQ}$  is recognized as low.
- 7) The output timing reference voltage level is  $V_{TT}$ .
- 8) For each of the terms, if not already an integer, round to the next highest integer.  $t_{CK}$  refers to the application clock period. WR refers to the WR parameter stored in the MR.
- 9) The clock frequency is allowed to change during self-refresh mode or precharge power-down mode.
- 10) For timing definition, refer to the Component data sheet.
- 11) Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output Slew Rate mis-match between  $\overline{DQS} / \overline{DQS}$  and associated  $\overline{DQ}$  in any given cycle.
- 12) MIN ( $t_{CL}$ ,  $t_{CH}$ ) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for  $t_{CL}$  and  $t_{CH}$ ).

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- 13) The  $t_{HZ}$ ,  $t_{RPST}$  and  $t_{LZ}$ ,  $t_{RPRE}$  parameters are referenced to a specific voltage level, which specify when the device output is no longer driving ( $t_{HZ}$ ,  $t_{RPST}$ ), or begins driving ( $t_{LZ}$ ,  $t_{RPRE}$ ).  $t_{HZ}$  and  $t_{LZ}$  transitions occur in the same access time windows as valid data transitions. These parameters are verified by design and characterization, but not subject to production test.
- 14) The Auto-Refresh command interval has been reduced to 3.9  $\mu$ s when operating the DDR2 DRAM in a temperature range between 85 °C and 95 °C.
- 15)  $0\text{ }^{\circ}\text{C} \leq T_{CASE} \leq 85\text{ }^{\circ}\text{C}$
- 16)  $85\text{ }^{\circ}\text{C} < T_{CASE} \leq 95\text{ }^{\circ}\text{C}$
- 17) A maximum of eight Auto-Refresh commands can be posted to any given DDR2 SDRAM device.
- 18) The  $t_{RRD}$  timing parameter depends on the page size of the DRAM organization. See **Table 4 “Ordering Information for RoHS Compliant Products” on Page 5**.
- 19) The maximum limit for the  $t_{WPST}$  parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
- 20) WR must be programmed to fulfill the minimum requirement for the  $t_{WR}$  timing parameter, where  $WR_{MIN}[\text{cycles}] = t_{WR}(\text{ns})/t_{CK}(\text{ns})$  rounded up to the next integer value.  $t_{DAL} = WR + (t_{RP}/t_{CK})$ . For each of the terms, if not already an integer, round to the next highest integer.  $t_{CK}$  refers to the application clock period. WR refers to the WR parameter stored in the MRS.
- 21) Minimum  $t_{WTR}$  is two clocks when operating the DDR2-SDRAM at frequencies  $\leq 200$  MHz.
- 22) User can choose two different active power-down modes for additional power saving via MRS address bit A12. In “standard active power-down mode” (MR, A12 = “0”) a fast power-down exit timing  $t_{XARD}$  can be used. In “low active power-down mode” (MR, A12 = “1”) a slow power-down exit timing  $t_{XARDS}$  has to be satisfied.



### 3.3.3 ODT AC Electrical Characteristics

**TABLE 20**

**ODT AC Characteristics and Operating Conditions for DDR2-667**

Symbol	Parameter / Condition	Values		Unit	Note
		Min.	Max.		
$t_{AOND}$	ODT turn-on delay	2	2	$t_{CK}$	
$t_{AON}$	ODT turn-on	$t_{AC.MIN}$	$t_{AC.MAX} + 0.7 \text{ ns}$	ns	1)
$t_{AONPD}$	ODT turn-on (Power-Down Modes)	$t_{AC.MIN} + 2 \text{ ns}$	$2 t_{CK} + t_{AC.MAX} + 1 \text{ ns}$	ns	
$t_{AOFD}$	ODT turn-off delay	2.5	2.5	$t_{CK}$	
$t_{AOF}$	ODT turn-off	$t_{AC.MIN}$	$t_{AC.MAX} + 0.6 \text{ ns}$	ns	2)
$t_{AOFPD}$	ODT turn-off (Power-Down Modes)	$t_{AC.MIN} + 2 \text{ ns}$	$2.5 t_{CK} + t_{AC.MAX} + 1 \text{ ns}$	ns	
$t_{ANPD}$	ODT to Power Down Mode Entry Latency	3	—	$t_{CK}$	
$t_{AXPD}$	ODT Power Down Exit Latency	8	—	$t_{CK}$	

- 1) ODT turn on time min. is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measure from  $t_{AOND}$ .
- 2) ODT turn off time min. is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from  $t_{AOFD}$ .

**TABLE 21**

**ODT AC Characteristics and Operating Conditions for DDR2-533 & DDR2-400**

Symbol	Parameter / Condition	Values		Unit	Note
		Min.	Max.		
$t_{AOND}$	ODT turn-on delay	2	2	$t_{CK}$	
$t_{AON}$	ODT turn-on	$t_{AC.MIN}$	$t_{AC.MAX} + 1 \text{ ns}$	ns	1)
$t_{AONPD}$	ODT turn-on (Power-Down Modes)	$t_{AC.MIN} + 2 \text{ ns}$	$2 t_{CK} + t_{AC.MAX} + 1 \text{ ns}$	ns	
$t_{AOFD}$	ODT turn-off delay	2.5	2.5	$t_{CK}$	
$t_{AOF}$	ODT turn-off	$t_{AC.MIN}$	$t_{AC.MAX} + 0.6 \text{ ns}$	ns	2)
$t_{AOFPD}$	ODT turn-off (Power-Down Modes)	$t_{AC.MIN} + 2 \text{ ns}$	$2.5 t_{CK} + t_{AC.MAX} + 1 \text{ ns}$	ns	
$t_{ANPD}$	ODT to Power Down Mode Entry Latency	3	—	$t_{CK}$	
$t_{AXPD}$	ODT Power Down Exit Latency	8	—	$t_{CK}$	

- 1) ODT turn on time min. is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measure from  $t_{AOND}$ .
- 2) ODT turn off time min. is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from  $t_{AOFD}$ .





### 3.4 $I_{DD}$ Specifications and Conditions

**TABLE 22**  
 **$I_{DD}$  Measurement Conditions**

Parameter	Symbol	Note 1)2)3)4)5)
<b>Operating Current 0</b> One bank Active - Precharge; $t_{CK} = t_{CK.MIN}$ , $t_{RC} = t_{RC.MIN}$ , $t_{RAS} = t_{RAS.MIN}$ , CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.	$I_{DD0}$	
<b>Operating Current 1</b> One bank Active - Read - Precharge; $I_{OUT} = 0$ mA, BL = 4, $t_{CK} = t_{CK.MIN}$ , $t_{RC} = t_{RC.MIN}$ , $t_{RAS} = t_{RAS.MIN}$ , $t_{RCD} = t_{RCD.MIN}$ , AL = 0, CL = CL <sub>MIN</sub> ; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.	$I_{DD1}$	6)
<b>Precharge Standby Current</b> All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CK.MIN}$ ; Other control and address inputs are SWITCHING, Databus inputs are SWITCHING.	$I_{DD2N}$	
<b>Precharge Power-Down Current</b> Other control and address inputs are STABLE, Data bus inputs are FLOATING.	$I_{DD2P}$	
<b>Precharge Quiet Standby Current</b> All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CK.MIN}$ ; Other control and address inputs are STABLE, Data bus inputs are FLOATING.	$I_{DD2Q}$	
<b>Active Standby Current</b> Burst Read: All banks open; Continuous burst reads; BL = 4; AL = 0, CL = CL <sub>MIN</sub> ; $t_{CK} = t_{CK.MIN}$ ; $t_{RAS} = t_{RAS.MAX}$ , $t_{RP} = t_{RP.MIN}$ ; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING; $I_{OUT} = 0$ mA.	$I_{DD3N}$	
<b>Active Power-Down Current</b> All banks open; $t_{CK} = t_{CK.MIN}$ , CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to LOW (Fast Power-down Exit);	$I_{DD3P(0)}$	
<b>Active Power-Down Current</b> All banks open; $t_{CK} = t_{CK.MIN}$ , CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to HIGH (Slow Power-down Exit);	$I_{DD3P(1)}$	
<b>Operating Current - Burst Read</b> All banks open; Continuous burst reads; BL = 4; AL = 0, CL = CL <sub>MIN</sub> ; $t_{CK} = t_{CKMIN}$ ; $t_{RAS} = t_{RASMAX}$ ; $t_{RP} = t_{RPMIN}$ ; CKE is HIGH, CS is HIGH between valid commands; Address inputs are SWITCHING; Data bus inputs are SWITCHING; $I_{OUT} = 0$ mA.	$I_{DD4R}$	6)
<b>Operating Current - Burst Write</b> All banks open; Continuous burst writes; BL = 4; AL = 0, CL = CL <sub>MIN</sub> ; $t_{CK} = t_{CK.MIN}$ ; $t_{RAS} = t_{RAS.MAX}$ , $t_{RP} = t_{RP.MAX}$ ; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING;	$I_{DD4W}$	
<b>Burst Refresh Current</b> $t_{CK} = t_{CK.MIN}$ , Refresh command every $t_{RFC} = t_{RFC.MIN}$ interval, CKE is HIGH, $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	$I_{DD5B}$	
<b>Distributed Refresh Current</b> $t_{CK} = t_{CK.MIN}$ , Refresh command every $t_{RFC} = t_{REFI}$ interval, CKE is LOW and $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	$I_{DD5D}$	



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Parameter	Symbol	Note 1)2)3)4)5)
<b>Self-Refresh Current</b> CKE ≤ 0.2 V; external clock off, CK and $\overline{\text{CK}}$ at 0 V; Other control and address inputs are FLOATING, Data bus inputs are FLOATING. $I_{\text{DD6}}$ current values are guaranteed up to $T_{\text{CASE}}$ of 85 °C max.	$I_{\text{DD6}}$	
<b>All Bank Interleave Read Current</b> All banks are being interleaved at minimum $t_{\text{RC}}$ without violating $t_{\text{RRD}}$ using a burst length of 4. Control and address bus inputs are STABLE during DESELECTS. $I_{\text{out}} = 0$ mA.	$I_{\text{DD7}}$	6)

- 1)  $V_{\text{DDQ}} = 1.8 \text{ V} \pm 0.1 \text{ V}$ ;  $V_{\text{DD}} = 1.8 \text{ V} \pm 0.1 \text{ V}$
- 2)  $I_{\text{DD}}$  specifications are tested after the device is properly initialized and  $I_{\text{DD}}$  parameter are specified with ODT disabled.
- 3) Definitions for  $I_{\text{DD}}$  see **Table 23**
- 4) For two rank modules: for all active current measurements the other rank is in Precharge Power-Down Mode  $I_{\text{DD2P}}$
- 5) For details and notes see the relevant Qimonda component data sheet
- 6)  $I_{\text{DD1}}$ ,  $I_{\text{DD4R}}$  and  $I_{\text{DD7}}$  current measurements are defined with the outputs disabled ( $I_{\text{OUT}} = 0$  mA). To achieve this on module level the output buffers can be disabled using an EMRS(1) (Extended Mode Register Command) by setting A12 bit to HIGH.

**TABLE 23**  
Definitions for  $I_{\text{DD}}$

Parameter	Description
LOW	$V_{\text{IN}} \leq V_{\text{IL(ac),MAX}}$ , HIGH is defined as $V_{\text{IN}} \geq V_{\text{IH(ac),MIN}}$
STABLE	Inputs are stable at a HIGH or LOW level
FLOATING	Inputs are $V_{\text{REF}} = V_{\text{DDQ}}/2$
SWITCHING	Inputs are changing between HIGH and LOW every other clock (once per 2 cycles) for address and control signals, and inputs changing between HIGH and LOW every other data transfer (once per cycle) for DQ signals not including mask or strobes



HYS[64/72]T256xxxHU-[3/.../5]-A  
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**TABLE 24**

**$I_{DD}$  Specification for HYS[64/72]T256020HU-3-A**

Product Type	HYS64T256020HU-3-A	HYS72T256020HU-3-A	Units	Note <sup>1)</sup>
<b>Organization</b>	<b>2 GB</b>	<b>2 GB</b>		
	<b>×64</b>	<b>×72</b>		
	<b>2 Ranks</b>	<b>2 Ranks</b>		
	<b>-3</b>	<b>-3</b>		
$I_{DD0}$	728	819	mA	2)
$I_{DD1}$	888	999	mA	2)
$I_{DD2N}$	960	1080	mA	3)
$I_{DD2P}$	96	108	mA	3)
$I_{DD2Q}$	640	720	mA	3)
$I_{DD3N}$	1040	1170	mA	3)
$I_{DD3P\_0}$ (fast)	336	378	mA	3)
$I_{DD3P\_1}$ (slow)	112	126	mA	3)
$I_{DD4R}$	1448	1629	mA	2)
$I_{DD4W}$	1448	1629	mA	2)
$I_{DD5B}$	1648	1854	mA	2)
$I_{DD5D}$	112	126	mA	3)4)
$I_{DD6}$	96	108	mA	3)4)
$I_{DD7}$	2088	2349	mA	2)

1) Calculated values from component data. ODT disabled.  $I_{DD1}$ ,  $I_{DD4R}$ , and  $I_{DD7}$ , are defined with the outputs disabled.

2) The other rank is in  $I_{DD2P}$  Precharge Power-Down Current mode

3) Both ranks are in the same  $I_{DD}$  current mode

4)  $I_{DD5D}$  and  $I_{DD6}$  values are for  $0^{\circ}\text{C} \leq T_{\text{Case}} \leq 85^{\circ}\text{C}$



HYS[64/72]T256xxxHU-[3/.../5]-A  
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**TABLE 25**

**$I_{DD}$  Specification for HYS[64/72]T256020HU-3S-A**

Product Type	HYS64T256020HU-3S-A	HYS72T256020HU-3S-A	Units	Note <sup>1)</sup>
<b>Organization</b>	<b>2 GB</b>	<b>2 GB</b>		
	<b>×64</b>	<b>×72</b>		
	<b>2 Ranks</b>	<b>2 Ranks</b>		
	<b>-3S</b>	<b>-3S</b>		
$I_{DD0}$	696	783	mA	2)
$I_{DD1}$	848	954	mA	2)
$I_{DD2N}$	960	1080	mA	3)
$I_{DD2P}$	96	108	mA	3)
$I_{DD2Q}$	624	702	mA	3)
$I_{DD3N}$	1040	1170	mA	3)
$I_{DD3P\_0}$ (fast)	336	378	mA	3)
$I_{DD3P\_1}$ (slow)	112	126	mA	3)
$I_{DD4R}$	1448	1629	mA	2)
$I_{DD4W}$	1448	1629	mA	2)
$I_{DD5B}$	1648	1854	mA	2)
$I_{DD5D}$	112	126	mA	3)4)
$I_{DD6}$	96	108	mA	3)4)
$I_{DD7}$	1984	2232	mA	2)

1) Calculated values from component data. ODT disabled.  $I_{DD1}$ ,  $I_{DD4R}$ , and  $I_{DD7}$ , are defined with the outputs disabled.

2) The other rank is in  $I_{DD2P}$  Precharge Power-Down Current mode

3) Both ranks are in the same  $I_{DD}$  current mode

4)  $I_{DD5D}$  and  $I_{DD6}$  values are for  $0^{\circ}\text{C} \leq T_{\text{Case}} \leq 85^{\circ}\text{C}$



HYS[64/72]T256xxxHU-[3/.../5]-A  
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**TABLE 26**

**$I_{DD}$  Specification for HYS[64/72]T256020HU-3.7-A**

Product Type	HYS64T256020HU-3.7-A	HYS72T256020HU-3.7-A	Units	Note <sup>1)</sup>
<b>Organization</b>	<b>2 GB</b>	<b>2 GB</b>		
	<b>×64</b>	<b>×72</b>		
	<b>2 Ranks</b>	<b>2 Ranks</b>		
	<b>-3.7</b>	<b>-3.7</b>		
$I_{DD0}$	646	726	mA	2)
$I_{DD1}$	726	816	mA	2)
$I_{DD2N}$	736	828	mA	3)
$I_{DD2P}$	91	103	mA	3)
$I_{DD2Q}$	512	576	mA	3)
$I_{DD3N}$	800	900	mA	3)
$I_{DD3P\_0}$ (fast)	272	306	mA	3)
$I_{DD3P\_1}$ (slow)	96	108	mA	3)
$I_{DD4R}$	1206	1356	mA	2)
$I_{DD4W}$	1166	1311	mA	2)
$I_{DD5B}$	1526	1716	mA	2)
$I_{DD5D}$	112	126	mA	3)4)
$I_{DD6}$	91	103	mA	3)4)
$I_{DD7}$	1886	2121	mA	2)

1) Calculated values from component data. ODT disabled.  $I_{DD1}$ ,  $I_{DD4R}$ , and  $I_{DD7}$ , are defined with the outputs disabled.

2) The other rank is in  $I_{DD2P}$  Precharge Power-Down Current mode

3) Both ranks are in the same  $I_{DD}$  current mode

4)  $I_{DD5D}$  and  $I_{DD6}$  values are for  $0^{\circ}\text{C} \leq T_{\text{Case}} \leq 85^{\circ}\text{C}$



HYS[64/72]T256xxxHU-[3/.../5]-A  
Unbuffered DDR2 SDRAM Modules

**TABLE 27**

**$I_{DD}$  Specification for HYS[64/72]T256020HU-5-A**

Product Type	HYS64T256020HU-5-A	HYS72T256020HU-5-A	Units	Note <sup>1)</sup>
<b>Organization</b>	<b>2 GB</b>	<b>2 GB</b>		
	<b>×64</b>	<b>×72</b>		
	<b>2 Ranks</b>	<b>2 Ranks</b>		
	<b>-5</b>	<b>-5</b>		
$I_{DD0}$	606	681	mA	2)
$I_{DD1}$	686	771	mA	2)
$I_{DD2N}$	560	630	mA	3)
$I_{DD2P}$	91	103	mA	3)
$I_{DD2Q}$	448	504	mA	3)
$I_{DD3N}$	640	720	mA	3)
$I_{DD3P\_0}$ (fast)	208	234	mA	3)
$I_{DD3P\_1}$ (slow)	96	108	mA	3)
$I_{DD4R}$	966	1086	mA	2)
$I_{DD4W}$	926	1041	mA	2)
$I_{DD5B}$	1486	1671	mA	2)
$I_{DD5D}$	112	126	mA	3)4)
$I_{DD6}$	92	103	mA	3)4)
$I_{DD7}$	1686	1896	mA	2)

1) Calculated values from component data. ODT disabled.  $I_{DD1}$ ,  $I_{DD4R}$ , and  $I_{DD7}$ , are defined with the outputs disabled.

2) The other rank is in  $I_{DD2P}$  Precharge Power-Down Current mode

3) Both ranks are in the same  $I_{DD}$  current mode

4)  $I_{DD5D}$  and  $I_{DD6}$  values are for  $0^{\circ}\text{C} \leq T_{\text{Case}} \leq 85^{\circ}\text{C}$



## 4 SPD Codes

This chapter lists all hexadecimal byte values stored in the EEPROM of the products described in this data sheet. SPD stands for serial presence detect. All values with XX in the table are module specific bytes which are defined during production.

### List of SPD Code Tables

- Table 28 “SPD codes for HYS64T256020HU-3-A” on Page 39
- Table 29 “SPD codes for HYS64T256020HU-3S-A” on Page 43
- Table 30 “SPD codes for HYS64T256020HU-3.7-A” on Page 47
- Table 31 “SPD codes for HYS64T256020HU-5-A” on Page 51

**TABLE 28**

SPD codes for HYS64T256020HU-3-A

Product Type		HYS64T256020HU-3-A	HYS72T256020HU-3-A
Organization		2 GByte	2 GByte
		×64	×72
		2 Ranks (×8)	2 Ranks (×8)
Label Code		PC2-5300U-444	PC2-5300E-444
JEDEC SPD Revision		Rev. 1.1	Rev. 1.1
Byte#	Description	HEX	HEX
0	Programmed SPD Bytes in EEPROM	80	80
1	Total number of Bytes in EEPROM	08	08
2	Memory Type (DDR2)	08	08
3	Number of Row Addresses	0E	0E
4	Number of Column Addresses	0A	0A
5	DIMM Rank and Stacking Information	61	61
6	Data Width	40	48
7	Not used	00	00
8	Interface Voltage Level	05	05
9	$t_{CK} @ CL_{MAX}$ (Byte 18) [ns]	30	30
10	$t_{AC}$ SDRAM @ $CL_{MAX}$ (Byte 18) [ns]	45	45
11	Error Correction Support (non-ECC, ECC)	00	02
12	Refresh Rate and Type	82	82
13	Primary SDRAM Width	08	08
14	Error Checking SDRAM Width	00	08
15	Not used	00	00
16	Burst Length Supported	0C	0C
17	Number of Banks on SDRAM Device	08	08
18	Supported CAS Latencies	38	38



HYS[64/72]T256xxxHU-[3/.../5]-A  
Unbuffered DDR2 SDRAM Modules

Product Type		HYS64T256020HU-3-A	HYS72T256020HU-3-A
Organization		2 GByte	2 GByte
		×64	×72
		2 Ranks (×8)	2 Ranks (×8)
Label Code		PC2-5300U-444	PC2-5300E-444
JEDEC SPD Revision		Rev. 1.1	Rev. 1.1
Byte#	Description	HEX	HEX
19	DIMM Mechanical Characteristics	00	00
20	DIMM Type Information	02	02
21	DIMM Attributes	00	00
22	Component Attributes	03	03
23	$t_{CK} @ CL_{MAX} -1$ (Byte 18) [ns]	30	30
24	$t_{AC}$ SDRAM @ $CL_{MAX} -1$ [ns]	45	45
25	$t_{CK} @ CL_{MAX} -2$ (Byte 18) [ns]	50	50
26	$t_{AC}$ SDRAM @ $CL_{MAX} -2$ [ns]	60	60
27	$t_{RP.MIN}$ [ns]	30	30
28	$t_{RRD.MIN}$ [ns]	1E	1E
29	$t_{RCD.MIN}$ [ns]	30	30
30	$t_{RAS.MIN}$ [ns]	2D	2D
31	Module Density per Rank	01	01
32	$t_{AS.MIN}$ and $t_{CS.MIN}$ [ns]	20	20
33	$t_{AH.MIN}$ and $t_{CH.MIN}$ [ns]	27	27
34	$t_{DS.MIN}$ [ns]	10	10
35	$t_{DH.MIN}$ [ns]	17	17
36	$t_{WR.MIN}$ [ns]	3C	3C
37	$t_{WTR.MIN}$ [ns]	1E	1E
38	$t_{RTP.MIN}$ [ns]	1E	1E
39	Analysis Characteristics	00	00
40	$t_{RC}$ and $t_{RFC}$ Extension	06	06
41	$t_{RC.MIN}$ [ns]	39	39
42	$t_{RFC.MIN}$ [ns]	7F	7F
43	$t_{CK.MAX}$ [ns]	80	80
44	$t_{DQSQ.MAX}$ [ns]	18	18
45	$t_{QHS.MAX}$ [ns]	22	22
46	PLL Relock Time	00	00
47	$T_{CASE.MAX}$ Delta / $\Delta T_{4R4W}$ Delta	50	50
48	Psi(T-A) DRAM	60	60
49	$\Delta T_0$ (DT0)	47	47
50	$\Delta T_{2N}$ (DT2N, UDIMM) or $\Delta T_{2Q}$ (DT2Q, RDIMM)	37	37
51	$\Delta T_{2P}$ (DT2P)	24	24





HYS[64/72]T256xxxHU-[3/.../5]-A  
Unbuffered DDR2 SDRAM Modules

Product Type		HYS64T256020HU-3-A	HYS72T256020HU-3-A
Organization		2 GByte	2 GByte
		×64	×72
		2 Ranks (×8)	2 Ranks (×8)
Label Code		PC2-5300U-444	PC2-5300E-444
JEDEC SPD Revision		Rev. 1.1	Rev. 1.1
Byte#	Description	HEX	HEX
52	$\Delta T_{3N}$ (DT3N)	28	28
53	$\Delta T_{3P.fast}$ (DT3P fast)	26	26
54	$\Delta T_{3P.slow}$ (DT3P slow)	1A	1A
55	$\Delta T_{4R}$ (DT4R) / $\Delta T_{4R4W}$ Sign (DT4R4W)	50	50
56	$\Delta T_{5B}$ (DT5B)	24	24
57	$\Delta T_7$ (DT7)	2F	2F
58	Psi(ca) PLL	00	00
59	Psi(ca) REG	00	00
60	$\Delta T_{PLL}$ (DTPLL)	00	00
61	$\Delta T_{REG}$ (DTREG) / Toggle Rate	00	00
62	SPD Revision	11	11
63	Checksum of Bytes 0-62	3B	4D
64	Manufacturer's JEDEC ID Code (1)	7F	7F
65	Manufacturer's JEDEC ID Code (2)	7F	7F
66	Manufacturer's JEDEC ID Code (3)	7F	7F
67	Manufacturer's JEDEC ID Code (4)	7F	7F
68	Manufacturer's JEDEC ID Code (5)	7F	7F
69	Manufacturer's JEDEC ID Code (6)	51	51
70	Manufacturer's JEDEC ID Code (7)	00	00
71	Manufacturer's JEDEC ID Code (8)	00	00
72	Module Manufacturer Location	xx	xx
73	Product Type, Char 1	36	37
74	Product Type, Char 2	34	32
75	Product Type, Char 3	54	54
76	Product Type, Char 4	32	32
77	Product Type, Char 5	35	35
78	Product Type, Char 6	36	36
79	Product Type, Char 7	30	30
80	Product Type, Char 8	32	32
81	Product Type, Char 9	30	30
82	Product Type, Char 10	48	48
83	Product Type, Char 11	55	55
84	Product Type, Char 12	33	33



HYS[64/72]T256xxxHU-[3/.../5]-A  
Unbuffered DDR2 SDRAM Modules

Product Type		HYS64T256020HU-3-A	HYS72T256020HU-3-A
Organization		2 GByte	2 GByte
		×64	×72
		2 Ranks (×8)	2 Ranks (×8)
Label Code		PC2-5300U-444	PC2-5300E-444
JEDEC SPD Revision		Rev. 1.1	Rev. 1.1
Byte#	Description	HEX	HEX
85	Product Type, Char 13	41	41
86	Product Type, Char 14	20	20
87	Product Type, Char 15	20	20
88	Product Type, Char 16	20	20
89	Product Type, Char 17	20	20
90	Product Type, Char 18	20	20
91	Module Revision Code	7x	7x
92	Test Program Revision Code	xx	xx
93	Module Manufacturing Date Year	xx	xx
94	Module Manufacturing Date Week	xx	xx
95 - 98	Module Serial Number	xx	xx
99 - 127	Not used	00	00
128 - 255	Blank for customer use	FF	FF



HYS[64/72]T256xxxHU-[3/.../5]-A  
Unbuffered DDR2 SDRAM Modules

**TABLE 29**  
SPD codes for HYS64T256020HU-3S-A

Product Type		HYS64T256020HU-3S-A	HYS72T256020HU-3S-A
Organization		2 GByte	2 GByte
		×64	×72
		2 Ranks (×8)	2 Ranks (×8)
Label Code		PC2-5300U-555	PC2-5300E-555
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2
Byte#	Description	HEX	HEX
0	Programmed SPD Bytes in EEPROM	80	80
1	Total number of Bytes in EEPROM	08	08
2	Memory Type (DDR2)	08	08
3	Number of Row Addresses	0E	0E
4	Number of Column Addresses	0A	0A
5	DIMM Rank and Stacking Information	61	61
6	Data Width	40	48
7	Not used	00	00
8	Interface Voltage Level	05	05
9	$t_{CK} @ CL_{MAX}$ (Byte 18) [ns]	30	30
10	$t_{AC}$ SDRAM @ $CL_{MAX}$ (Byte 18) [ns]	45	45
11	Error Correction Support (non-ECC, ECC)	00	02
12	Refresh Rate and Type	82	82
13	Primary SDRAM Width	08	08
14	Error Checking SDRAM Width	00	08
15	Not used	00	00
16	Burst Length Supported	0C	0C
17	Number of Banks on SDRAM Device	08	08
18	Supported CAS Latencies	38	38
19	DIMM Mechanical Characteristics	01	01
20	DIMM Type Information	02	02
21	DIMM Attributes	00	00
22	Component Attributes	03	03
23	$t_{CK} @ CL_{MAX} -1$ (Byte 18) [ns]	3D	3D
24	$t_{AC}$ SDRAM @ $CL_{MAX} -1$ [ns]	50	50
25	$t_{CK} @ CL_{MAX} -2$ (Byte 18) [ns]	50	50
26	$t_{AC}$ SDRAM @ $CL_{MAX} -2$ [ns]	60	60
27	$t_{RP.MIN}$ [ns]	3C	3C
28	$t_{RRD.MIN}$ [ns]	1E	1E
29	$t_{RCD.MIN}$ [ns]	3C	3C



HYS[64/72]T256xxxHU-[3/.../5]-A  
Unbuffered DDR2 SDRAM Modules

Product Type		HYS64T256020HU-3S-A	HYS72T256020HU-3S-A
Organization		2 GByte	2 GByte
		×64	×72
		2 Ranks (×8)	2 Ranks (×8)
Label Code		PC2-5300U-555	PC2-5300E-555
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2
Byte#	Description	HEX	HEX
30	$t_{RAS.MIN}$ [ns]	2D	2D
31	Module Density per Rank	01	01
32	$t_{AS.MIN}$ and $t_{CS.MIN}$ [ns]	20	20
33	$t_{AH.MIN}$ and $t_{CH.MIN}$ [ns]	27	27
34	$t_{DS.MIN}$ [ns]	10	10
35	$t_{DH.MIN}$ [ns]	17	17
36	$t_{WR.MIN}$ [ns]	3C	3C
37	$t_{WTR.MIN}$ [ns]	1E	1E
38	$t_{RTP.MIN}$ [ns]	1E	1E
39	Analysis Characteristics	00	00
40	$t_{RC}$ and $t_{RFC}$ Extension	06	06
41	$t_{RC.MIN}$ [ns]	3C	3C
42	$t_{RFC.MIN}$ [ns]	7F	7F
43	$t_{CK.MAX}$ [ns]	80	80
44	$t_{DQSQ.MAX}$ [ns]	18	18
45	$t_{QHS.MAX}$ [ns]	22	22
46	PLL Relock Time	00	00
47	$T_{CASE.MAX}$ Delta / $\Delta T_{4R4W}$ Delta	50	50
48	Psi(T-A) DRAM	58	58
49	$\Delta T_0$ (DT0)	37	37
50	$\Delta T_{2N}$ (DT2N, UDIMM) or $\Delta T_{2Q}$ (DT2Q, RDIMM)	32	32
51	$\Delta T_{2P}$ (DT2P)	21	21
52	$\Delta T_{3N}$ (DT3N)	24	24
53	$\Delta T_{3P.fast}$ (DT3P fast)	23	23
54	$\Delta T_{3P.slow}$ (DT3P slow)	17	17
55	$\Delta T_{4R}$ (DT4R) / $\Delta T_{4R4W}$ Sign (DT4R4W)	4A	4A
56	$\Delta T_{5B}$ (DT5B)	21	21
57	$\Delta T_7$ (DT7)	28	28
58	Psi(ca) PLL	00	00
59	Psi(ca) REG	00	00
60	$\Delta T_{PLL}$ (DTPLL)	00	00
61	$\Delta T_{REG}$ (DTREG) / Toggle Rate	00	00
62	SPD Revision	12	12



HYS[64/72]T256xxxHU-[3/.../5]-A  
Unbuffered DDR2 SDRAM Modules

Product Type		HYS64T256020HU-3S-A	HYS72T256020HU-3S-A
Organization		2 GByte	2 GByte
		×64	×72
		2 Ranks (×8)	2 Ranks (×8)
Label Code		PC2-5300U-555	PC2-5300E-555
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2
Byte#	Description	HEX	HEX
63	Checksum of Bytes 0-62	36	48
64	Manufacturer's JEDEC ID Code (1)	7F	7F
65	Manufacturer's JEDEC ID Code (2)	7F	7F
66	Manufacturer's JEDEC ID Code (3)	7F	7F
67	Manufacturer's JEDEC ID Code (4)	7F	7F
68	Manufacturer's JEDEC ID Code (5)	7F	7F
69	Manufacturer's JEDEC ID Code (6)	51	51
70	Manufacturer's JEDEC ID Code (7)	00	00
71	Manufacturer's JEDEC ID Code (8)	00	00
72	Module Manufacturer Location	xx	xx
73	Product Type, Char 1	36	37
74	Product Type, Char 2	34	32
75	Product Type, Char 3	54	54
76	Product Type, Char 4	32	32
77	Product Type, Char 5	35	35
78	Product Type, Char 6	36	36
79	Product Type, Char 7	30	30
80	Product Type, Char 8	32	32
81	Product Type, Char 9	30	30
82	Product Type, Char 10	48	48
83	Product Type, Char 11	55	55
84	Product Type, Char 12	33	33
85	Product Type, Char 13	53	53
86	Product Type, Char 14	41	41
87	Product Type, Char 15	20	20
88	Product Type, Char 16	20	20
89	Product Type, Char 17	20	20
90	Product Type, Char 18	20	20
91	Module Revision Code	5x	5x
92	Test Program Revision Code	xx	xx
93	Module Manufacturing Date Year	xx	xx
94	Module Manufacturing Date Week	xx	xx
95 - 98	Module Serial Number	xx	xx

HYS[64/72]T256xxxHU-[3/.../5]-A  
Unbuffered DDR2 SDRAM Modules

<b>Product Type</b>		<b>HYS64T256020HU-3S-A</b>	<b>HYS72T256020HU-3S-A</b>
<b>Organization</b>		<b>2 GByte</b>	<b>2 GByte</b>
		<b>×64</b>	<b>×72</b>
		<b>2 Ranks (×8)</b>	<b>2 Ranks (×8)</b>
<b>Label Code</b>		<b>PC2-5300U-555</b>	<b>PC2-5300E-555</b>
<b>JEDEC SPD Revision</b>		<b>Rev. 1.2</b>	<b>Rev. 1.2</b>
<b>Byte#</b>	<b>Description</b>	<b>HEX</b>	<b>HEX</b>
99 - 127	Not used	00	00
128 - 255	Blank for customer use	FF	FF



HYS[64/72]T256xxxHU-[3/.../5]-A  
Unbuffered DDR2 SDRAM Modules

**TABLE 30**  
SPD codes for HYS64T256020HU-3.7-A

Product Type		HYS64T256020HU-3.7-A	HYS72T256020HU-3.7-A
Organization		2 GByte	2 GByte
		×64	×72
		2 Ranks (×8)	2 Ranks (×8)
Label Code		PC2-4200U-444	PC2-4200E-444
JEDEC SPD Revision		Rev. 1.1	Rev. 1.1
Byte#	Description	HEX	HEX
0	Programmed SPD Bytes in EEPROM	80	80
1	Total number of Bytes in EEPROM	08	08
2	Memory Type (DDR2)	08	08
3	Number of Row Addresses	0E	0E
4	Number of Column Addresses	0A	0A
5	DIMM Rank and Stacking Information	61	61
6	Data Width	40	48
7	Not used	00	00
8	Interface Voltage Level	05	05
9	$t_{CK} @ CL_{MAX}$ (Byte 18) [ns]	3D	3D
10	$t_{AC}$ SDRAM @ $CL_{MAX}$ (Byte 18) [ns]	50	50
11	Error Correction Support (non-ECC, ECC)	00	02
12	Refresh Rate and Type	82	82
13	Primary SDRAM Width	08	08
14	Error Checking SDRAM Width	00	08
15	Not used	00	00
16	Burst Length Supported	0C	0C
17	Number of Banks on SDRAM Device	08	08
18	Supported CAS Latencies	38	38
19	DIMM Mechanical Characteristics	00	00
20	DIMM Type Information	02	02
21	DIMM Attributes	00	00
22	Component Attributes	01	01
23	$t_{CK} @ CL_{MAX} -1$ (Byte 18) [ns]	3D	3D
24	$t_{AC}$ SDRAM @ $CL_{MAX} -1$ [ns]	50	50
25	$t_{CK} @ CL_{MAX} -2$ (Byte 18) [ns]	50	50
26	$t_{AC}$ SDRAM @ $CL_{MAX} -2$ [ns]	60	60
27	$t_{RP.MIN}$ [ns]	3C	3C
28	$t_{RRD.MIN}$ [ns]	1E	1E
29	$t_{RCD.MIN}$ [ns]	3C	3C



HYS[64/72]T256xxxHU-[3/.../5]-A  
Unbuffered DDR2 SDRAM Modules

Product Type		HYS64T256020HU-3.7-A	HYS72T256020HU-3.7-A
Organization		2 GByte	2 GByte
		×64	×72
		2 Ranks (×8)	2 Ranks (×8)
Label Code		PC2-4200U-444	PC2-4200E-444
JEDEC SPD Revision		Rev. 1.1	Rev. 1.1
Byte#	Description	HEX	HEX
30	$t_{RAS.MIN}$ [ns]	2D	2D
31	Module Density per Rank	01	01
32	$t_{AS.MIN}$ and $t_{CS.MIN}$ [ns]	25	25
33	$t_{AH.MIN}$ and $t_{CH.MIN}$ [ns]	37	37
34	$t_{DS.MIN}$ [ns]	10	10
35	$t_{DH.MIN}$ [ns]	22	22
36	$t_{WR.MIN}$ [ns]	3C	3C
37	$t_{WTR.MIN}$ [ns]	1E	1E
38	$t_{RTP.MIN}$ [ns]	1E	1E
39	Analysis Characteristics	00	00
40	$t_{RC}$ and $t_{RFC}$ Extension	06	06
41	$t_{RC.MIN}$ [ns]	3C	3C
42	$t_{RFC.MIN}$ [ns]	7F	7F
43	$t_{CK.MAX}$ [ns]	80	80
44	$t_{DQSQ.MAX}$ [ns]	1E	1E
45	$t_{QHS.MAX}$ [ns]	28	28
46	PLL Relock Time	00	00
47	$T_{CASE.MAX}$ Delta / $\Delta T_{4R4W}$ Delta	51	51
48	Psi(T-A) DRAM	60	60
49	$\Delta T_0$ (DT0)	37	37
50	$\Delta T_{2N}$ (DT2N, UDIMM) or $\Delta T_{2Q}$ (DT2Q, RDIMM)	2A	2A
51	$\Delta T_{2P}$ (DT2P)	23	23
52	$\Delta T_{3N}$ (DT3N)	1E	1E
53	$\Delta T_{3P.fast}$ (DT3P fast)	1F	1F
54	$\Delta T_{3P.slow}$ (DT3P slow)	16	16
55	$\Delta T_{4R}$ (DT4R) / $\Delta T_{4R4W}$ Sign (DT4R4W)	43	43
56	$\Delta T_{5B}$ (DT5B)	22	22
57	$\Delta T_7$ (DT7)	2A	2A
58	Psi(ca) PLL	00	00
59	Psi(ca) REG	00	00
60	$\Delta T_{PLL}$ (DTPLL)	00	00
61	$\Delta T_{REG}$ (DTREG) / Toggle Rate	00	00
62	SPD Revision	11	11





HYS[64/72]T256xxxHU-[3/.../5]-A  
Unbuffered DDR2 SDRAM Modules

Product Type		HYS64T256020HU-3.7-A	HYS72T256020HU-3.7-A
Organization		2 GByte	2 GByte
		×64	×72
		2 Ranks (×8)	2 Ranks (×8)
Label Code		PC2-4200U-444	PC2-4200E-444
JEDEC SPD Revision		Rev. 1.1	Rev. 1.1
Byte#	Description	HEX	HEX
63	Checksum of Bytes 0-62	6A	7C
64	Manufacturer's JEDEC ID Code (1)	7F	7F
65	Manufacturer's JEDEC ID Code (2)	7F	7F
66	Manufacturer's JEDEC ID Code (3)	7F	7F
67	Manufacturer's JEDEC ID Code (4)	7F	7F
68	Manufacturer's JEDEC ID Code (5)	7F	7F
69	Manufacturer's JEDEC ID Code (6)	51	51
70	Manufacturer's JEDEC ID Code (7)	00	00
71	Manufacturer's JEDEC ID Code (8)	00	00
72	Module Manufacturer Location	xx	xx
73	Product Type, Char 1	36	37
74	Product Type, Char 2	34	32
75	Product Type, Char 3	54	54
76	Product Type, Char 4	32	32
77	Product Type, Char 5	35	35
78	Product Type, Char 6	36	36
79	Product Type, Char 7	30	30
80	Product Type, Char 8	32	32
81	Product Type, Char 9	30	30
82	Product Type, Char 10	48	48
83	Product Type, Char 11	55	55
84	Product Type, Char 12	33	33
85	Product Type, Char 13	2E	2E
86	Product Type, Char 14	37	37
87	Product Type, Char 15	41	41
88	Product Type, Char 16	20	20
89	Product Type, Char 17	20	20
90	Product Type, Char 18	20	20
91	Module Revision Code	5x	5x
92	Test Program Revision Code	xx	xx
93	Module Manufacturing Date Year	xx	xx
94	Module Manufacturing Date Week	xx	xx
95 - 98	Module Serial Number	xx	xx

HYS[64/72]T256xxxHU-[3/.../5]-A  
Unbuffered DDR2 SDRAM Modules

<b>Product Type</b>		<b>HYS64T256020HU-3.7-A</b>	<b>HYS72T256020HU-3.7-A</b>
<b>Organization</b>		<b>2 GByte</b>	<b>2 GByte</b>
		<b>×64</b>	<b>×72</b>
		<b>2 Ranks (×8)</b>	<b>2 Ranks (×8)</b>
<b>Label Code</b>		<b>PC2-4200U-444</b>	<b>PC2-4200E-444</b>
<b>JEDEC SPD Revision</b>		<b>Rev. 1.1</b>	<b>Rev. 1.1</b>
<b>Byte#</b>	<b>Description</b>	<b>HEX</b>	<b>HEX</b>
99 - 127	Not used	00	00
128 - 255	Blank for customer use	FF	FF



HYS[64/72]T256xxxHU-[3/.../5]-A  
Unbuffered DDR2 SDRAM Modules

**TABLE 31**  
SPD codes for HYS64T256020HU-5-A

Product Type		HYS64T256020HU-5-A	HYS72T256020HU-5-A
Organization		2 GByte	2 GByte
		×64	×72
		2 Ranks (×8)	2 Ranks (×8)
Label Code		PC2-3200U-333	PC2-3200E-333
JEDEC SPD Revision		Rev. 1.1	Rev. 1.1
Byte#	Description	HEX	HEX
0	Programmed SPD Bytes in EEPROM	80	80
1	Total number of Bytes in EEPROM	08	08
2	Memory Type (DDR2)	08	08
3	Number of Row Addresses	0E	0E
4	Number of Column Addresses	0A	0A
5	DIMM Rank and Stacking Information	61	61
6	Data Width	40	48
7	Not used	00	00
8	Interface Voltage Level	05	05
9	$t_{CK} @ CL_{MAX}$ (Byte 18) [ns]	50	50
10	$t_{AC}$ SDRAM @ $CL_{MAX}$ (Byte 18) [ns]	60	60
11	Error Correction Support (non-ECC, ECC)	00	02
12	Refresh Rate and Type	82	82
13	Primary SDRAM Width	08	08
14	Error Checking SDRAM Width	00	08
15	Not used	00	00
16	Burst Length Supported	0C	0C
17	Number of Banks on SDRAM Device	08	08
18	Supported CAS Latencies	38	38
19	DIMM Mechanical Characteristics	00	00
20	DIMM Type Information	02	02
21	DIMM Attributes	00	00
22	Component Attributes	01	01
23	$t_{CK} @ CL_{MAX} -1$ (Byte 18) [ns]	50	50
24	$t_{AC}$ SDRAM @ $CL_{MAX} -1$ [ns]	60	60
25	$t_{CK} @ CL_{MAX} -2$ (Byte 18) [ns]	50	50
26	$t_{AC}$ SDRAM @ $CL_{MAX} -2$ [ns]	60	60
27	$t_{RP.MIN}$ [ns]	3C	3C
28	$t_{RRD.MIN}$ [ns]	1E	1E
29	$t_{RCD.MIN}$ [ns]	3C	3C



HYS[64/72]T256xxxHU-[3/.../5]-A  
Unbuffered DDR2 SDRAM Modules

Product Type		HYS64T256020HU-5-A	HYS72T256020HU-5-A
Organization		2 GByte	2 GByte
		×64	×72
		2 Ranks (×8)	2 Ranks (×8)
Label Code		PC2-3200U-333	PC2-3200E-333
JEDEC SPD Revision		Rev. 1.1	Rev. 1.1
Byte#	Description	HEX	HEX
30	$t_{RAS.MIN}$ [ns]	28	28
31	Module Density per Rank	01	01
32	$t_{AS.MIN}$ and $t_{CS.MIN}$ [ns]	35	35
33	$t_{AH.MIN}$ and $t_{CH.MIN}$ [ns]	47	47
34	$t_{DS.MIN}$ [ns]	15	15
35	$t_{DH.MIN}$ [ns]	27	27
36	$t_{WR.MIN}$ [ns]	3C	3C
37	$t_{WTR.MIN}$ [ns]	28	28
38	$t_{RTP.MIN}$ [ns]	1E	1E
39	Analysis Characteristics	00	00
40	$t_{RC}$ and $t_{RFC}$ Extension	06	06
41	$t_{RC.MIN}$ [ns]	37	37
42	$t_{RFC.MIN}$ [ns]	7F	7F
43	$t_{CK.MAX}$ [ns]	80	80
44	$t_{DQSQ.MAX}$ [ns]	23	23
45	$t_{QHS.MAX}$ [ns]	2D	2D
46	PLL Relock Time	00	00
47	$T_{CASE.MAX}$ Delta / $\Delta T_{4R4W}$ Delta	51	51
48	Psi(T-A) DRAM	60	60
49	$\Delta T_0$ (DT0)	33	33
50	$\Delta T_{2N}$ (DT2N, UDIMM) or $\Delta T_{2Q}$ (DT2Q, RDIMM)	20	20
51	$\Delta T_{2P}$ (DT2P)	23	23
52	$\Delta T_{3N}$ (DT3N)	18	18
53	$\Delta T_{3P.fast}$ (DT3P fast)	18	18
54	$\Delta T_{3P.slow}$ (DT3P slow)	16	16
55	$\Delta T_{4R}$ (DT4R) / $\Delta T_{4R4W}$ Sign (DT4R4W)	35	35
56	$\Delta T_{5B}$ (DT5B)	21	21
57	$\Delta T_7$ (DT7)	25	25
58	Psi(ca) PLL	00	00
59	Psi(ca) REG	00	00
60	$\Delta T_{PLL}$ (DTPLL)	00	00
61	$\Delta T_{REG}$ (DTREG) / Toggle Rate	00	00
62	SPD Revision	11	11



HYS[64/72]T256xxxHU-[3/.../5]-A  
Unbuffered DDR2 SDRAM Modules

Product Type		HYS64T256020HU-5-A	HYS72T256020HU-5-A
Organization		2 GByte	2 GByte
		×64	×72
		2 Ranks (×8)	2 Ranks (×8)
Label Code		PC2-3200U-333	PC2-3200E-333
JEDEC SPD Revision		Rev. 1.1	Rev. 1.1
Byte#	Description	HEX	HEX
63	Checksum of Bytes 0-62	B5	C7
64	Manufacturer's JEDEC ID Code (1)	7F	7F
65	Manufacturer's JEDEC ID Code (2)	7F	7F
66	Manufacturer's JEDEC ID Code (3)	7F	7F
67	Manufacturer's JEDEC ID Code (4)	7F	7F
68	Manufacturer's JEDEC ID Code (5)	7F	7F
69	Manufacturer's JEDEC ID Code (6)	51	51
70	Manufacturer's JEDEC ID Code (7)	00	00
71	Manufacturer's JEDEC ID Code (8)	00	00
72	Module Manufacturer Location	xx	xx
73	Product Type, Char 1	36	37
74	Product Type, Char 2	34	32
75	Product Type, Char 3	54	54
76	Product Type, Char 4	32	32
77	Product Type, Char 5	35	35
78	Product Type, Char 6	36	36
79	Product Type, Char 7	30	30
80	Product Type, Char 8	32	32
81	Product Type, Char 9	30	30
82	Product Type, Char 10	48	48
83	Product Type, Char 11	55	55
84	Product Type, Char 12	35	35
85	Product Type, Char 13	41	41
86	Product Type, Char 14	20	20
87	Product Type, Char 15	20	20
88	Product Type, Char 16	20	20
89	Product Type, Char 17	20	20
90	Product Type, Char 18	20	20
91	Module Revision Code	5x	5x
92	Test Program Revision Code	xx	xx
93	Module Manufacturing Date Year	xx	xx
94	Module Manufacturing Date Week	xx	xx
95 - 98	Module Serial Number	xx	xx

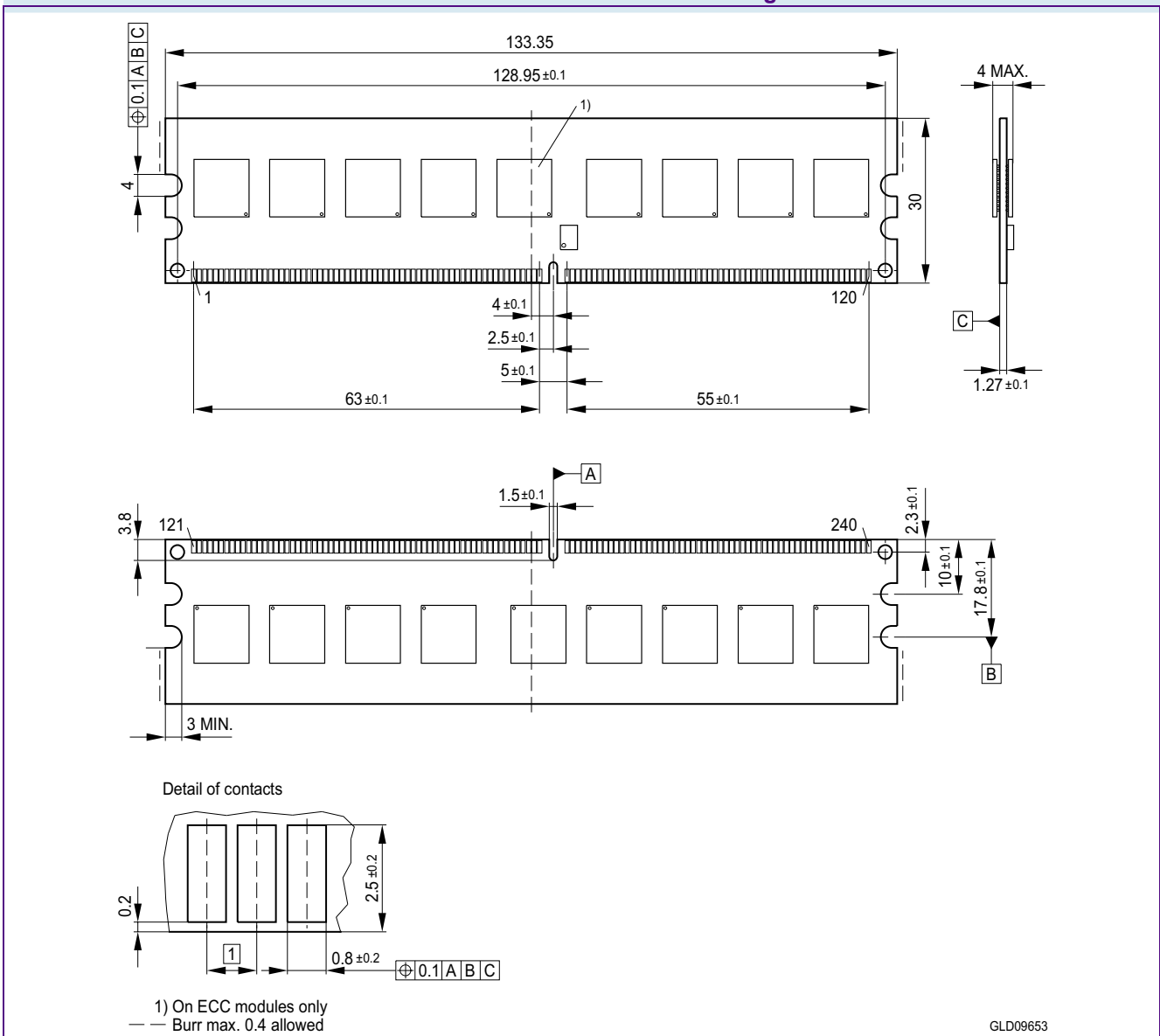
HYS[64/72]T256xxxHU-[3/.../5]-A  
Unbuffered DDR2 SDRAM Modules

<b>Product Type</b>		<b>HYS64T256020HU-5-A</b>	<b>HYS72T256020HU-5-A</b>
<b>Organization</b>		<b>2 GByte</b>	<b>2 GByte</b>
		<b>×64</b>	<b>×72</b>
		<b>2 Ranks (×8)</b>	<b>2 Ranks (×8)</b>
<b>Label Code</b>		<b>PC2-3200U-333</b>	<b>PC2-3200E-333</b>
<b>JEDEC SPD Revision</b>		<b>Rev. 1.1</b>	<b>Rev. 1.1</b>
<b>Byte#</b>	<b>Description</b>	<b>HEX</b>	<b>HEX</b>
99 - 127	Not used	00	00
128 - 255	Blank for customer use	FF	FF



# 5 Package Outlines

**FIGURE 6**  
Package Outline Raw Card B L-DIM-240-2



## Notes

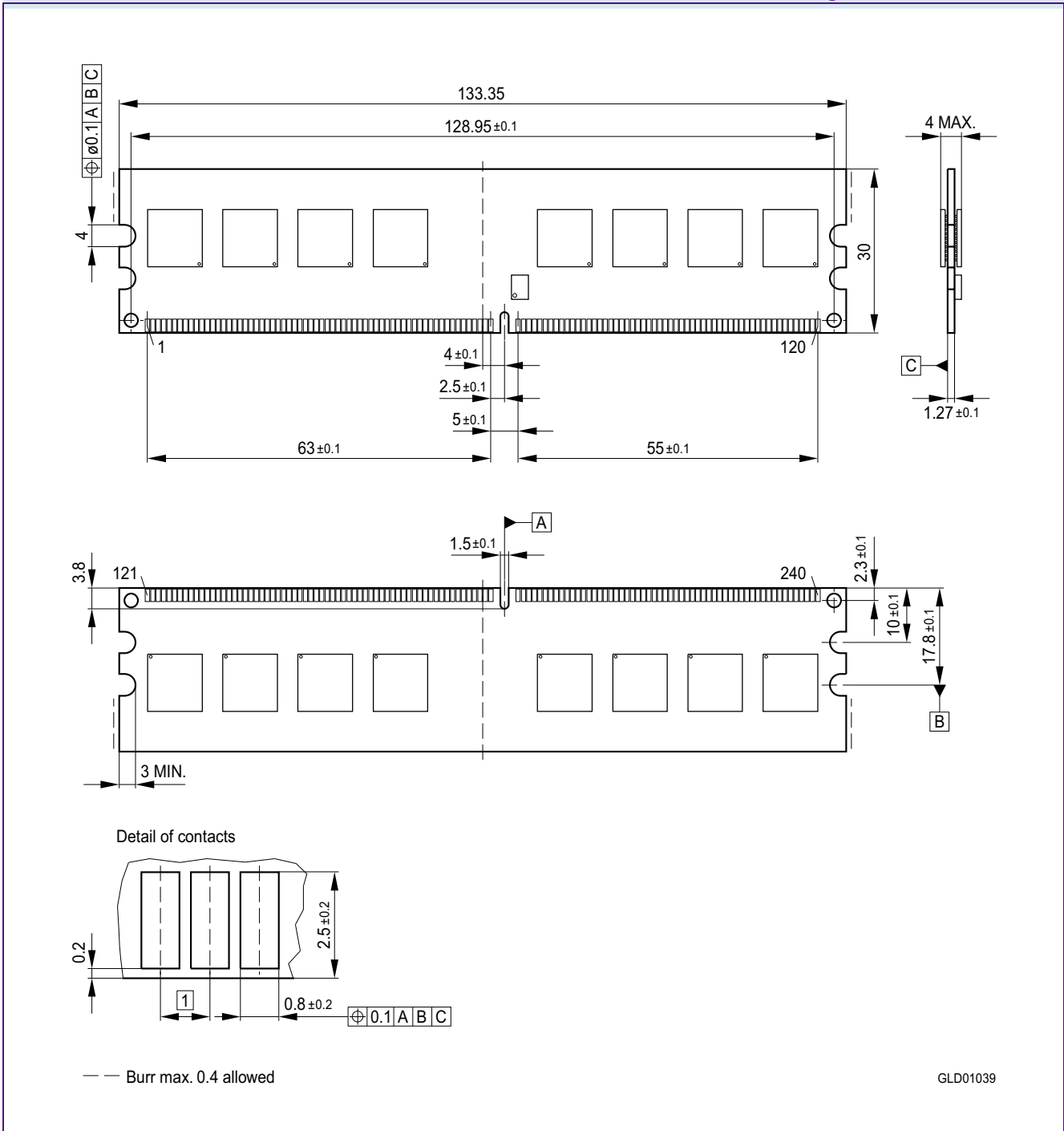
1. The chip is only found on ECC modules.
2. General tolerances +/- 0.15
3. Drawing according to ISO 8015







**FIGURE 8**  
Package Outline L-DIM-240-9



**Notes**

1. General tolerances +/- 0.15
2. Drawing according to ISO 8015



# 6 Product Type Nomenclature (DDR2 DRAMs and DIMMs)

Qimonda’s nomenclature uses simple coding combined with some proprietary coding. **Table 32** provides examples for module and component product type number as well as the field number. The detailed field description together with possible values and coding explanation is listed for modules in **Table 33** and for components in **Table 34**.

**TABLE 32**  
Nomenclature Fields and Examples

Example for	Field Number										
	1	2	3	4	5	6	7	8	9	10	11
Micro-DIMM	HYS	64	T	64/128	0	2	0	K	M	-5	-A
DDR2 DRAM	HYB	18	T	512/1G	16		0	A	C	-5	

**TABLE 33**  
DDR2 DIMM Nomenclature

Field	Description	Values	Coding
1	Qimonda Module Prefix	HYS	Constant
2	Module Data Width [bit]	64	Non-ECC
		72	ECC
3	DRAM Technology	T	DDR2
4	Memory Density per I/O [Mbit]; Module Density <sup>1)</sup>	32	256 MByte
		64	512 MByte
		128	1 GByte
		256	2 GByte
		512	4 GByte
5	Raw Card Generation	0 .. 9	Look up table
6	Number of Module Ranks	0, 2, 4	1, 2, 4
7	Product Variations	0 .. 9	Look up table
8	Package, Lead-Free Status	A .. Z	Look up table
9	Module Type	D	SO-DIMM
		M	Micro-DIMM
		R	Registered
		U	Unbuffered
		F	Fully Buffered



HYS[64/72]T256xxxHU-[3/.../5]-A  
Unbuffered DDR2 SDRAM Modules

Field	Description	Values	Coding
10	Speed Grade	-2.5F	PC2-6400 5-5-5
		-2.5	PC2-6400 6-6-6
		-3	PC2-5300 4-4-4
		-3S	PC2-5300 5-5-5
		-3.7	PC2-4200 4-4-4
		-5	PC2-3200 3-3-3
11	Die Revision	-A	First
		-B	Second

1) Multiplying “Memory Density per I/O” with “Module Data Width” and dividing by 8 for Non-ECC and 9 for ECC modules gives the overall module memory density in MBytes as listed in column “Coding”.

**TABLE 34**  
DDR2 DRAM Nomenclature

Field	Description	Values	Coding
1	Qimonda Component Prefix	HYB	Constant
2	Interface Voltage [V]	18	SSTL_18
3	DRAM Technology	T	DDR2
4	Component Density [Mbit]	256	256 Mbit
		512	512 Mbit
		1G	1 Gbit
		2G	2 Gbit
5+6	Number of I/Os	40	×4
		80	×8
		16	×16
7	Product Variations	0 .. 9	Look up table
8	Die Revision	A	First
		B	Second
9	Package, Lead-Free Status	C	FBGA, lead-containing
		F	FBGA, lead-free
10	Speed Grade	-25F	DDR2-800 5-5-5
		-2.5	DDR2-800 6-6-6
		-3	DDR2-667 4-4-4
		-3S	DDR2-667 5-5-5
		-3.7	DDR2-533 4-4-4
		-5	DDR2-400 3-3-3



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#### **Warnings**

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Qimonda Office.

Qimonda Components may only be used in life-support devices or systems with the express written approval of Qimonda, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.