DAVICOM Semiconductor, Inc.

DM9621A

USB2.0 to 10/100M Fast Ethernet Controller

DATA SHEET

Final

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1 Features

- **USB Interface**
  - USB2.0 Device
  - Support 12Mbps full speed operation
  - Support 480Mbps high speed operation
  - Support suspend mode and remote wake-up resume
  - Support USB standard commands
  - Support vendor specific commands
  - Efficient TX/RX FIFO auto management.
  - Embedded SRAM for RX/TX packet buffering
  - Supports 4 endpoints (Control, Interrupt, Bulk_IN, Bulk_OUT)
  - Supported Classes：USB Common Class / USB Communications Class

- **Ethernet**
  - Support IEEE802.3u 100BASE-TX and with IEEE802.3 10BASE-T standards
  - Support IEEE802.3x flow control function for 100BASE-TX and 10BASE-T.
  - Support IEEE 802.3az Energy Efficient Ethernet (EEE)
  - Built-in 10/100Mbps Fast-Ethernet PHY with Auto-MDIX
  - Supports RMII interface or 8 pins GPIO
  - Support Auto-Negotiation function
  - Back Pressure Mode for Half-Duplex mode flow Control
  - PAUSE frame for Full-Duplex flow control
  - Support Power management: Wake-on-LAN, ARP/NDP Offload
  - Supports GPIO, wakeup frame, link status change and Magic packet events for remote wake-up
  - Support TCP / UDP / IPv4 checksum offload checking and generating

- **EEPROM Interface**
  - Supports 128/256/512 bytes (93C46/93C56/93C66) of serial EEPROM(for storing USB Descriptors)
  - 93C46/93C56/93C66 auto-detection

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- **LED Indications**
  - Ethernet – Link / Act indication
  - Ethernet – Speed (10M / 100M) indication
  - USB speed indication (full / high speed + traffic modes)

- **Clock**
  - Single 25MHz / 30 ppm crystal or oscillator
  - Optional 12MHz crystal for USB

- **Power Input**
  - Low-Power, Single-Supply 3.3V, 0.18um CMOS Technology
  - Built in 3.3V to 1.8V regulator

- **Miscellaneous**
  - Very low power consumption in suspend mode
  - Power Reduced Mode (cable detection), and Power Down Mode
  - Compatible with 5.0V tolerant I/O

1.1 General Description

The DM9621A USB to 10/100Mbps Fast Ethernet controller is a high performance and highly integrated ASIC with embedded SSRAM for packet buffering. It enables low cost and affordable Fast Ethernet network connection to desktop, notebook PC, and embedded system using popular USB ports.

It has an USB interface to communicate with USB host controller and is compliant with USB specification V1.0, V1.1 and V2.0. It implements 10/100Mbps Ethernet LAN function based on IEEE802.3, and IEEE802.3u standards.

DM9621A integrates an on-chip 10/100Mbps Ethernet PHY to simplify system design and provides an optional Reduce media-independent interface (RMII).

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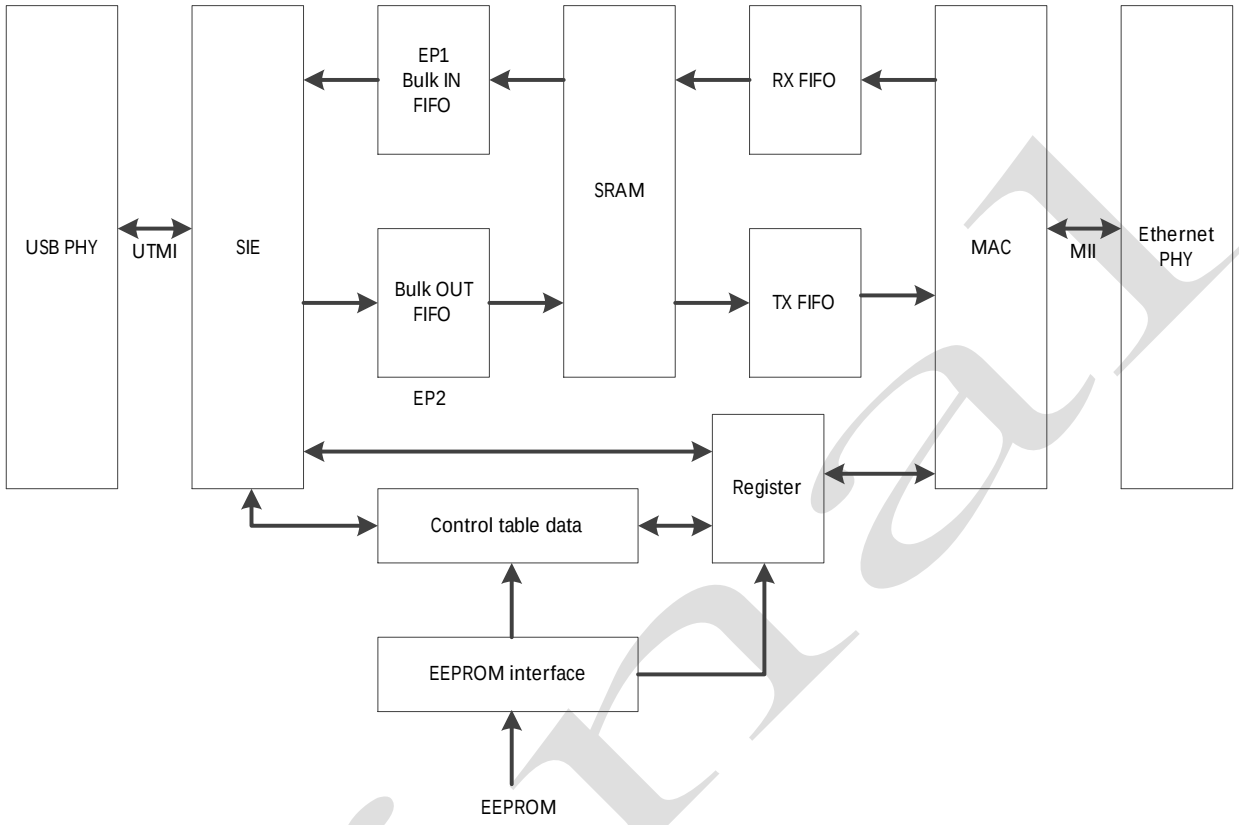
2 Block Diagram and Block Description



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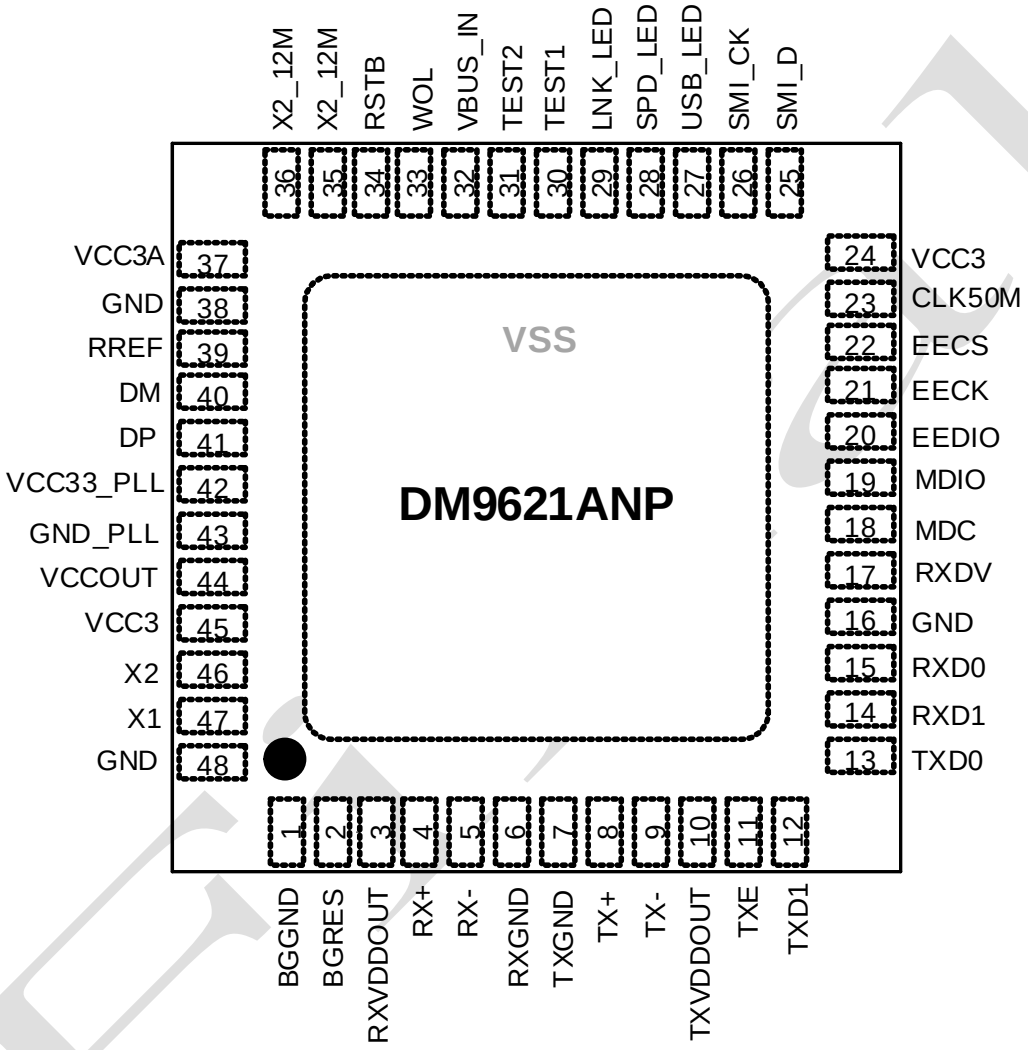
3 Pin Configuration

3.1 48-Pin QFN with RMII Interface



Note: The DM9621ANP IC employs a QFN package, which means the absence of a pin dedicated to ground (GND). In the QFN package, the GND is located at the bottom of the IC directly in the middle. Square is where the GND is connected. Exposed pad (VSS) on bottom of package must be connected to ground.

3.2 48-Pin QFN with RMII Interface

I = Input O = Output I/O = Input / Output
O/D = Open Drain P = Power

3.2.1 RMII Interface

Pin No.	Pin Name	I/O	Description
11	TXE	O	External RMII Transmit Enable GPIO2_0 in GPIO mode
12,13	TXD[1:0]	O	External RMII Transmit Data TXD[1] as GPIO2_1 in GPIO mode TXD[0] as GPIO2_2 in GPIO mode
14,15	RXD[1:0]	I	External RMII Receive Data RXD[1] as GPIO2_3 in GPIO mode RXD[0] as GPIO2_4 in GPIO mode
17	RXDV	I	External RMII Receive Data Valid GPIO2_5 in GPIO mode
18	MDC	O	MII Serial Management Data Clock
19	MDIO	I/O	MII Serial Management Data GPIO2_6 in GPIO mode
23	CLK50M	I	RMII 50MHz Clock GPIO2_7 in GPIO mode

3.2.2 EEPROM Interface

Pin No.	Pin Name	I/O	Description
20	EEDIO	I/O	Data to/from EEPROM
21	EECK	O	Clock to EEPROM
22	EECS	O	Chip Select to EEPROM

3.2.3 USB Interface

Pin No.	Pin Name	I/O	Description
37	VCC3A	P	3.3V for USB
38	GND	P	Ground for USB
39	RREF	I	Reference resistor to analog USB ground (12K 1% for USB)
40	DM	I/O	USB Data Minus
41	DP	I/O	USB Data Plus
42	VCC33_PLL	P	3.3V for USB PLL
43	GND_PLL	P	Ground for USB PLL
44	VCCOUT	O	1.8V power out for USB

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3.2.4 Clock Interface

Pin No.	Pin Name	I/O	Description
46	X2	O	Crystal 25MHz Out for Ethernet
47	X1	I	Crystal 25MHz In for Ethernet
35	X1_12M	I	Crystal 12MHz In for USB (Option, used when strap pin 22 EECS pull-high), Normal N.C. * Note1
36	X2_12M	O	Crystal 12MHz out for USB (Option, used when strap pin 22 EECS pull-high), Normal N.C. * Note1

* Note1: When strap pin 22 EECS pull-low, 12MHz clock from internal PLL, detail see 3.3 strap pins table (Page 11)

3.2.5 LED Interface

Pin No.	Pin Name	I/O	Description
27	USB_LED	O	USB LED Active low for USB HS mode Floating for USB FS mode Flash if traffic on USB
28	SPD_LED	O	SPEED LED Active low for Ethernet 100M Floating for Ethernet 10M
29	LNK_LED	O	Link LED Active low for Ethernet link Floating for Ethernet non-link Flash if traffic on Ethernet

3.2.5 10/100 PHY

Pin No.	Pin Name	I/O	Description
1	BGGND	P	Band gap ground.
2	BGRES	I/O	Band gap pin. Connect 6.98K 1% resister to GND
3	RXVDDOUT	O	1.8V power out for RX
4	RX+	I	TP RX input
5	RX-	I	TP RX input
6	RXGND	P	RX ground
7	TXGND	P	TX ground
8	TX+	O	TP TX output
9	TX-	O	TP TX output
10	TXVDDOUT	O	1.8V power out for TX power

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3.2.6 Miscellaneous

Pin No.	Pin Name	I/O	Description
25	SMI_D	I/O	Serial Management Interface Data. Tie to ground in application.
26	SMI_CK	I/O	Serial Management Interface Clock. Tie to ground in application. This pin can also as a GPIO wakeup event defined in register 0FH.
32	VBUS_IN	I	VBUS input Tie to high in bus power mode
33	WOL	O	Issue a wake-up signal when wake-up event happens.
34	RSTB	I	Hardware Reset Active low signal to initiate the DM9621A
31	TEST2	I	Test Mode 2, tie to ground in application.
30	TEST1	I	Define Pin11-15, 17-19 mode 1 = GPIO controlled by registers 34H~35H 0 = RMII

3.2.7 Power

Pin No.	Pin Name	I/O	Description
24,45	VCC3	P	Digital Power 3.3V
16,48	GND	P	Digital Ground

3.3 Strap Pin Table

1: pull-high 1K~10K, 0: default floating.

Pin No.	Pin Name	Description
12	TXD[1]	1 = EEPROM force to 93C46 type 0 = EEPROM type auto-detection
13	TXD[0]	RX packet header format 1 = 4-byte Ethernet RX header mode : The 4 bytes in Ethernet RX packet header are RX _flag, RX_status, byte_ctr_low, and byte_ctr_high respectively. 0 = 3-byte Ethernet RX packet header mode: The 3 bytes in Ethernet RX packet header are RX_status, byte_ctr_low, and byte_ctr_high respectively.
22	EECS	1 = 12MHz clock from external crystal 0 = 12MHz clock from internal PLL

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4 Vender Control an Status Register Set

The DM9621A implements several control and status registers, which can be accessed by the USB vendor register type commands. All CRs are set to their default values by hardware or software reset unless otherwise specified.

Register	Description	Offset	Default value after reset
NCR	Network Control Register	00H	00H
NSR	Network Status Register	01H	00H
TCR	TX Control Register	02H	00H
RCR	RX Control Register	05H	00H
RSR	RX Status Register	06H	00H
ROCR	Receive Overflow Counter Register	07H	00H
BPTR	Back Pressure Threshold Register	08H	37H
FCTR	Flow Control Threshold Register	09H	38H
FCR	RX Flow Control Register	0AH	00H
EPCR	EEPROM & PHY Control Register	0BH	00H
EPAR	EEPROM & PHY Address Register	0CH	40H
EPDRL	EEPROM & PHY Low Byte Data Register	0DH	Unknown
EPDRH	EEPROM & PHY High Byte Data Register	0EH	Unknown
WCR	Wake Up Control Register	0FH	00H
PAR	Physical Address Register	10H-15H	Determined by EEPROM
MAR	Multicast Address Register	16H-1DH	0000000000000080
GPCR	General Purpose Control Register	1EH	01H
GPR	General Purpose Register	1FH	Unknown
VID	Vendor ID	28H-29H	0A46H
PID	Product ID	2AH-2BH	9621H
CHIPR	CHIP revision	2CH	01H
TSCR	TX Special Control Register	2DH	00H
TCSCR	Transmit Check Sum Control Register	31H	00H
RCSCSR	Receive Check Sum Control Status Register	32H	00H
GPCR2	General Purpose Control Register 2	34H	00H
GPR2	General Purpose Register 2	35H	00H
EEP_CTRL	EEPROM and PHY Control Register	3AH	00H
PPCSR	Pause Packet Control Status Register	3DH	04H
TX_CTR	Transmit Packet Counter	81H	00H
UPERR	USB Packet Error Counter	82H	00H
CRC_CTR	Ethernet Receive Packet CRC Error Counter	83H	00H
EXCOL_CTR	Ethernet Transmit Excessive Collision Counter	84H	00H
COL_CTR	Ethernet Transmit Collision Counter	85H	00H
LCOL_CTR	Ethernet Transmit Late Collision Counter	86H	00H
MODE_CTL	Mode Control	91H	00H
SQUELCH	USB squelch Control	95H	04H
USB_ADR	USB Address	96H	00H
USBDA	USB device address register	F0H	00H
RXC	Received packet counter register	F1H	00H
TXC/USBS	Transmit packet counter/USB status register	F2H	10H
USBC	USB control register	F4H	00H

Key to Default

In the register description that follows, the default column takes the form:

<Reset Value>:

1 = Bit set to logic one
0 = Bit set to logic zero
X = No default value
P = power on reset default value
H = hardware reset command default value
S = software reset default value
E = default value from EEPROM
T = default value from strap pin

<Access Type>:

RO = Read only
RW = Read/Write
R/C = Read and Clear
RW/C1 = Read/Write and Cleared by write 1
WO = Write only

Reserved bits are shaded and should be written with 0.
Reserved bits are undefined on read access.

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4.1 Network Control Register (00H)

Bit	Name	Default	Description
7	EXT_PHY	PT0,RW	**External PHY Mode** (valid when pin TEST1 tie to ground) 1 = Select external PHY 0 = Select Internal PHY This bit can be forced by register 2EH bit 5.
6	WAKEEN	PE0,RW	**Wakeup Event Enable** This but enables the wakeup function. Clearing this bit will also clear all wakeup event status.
5	WCR_MODE	PHS,RW	**Write To Clear Mode** The following register bits are cleared by write ‘1”. Register 1 bit 2 and 3 Register 7 Register 0AH bit 2 Register 82H ~ 86H
4	FCOL	PHS0,RW	**Force Collision in Loopback Mode** Used for testing only.
3	FDX	PHS0,RW	**Full-Duplex Mode** 1 = Full-Duplex mode 0 = Half-Duplex mode Read only in Internal PHY mode. This bit can be written only in External PHY mode. This bit can also be forced by register 2EH bit 5 and 1.
2:1	LBK	PH00,RW	**Loopback Mode** 00 = Normal 01 = MAC internal loopback 10 = Internal PHY digital loopback 11 = Internal PHY analog loopback
0	RST	PH0,RW	**Software Reset** When write “1” to this bit, DM9621A enters software reset mode and will be automatically cleared after 10us. Write “0” to this bit can end the software reset mode.

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4.2 Network Status Register (01H)

Bit	Name	Default	Description
7	SPEED	PHS0, RW	**Media Speed Status** 1 = 10Mbps 0 = 100Mbps This bit is no meaning when LINKST=0. This bit read only in internal PHY mode and it can be written in external PHY mode. This bit can also be forced by register 2EH bit 5 and 2.
6	LINKST	PHS0, RO	**Link Status** 1 = Link OK 0 = Link failed This bit read only in internal PHY mode and it can be written in external PHY mode. This bit can also be forced by register 2EH bit 5 and 0.
5	WAKEST	P0, W/C1	**Wakeup Event Status** This bit is set when wakeup event status asserted. This bit is cleared by write “1” or when wakeup mode disabled.
4	RESERVED	PHS0, RO	Reserved
3	RESERVED	PHS0, RW/C1	Reserved
2	RESERVED	PHS0, RW/C1	Reserved
1	RXOV	PHS0, RO	**RX FIFO Overflow Status** This bit is set when RX FIFO free space is less than 544-byte This bit be cleared when RX FIFO free space is more than 2K.
0	RXRDY	PHS0, RO	**RX Packet Ready** This bit is set when there are one or more packets in RX FIFO.

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4.3 TX Control Register (02H)

Bit	Name	Default	Description
7	RESERVED	0,RO	Reserved
6	TJDIS	PHS0, RW	**Transmit Jabber Disable** The transmit Jabber Timer(2048 bytes) is disabled. Otherwise the transmit packet size can more than 2048-byte.
5	EXCECM	PHS0, RW	**Excessive Collision Mode Control** 1 = still try to transmit this packet 0 = abort this packet when excessive collision count more than 15
4	RESERVED	PHS0, RW	Reserved
3	RESERVED	PHS0, RW	Reserved
2	PAD_DIS1	PHS0, RW	**TX Packet PAD Append Control** 1 = the transmit packet size is unchanged from original setting 0 = the transmit packet size is appended to at least 64-byte
1	CRC_DIS1	PHS0, RW	**TX Packet Index II CRC Appends Control** 1 = the CRC field is not appended 0 = the CRC field is appended automatically
0	RESERVED	PHS0, RW	Reserved

4.4 RX Control Register (05H)

Bit	Name	Default	Description
7	HASHALL	PHS0,RW	Filter All Address in Hash Table
6	WTDIS	PHS0,RW	**Watchdog Timer Disable** When set, the Watchdog Timer(2048 bytes) is disabled and the RX packet may more than 2048-byte. When cleared, the Watchdog Timer(2048 bytes) is enabled and he RX packet is truncated after the data more than 2048-byte.
5	DIS_LONG	PHS0,RW	**Discard Long Packet** The packets with length over 1522-byte are discarded from RX memory.
4	DIS_CRC	PHS0,RW	**Discard CRC Error Packet** The packets with CRC error are discarded from RX memory.
3	ALL	PHS0,RW	**Pass All Multicast** The packets with multicast destination address are stored to RX memory.
2	RUNT	PHS0,RW	**Pass Runt Packet** The packets with size less than 64-byte are stored to RX memory.
1	PRMSC	PHS0,RW	**Promiscuous Mode** The destination address is do not be checked.
0	RXEN	PHS0,RW	**RX Enable** The received accepted packets can be stored to RX memory.

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4.5 RX Status Register (06H)

Bit	Name	Default	Description
7	RF	PHS0,RO	**Runt Frame** It is set to indicate the received frame has the size smaller than 64 bytes.
6	MF	PHS0,RO	**Multicast Frame** It is set to indicate the received frame has a multicast address.
5	LCS	PHS0,RO	**Late Collision Seen** It is set to indicate a late collision found during the frame reception.
4	RWTO	PHS0,RO	**Receive Watchdog Time-Out** It is set to indicate receive more than 2048 bytes.
3	PLE	PHS0,RO	**Physical Layer Error** It is set to indicate a physical layer error found during the frame reception.
2	AE	PHS0,RO	**Alignment Error** It is set to indicate the received frame ends with a non-byte boundary.
1	CE	PHS0,RO	**CRC Error** It is set to indicate the received frame ends with a CRC error.
0	FOE	PHS0,RO	**FIFO Overflow Error** It is set to indicate a FIFO Overflow error happens during the frame reception.

4.6 Receive Overflow Counter Register (07H)

07H can be cleared by writing any data this byte. They also can be cleared by read this byte if register 0H bit 5 is “0”.

Bit	Name	Default	Description
7	RXFU	PHS0, RW/C	**Receive Overflow Counter Overflow** This bit is set when the ROC has an overflow condition.
6:0	ROC	PHS0, RW/C	**Receive Overflow Counter** This is a statistic counter to indicate the received packet count upon FIFO overflow.

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4.7 Back Pressure Threshold Register (08H)

Bit	Name	Default	Description
7:4	BPHW	PHS3h, RW	Back Pressure High Water Overflow Threshold. MAC will generate the jam pattern when RX SRAM free space is lower than this threshold value. Default is 3K-byte free space. Please don't exceed SRAM size. (1 unit=1K bytes)
3:0	JPT	PHS7h, RW	Jam Pattern Time. Default is 100us. Bit3 Bit2 Bit1 Bit0 Time 0 0 0 0 2.5us 0 0 0 1 5us 0 0 1 0 7.5us 0 0 1 1 12.5us 0 1 0 0 25us 0 1 0 1 50us 0 1 1 0 75us 0 1 1 1 100us 1 0 0 0 125us 1 0 0 1 150us 1 0 1 0 175us 1 0 1 1 200us 1 1 0 0 2250us 1 1 0 1 250us 1 1 1 0 275us 1 1 1 1 300us

4.8 Flow Control Threshold Register (09H)

Bit	Name	Default	Description
7:4	HWOT	PHS3h, RW	**RX FIFO High Water Overflow Threshold** Send a pause packet with pause_time=FFFFH when the RX RAM free space is less than this value., If this value is zero, its meaning is no free RX SARM space. Default is 3K-byte free space. Please don't exceed SRAM size. (1 unit=1K bytes)
3:0	LWOT	PHS8h, RW	**RX FIFO Low Water Overflow Threshold** Send a pause packet with pause_time=0000 when RX SARM free space is larger than this value. This pause packet is enabled after high water pause packet transmitted. Default SRAM free space is 8K-byte. Please don't exceed SRAM size. (1 unit=1K bytes)

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4.9 RX/TX Flow Control Register (0AH)

Bit	Name	Default	Description
7	TXP0	PHS0,RW	**Force to TX Pause Packet with Time 0000H** This bit will be automatically cleared after pause packet transmission completion. Set to TX pause packet with time = 0000H.
6	TXPF	PHS0,RW	**Force to TX Pause Packet with Time FFFFH** This bit will be automatically cleared after pause packet transmission completion. Set to TX pause packet with time = FFFFH.
5	TXPEN	PHS0,RW	**TX Pause Packet Enable** Enable the pause packet for high/low water threshold of register 09H in Full-Duplex mode.
4	BKPA	PHS0,RW	**Back Pressure Packet Mode Enable** Generate a jam pattern when any packet coming and RX SRAM over BPHW of register 8H in Half-Duplex mode.
3	BKPM	PHS0,RW	**Back Pressure DA Mode** Generate a jam pattern when a packet's DA match and RX SRAM over BPHW of register 8H in Half-Duplex mode.
2	RXPS	PHS0, RW/C	**RX Pause Packet Status** This bit latched the RX pause packet in Full-Duplex mode. This bit can be cleared by write "1" to this bit or cleared automatically after read if register 0H bit 5 is "0".
1	RXPCS	PHS0,RO	**RX Pause Packet Current Status** When set, it indicated that the pause timer is not down count to "0" yet.
0	FLCE	PHS0,RW	**Flow Control Enable** When set, it enable the flow control mode(i.e. can to disable TX function).

4.10 EEPROM & PHY Control Register (0BH)

Bit	Name	Default	Description
7	NO_EEP	P0,RO	**EEPROM Absent** When set, it indicates the EEPROM 93C46 or 93C56/66 is not detected.
6	EE_TYPE	P0,RO	**EEPROM Type** 1 = 93C56/66 0 = 93C46
5	REEP	PH0,RW	**Reload EEPROM** The EEPROM is re-loaded. Driver needs to clear it after operation complete.
4	WEP	PH0,RW	**Write EEPROM Enable** The written ability of EEPROM is enabled.
3	EPOS	PH0,RW	**EEPROM or PHY Operation Select** When reset, select EEPROM; when set, select PHY.
2	ERPRR	PH0,RW	**EEPROM Read or PHY Register Read Command** Write "1" to start EEPROM or PHY read operation. This bit will be cleared after the completion of read operation.
1	ERPRW	PH0,RW	**EEPROM Write or PHY Register Write Command** Write "1" to start EEPROM or PHY write operation. This bit will be cleared after the completion of write operation.
0	ERRE	PH0,RO	**EEPROM Access Status or PHY Access Status** When set, it indicates that the EEPROM or PHY access is in progress.

4.11 EEPROM & PHY Address Register (0CH)

Bit	Name	Default	Description
7:6	PHY_ADR	PH01,RW	**PHY Address** bit [1:0] or EEPROM Word Address[7:6] If it is in PHY mode operation , the PHY address bit [4:2] is force to 0. Force to 01 if internal PHY is selected. Or EEPROM Word Address[7:6] if EEPROM 93C56/66 is used
5:0	EROA	PH0,RW	EEPROM Word Address[5:0] or PHY Register Number

4.12 EEPROM & PHY Data Register (EE_PHY_L：0DH EE_PHY_H：0EH)

Bit	Name	Default	Description
7:0	EE_PHY_L	X,RW	EEPROM or PHY Low Byte Data
7:0	EE_PHY_H	X,RW	EEPROM or PHY High Byte Data

4.13 Wake Up Control Register (0FH)

Bit	Name	Type	Description
7	SMI_EN	P0,RW	**SMI_C Event Enable** When set, enable SMI_C as GPIO Wake-up Event. This event occurred in 100ms low state and then 100ms high state in SMI_C pin
6	SMI_ST	P0,RO	**SMI_C Even Status** When set, indicates SMI_C Event occurred.
5	LINKEN	PE0,RW	**Link Change Event Enable** When set, enable Link Status Change Wake-up Event.
4	SAMPLEEN	PE0,RW	**Sample Frame Match Event Enable** When set, enable Sample Frame Wake-up Event.
3	MAGICEN	PE0,RW	**Magic Packet Event Enable** When set, enable Magic Packet Wake-up Event.
2	LINKST	P0,RO	**Link change Event Status** When set, indicates link change and Link Status Change Event occurred.
1	SAMPLEST	P0,RO	**Sample Frame Mtach Event Status** When set, indicates the sample frame is received and Sample Frame Event occurred. This bit will not be affected after a software reset.
0	MAGICST	P0,RO	**Magic Packet Event Status** When set, indicates the Magic Packet is received and Magic packet Event occurred. This bit will not be affected after a software reset.

4.14 Physical Address Register (10H~15H)

Bit	Name	Default	Description
7:0	PAB5	E,RW	Physical Address Byte 5 (15H)
7:0	PAB4	E,RW	Physical Address Byte 4 (14H)
7:0	PAB3	E,RW	Physical Address Byte 3 (13H)
7:0	PAB2	E,RW	Physical Address Byte 2 (12H)
7:0	PAB1	E,RW	Physical Address Byte 1 (11H)
7:0	PAB0	E,RW	Physical Address Byte 0 (10H)

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4.15 Multicast Address Register (16H~1DH)

Bit	Name	Default	Description
7:0	MAB7	P80,RW	Multicast Address Byte 7 (1DH)
7:0	MAB6	P00,RW	Multicast Address Byte 6 (1CH)
7:0	MAB5	P00,RW	Multicast Address Byte 5 (1BH)
7:0	MAB4	P00,RW	Multicast Address Byte 4 (1AH)
7:0	MAB3	P00,RW	Multicast Address Byte 3 (19H)
7:0	MAB2	P00,RW	Multicast Address Byte 2 (18H)
7:0	MAB1	P00,RW	Multicast Address Byte 1 (17H)
7:0	MAB0	P00,RW	Multicast Address Byte 0 (16H)

4.16 General Purpose Control Register (1EH)

Bit	Name	Default	Description
7:4	RESERVED	P0,RO	Reserved
3:0	RESERVED	P0111, RW	Reserved

4.17 General Purpose Register (1FH)

Bit	Name	Default	Description
7:4	RESERVED	P0,RO	Reserved
3:1	RESERVED	P0,RW	Reserved
0	GEPIO0	PE1,RW	**General Purpose** When the correspondent bit of General Purpose Control Register is 1, the value of the bit is output to pin GEPIO0. When the correspondent bit of General Purpose Control Register is 0, the value of the bit be read is reflected from pin GEPIO0. GEPIO0 default output 1 to POWER_DOWN internal PHY. Driver need to clear this POWER_DOWN signal by write “0” when it wants PHY active. If other device need, it also can refer this signal. This default value can be programmed by EEPROM. Please refer EEPROM description.

4.18 Vendor ID Register (28H~29H)

Bit	Name	Default	Description
7:0	VIDH	0AH,RO	Vendor ID high byte (29H)
7:0	VIDL	46H,RO	Vendor ID low byte (28H)

4.19 Product ID Register (2AH~2BH)

Bit	Name	Default	Description
7:0	PIDH	96H,R	Product ID high byte (2BH)
7:0	PIDL	20H,R	Product ID low byte (2AH)

4.20 Chip Revision Register (2CH)

Bit	Name	Default	Description
7:0	CHIPR	01H,RO	CHIP revision

4.21 TX Special Control Register (2DH)

Bit	Name	Default	Description
7	RESERVED	PH0,RW	Reserved
6	LCOL_TRY	PH0,RW	Late Collision Retry
5	RESERVED	PH0,RW	Reserved
3	RESERVED	PH0,RW	Reserved
3:0	TX_GAP	PH0,RW	TX Inter frame Gap 0XXX = 96-bit 1000 = 64-bit 1001 = 72-bit 1010 = 80-bit 1011 = 88-bit 1100 = 96-bit 1101 = 104-bit 1110 = 112-bit 1111 = 120-bit

4.22 External PHY Force Mode Control Register (2EH)

Bit	Name	Default	Description
7:6	RESERVED	0,RO	Reserved
5	EXTERNAL	HP0,RW	Force to external PHY mode
4	RESERVED	0,RO	Reserved
3	RESERVED	PH0,RW	Reserved
2	SPEED	HP0,RW	**Force external PHY Speed Mode** in MAC register 1 bit 7 1 = Force to 10Mbps mode 0 = Force to 100Mbps mode
1	DUPLEX	HP0,RW	**Force External PHY Duplex Mode** in MAC register 0 bit 3 1 = Force to Half-Duplex 0 = Force to Full-Duplex
0	LINK	HP0,RW	**Force external PHY Link Mode** in MAC register 1 bit 6 1 = Force to link OFF 0 = Force to link ON

4.23 Transmit Check Sum Control Register (31H)

Bit	Name	Default	Description
7:3	RESERVED	0,RO	Reserved
2	UDPCSE	HPS0,RW	UDP Checksum Generation Enable
1	TCPCSE	HPS0,RW	TCP Checksum Generation Enable
0	IPCSE	HPS0,RW	IP Checksum Generation Enable

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4.24 Receive Check Sum Control Status Register (32H)

Bit	Name	Default	Description
7	UDPS	HPS0,RO	**UDP Checksum Status** 1 = UDP packet checksum error 0 = UDP packet checksum OK, or this is not UDP packet
6	TCPS	HPS0,RO	**TCP Checksum Status** 1 = TCP packet checksum error 0 = TCP packet checksum OK, or this is not TCP packet
5	IPS	HPS0,RO	**IP Checksum Status** 1 = IP packet checksum error 0 = IP packet checksum OK, this is not IP packet
4	UDPP	HPS0,RO	UDP Packet
3	TCPP	HPS0,RO	TCP Packet
2	IPP	HPS0,RO	IP Packet
1	RCSEN	HPS0,RW	**Receive Checksum Checking Enable** The checksum status will store in packet first byte of status header in 4-byte RX header register 91h.bit7 mode.
0	DCSE	HPS0,RW	**Discard Checksum Error Packet** When set, if IP/TCP/UDP checksum field is error, this packet will be discarded.

4.25 External PHY Ceiver Address Register (33H)

Bit	Name	Default	Description
7	ADR_EN	HPS0,RW	**External PHY Address Enabled** When set in external MII mode, the external PHYceiver address is defined at bit 4:0.
6:5	Reserved	HPS0,RO	Reserved
4:0	EPHYADR	HPS01, RW	**External PHY Address Bit 4:0** The PHY address in external MII mode.

4.26 General Purpose Control Register 2 (34H)

Bit	Name	Default	Description
7:0	GPC2	HP0,RW	**General Purpose Control 2** Define the input mode (“0”,) or output mode (“1”) of pins GP_GRP2. Where the GP_GRP2 are pins GPIO2 listed in pin description

4.27 General Purpose Register 2 (35H)

Bit	Name	Default	Description
7:0	GPD2	HP0,RW	**General Purpose Register 2 Data** When the correspondent bit of General Purpose Control Register 2 is set, i.e. output mode, the value of the bit is reflected to pins GP_GPR2 When the correspondent bit of General Purpose Control Register 2 is 0, i.e. input mode, the value of the bit to be read is reflected from correspondent pins GP_GPR2.

NOTE: DM9621/9621a no register 36H,37H

4.28 EEPROM and PHY Control Register (3AH)

Bit	Name	Default	Description
7	FORCE_46	PT0,RW	Force EEPROM to 93C46 type
6	DET_46	P0,RO	Auto-detect EEPROM as 93C46
5	DET_56	P0,RO	Auto-detect EEPROM as 93C56/66
4:3	EECK_SPD	P0,RW	**Re-define EEPROM EECK speed** 00=0.2Mhz, 01=0.5MHz, 10=1MHz, 11=2MHz
2	NO_PRE	P0,RW	Do no generate Ethernet PHY preamble in MDIO
1:0	MDC_SPD	P0,RW	**Re-define Ethernet PHY MDC speed** 00=1Mhz, 01=3.1MHz, 10=12.5MHz, 11=0.25MHz

4.29 Pause Packet Control/Status Register (3DH)

Bit	Name	Default	Description
7:4	PAUSE_CTR	P0,RO	**Pause Packet Counter** The Pause packet counter before RX SRAM flow control low threshold reached.
3:0	PAUSE_MAX	PHS4, RW	**Max. Pause Packet Count** The maximum pause packet with timer FFFFH is transmit, when the RX SRAM is still in high threshold when pause timer timeout.

4.30 IEEE802.3az Enter Time Register (3EH)

Bit	Name	Default	Description
7	RESERVED	P,RO	Reserved
6:0	ENTER_TIME	PHS5, RW	**Timer to Enter EEE LPI Mode** (unit 2us) When the idle time of transmit is greater than this timer, the DM9621A enter Low Power Idle mode.

4.31 IEEE802.3az Leave Time Register (3FH)

Bit	Name	Default	Description
7	EEE_EN	P0,RO	EEE Enable
6:0	LEAVE_TIME	PHSF, RW	**Timer to Leave EEE LPI Mode** (unit 2us) In Low Power Idle mode, when the TX SRAM have packets to be transmit, the DM9621A enter normal operation mode after this timer timeout.

4.32 Link Up/Down Wakeup Event Register (51H)

Bit	Name	Default	Description
7:2	RESERVED	P,RO	Reserved
1	LINK_DW_D	PHS0, RW	**Link Down WOL Control** 1 = Enable link down wakeup event 0 = Disable link down wakeup event
0	LINK_UP_D	PHS1, RW	**Link UP WOL Control** 1 = Enable link up wakeup event 0 = Disable link up wakeup event

4.33 IPv6 NA/ARP Register (52H)

Bit	Name	Default	Description
7:4	RESERVED	P,RO	Reserved
3	IPV6_ND_A	PHS0, RW	**IPv6 Neighbor Solicitation Remote Address Control** 1= Enable to check remote address field 0 = Disable to check remote address field
2	IP_ARP_A	PHS0, RW	**IP ARP Request Destination IP Address Control** 1 = Enable to check DST IP address field 0 = Disable to check DST IP address field
1	IPV6_NA_E	PHS0, RW	**IPv6 Neighbor Advertisement Control** 1 = Enabled 0 = Disabled
0	IP_ARP_E	PHS0, RW	**IP ARP Offload Control** 1 = Enabled 0 = Disabled

4.34 Minimum RX SOF Control Register (58H)

Bit	Name	Default	Description
7:0	SOF_count	PS0,RO	**SOF Control Counter** The minimum SOF count to report packet ready in Multi-RX mode

4.35 Minimum RX Burst Counter Register (59H)

Bit	Name	Default	Description
7:0	RX_count	PS0,RO	**Multi-RX Mode** Minimum RX byte count (Unit: 512-byte) to report packet ready in Multi-RX mode.

4.36 Transmit Packet Counter (81H)

Bit	Name	Default	Description
7:0	TX_CTR	PS0,RO	**TX Packet Count** The TX packet count in TX SRAM.

4.37 USB Packet Error Counter (82H)

Bit	Name	Default	Description
7:0	USB_ERR	PHS0, RW/C	**USB Data Error Count** This counter is increased when there has been data CRC error in USB packet. This counter can be cleared by read if register 5 is “0” or by write to this register with any data.

4.38 Ethernet Receive Packet CRC Error Counter (83H)

Bit	Name	Default	Description
7:0	RX_ERR	PHS0, RW/C	**Ethernet RX Packet CRC Error Count** This counter is increased when there has been CRC error in Ethernet receive packet. This counter can be cleared by read if register 5 is “0” or by write to this register with any data.

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4.39 Ethernet Transmit Excessive Collision Counter (84H)

Bit	Name	Default	Description
7:0	ECOL_CTR	PHS0, RW/C	**Ethernet TX Packet Excessive Collision Count** This counter is increased when there has been excessive collision, i.e. continued 16 collisions, in Ethernet transmit packet. This counter can be cleared by read if register 5 is “0” or by write to this register with any data.

4.40 Ethernet Transmit Collision Counter (85H)

Bit	Name	Default	Description
7:0	COL_CTR	PHS0, RW/C	**Ethernet TX Packet Collision Count** This counter is increased when there has been collision in Ethernet transmit packet. This counter can be cleared by read if register 5 is “0” or by write to this register with any data.

4.41 Ethernet Transmit Late Collision Counter (86H)

Bit	Name	Default	Description
7:0	LCOL_CTR	PHS0, RW/C	**Ethernet TX Packet Late Collision Count** This counter is increased when there has been late collision in Ethernet transmit packet. This counter can be cleared by read if register 5 is “0” or by write to this register with any data.

4.42 RX Header Control/Status Register (91H)

Bit	Name	Default	Description
7	RX Header MODE	PT,RW	**RX Header Mode** Reference to sec. 7.1.3.1 1 = 4-byte RX header 0 = 3-byte RX header. This is compatible with DM9601.
6:4	RESERVED	P,RO	Reserved
3	Multi RX_USB	PT,RW	**USB Bulk IN Transfer for Ethernet RX Packet** 1 = Multiple Ethernet RX packets in one USB Bulk IN transfer 0 = Only one Ethernet RX packet in one USB Bulk IN transfer
2	Multi TX _ USB	PT,RW	**USB Bulk OUT Transfer for Ethernet TX Packet** 1 = Allow multiple Ethernet TX packets in one USB Bulk OUT transfer 0 = Only one Ethernet TX packet in one USB Bulk OUT transfer
1:0	RESERVED	P0,RW	Reserved

4.43 USB Squelch Control (95H)

Bit	Name	Default	Description
7:2	RESERVED	P0,RO	Reserved
2:0	SQUELCH	P101, RW	**Reference Voltage for USB Squelch Circuit** 000 for Reference voltage = 27.5mV 100 for Reference voltage = 137.5mV (default) 111 for Reference voltage = 220mV

4.44 USB Address (96H)

Bit	Name	Default	Description
7:0	USB_ADR	P0,RO	USB Address

4.45 USB Device Address Register (F0H)

Bit	Name	Default	Description
7	RESERVED	0,RO	Reserved
6:0	USBFA	0,RO	USB device address

4.46 Receive Packet Counter Register (F1H)

Bit	Name	Default	Description
7:0	RXC	0,RO	RXC is the packet counter received in SRAM

4.47 USB Status Register (F2H)

Bit	Name	Default	Description
7	RXFAULT	0,RC	Indicate RX has unexpected condition
6	SUSFLAG	0,RC	Indicate device has suspend condition
5	EP1RDY	0,RO	Indicate there are data ready for read from EP1 pipe
4	RESERVED	0,RO	Reserved
3	BOFAULT	0,RO	Indicate Bulk Out has unexpected condition
2	TXC2	0,RO	Represent there is full in transmit buffer
1	TXC1	0,RO	Represent there is almost full in transmit buffer
0	TXC0	0,RO	Represent there have packets in transmit buffer.

4.48 USB Control Register (F4H)

Bit	Name	Default	Description
7:6	RESERVED	0,RW	Reserved
5	EP3ACK	0,RW	When set and EP3_NAK=0, EP3 will always return 8-byte data to host per interrupt-interval
4	EP3NAK	0,RW	When set, EP3 will always return NAK.
3:1	RESERVED	0,RW	Reserved
0	MEMTST	0,RW	Before any memory-command, this bit must be set to 1. When in MEM_TST, TX/RX FIFO controller will be flushed.

Final

5 EEPROM Format

Name	Word	Offset	Description
MAC Address	0	0~5	6 byte Ethernet Address
Auto Load Control	3	6~7	If Bit 1:0 = 01: Update vendor ID and product ID If Bit 3:2 = 01: Reserved If Bit 5:4 = 01: Accept setting of WORD7[10] and WORD6 If Bit 7:6 = 01: Accept setting of WORD7[11,3:0] If Bit 9:8 = 01: Accept setting of WORD7[6:4] If Bit 11:10 = 01: Accept setting of WORD7[7] If Bit 13:12 = 01: Accept setting of WORD7[9:8] If Bit 15:14 = 01: Accept setting of WORD7[15:12], WORD11
Vendor ID	4	8~9	2 byte vendor ID (Default: 0A46h)
Product ID	5	10~11	2 byte product ID (Default: 9621h)
802.3az Control	6	12~13	Bit 6:0 = Load into register 3EH bit [6:0] Bit 14:8 = Load into register 3FH bit [6:0] Bit 15 = Load into register 3FH bit [7]
Wake-UP Mode Control	7	14~15	Bit 0:1 = WOL active low when set (default: active high) Bit 1:1 = WOL is pulse mode (default: level mode) Bit 2:1 = Wakeup event enabled, load into register 0 bit 6. (default: no) Bit 3 = Reserved Bit 4:1 = Magic wakeup event enabled if USB in suspend state (default: no) Bit 5:1 = link_change wakeup event enabled if USB in suspend state (default: no) Bit 6 = Reserved Bit 7 = LED mode 1 (default: 0) Bit 8:1 = Internal PHY is enabled after power-on (default: no) Bit 9:1 = Ethernet PHY in fiber mode (default: no) Bit 10 = Reserved Bit 11:1 = WOL SMI event enable, to register 0FH bit 7 (default: no) Bit 12:Reserved, set to “0” in application Bit 13:Reserved, set to “0” in application Bit 14:1 = Enable MDIX (default: yes) Bit 15 = Reserved, set to “0” in application
String1 Address	8	16	Vendor describe string start address
String1 Length	8	17	Vendor describe string length
String2 Address	9	18	Product describe string start address
String2 Length	9	19	Product describe string length
String3 Address	10	20	Product describe string start address
String3 Length	10	21	Product describe string length
USB Control	11	22~23	Bit 7:0 = USB maximum power. Unit is 2ma., default 5AH Bit 15:8 = USB class code
EP3 Interrupt Interval	12	24	Bit 3:0 EP3 interrupt interval, default 0BH

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6 PHY Register Description

ADD	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00	CONTROL	Reset	Loop Back	Speed select	Auto-N Enable	Power Down	Isolate	Restart Auto-N	Full Duplex	Coll. Test	Reserved						
		0	0	1	1	0	0	0	1	0	000_0000						
01	STATUS	T4 Cap.	TX FDX Cap.	TX HDX Cap.	10 FDX Cap.	10 HDX Cap.	Reserved				Pream. Supr.	Auto-N Compl.	Remote Fault	Auto-N Cap.	Link Status	Jabber Detect	Extd Cap.
		0	1	1	1	1	0000				1	0	0	1	0	0	1
02	PHYID1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1
03	PHYID2	1	0	1	1	1	0	Model No.						Version No.			
								001010						0000			
04	Auto-Neg. Advertise	Next Page	FLP Rcv Ack	Remote Fault	Reserved		FC Adv	T4 Adv	TX FDX Adv	TX HDX Adv	10 FDX Adv	10 HDX Adv	Advertised Protocol Selector Field				
05	Link Part. Ability	LP Next Page	LP Ack	LP RF	Reserved		LP FC	LP T4	LP TX FDX	LP TX HDX	LP 10 FDX	LP 10 HDX	Link Partner Protocol Selector Field				
06	Auto-Neg. Expansion	Reserved											Pardet Faul	LP Next Pg Able	Next Pg Able	New Pg Rcv	LP AutoN Cap.
10	Specified Config	BP 4B5B	BP SCR	BP ALIGN	BP_ ADPOK	Reserved	TX	Reserved	Reserved	Force 100LNK	Reserved	Reserved	RPDCTR-EN	Reset St. Mch	Pream. Supr.	Sleep mode	Reserved
11	Specified Conf/Sta	100 FDX	100 HDX	10 FDX	10 HDX	Reserved	Reserved	Reserved	PHY ADDR [4:0]					Auto-N. Monitor Bit [3:0]			
12	10T Conf/Stat	Rsvd	LP Enable	HBE Enable	SQUE Enable	JAB Enable	Reserved	Reserved									Polarity Reverse
13	PWDOR	Reserved							PD10DRV	PD100I	PDchip	PDcrm	PDaeq	PDdrv	PDecli	PDeclo	PD10
14	Specified Config	TSTSE1	TSTSE2	FORCE_ TXSD	FORCE_ FEF	PREAM BLEX	TX10M_ PWR	NWAY_ PWR	Reserved	MDIX_ CNTL	AutoNeg_ dlpbk	Mdix_fix Value	Mdix_ down	MonSel1	MonSel0	Reserved	PD_ value
1B	DSP_CTRL	DSP CONTROL															
1D	PSCR	Reserved				preamblex	amplitude	TX_PWR	Reserved								

Key to Default

In the register description that follows, the default column takes the form:

<Reset Value>:
- 1 Bit set to logic one
- 0 Bit set to logic zero
- X No default value
- (PIN#) Value latched in from pin # at reset

<Access Type>:
- RO = Read only
- RW = Read/Write

<Attribute(s)>:
- SC = Self clearing
- P = Value permanently set
- LL = Latching low
- LH = Latching high

6.1 Basic Mode Control Register (BMCR) – 00H

Bit	Bit Name	Default	Description
15	Reset	0,RW/SC	**Reset** 1 = Software reset 0 = Normal operation This bit sets the status and controls the PHY registers to their default states. This bit, which is self-clearing, will keep returning a value of one until the reset process is completed.
14	Loopback	0,RW	**Loopback** Loop-back control register 1 = Loop-back enabled 0 = Normal operation When in 100Mbps operation mode, setting this bit may cause the descrambler to lose synchronization and produce a 1300ms "dead time" before any valid data appear at the MII receive outputs
13	Speed Selection	1,RW	**Speed Select** 1 = 100Mbps 0 = 10Mbps Link speed may be selected either by this bit or by Auto-Negotiation. When Auto-Negotiation is enabled and bit 12 is set, this bit will return auto-negotiation selected media type.
12	Auto-Negotiation Enable	1,RW	**Auto-Negotiation Enable** 1 = Auto-Negotiation is enabled, bit 8 and 13 will be in Auto-Negotiation status
11	Power Down	0,RW	**Power Down** While in the power-down state, the PHY should respond to management transactions. During the transition to power-down state and while in the power-down state, the PHY should not generate spurious signals on the MII. 1 = Power down 0 = Normal operation
10	Isolate	0,RW	**Isolate** 1 = Isolates (Reserved) 0 = Normal operation
9	Restart Auto-Negotiation	0,RW/SC	**Restart Auto-Negotiation** 1 = Restart Auto-Negotiation. Re-initiates the Auto-Negotiation process. When Auto-Negotiation is disabled (bit 12 of this register cleared), this bit has no function and it should be cleared. This bit is self-clearing and it will keep returning a value of 1 until Auto-Negotiation is initiated by the PHY. The operation of the Auto-Negotiation process will not be affected by the management entity that clears this bit 0 = Normal operation
8	Duplex Dode	1,RW	**Duplex mode** 1 = Full-Duplex operation. Duplex selection is allowed when Auto-Negotiation is disabled (bit 12 of this register is cleared). With Auto-Negotiation enabled, this bit reflects the duplex capability selected by Auto-Negotiation 0 = Normal operation

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7	Collision Test	0,RW	**Collision Test** 1 = Collision test enabled. When set, this bit will cause the COL signal to be asserted in response to the assertion of TX_EN 0 = Normal operation
6:0	RESERVED	0,RO	**Reserved** Write as 0, ignore on read

6.2 Basic Mode Status Register (BMSR) – 01H

Bit	Bit Name	Default	Description
15	100BASE-T4	0,RO/P	**100BASE-T4 Capable** 1 = Able to perform in 100BASE-T4 mode 0 = Not able to perform in 100BASE-T4 mode
14	100BASE-TX Full-Duplex	1,RO/P	**100BASE-TX Full-Duplex Capable** 1 = Able to perform 100BASE-TX in Full-Duplex mode 0 = Not able to perform 100BASE-TX in Full-Duplex mode
13	100BASE-TX Half-Duplex	1,RO/P	**100BASE-TX Half- Duplex Capable** 1 = Able to perform 100BASE-TX in Half-Duplex mode 0 = Not able to perform 100BASE-TX in Half-Duplex mode
12	10BASE-T Full-Duplex	1,RO/P	**10BASE-T Full-Duplex Capable** 1 = Able to perform 10BASE-T in Full-Duplex mode 0 = Not able to perform 10BASE-TX in Full-Duplex mode
11	10BASE-T Half-Duplex	1,RO/P	**10BASE-T Half-Duplex Capable** 1 = Able to perform 10BASE-T in Half-Duplex mode 0 = Not able to perform 10BASE-T in Half-Duplex mode
10:7	RESERVED	0,RO	**Reserved** Write as 0, ignore on read
6	MF Preamble Suppression	0,RO	**MII Frame Preamble Suppression** 1 = PHY will accept management frames with preamble suppressed 0 = PHY will not accept management frames with preamble suppressed
5	Auto-Negotiation Complete	0,RO	**Auto-Negotiation Complete** 1 = Auto-Negotiation process completed 0 = Auto-Negotiation process not completed
4	Remote fault	0,RO/LH	**Remote Fault** 1 = Remote fault condition detected (cleared on read or by a chip reset). Fault criteria and detection method is PHY implementation specific. This bit will set after the RF bit in the ANLPAR (bit 13, register address 05) is set 0 = No remote fault condition detected
3	Auto-Negotiation Ability	1,RO/P	**Auto Configuration Ability** 1 = Able to perform Auto-Negotiation 0 = Not able to perform Auto-Negotiation
2	Link Status	0,RO/LL	**Link Status** 1 = Valid link is established (for either 10Mbps or 100Mbps operation) 0 = Link is not established The link status bit is implemented with a latching function, so that the occurrence of a link failure condition causes the link status bit to be cleared and remain cleared until it is read via the management interface

1	Jabber Detect	0,RO/LH	**Jabber Detect** 1 = Jabber condition detected 0 = No jabber This bit is implemented with a latching function. Jabber conditions will set this bit unless it is cleared by a read to this register through a management interface or a PHY reset. This bit works only in 10Mbps mode
0	Extended Capability	1,RO/P	**Extended Capability** 1 = Extended register capable 0 = Basic register capable only

6.3 PHY ID Identifier Register #1 (PHYID1) – 02H

The PHY Identifier Registers #1 and #2 work together in a single identifier of the DM9621A. The Identifier consists of a concatenation of the Organizationally Unique Identifier (OUI), a vendor's model number, and a model revision number. DAVICOM Semiconductor's IEEE assigned OUI is 00606E.

Bit	Bit Name	Default	Description
15:0	OUI_MSB	<0181h>	**OUI Most Significant Bits** This register stores bit 3 to 18 of the OUI (00606E) to bit 15 to 0 of this register respectively. The most significant two bits of the OUI are ignored (the IEEE standard refers to these as bit 1 and 2)

6.4 PHY Identifier Register #2 (PHYID2) – 03H

Bit	Bit Name	Default	Description
15:10	OUI_LSB	<101110>, RO/P	**OUI Least Significant Bits** Bit 19 to 24 of the OUI (00606E) are mapped to bit 15 to 10 of this register respectively
9:4	VNDR_MDL	<001010>, RO/P	**Vendor Model Number** Six bits of vendor model number mapped to bit 9 to 4 (most significant bit to bit 9)
3:0	MDL_REV	<0000>, RO/P	**Model Revision Number** Four bits of vendor model revision number mapped to bit 3 to 0 (most significant bit to bit 3)

Final

6.5 Auto-Negotiation Advertisement Register(ANAR) – 04H

This register contains the advertised abilities of this DM9621A device as they will be transmitted to its link partner during Auto-Negotiation.

Bit	Bit Name	Default	Description
15	NP	0,RO/P	**Next Page Indication** 1 = Next page available 0 = No next page available The PHY has no next page, so this bit is permanently set to 0
14	ACK	0,RO	**Acknowledge** 1 = Link partner ability data reception acknowledged 0 = Not acknowledged The PHY's Auto-Negotiation state machine will automatically control this bit in the outgoing FLP bursts and set it at the appropriate time during the Auto-Negotiation process. Software should not attempt to write to this bit.
13	RF	0,RW	**Remote Fault** 1 = Local device senses a fault condition 0 = No fault detected
12:11	RESERVED	X,RW	**Reserved** Write as 0, ignore on read
10	FCS	0,RW	**Flow Control Support** 1 = Controller chip supports flow control ability 0 = Controller chip doesn't support flow control ability
9	T4	0,RO/P	**100BASE-T4 Support** 1 = 100BASE-T4 is supported by the local device 0 = 100BASE-T4 is not supported The PHY does not support 100BASE-T4 so this bit is permanently set to 0
8	TX_FDX	1,RW	**100BASE-TX Full-Duplex Support** 1 = 100BASE-TX Full-Duplex is supported by the local device 0 = 100BASE-TX Full-Duplex is not supported
7	TX_HDX	1,RW	**100BASE-TX Support** 1 = 100BASE-TX is supported by the local device 0 = 100BASE-TX is not supported
6	10_FDX	1,RW	**10BASE-T Full-Duplex Support** 1 = 10BASE-T Full-Duplex is supported by the local device 0 = 10BASE-T Full-Duplex is not supported
5	10_HDX	1,RW	**10BASE-T Support** 1 = 10BASE-T is supported by the local device 0 = 10BASE-T is not supported
4:0	Selector	<00001>,RW	**Protocol Selection Bits** These bits contain the binary encoded protocol selector supported by this node. <00001> indicates that this device supports IEEE 802.3 CSMA/CD.

Final

6.6 Auto-Negotiation Link Partner Ability Register (ANLPAR) – 05H

Bit	Bit Name	Default	Description
15	NP	0,RO	**Next Page Indication** 0 = Link partner, no next page available 1 = Link partner, next page available
14	ACK	0,RO	**Acknowledge** 1 = Link partner ability data reception acknowledged 0 = Not acknowledged The PHY's Auto-Negotiation state machine will automatically control this bit from the incoming FLP bursts. Software should not attempt to write to this bit.
13	RF	0,RO	**Remote Fault** 1 = Remote fault indicated by link partner 0 = No remote fault indicated by link partner
12:11	RESERVED	X,RO	**Reserved** Write as 0, ignore on read
10	FCS	0,RW	**Flow Control Support** 1 = Controller chip supports flow control ability by link partner 0 = Controller chip doesn't support flow control ability by link partner
9	T4	0,RO	**100BASE-T4 Support** 1 = 100BASE-T4 is supported by the link partner 0 = 100BASE-T4 is not supported by the link partner
8	TX_FDX	0,RO	**100BASE-TX Full-Duplex Support** 1 = 100BASE-TX Full-Duplex is supported by the link partner 0 = 100BASE-TX Full-Duplex is not supported by the link partner
7	TX_HDX	0,RO	**100BASE-TX Support** 1 = 100BASE-TX Half-Duplex is supported by the link partner 0 = 100BASE-TX Half-Duplex is not supported by the link partner
6	10_FDX	0,RO	**10BASE-T Full-Duplex Support** 1 = 10BASE-T Full-Duplex is supported by the link partner 0 = 10BASE-T Full-Duplex is not supported by the link partner
5	10_HDX	0,RO	**10BASE-T Support** 1 = 10BASE-T Half-Duplex is supported by the link partner 0 = 10BASE-T Half-Duplex is not supported by the link partner
4:0	Selector	<00000>,RO	**Protocol Selection Bits** Link partner's binary encoded protocol selector

Final

6.7 Auto-Negotiation Expansion Register (ANER)- 06H

Bit	Bit Name	Default	Description
15:5	RESERVED	X,RO	**Reserved** Write as 0, ignore on read
4	PDF	0,RO/LH	**Local Device Parallel Detection Fault** 1 = A fault detected via parallel detection function. 0 = No fault detected via parallel detection function
3	LP_NP_ABLE	0,RO	**Link Partner Next Page Able** 1 = Link partner, next page available 0 = Link partner, no next page
2	NP_ABLE	0,RO/P	**Local Device Next Page Able** 1 = Next page available 0 = No next page
1	PAGE_RX	0,RO/LH	**New Page Received** A new link code word page received. This bit will be automatically cleared when the register (register 6) is read by management.
0	LP_AN_ABLE	0,RO	**Link Partner Auto-Negotiation Able** A “1” in this bit indicates that the link partner supports Auto-Negotiation.

Final

6.8 DAVICOM Specified Configuration Register (DSCR) – 10H

Bit	Bit Name	Default	Description
15	BP_4B5B	0,RW	**Bypass 4B5B Encoding and 5B4B Decoding** 1 = 4B5B encoder and 5B4B decoder function bypassed 0 = Normal 4B5B and 5B4B operation
14	BP_SCR	0,RW	**Bypass Scrambler/Descrambler Function** 1 = Scrambler and descrambler function bypassed 0 = Normal scrambler and descrambler operation
13	BP_ALIGN	0,RW	**Bypass Symbol Alignment Function** 1 = Receive functions (descrambler, symbol alignment and symbol decoding functions) bypassed. Transmit functions (symbol encoder and scrambler) bypassed 0 = Normal operation
12	BP_ADPOK	0,RW	**BYPASS ADPOK** Force signal detector (SD) active. This register is for debug only, not release to customer. 1=Force SD is OK 0=Normal operation
11	RESERVED	0,RO	**Reserved** Write as 0, ignore on read.
10	TX	1,RW	**100BASE-TX or FX Mode Control** 1 = 100BASE-TX operation 0 = 100BASE-FX operation
9	RESERVED	0,RO	**Reserved**
8	RESERVED	0,RO	**Reserved** Write as 0, ignore on read.
7	F_LINK_100	0,RW	**Force good link in 100Mbps** 1 = Force 100Mbps good link status 0 = Normal 100Mbps operation This bit is useful for diagnostic purposes.
6	RESERVED	0,RO	**Reserved:** Write as 0, ignore on read.
5	RESERVED	0,RO	**Reserved:** Write as 0, ignore on read.
4	RPDCTR-EN	1,RW	**Reduced Power Down Control Enable** This bit is used to enable automatic reduced power down. 1 = Enable automatic reduced power down 0 = Disable automatic reduced power down.
3	SMRST	0,RW	**Reset State Machine** When writes 1 to this bit, all state machines of PHY will be reset. This bit is self-clear after reset is completed.
2	MFPSC	1,RW	**MF Preamble Suppression Control** MII frame preamble suppression control bit 1 = MF preamble suppression bit on 0 = MF preamble suppression bit off
1	SLEEP	0,RW	**Sleep Mode** Writing a 1 to this bit will cause PHY entering the Sleep mode and power down all circuit except oscillator and clock generator circuit. When waking up from Sleep mode (write this bit to 0), the configuration will go back to the state before sleep; but the state machine will be reset.
0	RESERVED	0,RW	**Reserved** Force to 0 in application.

Final

6.9 DAVICOM Specified Configuration and Status Register (DSCSR) – 11H

Bit	Bit Name	Default	Description
15	100FDX	1,RO	**100M Full-Duplex Operation Mode** After Auto-Negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 100M Full-Duplex mode. The software can read bit[15:12] to see which mode is selected after Auto-Negotiation. This bit is invalid when it is not in the Auto-Negotiation mode.
14	100HDX	1,RO	**100M Half-Duplex Operation Mode** After Auto-Negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 100M Half-Duplex mode. The software can read bit[15:12] to see which mode is selected after Auto-Negotiation. This bit is invalid when it is not in the Auto-Negotiation mode.
13	10FDX	1,RO	**10M Full-Duplex Operation Mode** After Auto-Negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 10M Full-Duplex mode. The software can read bit[15:12] to see which mode is selected after Auto-Negotiation. This bit is invalid when it is not in the Auto-Negotiation mode.
12	10HDX	1,RO	**10M Half-Duplex Operation Mode** After Auto-Negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 10M Half-Duplex mode. The software can read bit[15:12] to see which mode is selected after Auto-Negotiation. This bit is invalid when it is not in the Auto-Negotiation mode.
11:9	RESERVED	0,RO	**Reserved** Write as 0, ignore on read.
8:4	PHYADR[4:0]	(PHYADR), RW	**PHY Address Bit 4:0** The first PHY address bit transmitted or received is the MSB of the address (bit 4). A station management entity connected to multiple PHY entities must know the appropriate address of each PHY.
3:0	ANMB[3:0]	0,RO	**Auto-Negotiation Monitor Bits:** These bits are for debug only. The Auto-Negotiation status will be written to these bits. B3 B2 B1 B0 0 0 0 0 In IDLE state 0 0 0 1 Ability match 0 0 1 0 Acknowledge match 0 0 1 1 Acknowledge match fail 0 1 0 0 Consistency match 0 1 0 1 Consistency match fail 0 1 1 0 Parallel detects signal_link_ready 0 1 1 1 Parallel detects signal_link_ready fail 1 0 0 0 Auto-Negotiation completed successfully

Final

6.10 10BASE-T Configuration/Status (10BTCSR) – 12H

Bit	Bit Name	Default	Description
15	RESERVED	0,RO	**Reserved** Write as 0, ignore on read.
14	LP_EN	1,RW	**Link Pulse Enable** 1 = Transmission of link pulses enabled 0 = Link pulses disabled, good link condition forced This bit is valid only in 10Mbps operation.
13	HBE	1,RW	**Heartbeat Enable** 1 = Heartbeat function enabled 0 = Heartbeat function disabled When the PHY is configured for Full-Duplex operation, this bit will be ignored (the collision/heartbeat function is invalid in Full-Duplex mode).
12	SQUELCH	1,RW	**Squelch Enable** 1 = Normal Squelch 0 = Low Squelch
11	JABEN	1,RW	**Jabber Enable** Enables or disables the Jabber function when the PHY is in 10BASE-T Full-Duplex or 10BASE-T transceiver loopback mode 1 = Jabber function enabled 0 = Jabber function disabled
10:1	RESERVED	0,RO	**Reserved** Write as 0, ignore on read.
0	POLR	0,RO	**Polarity Reversed** When this bit is set to 1, it indicates that the 10Mbps cable polarity is reversed. This bit is set and cleared by 10BASE-T module automatically.

6.11 Power down Control Register (PWDOR) – 13H

Bit	Bit Name	Default	Description
15:9	RESERVED	0, RO	Reserved Read as 0, ignore on write
8	PD10DRV	0, RW	Vendor power down control test
7	PD100DL	0, RW	Vendor power down control test
6	PDchip	0, RW	Vendor power down control test
5	PDcom	0, RW	Vendor power down control test
4	PDaeq	0, RW	Vendor power down control test
3	PDdrv	0, RW	Vendor power down control test
2	PDedi	0, RW	Vendor power down control test
1	PDedo	0, RW	Vendor power down control test
0	PD10	0, RW	Vendor power down control test

***** When selected, the power down value is control by Register 14H

6.12 (Specified Config) Register – 14H

Bit	Bit Name	Default	Description
15	TSTSE1	0,RW	Vendor test select control
14	TSTSE2	0,RW	Vendor test select control
13	FORCE_TXSD	0,RW	**Force Signal Detect** 1 = Force SD signal OK in 100M 0 = Normal SD signal.
12	FORCE_FEF	0,RW	Vendor test select control
11	PREAMBLEX	1,RW	**Preamble Saving Control** 1 = Transmit preamble bit count is normal in 10BASE-T mode 0 = When bit 10 is set, the 10BASE-T transmit preamble count is reduced. When bit 11 of register 1DH is set, 12-bit preamble is reduced; otherwise 22-bit preamble is reduced.
10	TX10M_PWR	1,RW	**10BASE-T Mode Transmit Power Saving Control** 1 = Enable transmit power saving in 10BASE-T mode 0 = Disable transmit power saving in 10BASE-T mode
9	NWAY_PWR	0,RW	**Auto-Negotiation Power Saving Control** 1 = Disable power saving during Auto-Negotiation period 0 = Enable power saving during Auto-Negotiation period
8	RESERVED	0,RW	Reserved
7	MDIX_CNTL	MDI/MDIX,RO	**The Polarity of MDI/MDIX Value** 1 = MDIX mode 0 = MDI mode
6	AutoNeg_lpbk	0,RW	**Auto-Negotiation Loop-back** 1 = Test internal digital Auto-Negotiation Loop-back 0 = Normal
5	Mdix_fix Value	0, RW	**MDIX_CNTL Force Value** When Mdix_down = 1, MDIX_CNTL value depend on the register value.
4	Mdix_do wn	0,RW	**MDIX Down** Manual force MDI/MDIX. 1 = Disable HP Auto-MDIX, MDIX_CNTL value depend on 14H bit 5 0 = Enable HP Auto-MDIX
3	MonSel1	0,RW	Vendor Monitor Select
2	MonSel0	0,RW	Vendor Monitor Select
1	RESERVED	0,RW	**Reserved** Force to 0, in application.
0	PD_value	0,RW	**Power Down Control Value** Decision the value of each field Register 13H 1 = Power down 0 = Normal

Final

6.13 DSP Control (DSP_CTRL) – 1BH

Bit	Bit Name	Default	Description
15:0	DSP_CTRL	0,RW	**DSP Control** For internal testing only

6.14 Power Saving Control Register (PSCR) – 1DH

Bit	Bit Name	Default	Description
15:13	RESERVED	0,RO	Reserved
12	LPI	0,RO	Low Power Idle Mode
11	PREAMBLEX	0,RW	**Preamble Saving Control** When both bit 10and 11 of register 14H are set, the 10BASE-T transmit preamble count is reduced. 1 = 12-bit preamble is reduced. 0 = 22-bit preamble is reduced.
10	AMPLITUDE	0,RW	**Transmit Amplitude Control Disabled** 1 = When cable is unconnected with link partner, the TX amplitude is reduced for power saving. 0 = Disable Transmit amplitude reduce function
9	TX_PWR	0,RW	**Transmit Power Saving Control Disabled** 1 = When cable is unconnected with link partner, the driving current of transmit is reduced for power saving. 0 = Disable transmit driving power saving function
8:0	RESERVED	0,RO	Reserved

Final

7 Functional Description

7.1 USB Functional Description

7.1.1 USB Functional Description

1. Support Standard Command

Setup Stage					Data Stage
BmReqType	BRequest	wValue	wIndex	wLength	Data
00000000B	CLEAR_FEATURE	Feature Selector	Zero	Zero	None
00000001B			Interface		
00000010B			Endpoint		
10000000B	GET_CONFIGURATION	Zero	Zero	One	Configuration value
10000000B	GET_DESCRIPTOR	Descriptor type/index	Zero/LID	Length	Descriptor
10000001B	GET_INTERFACE	Zero	Interface	One	Alternate Interface
10000000B	GET_STATUS	Zero	Zero	Two	Status
10000001B			Interface		
10000010B			Endpoint		
00000000B	SET_ADDRESS	Device address	Zero	Zero	None
00000000B	SET_CONFIGURATION	Configuration value	Zero	Zero	None
00000000B	SET_DESCRIPTOR	Descriptor type/index	Zero/LID	Length	Descriptor
00000000B	SET_FEATURE	Feature Selector	Zero	Zero	None
00000001B			Interface		
00000010B			Endpoint		
00000001B	SET_INTERFACE	Alternate setting	Interface	Zero	None
10000010B	SYNCH_FRAME	Zero	Endpoint	Two	Frame Number

2. Not Supported Standard Commands

- Clear_Feature (Interface)
- Set_Feature (Interface)
- Set_Descriptor ( )
- Sync_Frame ( )

Final

7.1.2 Vender Commands

There are two types of vendor's command. We can access internal register maximum 64 bytes, and can access internal memory.

7.1.2.1 Register Type

READ_REGISTER ( )
Setup Stage

BmReqType	BReq	WValue		WIndex		WLength	
Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
C0H	00H	00H	00H	RegOffset[7:0]	00H	BC[7:0]	00H

WRITE_REGISTER ( )
Setup Stage

BmReqType	BReq	WValue		WIndex		WLength	
Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
40H	01H	00H	00H	RegOffset[7:0]	00H	BC[7:0]	00H

WRITE1_REGISTER ( )
Setup Stage

BmReqType	BReq	WValue		WIndex		WLength	
Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
40H	03H	Data[7:0]	00H	RegOffset[7:0]	00H	0000H	40H

7.1.2.2 Memory Type

These kind of commands are valid when the bit "MEM_MODE " is set, otherwise device will respond with request error when receiving these commands.

READ_MEMORY ( )
Setup Stage

BmReqType	BReq	WValue		WIndex		WLength	
Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
C0H	02H	00H	00H	MemOff[7:0]	MemOff[15:8]	BC[7:0]	00H

WRITE_MEMORY ( )
Setup Stage

BmReqType	BReq	WValue		WIndex		WLength	
Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
C0H	02H	00H	00H	MemOff[7:0]	MemOff[15:8]	BC[7:0]	00H

WRITE1_MEMORY ( )
Setup Stage

BmReqType	BReq	WValue		WIndex		WLength	
Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
40H	07H	Data[7:0]	00H	MemOff[7:0]	MemOff[15:8]	0000H	40H

7.1.3 Interface 0 Configuration

Definition: len-byte is 64-byte in full speed mode and 256-byte in high speed mode.

7.1.3.1 Endpoint 1

Type: Bulk In
Packet Padload: len-byte
When host accessing EP1.

If IN-FIFO is full, device will send len-byte data.
If IN-FIFO isn't full and Ethernet packet isn't end, device will send a NAK.
If IN-FIFO isn't full and Ethernet packet is end, device will send the surplus data in IN-FIFO.

Data Format

For 3-byte header mode (when Register 91H bit 7 is "0")

Fist byte	Ethernet Receive Packet Status, the bit format is same as register 6 (RSR)
Second byte	Ethernet Receive Packet byte count low
Third byte	Ethernet Receive Packet byte count high
The others	Ethernet Receive Packet Data

For 4-byte header mode (when Register 91H bit 7 is "1" or pin GPIO2_2 is pull-high)

Fist byte	Ethernet Receive Packet Checksum Status, the bit[7:2] format is same as register 32H (RCSCSR)
Second byte	Ethernet Receive Packet Status, the bit format is same as register 6 (RSR)
Third byte	Ethernet Receive Packet byte count low
Fourth byte	Ethernet Receive Packet byte count high
The others	Ethernet Receive Packet Data

7.1.3.2 Endpoint 2

Type: Bulk Out
Packet Padload: len-byte
When host accessing EP2.

If OUT-FIFO isn't full, host sends data, device response ACK.
If OUT-FIFO is full, host sends data, device response NAK.
If host sends data less len-byte or zero byte, it means Ethernet packet end.

Data Format

Fist byte	Ethernet Transmit Packet byte count low
Second byte	Ethernet Transmit Packet byte count high
The others	Ethernet Transmit Packet data

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7.1.3.3 Endpoint 3

Type: Interrupt In
Packet Load: 8-byte
When host accessing EP3.
If no interrupt condition, device response NAK.
If interrupt condition, device will send content back to host.

Data Format

Offset	Name	Description
Byte 0	NSR	Network status register
Byte 1	TSR1	Reserved
Byte 2	TSR2	Reserved
Byte 3	RSR	RX status register
Byte 4	ROCR	Received overflow counter register
Byte 5	RXC	Received packet counter
Byte 6	TXC	Transmit packet counter
Byte 7	GPR	Reserved

Final

7.1.4 Descriptor Values

All descriptors are stored in its default values. Values which are "?" in the table below are under define.

Device Descriptor/18-Byte

Offset	Field	Size	Value	Description
0	bLength	1	12H	Size of descriptor in bytes
1	bDescriptorType	1	01H	DEVICE Descriptor Type
2	bcdUSB	2	0200H	USB BCD version
4	bDeviceClass	1	00H	Class code, assign by USB Zero: No device level class 01H~FEH : Valid device class FFH : Vender-specific
5	bDeviceSubClass	1	00H	SubClass code, assign by USB
6	bDeviceProtocol	1	00H	Protocol code, assign by USB
7	bMaxPacketSize0	1	08H	Maximum PL for EP0(8,16,32,64)
8	idVender	2	0A46H	Vendor ID(0A46) (fm EEP)
10	idProduce	2	9621H	Product ID 9621H, RX header is 4-byte mode
12	bcdDevice	2	0101H	Device release number
14	iManufacturer	1	01H	Index of string descriptor for manufacturer
15	iProduct	1	02H	Index of string descriptor for product
16	iSerialNumber	1	03H	Index of string descriptors for serial number
17	bNumConfigurations	1	01H	Number of configurations

Configuration0 Descriptor/9-Byte

Offset	Field	Size	Value	Description
0	bLength	1	09H	Size of descriptors
1	bDescriptorType	1	02H	CONFIGURATION Descriptor Type
2	wTotalLength	2	0027H	Total descriptor length
4	bNumInterfaces	1	01H	Number of interfaces
5	bConfigurationValue	1	01H	Value of this configuration
6	iConfiguration	1	00H	Index of string descriptor for configuration
7	bmAttributes	1	A(8)0H	Configuration characteristics D7:Reserved (set to 1) D6: Self-powered D5: Remote WakeUp 1 = if REG00H bit 6 is "1" 0 = if REG00H bit 6 is "0" D4: Reserved (reset to 0)
8	MaxPower	1	3CH	Maximum power, 2mA units (fm EEP)

Interface0 Descriptor/9-Byte

Offset	Field	Size	Value	Description
0	bLength	1	09H	Size of this descriptor
1	bDescriptorType	1	04H	INTERFACE Descriptor Type
2	bInterfaceNumber	1	00H	Number of interface
3	bAlternateSetting	1	00H	Value used to select alternate setting
4	bNumEndpoints	1	03H	Number of ednpoints
5	bInterfaceClass	1	00H	Class code
6	bInterfaceSubClass	1	00H	SunClass code
7	bInterfaceProtocol	1	00H	Protocol code
8	iInterface	1	00H	Index of string for this interface

Endpoint1 Descriptor/6-Byte

Offset	Field	Size	Value	Description
0	bLength	1	07H	Size of this descriptor
1	bDescriptorType	1	05H	ENDPOINT Descriptor Type
2	bEndpointAddress	1	81H	Address of the endpoint Bit3~0: The endpoint number Bit 6~4: Reserved(0) Bit7 : Direction(Control EP exclude) 1 = IN endpoint 0 = OUT endpoint
3	bmAttributes	1	02H	EP's attributes Bit1~0: Transfer Type 00 = Control 01 = Isochronous 10 = Bulk 11 = Interrupt
4	wMaxPacketSize	2	0040H	Maximum packet size of this EP (0200H for high speed)
6	bInterval	1	00H	Interval for polling (periodical pipe) (fm EEP) Interrupt Tpye = 1 ~ 255 (ms) Isochronoous Type = 1 (ms)

Endpoint 2 Descriptor/6-Byte

Offset	Field	Size	Value	Description
0	bLength	1	07H	Size of this descriptor
1	bDescriptorType	1	05H	ENDPOINT Descriptor Type
2	bEndpointAddress	1	02H	Address of the endpoint Bit3~0: The endpoint number Bit 6~4: Reserved(0) Bit7: Direction(Control EP exclude) 1 = IN endpoint 0 = OUT endpoint
3	bmAttributes	1	02H	EP's attributes Bit1~0: Transfer Type 00 = Control 01 = Isochronous 10 = Bulk 11 = Interrupt
4	wMaxPacketSize	2	0040H	Maximum packet size of this EP (0200H for high speed)
6	bInterval	1	00H	Interval for polling (periodical pipe) (fm EEP) Interrupt Tpye = 1 ~ 255 (ms) Isochronoous Type = 1 (ms)

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Endpoint3 Descriptor/6-Byte

Offset	Field	Size	Value	Description
0	bLength	1	07H	Size of this descriptor
1	bDescriptorType	1	05H	ENDPOINT Descriptor Type
2	bEndpointAddress	1	83H	Address of the endpoint Bit3~0: The endpoint number Bit 6~4: Reserved(0) Bit7: Direction(Control EP exclude) 1 = IN endpoint 0 = OUT endpoint
3	bmAttributes	1	03H	EP's attributes Bit1~0: Transfer Type 00 = Control 01 = Isochronous 10 = Bulk 11 = Interrupt
4	wMaxPacketSize	2	0008H	Maximum packet size of this EP
6	bInterval	1	01H	Interval for polling (periodical pipe) Interrupt Tpye = 1 ~ 255 (ms) Isochronoous Type = 1 (ms)

String0 Descriptor/Code array

Offset	Field	Size	Value	Description
0	bLength	1	04H	Size of this descriptor
1	bDescriptorType	1	03H	STRING Descriptor Type
2	wLANGID[1]	2	0409H	LANGID code(Eng.)

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7.1.5 Descriptors of String/1/2/3 Are Loaded From EEPROM

String1 Descriptor/UNICODE String

Offset	Field	Size	Value	Description
0	bLength	1		Descriptor length loading from EEPROM
1	bDescriptorType	1	03H	STRING Descriptor Type
2~	bString	n		Manufacture

String2 Descriptor/UNICODE String

Offset	Field	Size	Value	Description
0	bLength	1		Descriptor length loading from EEPROM
1	bDescriptorType	1	03H	STRING Descriptor Type
2~	bString	n		Product

String3 Descriptor/UNICODE String

Offset	Field	Size	Value	Description
0	bLength	1		Descriptor length loading from EEPROM
1	bDescriptorType	1	03H	STRING Descriptor Type
2~	bString	n		Serial Number

7.1.6 Descriptors of String/1/2/3 If No EEPROM Exist

String1 Descriptor/UNICODE String

Offset	Field	Size	Value	Description
0	bLength	1	04H	Descriptor length
1	bDescriptorType	1	03H	STRING Descriptor Type
2~	bString	2	0020H	Manufacture

String2 Descriptor/UNICODE String

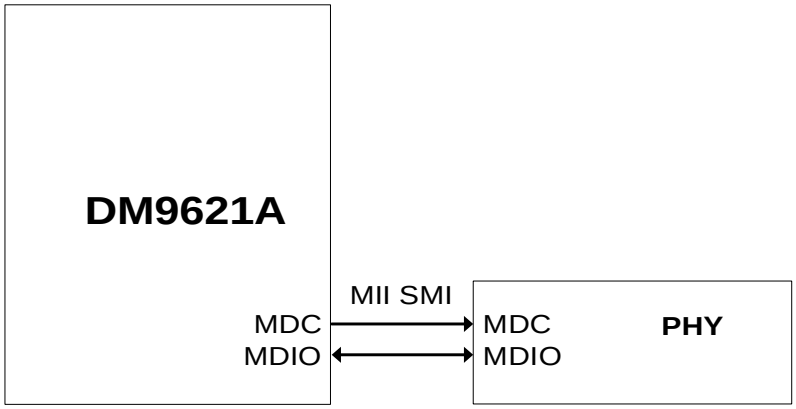
Offset	Field	Size	Value	Description
0	bLength	1	10H	Descriptor length
1	bDescriptorType	1	03H	STRING Descriptor Type
2~	bString	14		55 00 53 00 42 00 20 00 45 00 74 00 68 00

String3 Descriptor/UNICODE String

Offset	Field	Size	Value	Description
0	bLength	1	04H	Descriptor length
1	bDescriptorType	1	03H	STRING Descriptor Type
2~	bString	2	0031H	Serial Number

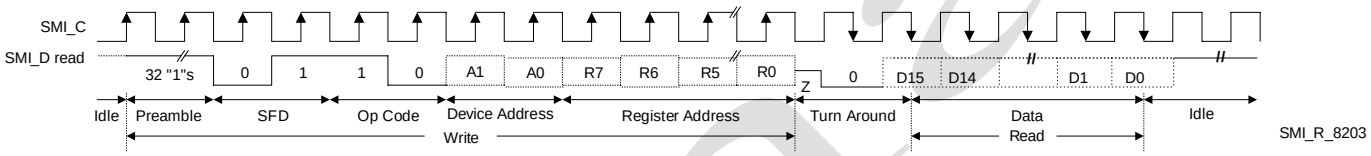
7.2 Ethernet Functional Description

7.2.1 Serial Management Interface

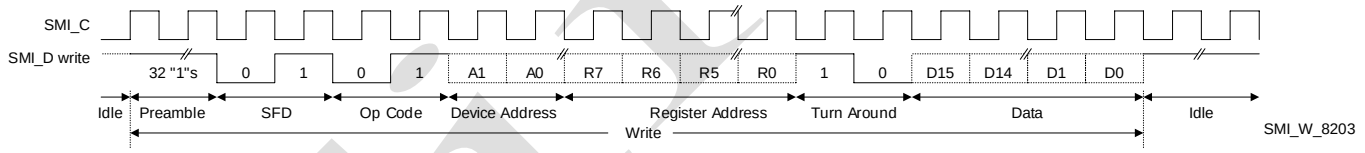


External PHY can be accessed via the MDC, MDIO

SMI - Read Frame Structure



SMI - Write Frame Structure



Final

7.2.2 100Base-TX Operation

The block diagram in figure 3 provides an overview of the functional blocks contained in the transmit section. The transmitter section contains the following functional blocks:

- 4B5B Encoder
- Scrambler
- Parallel to Serial Converter
- NRZ to NRZI Converter
- NRZI to MLT-3
- MLT-3 Driver

7.2.3 4B5B Encoder

The 4B5B encoder converts 4-bit (4B) nibble data generated by the MAC Reconciliation Layer into a 5-bit (5B) code group for transmission, reference Table 1. This conversion is required for control and packet data to be combined in code groups. The 4B5B encoder substitutes the first 8 bits of the MAC preamble with a J/K code-group pair (11000 10001) upon transmit. The 4B5B encoder continues to replace subsequent 4B preamble and data nibbles with corresponding 5B code-groups. At the end of the transmit packet, upon the deassertion of the Transmit Enable signal from the MAC Reconciliation layer, the 4B5B encoder injects the T/R code-group pair (01101 00111) indicating end of frame. After the T/R code-group pair, the 4B5B encoder continuously injects IDLEs into the transmit data stream until Transmit Enable is asserted and the next transmit packet is detected.

The DM9621A includes a Bypass 4B5B conversion option within the 100Base-TX Transmitter for support of applications like 100 Mbps repeaters which do not require 4B5B conversion.

7.2.4 Scrambler

The scrambler is required to control the radiated emissions (EMI) by spreading the transmit energy across the frequency spectrum at the media connector and on the twisted pair cable in 100Base-TX operation.
By scrambling the data, the total energy presented to the cable is randomly distributed over a wide frequency range. Without the scrambler, energy levels on the cable could peak beyond FCC limitations at frequencies related to repeated 5B sequences like continuous transmission of IDLE symbols. The scrambler output is combined with the NRZ 5B data from the code-group encoder via an XOR logic function. The result is a scrambled data stream with sufficient randomization to decrease radiated emissions at critical frequencies.

7.2.5 Parallel to Serial Converter

The Parallel to Serial Converter receives parallel 5B scrambled data from the scrambler and serializes it (converts it from a parallel to a serial data stream). The serialized data stream is then presented to the NRZ to NRZI Encoder block.

7.2.6 NRZ to NRZI Encoder

After the transmit data stream has been scrambled and serialized, the data must be NRZI encoded for compatibility with the TP-PMD standard for 100Base-TX transmission over Category-5 unshielded twisted pair cable.

7.2.7 MLT-3 Converter

The MLT-3 conversion is accomplished by converting the data stream output from the NRZI encoder into two binary data streams with alternately phased logic one events.

7.2.8 MLT-3 Driver

The two binary data streams created at the MLT-3 converter are fed to the twisted pair output driver which converts these streams to current sources and alternately drives either side of the transmit transformer primary winding resulting in a minimal current MLT-3 signal. Refer to figure 4 for the block diagram of the MLT-3 converter.

7.2.9 4B5B Code Group

Symbol	Meaning	4B code 3210	5B Code 43210
0	Data 0	0000	11110
1	Data 1	0001	01001
2	Data 2	0010	10100
3	Data 3	0011	10101
4	Data 4	0100	01010
5	Data 5	0101	01011
6	Data 6	0110	01110
7	Data 7	0111	01111
8	Data 8	1000	10010
9	Data 9	1001	10011
A	Data A	1010	10110
B	Data B	1011	10111
C	Data C	1100	11010
D	Data D	1101	11011
E	Data E	1110	11100
F	Data F	1111	11101
I	Idle	undefined	11111
J	SFD (1)	0101	11000
K	SFD (2)	0101	10001
T	ESD (1)	undefined	01101
R	ESD (2)	undefined	00111
H	Error	undefined	00100
V	Invalid	undefined	00000
V	Invalid	undefined	00001
V	Invalid	undefined	00010
V	Invalid	undefined	00011
V	Invalid	Undefined	00101
V	Invalid	undefined	00110
V	Invalid	undefined	01000
V	Invalid	undefined	01100
V	Invalid	undefined	10000
V	Invalid	undefined	11001

Table 1

Final

7.2.10 100Base-TX Receiver

The 100Base-TX receiver contains several function blocks that convert the scrambled 125Mb/s serial data to synchronous 4-bit nibble data that is then provided to the MII.
The receive section contains the following functional blocks:

- Signal Detect
- Digital Adaptive Equalization
- MLT-3 to Binary Decoder
- Clock Recovery Module
- NRZI to NRZ Decoder
- Serial to Parallel
- Descrambler
- Code Group Alignment
- 4B5B Decoder

7.2.11 Signal Detect

The signal detect function meets the specifications mandated by the ANSI XT12 TP-PMD 100Base-TX Standards for both voltage thresholds and timing parameters.

7.2.12 Adaptive Equalization

When transmitting data at high speeds over copper twisted pair cable, attenuation based on frequency becomes a concern. In high speed twisted pair signaling, the frequency content of the transmitted signal can vary greatly during normal operation based on the randomness of the scrambled data stream. This variation in signal attenuation caused by frequency variations must be compensated for to ensure the integrity of the received data. In order to ensure quality transmission when employing MLT-3 encoding, the compensation must be able to adapt to various cable lengths and cable types depending on the installed environment. The selection of long cable lengths for a given implementation, requires significant compensation which will be over-kill in a situation that includes shorter, less attenuating cable lengths. Conversely, the selection of short or intermediate cable lengths requiring less compensation will cause serious under-compensation for longer length cables. Therefore, the compensation or equalization must be adaptive to ensure proper conditioning of the received signal independent of the cable length.

7.2.13 MLT-3 to NRZI Decoder

The DM9621A decodes the MLT-3 information from the Digital Adaptive Equalizer into NRZI data. The relationship between NRZI and MLT-3 data is shown in figure 4.

7.2.14 Clock Recovery Module

The Clock Recovery Module accepts NRZI data from the MLT-3 to NRZI decoder. The Clock Recovery Module locks onto the data stream and extracts the 125Mhz reference clock. The extracted and synchronized clock and data are presented to the NRZI to NRZ Decoder.

7.2.15 NRZI to NRZ

The transmit data stream is required to be NRZI encoded in for compatibility with the TP-PMD standard for 100Base-TX transmission over Category-5 unshielded twisted pair cable. This conversion process must be reversed on the receive end. The NRZI to NRZ decoder, receives the NRZI data stream from the Clock Recovery Module and converts it to a NRZ data stream to be presented to the Serial to Parallel conversion block.

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7.2.16 Serial to Parallel

The Serial to Parallel Converter receives a serial data stream from the NRZI to NRZ converter, and converts the data stream to parallel data to be presented to the descrambler.

7.2.17 Descrambler

Because of the scrambling process required to control the radiated emissions of transmit data streams, the receiver must descramble the receive data streams. The descrambler receives scrambled parallel data streams from the Serial to Parallel converter, descrambles the data streams, and presents the data streams to the Code Group alignment block.

7.2.18 Code Group Alignment

The Code Group Alignment block receives un-aligned 5B data from the descrambler and converts it into 5B code group data. Code Group Alignment occurs after the J/K is detected, and subsequent data is aligned on a fixed boundary.

7.2.19 4B5B Decoder

The 4B5B Decoder functions as a look-up table that translates incoming 5B code groups into 4B (Nibble) data. When receiving a frame, the first 2 5-bit code groups received are the start-of-frame delimiter (J/K symbols). The J/K symbol pair is stripped and two nibbles of preamble pattern are substituted. The last two code groups are the end-of-frame delimiter (T/R symbols).

The T/R symbol pair is also stripped from the nibble presented to the Reconciliation layer.

7.2.20 10Base-T Operation

The 10Base-T transceiver is IEEE 802.3u compliant. When the DM9621A is operating in 10Base-T mode, the coding scheme is Manchester. Data processed for transmit is presented to the MII interface in nibble format, converted to a serial bit stream, then Manchester encoded. When receiving, the Manchester encoded bit stream is decoded and converted into nibble format for presentation to the MII interface.

7.2.21 Collision Detection

For Half-Duplex operation, a collision is detected when the transmit and receive channels are active simultaneously. When a collision has been detected, it will be reported by the COL signal on the MII interface. Collision detection is disabled in Full-Duplex operation.

7.2.22 Carrier Sense

Carrier Sense (CRS) is asserted in Half-Duplex operation during transmission or reception of data. During Full-Duplex mode, CRS is asserted only during receive operations.

7.2.23 Auto-Negotiation

The objective of Auto-Negotiation is to provide a means to exchange information between segment linked devices and to automatically configure both devices to take maximum advantage of their abilities. It is important to note that Auto-Negotiation does not test the link segment characteristics. The Auto-Negotiation function provides a means for a device to advertise supported modes of operation to a remote link partner, acknowledge the receipt and understanding of common modes of operation, and to reject un-shared modes of operation. This allows devices on both ends of a segment to establish a link at the best common mode of operation. If more than one common mode exists between the two devices, a mechanism is provided to allow the devices to resolve to a single mode of operation using a predetermined priority resolution function.

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7.2.24 Auto-Negotiation (continued)

Auto-Negotiation also provides a parallel detection function for devices that do not support the Auto-Negotiation feature. During Parallel detection there is no exchange of configuration information, instead, the receive signal is examined. If it is discovered that the signal matches a technology that the receiving device supports, a connection will be automatically established using that technology. This allows devices that do not support Auto-Negotiation but support a common mode of operation to establish a link.

7.2.25 Energy-Efficient Ethernet (EEE)

DM9621A support IEEE 802.3az Energy-Efficient Ethernet (EEE) for 100Base-TX transmission. When DM9621A detects low link utilization, it requests the transmitter to enter the Low Power Idle (LPI) mode and send appropriate symbols over the link. Upon receiving and decoding those symbols, the receiver can enter the LPI mode. The transmitter and receiver can enter and exit low power states independently. Energy is conserved by deactivating the corresponding functional blocks.

Auto-Negotiation function is used to determine whether both link partners support EEE. If both link partners support EEE capability of 100Base-TX, DM9621A enables the EEE function to save power when no packets are being transmitted. PHY register 1D bit 12 is high to indicate the status.

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8 DC and AC Electrical Characteristics

8.1 Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit	Conditions
DVDD	Supply Voltage	-0.3	3.6	V	*1
VIN	DC Input Voltage (VIN)	-0.5	5.5	V	*2
VOUT	DC Output Voltage(VOUT)	-0.3	3.6	V	*2
T_{STG}	Storage Temperature range	-65	+150	°C	-
TA	Ambient Temperature	0	+70	°C	-
LT	Lead Temperature (L_T, soldering, 10 sec.).	-	+260	°C	

*1: Power pin
*2: IO pin

8.1.1 Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
DVDD	Supply Voltage	3.135	3.300	3.465	V	
PD (Power Dissipation) *1	100BASE-TX	---	163	---	mA	3.3V
	100BASE-TX AZ Enable W/O Traffic	---	118	---	mA	3.3V
	100BASE-TX AZ Enable With Traffic	---	160	---	mA	3.3V
	10BASE-T	---	163	---	mA	3.3V
	10BASE-T idle	---	135	---	mA	3.3V
	USB suspend mode	---	2.48	---	mA	3.3V

*1: demo board testing result

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8.2 DC Electrical Characteristics (VDD = 3.3V)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Inputs						
V_{IL}	Input Low Voltage	-	-	0.8	V	
V_{IH}	Input High Voltage	2.0	-	-	V	
I_{IL}	Input Low Leakage Current	-1	-	-	uA	VIN = 0.0V
I_{IH}	Input High Leakage Current	-	-	1	uA	VIN = 3.3V
Outputs						
V_{OL}	Output Low Voltage	-	-	0.4	V	IOL = 4mA
V_{OH}	Output High Voltage	2.4	-	-	V	IOH = -4mA
Receiver						
V_{ICM}	RX+/RX- Common Mode Input Voltage	-	1.8	-	V	100 W Termination Across
Transmitter						
$V_{TD}100$	100TX+/- Differential Output Voltage	1.9	2.0	2.1	V	Peak to Peak
$V_{TD}10$	10TX+/- Differential Output Voltage	4.4	5	5.6	V	Peak to Peak
$I_{TD}100$	100TX+/- Differential Output Current	|19|	|20|	|21|	mA	Absolute Value
$I_{TD}10$	10TX+/- Differential Output Current	|44|	|50|	|56|	mA	Absolute Value

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8.3 AC Electrical Characteristics & Timing Waveforms

8.3.1 TP Interface

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
$t_{TR/F}$	100TX+/- Differential Rise/Fall Time	3.0	-	5.0	ns	
t_{TM}	100TX+/- Differential Rise/Fall Time Mismatch	0	-	0.5	ns	
t_{TDC}	100TX+/- Differential Output Duty Cycle Distortion	0	-	0.5	ns	
$T_{t/T}$	100TX+/- Differential Output Peak-to-Peak Jitter	0	-	1.4	ns	
X_{OST}	100TX+/- Differential Voltage Overshoot	0	-	5	%	

8.3.2 Oscillator/Crystal Timing (25°C)

Symbol	Parameter	Min.	Typ	Max.	Unit	Conditions
T_{CKC}	OSC Clock Cycle	39.9988	40	40.0012	ns	30ppm
T_{PWH}	OSC Pulse Width High	-	20	-	ns	
T_{PWL}	OSC Pulse Width Low	-	20	-	ns	

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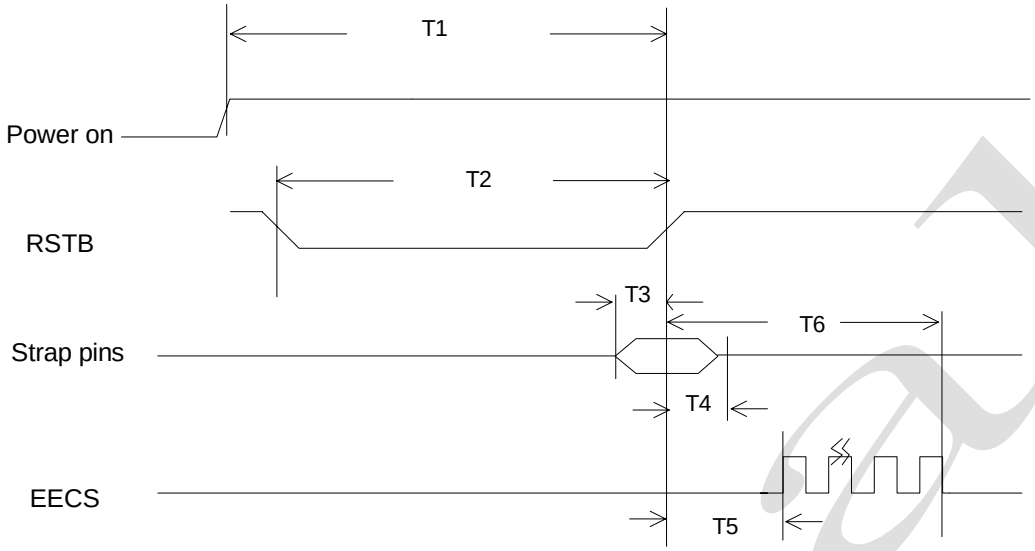
9 AC Timing Waveform

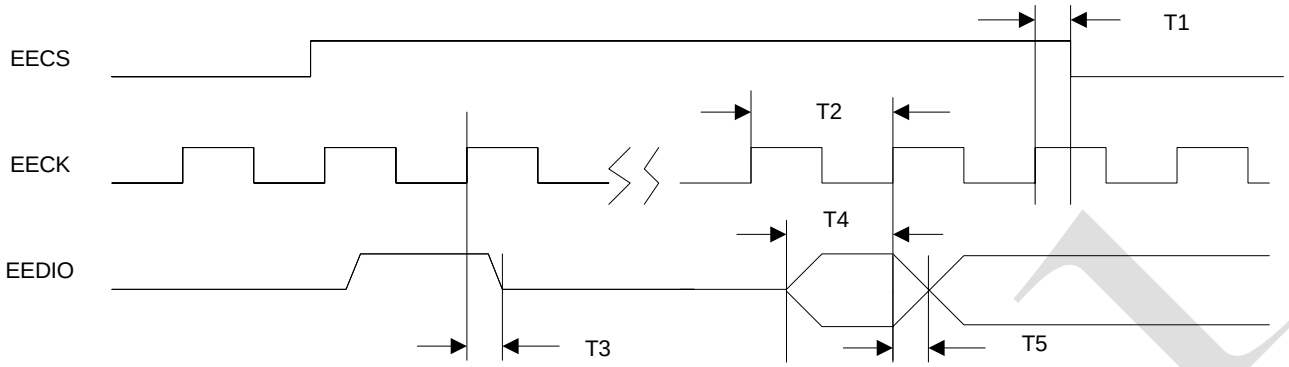
9.1 Power On Reset Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
T1	Power on reset time	15	-	-	ms	-
T2	RSTB Low Period	5	-	-	ms	
T3	Strap pin setup time with RSTB	40	-	-	ns	-
T4	Strap pin hold time with RSTB	40	-	-	ns	-
T5	RSTB high to EECS high	-	1	-	us	-
T6	RSTB high to EECS burst end	-	--	1.85	ms	-

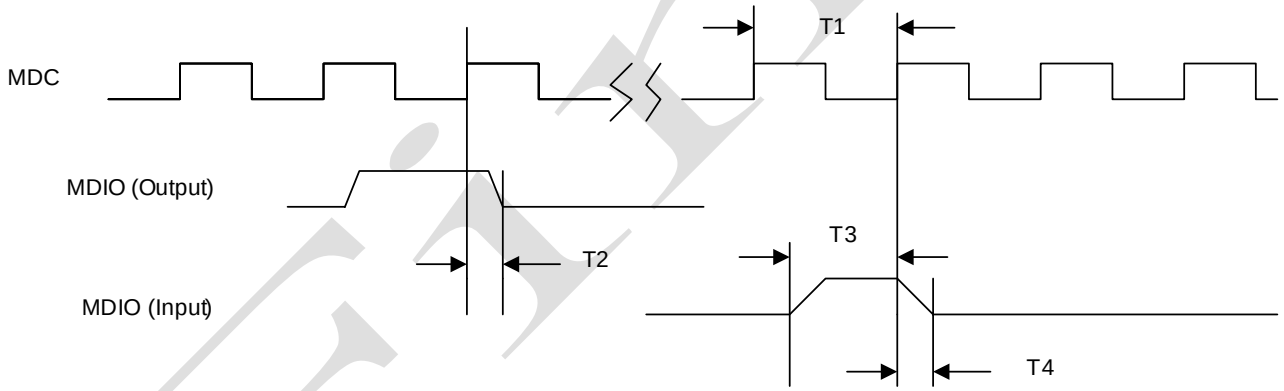
Final

9.2 EEPROM Timing



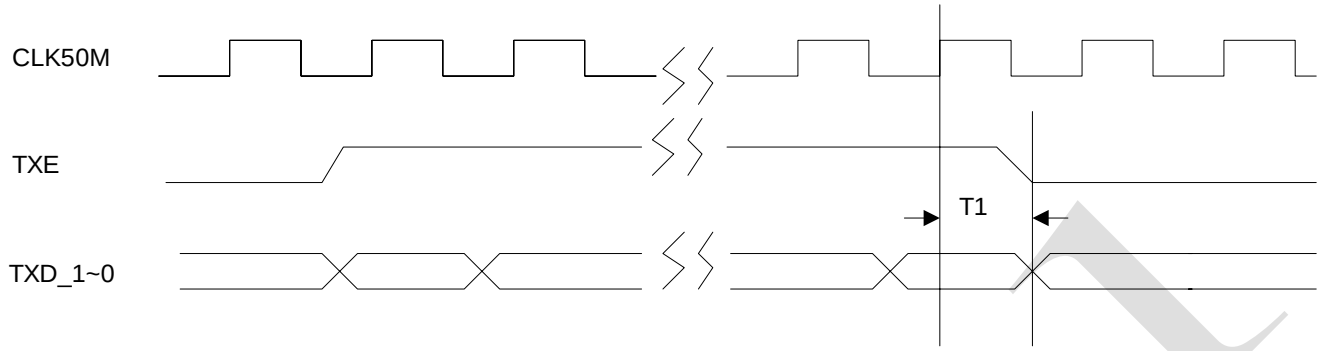
Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	EECS Hold Time		4.2		us
T2	EECK cycle time		5.12		us
T3	EEDIO Hold Time in output state		4.2		us
T4	EEDIO Setup Time in input state	8			ns
T5	EEDIO Hold Time in input state	1			ns

9.3 MII Management Timing



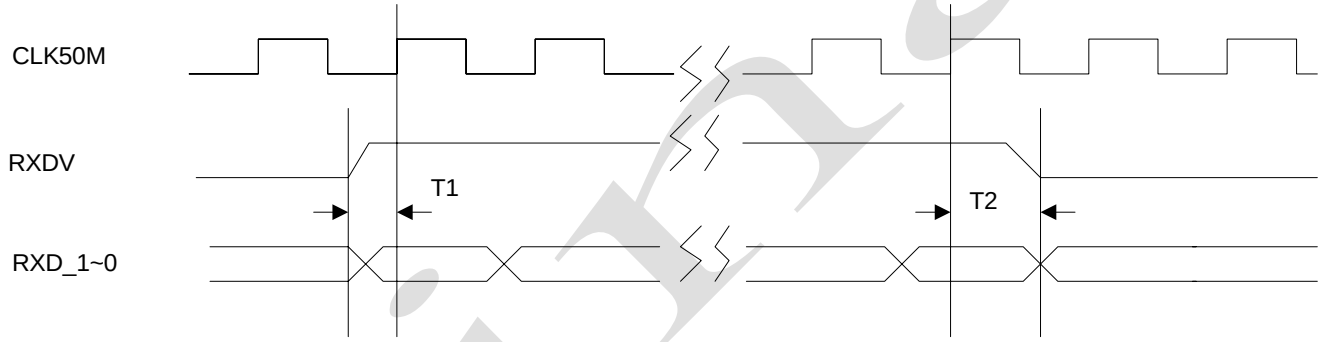
Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	MDC Frequency		1.04		MHz
T2	MDIO Output Delay Time		600		ns
T3	MDIO by External MII Setup Time	368			ns
T4	MDIO by External MII Hold Time	1			ns

9.4 RMII TX Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit
T_1	TXE,TXD_1~0 Delay Time		6		ns

9.5 RMII TX Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	RXDV,RXD_1~0 Setup Time	2			ns
T2	RXDV,RXD_1~0 Hold Time	3			ns

Final

10 Magnetic and Crystal Selection Guide

10.1 Magnetic Selection Guide

Refer to Table 1 for transformer requirements. Transformers, meeting these requirements, are available from a variety of magnetic manufacturers. Designers should test and qualify all magnetic before using them in an application. The transformers listed in Table 1 are electrical equivalents, but may not be pin-to-pin equivalents. Designers should test and qualify all magnetic specifications before using them in an application. RoHS regulations, please contact with your magnetic vendor, this table only for you reference

Manufacturer	Part Number
DELTA	LFE8505-DC, LFE8563-DC, LFE8583-DC
MAGCOM	HS9016, HS9024
Halo	TG110-S050N2, TG110-LC50N2
Bel Fuse	S558-5999-W2

Table 1

10.2 Crystal Selection Guide

A crystal can be used to generate the 25MHz reference clock instead of an oscillator. The crystal must be a fundamental type, and series-resonant. Connects to pins X1 and X2, and shunts each crystal lead to ground with a 15pf capacitor (see figure 10-1).

PARAMETER	SPEC
Type	Fundamental, series-resonant
Frequency	25.000 MHz +/- 30ppm
Equivalent Series Resistance	25 ohms max
Load Capacitance	22 pF typ.
Case Capacitance	7 pF max.
Power Dissipation	1mW max.

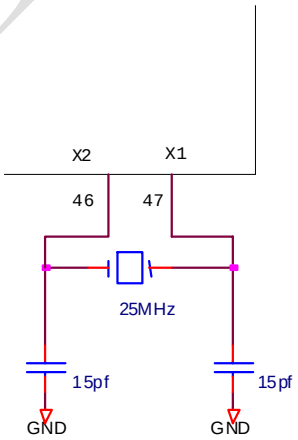
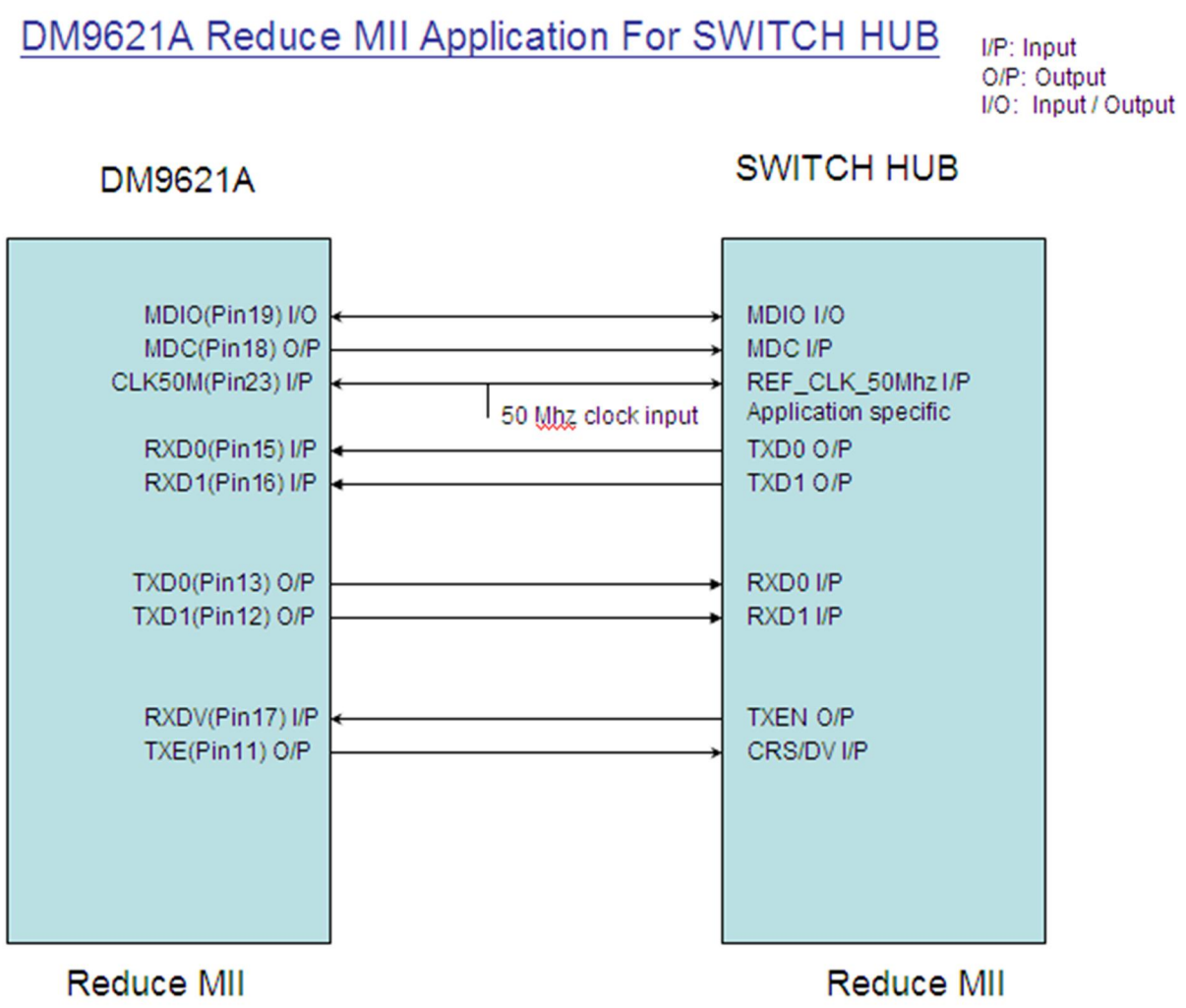


Figure 10-1

Crystal Circuit Diagram

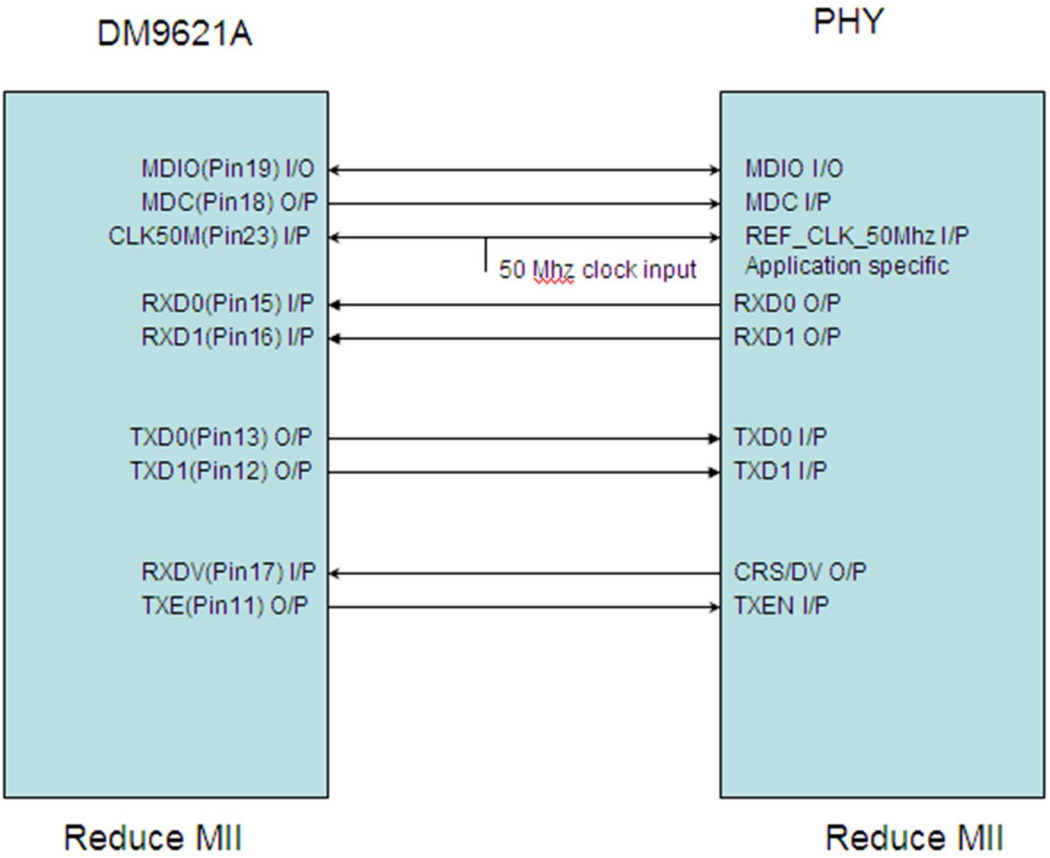
Final

11 Application Circuit



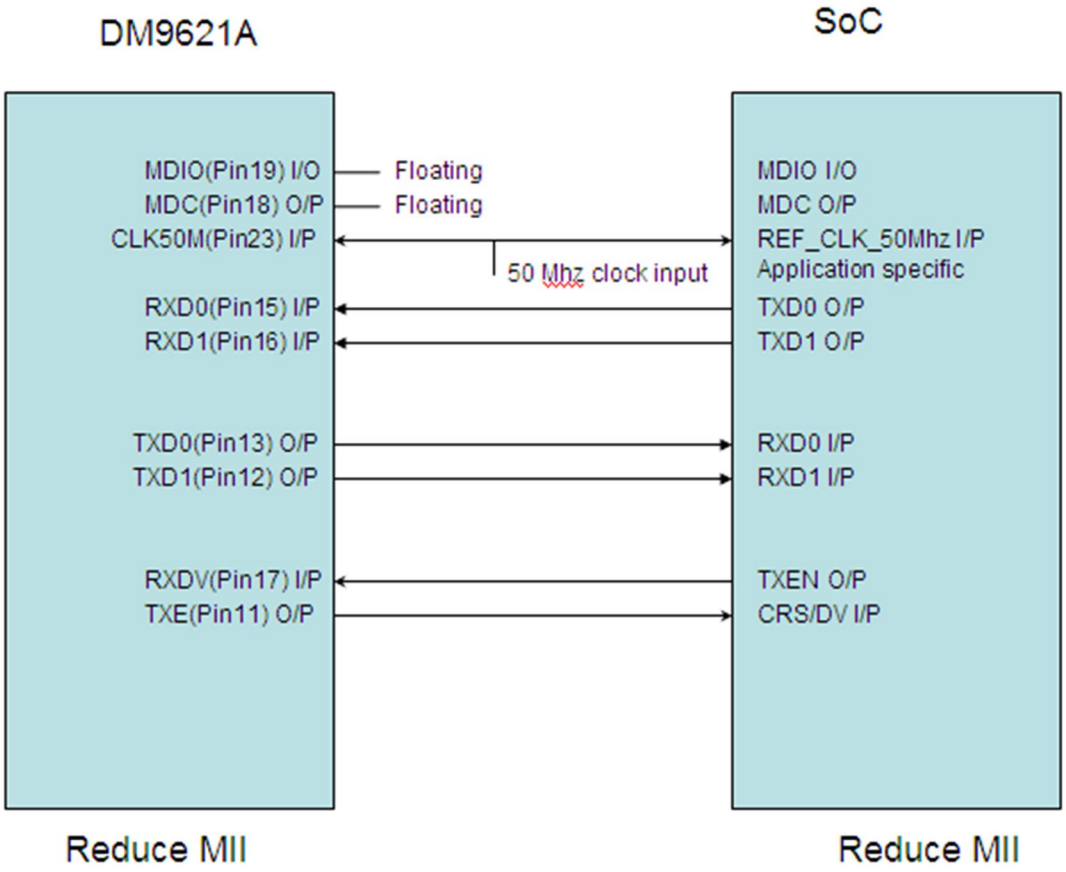
DM9621A Reduce MII Application For PHY

I/P: Input
O/P: Output
I/O: Input / Output



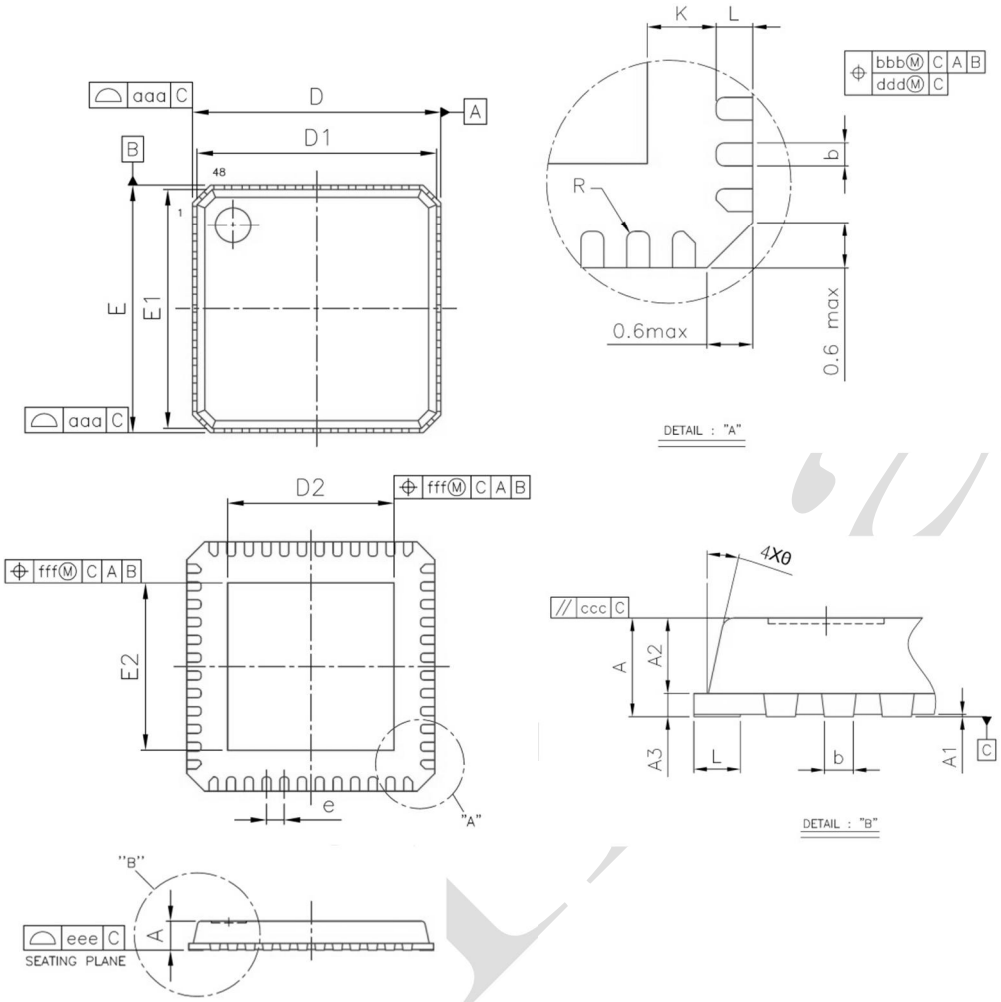
DM9621A Reduce MII Application For SoC

I/P: Input
O/P: Output
I/O: Input / Output



12 Package Information

QFN 48L Outline Dimension unit: inch/mm



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	0.60	0.65	0.70	0.024	0.026	0.028
A3	0.02 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D/E	6.90	7.00	7.10	0.272	0.276	0.280
D1/E1	6.75 BSC			0.266 BSC		
D2/E2	4.90	5.05	5.20	0.193	0.199	0.205
e	0.50 BSC			0.020 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
θ	0°	---	14°	0°	---	14°
R	0.09	---	---	0.004	---	---
K	0.20	---	---	0.008	---	---
aaa	0.15			0.006		
bbb	0.10			0.004		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

NOTE:
1. CONTROLLING DIMENSION: MILLIMETER
2. REFERENCE DOCUMENT: JEDEC MO-220

13 Ordering Information

Part Number	Pin Count	Package
DM9621ANP	48	QFN (Pb-Free)

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WARNING
Conditions beyond those listed for the absolute maximum may destroy or damage the products. In addition, conditions for sustained periods at near the limits of the operating ranges will stress and may temporarily (and permanently) affect and damage structure, performance and function.