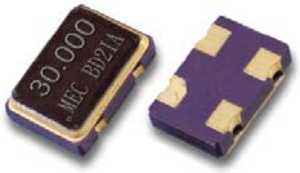
Clock Oscillators [Tight Frequency Tolerance] *HR53 series* *1.8 V*

SMD CMOS output
5.0 x 3.2 x 1.2 mm



RoHS Compliance

Features

- ± 2.0 ppm at 25°C , ± 8.0 ppm over -10°C ~ 70°C , ± 15 ppm over -40°C ~ 85°C
- Ultra Small SMD seam sealed clock crystal oscillator units.
- Tri-state function available.

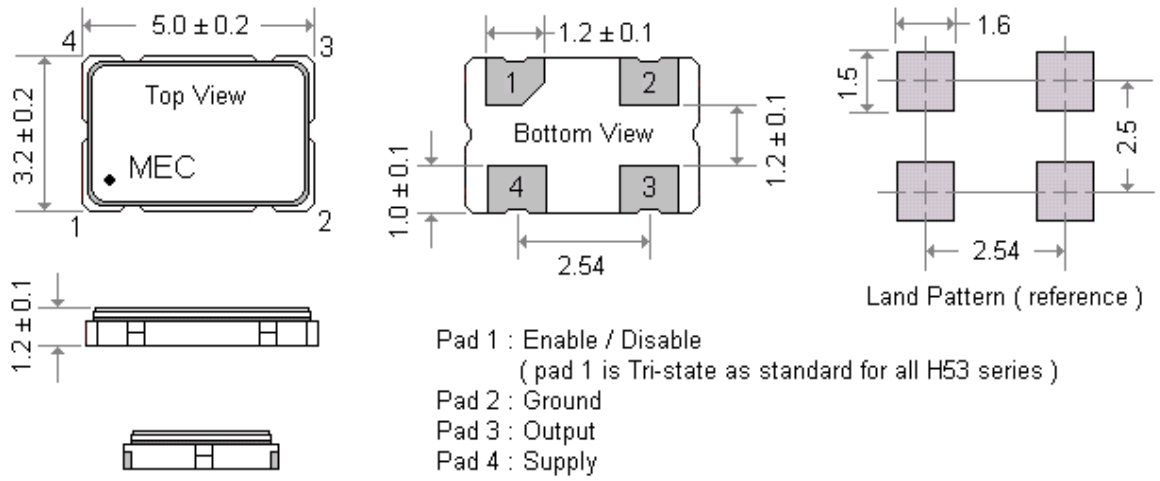
Applications

- Low jitter. Peak-to-peak period jitter is 70 ps typical
- Low phase noise: -138 dBc/Hz at 1 KHz offset
- Low Current Consumption
- 1.8V, 2.5V or 3.3V supply voltages.

General Specifications

Paramenters			Electrical Spec.						
Input Voltage (V_{DD})			1.8 V ± 5 %						
Frequency Range			1.0 ~ 56.0 MHz						
Output Wave Form			CMOS output						
Output Logic High " 1 "			V_{DD} - 0.4V (min.)						
Output Logic Low " 0 "			0.1 V (typical) , 0.4 V (max.)						
Frequency Tolerance	at 25 °C		± 2.0 ppm (max.)						
Frequency Stability	Commercial	(-10°C to +70°C)	the code " C " , For example : " C7 " ± 7 ppm over -10°C to +70°C						
	Industrial	(-40°C to +85°C)	the code " I " , For example : " I15 " ± 15 ppm over -40°C to +85°C						
Output Load			15 pF						
Rise Time (Tr) / Fall Time (Tf)			2.0 nsec. (typ.) ; 4.0 nsec. (max.) , 10% → 90% of waveform						
Duty Cycle			50% ± 5% [measured at 50% V_{DD}]						
Current Consumption			1.0 ~ 19.99 MHz		20.0 ~ 39.99 MHz		40.0 ~ 56.0 MHz		
			1.5 mA		3.0 mA		4.5 mA		
Start - Up Time (Ts)			5 m sec.(typical)						
Storage Temperature			- 50°C to 100°C						
Aging			± 3 ppm per year (max.)						
Phase Noise (typical) [25.0 MHz]			Offset	10 Hz	100 Hz	1K Hz	10 KHz	100KHz	1 MHz	10 MHz
			dBc / Hz	-65	-90	-135	-145	-148	-152	-155

Outline Dimensions (Unit : mm)



Pad 1 : Enable / Disable
(pad 1 is Tri-state as standard for all H53 series)
Pad 2 : Ground
Pad 3 : Output
Pad 4 : Supply

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