

# DATA SHEET

**74LVC1G02**

Single 2-input NOR gate

Product specification  
Supersedes data of 2002 Oct 02

2004 Sep 07

## Single 2-input NOR gate

## 74LVC1G02

## FEATURES

- Wide supply voltage range from 1.65 V to 5.5 V
- High noise immunity
- Complies with JEDEC standard:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8B/JESD36 (2.7 V to 3.6 V).
- $\pm 24$  mA output drive ( $V_{CC} = 3.0$  V)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Multiple package options
- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from  $-40$  °C to  $+85$  °C and  $-40$  °C to  $+125$  °C.

## DESCRIPTION

The 74LVC1G02 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Input can be driven from either 3.3 V or 5 V devices. These features allow the use of these devices in a mixed 3.3 V and 5 V environment.

Schmitt trigger action at all inputs makes the circuit tolerant for slower input rise and fall time.

This device is fully specified for partial power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

The 74LVC1G02 provides the single 2-input NOR function.

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25$  °C;  $t_r = t_f \leq 2.5$  ns.

| SYMBOL            | PARAMETER                                    | CONDITIONS  | TYPICAL | UNIT |
|-------------------|--|---|---------|------|
| $t_{PHL}/t_{PLH}$ | propagation delay<br>inputs A, B to output Y | $V_{CC} = 1.8$ V; $C_L = 30$ pF; $R_L = 1$ k $\Omega$ | 3.2     | ns   |
|                   |  | $V_{CC} = 2.5$ V; $C_L = 30$ pF; $R_L = 500$ $\Omega$ | 2.2     | ns   |
|                   |  | $V_{CC} = 2.7$ V; $C_L = 50$ pF; $R_L = 500$ $\Omega$ | 2.5     | ns   |
|                   |  | $V_{CC} = 3.3$ V; $C_L = 50$ pF; $R_L = 500$ $\Omega$ | 2.1     | ns   |
|                   |  | $V_{CC} = 5.0$ V; $C_L = 50$ pF; $R_L = 500$ $\Omega$ | 1.7     | ns   |
| $C_I$             | input capacitance                            |   | 5       | pF   |
| $C_{PD}$          | power dissipation capacitance per buffer     | $V_{CC} = 3.3$ V; notes 1 and 2                       | 14      | pF   |

## Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu$ W).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in Volts;

$N$  = total load switching outputs;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

2. The condition is  $V_I = \text{GND}$  to  $V_{CC}$ .

# Single 2-input NOR gate

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### FUNCTION TABLE

See note 1.

| INPUT |   | OUTPUT |
|-------|---|--------|
| A     | B | Y      |
| L     | L | H      |
| L     | H | L      |
| H     | L | L      |
| H     | H | L      |

### Note

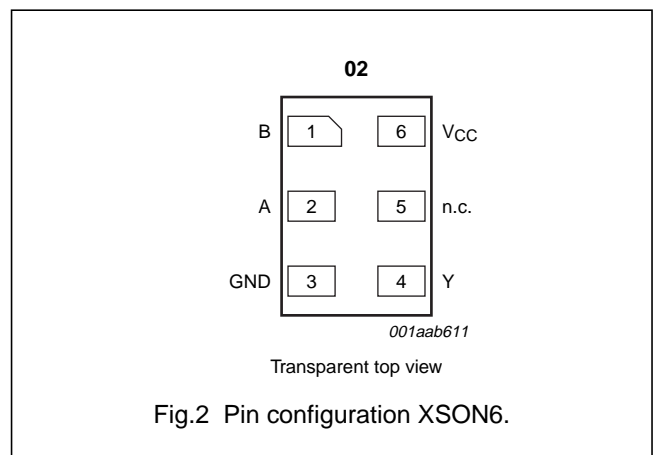
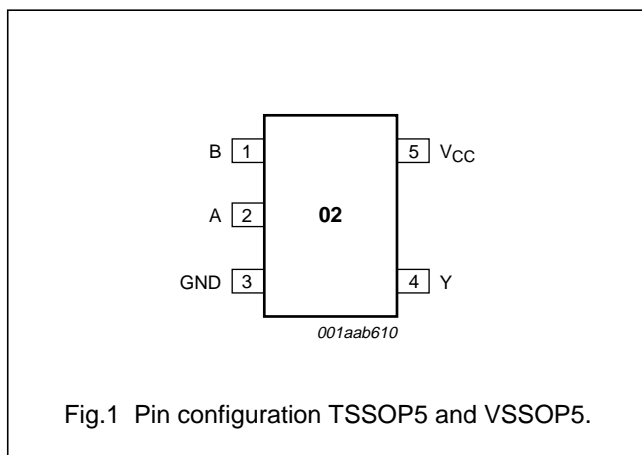
- 1. H = HIGH voltage level;  
L = LOW voltage level.

### ORDERING INFORMATION

| TYPE NUMBER | PACKAGE           |      |         |          |        |         |
|-------------|-------------------|------|---------|----------|--------|---------|
|             | TEMPERATURE RANGE | PINS | PACKAGE | MATERIAL | CODE   | MARKING |
| 74LVC1G02GW | -40 °C to +125 °C | 5    | SC-88A  | plastic  | SOT353 | VB      |
| 74LVC1G02GV | -40 °C to +125 °C | 5    | SC-74A  | plastic  | SOT753 | V02     |
| 74LVC1G02GM | -40 °C to +125 °C | 5    | XSON6   | plastic  | SOT886 | VB      |

### PINNING

| PIN (TSSOP5 AND VSSOP5) | PIN (XSON6) | SYMBOL          | DESCRIPTION    |
|-------------------------|-------------|-----------------|----------------|
| 1                       | 1           | B               | data input B   |
| 2                       | 2           | A               | data input A   |
| 3                       | 3           | GND             | ground (0 V)   |
| 4                       | 4           | Y               | data output Y  |
| -                       | 5           | n.c.            | not connected  |
| 5                       | 6           | V <sub>CC</sub> | supply voltage |



# Single 2-input NOR gate

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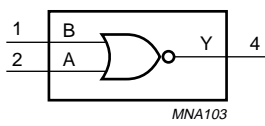


Fig.3 Logic symbol.

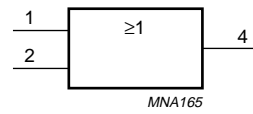


Fig.4 IEE/IEC logic symbol.

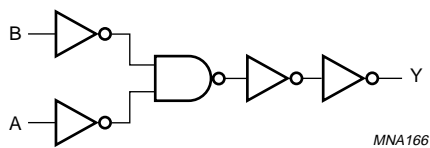


Fig.5 Logic diagram.

## Single 2-input NOR gate

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## RECOMMENDED OPERATING CONDITIONS

| SYMBOL     | PARAMETER                     | CONDITIONS                      | MIN. | MAX.     | UNIT |
|------------|-------------------------------|---------------------------------|------|----------|------|
| $V_{CC}$   | supply voltage                |                                 | 1.65 | 5.5      | V    |
| $V_I$      | input voltage                 |                                 | 0    | 5.5      | V    |
| $V_O$      | output voltage                | active mode                     | 0    | $V_{CC}$ | V    |
|            |                               | $V_{CC} = 0$ V; Power-down mode | 0    | 5.5      | V    |
| $T_{amb}$  | operating ambient temperature |                                 | -40  | +125     | °C   |
| $t_r, t_f$ | input rise and fall times     | $V_{CC} = 1.65$ V to 2.7 V      | 0    | 20       | ns/V |
|            |                               | $V_{CC} = 2.7$ V to 5.5 V       | 0    | 10       | ns/V |

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

| SYMBOL            | PARAMETER                      | CONDITIONS                     | MIN. | MAX.           | UNIT |
|-------------------|--------------------------------|--------------------------------|------|----------------|------|
| $V_{CC}$          | supply voltage                 |                                | -0.5 | +6.5           | V    |
| $I_{IK}$          | input diode current            | $V_I < 0$ V                    | -    | -50            | mA   |
| $V_I$             | input voltage                  | note 1                         | -0.5 | +6.5           | V    |
| $I_{OK}$          | output diode current           | $V_O > V_{CC}$ or $V_O < 0$ V  | -    | ±50            | mA   |
| $V_O$             | output voltage                 | active mode; notes 1 and 2     | -0.5 | $V_{CC} + 0.5$ | V    |
|                   |                                | Power-down mode; notes 1 and 2 | -0.5 | +6.5           | V    |
| $I_O$             | output source and sink current | $V_O = 0$ V to $V_{CC}$        | -    | ±50            | mA   |
| $I_{CC}, I_{GND}$ | $V_{CC}$ or GND current        |                                | -    | ±100           | mA   |
| $T_{stg}$         | storage temperature            |                                | -65  | +150           | °C   |
| $P_D$             | power dissipation              | $T_{amb} = -40$ °C to +125 °C  | -    | 250            | mW   |

## Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. When  $V_{CC} = 0$  V (Power-down mode), the output voltage can be 5.5 V in normal operation.

## Single 2-input NOR gate

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## DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| SYMBOL                                    | PARAMETER                                   | TEST CONDITIONS  |                     | MIN.                   | TYP. <sup>(1)</sup> | MAX.                   | UNIT |
|---|---|--|---------------------|------------------------|---------------------|------------------------|------|
|   |   | OTHER  | V <sub>CC</sub> (V) |                        |                     |                        |      |
| <b>T<sub>amb</sub> = -40 °C to +85 °C</b> |   |  |                     |                        |                     |                        |      |
| V <sub>IH</sub>                           | HIGH-level input voltage                    |  | 1.65 to 1.95        | 0.65 × V <sub>CC</sub> | –                   | –                      | V    |
|   |   |  | 2.3 to 2.7          | 1.7                    | –                   | –                      | V    |
|   |   |  | 2.7 to 3.6          | 2.0                    | –                   | –                      | V    |
|   |   |  | 4.5 to 5.5          | 0.7 × V <sub>CC</sub>  | –                   | –                      | V    |
| V <sub>IL</sub>                           | LOW-level input voltage                     |  | 1.65 to 1.95        | –                      | –                   | 0.35 × V <sub>CC</sub> | V    |
|   |   |  | 2.3 to 2.7          | –                      | –                   | 0.7                    | V    |
|   |   |  | 2.7 to 3.6          | –                      | –                   | 0.8                    | V    |
|   |   |  | 4.5 to 5.5          | –                      | –                   | 0.3 × V <sub>CC</sub>  | V    |
| V <sub>OL</sub>                           | LOW-level output voltage                    | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub><br>I <sub>O</sub> = 100 μA<br>I <sub>O</sub> = 4 mA<br>I <sub>O</sub> = 8 mA<br>I <sub>O</sub> = 12 mA<br>I <sub>O</sub> = 24 mA<br>I <sub>O</sub> = 32 mA       | 1.65 to 5.5         | –                      | –                   | 0.1                    | V    |
|   |   |  | 1.65                | –                      | –                   | 0.45                   | V    |
|   |   |  | 2.3                 | –                      | –                   | 0.3                    | V    |
|   |   |  | 2.7                 | –                      | –                   | 0.4                    | V    |
|   |   |  | 3.0                 | –                      | –                   | 0.55                   | V    |
|   |   |  | 4.5                 | –                      | –                   | 0.55                   | V    |
| V <sub>OH</sub>                           | HIGH-level output voltage                   | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub><br>I <sub>O</sub> = -100 μA<br>I <sub>O</sub> = -4 mA<br>I <sub>O</sub> = -8 mA<br>I <sub>O</sub> = -12 mA<br>I <sub>O</sub> = -24 mA<br>I <sub>O</sub> = -32 mA | 1.65 to 5.5         | V <sub>CC</sub> - 0.1  | –                   | –                      | V    |
|   |   |  | 1.65                | 1.2                    | –                   | –                      | V    |
|   |   |  | 2.3                 | 1.9                    | –                   | –                      | V    |
|   |   |  | 2.7                 | 2.2                    | –                   | –                      | V    |
|   |   |  | 3.0                 | 2.3                    | –                   | –                      | V    |
|   |   |  | 4.5                 | 3.8                    | –                   | –                      | V    |
| I <sub>LI</sub>                           | input leakage current                       | V <sub>I</sub> = 5.5 V or GND  | 5.5                 | –                      | ±0.1                | ±5                     | μA   |
| I <sub>off</sub>                          | power OFF leakage current                   | V <sub>I</sub> or V <sub>O</sub> = 5.5 V   | 0                   | –                      | ±0.1                | ±10                    | μA   |
| I <sub>CC</sub>                           | quiescent supply current                    | V <sub>I</sub> = V <sub>CC</sub> or GND;<br>I <sub>O</sub> = 0 A   | 5.5                 | –                      | 0.1                 | 10                     | μA   |
| ΔI <sub>CC</sub>                          | additional quiescent supply current per pin | V <sub>I</sub> = V <sub>CC</sub> - 0.6 V;<br>I <sub>O</sub> = 0 A  | 2.3 to 5.5          | –                      | 5                   | 500                    | μA   |

## Single 2-input NOR gate

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| SYMBOL                                     | PARAMETER                                   | TEST CONDITIONS   |                     | MIN.                   | TYP. <sup>(1)</sup> | MAX.                   | UNIT |
|--|---|---|---------------------|------------------------|---------------------|------------------------|------|
|  |   | OTHER   | V <sub>CC</sub> (V) |                        |                     |                        |      |
| <b>T<sub>amb</sub> = -40 °C to +125 °C</b> |   |   |                     |                        |                     |                        |      |
| V <sub>IH</sub>                            | HIGH-level input voltage                    |   | 1.65 to 1.95        | 0.65 × V <sub>CC</sub> | –                   | –                      | V    |
|  |   |   | 2.3 to 2.7          | 1.7                    | –                   | –                      | V    |
|  |   |   | 2.7 to 3.6          | 2.0                    | –                   | –                      | V    |
|  |   |   | 4.5 to 5.5          | 0.7 × V <sub>CC</sub>  | –                   | –                      | V    |
| V <sub>IL</sub>                            | LOW-level input voltage                     |   | 1.65 to 1.95        | –                      | –                   | 0.35 × V <sub>CC</sub> | V    |
|  |   |   | 2.3 to 2.7          | –                      | –                   | 0.7                    | V    |
|  |   |   | 2.7 to 3.6          | –                      | –                   | 0.8                    | V    |
|  |   |   | 4.5 to 5.5          | –                      | –                   | 0.3 × V <sub>CC</sub>  | V    |
| V <sub>OL</sub>                            | LOW-level output voltage                    | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>               | 1.65 to 5.5         | –                      | –                   | 0.1                    | V    |
|  |   | I <sub>O</sub> = 100 μA   | 1.65                | –                      | –                   | 0.70                   | V    |
|  |   | I <sub>O</sub> = 4 mA   | 2.3                 | –                      | –                   | 0.45                   | V    |
|  |   | I <sub>O</sub> = 8 mA   | 2.7                 | –                      | –                   | 0.60                   | V    |
|  |   | I <sub>O</sub> = 12 mA  | 3.0                 | –                      | –                   | 0.80                   | V    |
|  |   | I <sub>O</sub> = 24 mA  | 4.5                 | –                      | –                   | 0.80                   | V    |
| V <sub>OH</sub>                            | HIGH-level output voltage                   | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>               | 1.65 to 5.5         | V <sub>CC</sub> – 0.1  | –                   | –                      | V    |
|  |   | I <sub>O</sub> = –100 μA  | 1.65                | 0.95                   | –                   | –                      | V    |
|  |   | I <sub>O</sub> = –4 mA  | 2.3                 | 1.7                    | –                   | –                      | V    |
|  |   | I <sub>O</sub> = –8 mA  | 2.7                 | 1.9                    | –                   | –                      | V    |
|  |   | I <sub>O</sub> = –12 mA   | 3.0                 | 2.0                    | –                   | –                      | V    |
|  |   | I <sub>O</sub> = –24 mA   | 4.5                 | 3.4                    | –                   | –                      | V    |
| I <sub>LI</sub>                            | input leakage current                       | V <sub>I</sub> = 5.5 V or GND                                     | 5.5                 | –                      | ±0.1                | ±100                   | μA   |
| I <sub>off</sub>                           | power OFF leakage current                   | V <sub>I</sub> or V <sub>O</sub> = 5.5 V                          | 0                   | –                      | ±0.1                | ±200                   | μA   |
| I <sub>CC</sub>                            | quiescent supply current                    | V <sub>I</sub> = V <sub>CC</sub> or GND;<br>I <sub>O</sub> = 0 A  | 5.5                 | –                      | 0.1                 | 200                    | μA   |
| ΔI <sub>CC</sub>                           | additional quiescent supply current per pin | V <sub>I</sub> = V <sub>CC</sub> – 0.6 V;<br>I <sub>O</sub> = 0 A | 2.3 to 5.5          | –                      | 5                   | 5000                   | μA   |

**Note**

1. All typical values are measured at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.

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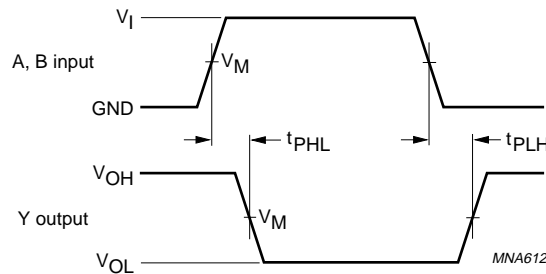
74LVC1G02

**AC CHARACTERISTICS**

GND = 0 V;  $t_r = t_f \leq 2.0$  ns.

| SYMBOL                                     | PARAMETER                      | TEST CONDITIONS  |                     | MIN. | TYP. | MAX. | UNIT |
|--|--------------------------------|------------------|---------------------|------|------|------|------|
|  |                                | WAVEFORMS        | V <sub>CC</sub> (V) |      |      |      |      |
| <b>T<sub>amb</sub> = -40 °C to +85 °C</b>  |                                |                  |                     |      |      |      |      |
| t <sub>PHL</sub> /t <sub>PLH</sub>         | propagation delay<br>A, B to Y | see Figs 6 and 7 | 1.65 to 1.95        | 1.0  | 3.2  | 8.0  | ns   |
|  |                                |                  | 2.3 to 2.7          | 0.5  | 2.2  | 5.5  | ns   |
|  |                                |                  | 2.7                 | 0.5  | 2.5  | 5.5  | ns   |
|  |                                |                  | 3.0 to 3.6          | 0.5  | 2.1  | 4.5  | ns   |
|  |                                |                  | 4.5 to 5.5          | 0.5  | 1.7  | 4.0  | ns   |
| <b>T<sub>amb</sub> = -40 °C to +125 °C</b> |                                |                  |                     |      |      |      |      |
| t <sub>PHL</sub> /t <sub>PLH</sub>         | propagation delay<br>A, B to Y | see Figs 6 and 7 | 1.65 to 1.95        | 1.0  | –    | 10.5 | ns   |
|  |                                |                  | 2.3 to 2.7          | 0.5  | –    | 7.0  | ns   |
|  |                                |                  | 2.7                 | 0.5  | –    | 7.0  | ns   |
|  |                                |                  | 3.0 to 3.6          | 0.5  | –    | 6.0  | ns   |
|  |                                |                  | 4.5 to 5.5          | 0.5  | –    | 5.5  | ns   |

**AC WAVEFORMS**



| V <sub>CC</sub>  | V <sub>M</sub>        | INPUT           |                                 |
|------------------|-----------------------|-----------------|---------------------------------|
|                  |                       | V <sub>I</sub>  | t <sub>r</sub> = t <sub>f</sub> |
| 1.65 V to 1.95 V | 0.5 × V <sub>CC</sub> | V <sub>CC</sub> | ≤ 2.0 ns                        |
| 2.3 V to 2.7 V   | 0.5 × V <sub>CC</sub> | V <sub>CC</sub> | ≤ 2.0 ns                        |
| 2.7 V            | 1.5 V                 | 2.7 V           | ≤ 2.5 ns                        |
| 3.0 V to 3.6 V   | 1.5 V                 | 2.7 V           | ≤ 2.5 ns                        |
| 4.5 V to 5.5 V   | 0.5 × V <sub>CC</sub> | V <sub>CC</sub> | ≤ 2.5 ns                        |

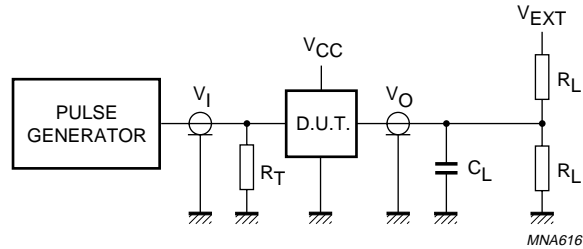
V<sub>OL</sub> and V<sub>OH</sub> are typical output voltage drop that occur with the output load.

Fig.6 Input A, B to output Y propagation delay times.



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| V <sub>CC</sub>  | V <sub>I</sub>  | C <sub>L</sub> | R <sub>L</sub> | V <sub>EXT</sub>                   |                                    |                                    |
|------------------|-----------------|----------------|----------------|------------------------------------|------------------------------------|------------------------------------|
|                  |                 |                |                | t <sub>PLH</sub> /t <sub>PHL</sub> | t <sub>PZH</sub> /t <sub>PHZ</sub> | t <sub>PZL</sub> /t <sub>PLZ</sub> |
| 1.65 V to 1.95 V | V <sub>CC</sub> | 30 pF          | 1 kΩ           | open                               | GND                                | 2 × V <sub>CC</sub>                |
| 2.3 V to 2.7 V   | V <sub>CC</sub> | 30 pF          | 500 Ω          | open                               | GND                                | 2 × V <sub>CC</sub>                |
| 2.7 V            | 2.7 V           | 50 pF          | 500 Ω          | open                               | GND                                | 6 V                                |
| 3.0 V to 3.6 V   | 2.7 V           | 50 pF          | 500 Ω          | open                               | GND                                | 6 V                                |
| 4.5 V to 5.5 V   | V <sub>CC</sub> | 50 pF          | 500 Ω          | open                               | GND                                | 2 × V <sub>CC</sub>                |

Definitions for test circuit:

R<sub>L</sub> = Load resistor.

C<sub>L</sub> = Load capacitance including jig and probe capacitance.

R<sub>T</sub> = Termination resistance should be equal to the output impedance Z<sub>o</sub> of the pulse generator.

Fig.7 Load circuitry for switching times.

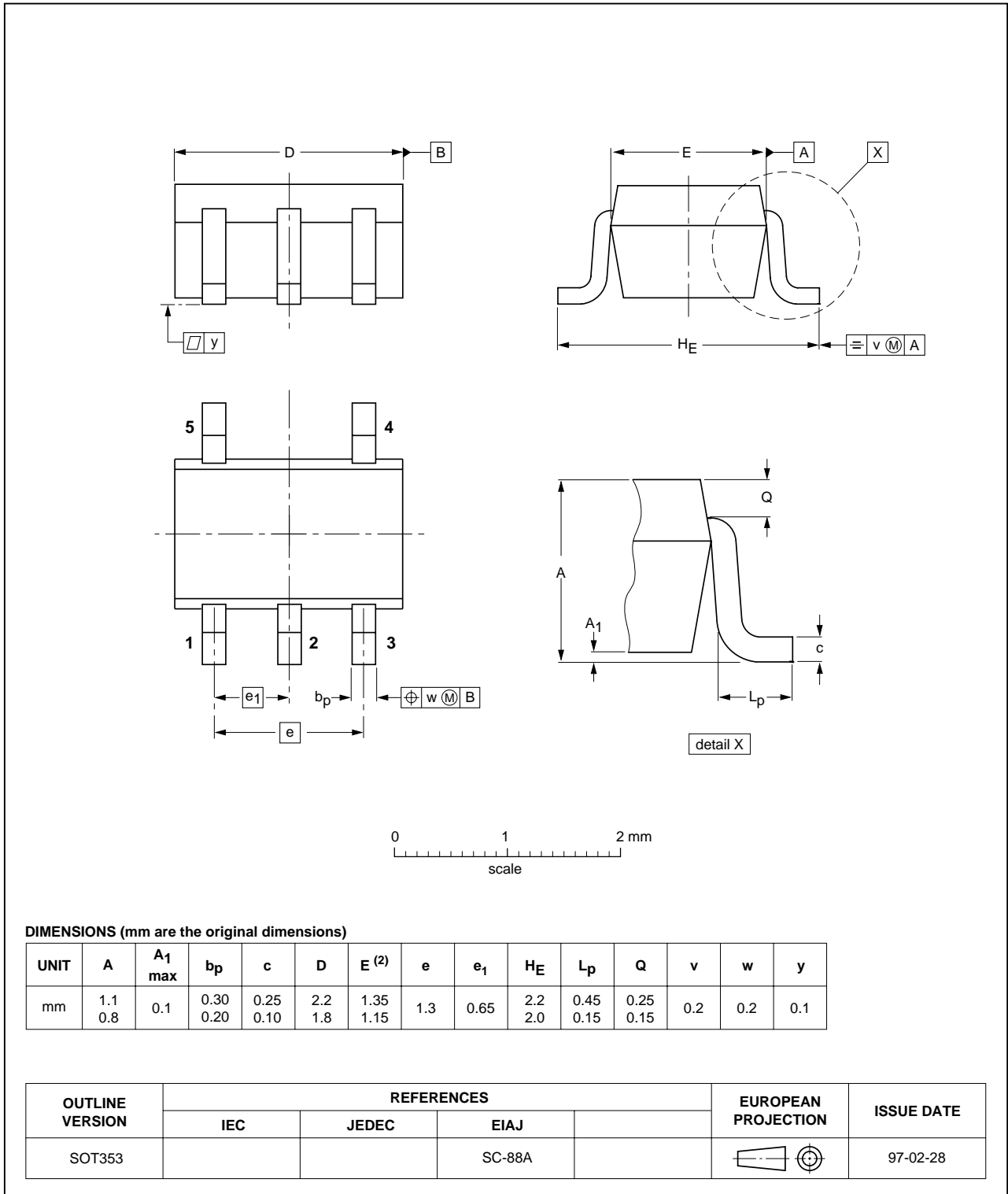
Single 2-input NOR gate

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PACKAGE OUTLINES

Plastic surface mounted package; 5 leads

SOT353

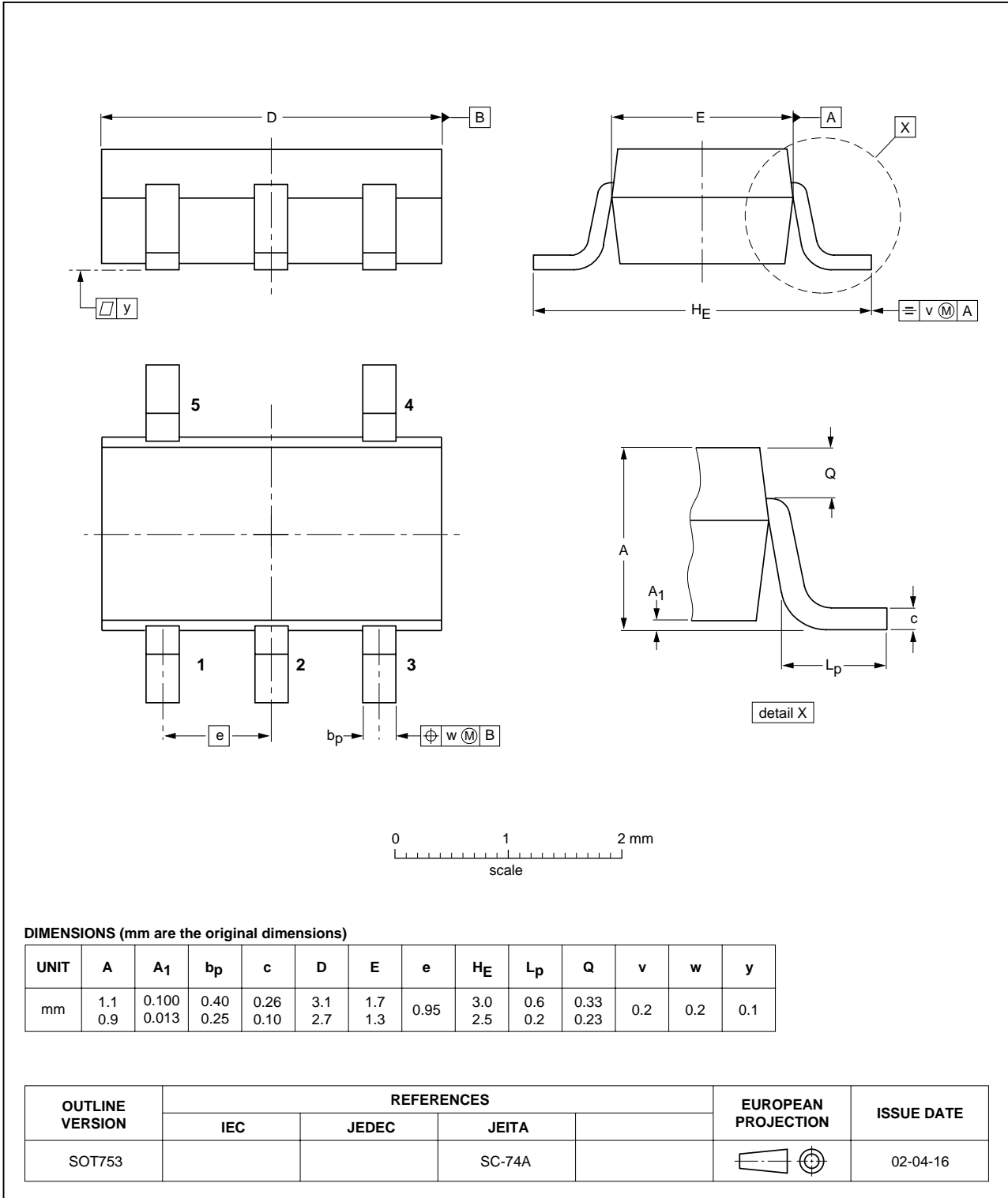


Single 2-input NOR gate

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Plastic surface mounted package; 5 leads

SOT753

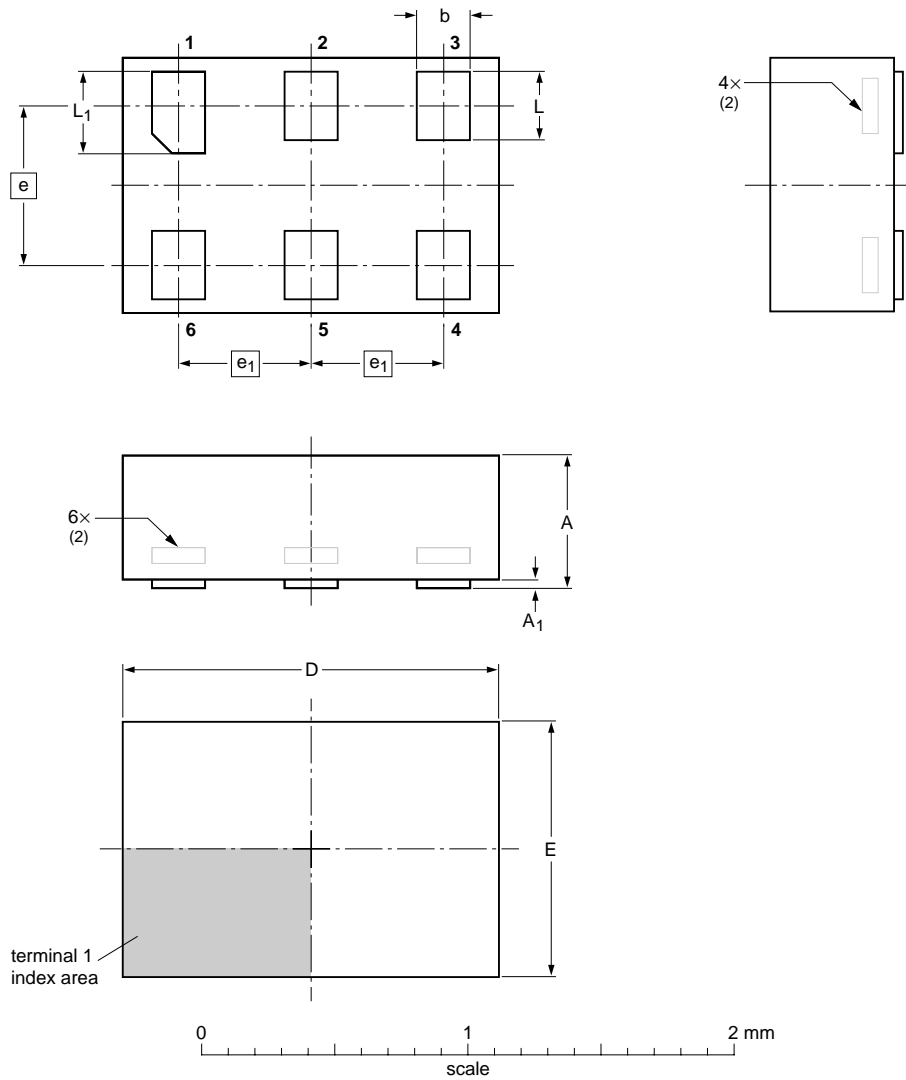


Single 2-input NOR gate

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XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm

SOT886



**DIMENSIONS (mm are the original dimensions)**

| UNIT | A <sup>(1)</sup><br>max | A <sub>1</sub><br>max | b            | D          | E            | e   | e <sub>1</sub> | L            | L <sub>1</sub> |
|------|-------------------------|-----------------------|--------------|------------|--------------|-----|----------------|--------------|----------------|
| mm   | 0.5                     | 0.04                  | 0.25<br>0.17 | 1.5<br>1.4 | 1.05<br>0.95 | 0.6 | 0.5            | 0.35<br>0.27 | 0.40<br>0.32   |

**Notes**

1. Including plating thickness.
2. Can be visible in some manufacturing processes.

| OUTLINE VERSION | REFERENCES |        |       | EUROPEAN PROJECTION | ISSUE DATE           |
|-----------------|------------|--------|-------|---------------------|----------------------|
|                 | IEC        | JEDEC  | JEITA |                     |                      |
| SOT886          |            | MO-252 |       |                     | 04-07-15<br>04-07-22 |

## Single 2-input NOR gate

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## DATA SHEET STATUS

| LEVEL | DATA SHEET STATUS <sup>(1)</sup> | PRODUCT STATUS <sup>(2)(3)</sup> | DEFINITION   |
|-------|----------------------------------|----------------------------------|--|
| I     | Objective data                   | Development                      | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.  |
| II    | Preliminary data                 | Qualification                    | This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.             |
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