# PTN5150

## CC logic for USB Type-C applications

Rev. 1 — 9 December 2016 Product data sheet

## 1. General description

PTN5150 is a small thin low power CC Logic chip supporting the USB Type-C connector application with Configuration Channel (CC) control logic detection and indication functions. The features of PTN5150 enable USB Type-C connector to be used in both host and device ends of the Type-C cable. It can support Type-C to USB legacy cables and adapters defined in USB Type-C Spec. PTN5150 can work autonomously, or can connect to a controller through $I^2C$-bus interface.

PTN5150 can be configured to dual role, host, or device mode through external configuration pin or through I2C interface. The CC control logic detection and indication block supports 3 current modes (default current 500 mA/900 mA, medium current 1.5 A and high current 3.0 A) in DFP advertisement's perspective. When in UFP advertisement's perspective, the control logic will detect if a DFP with different pull-up Rp current source is connected. In addition, it will detect if Ra is present on CC1/CC2 pins. Upon detection of plug orientation, pin ID will indicate if PTN5150 is working under either host role or device role, and other status will also be reflected in I2C registers.

## 2. Features and benefits

- Support type C connector with existing chipsets
  - USB Type-C Rev 1.1 compliance
  - Compatible with legacy OTG hardware and software
  - Support plug, orientation, role and charging current detection.
  - USB-ID pin for OTG application
  - $I^2C$-bus interface support for fast mode
- CC control logic detection and indication
  - PORT input pin to configure in DRP (Hi-Z), UFP (low) or DFP (high)
  - Current mode detection when PTN5150 is operating under UFP (device) role: default current mode (<0.5 A/0.9 A); medium current mode (<1.5 A); high current mode (<3.0 A)
  - Integrated accurate Rp current sources to support default mode and high current mode under host mode: default current mode at 80 μA; medium current mode at 180 μA; high current mode at 330 μA
  - Integrate Rd resistor in UFP mode
  - Report detail port states and accessory modes in I2C registers
  - Support VCONN1/2 power detected status through VCONN Status I2C register 0AH
- Current consumption:
  - Hibernation mode: 4.5 μA
  - Standby in DRP mode: 15 μA

- Standby in DFP mode: 15 μA
- Standby in UFP mode: 15 μA

- Power supply: VDD = 2.7 V to 5.5 V
- VBUS_DET: 28 V Absolute Max Tolerance
- High ESD protection for VBUS and CC1/2 pins
  - ESD protection exceeds 7000 V HBM per JDS-001-2012 and 500 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Operating Temperature Range: −40 °C to +85 °C
- X2QFN12 package 1.6 mm × 1.6 mm × 0.35 mm, 0.4 mm pitch

# 3. Applications

- Tablets/Mobile Devices
- Ultrabook/Notebook Computers
- Docking Stations

# 4. Ordering information

**Table 1. Ordering information**

| Type number | Topside marking | Package | | |
|---|---|---|---|---|
| | | Name | Description | Version |
| PTN5150HX | 50 | X2QFN12 | Plastic, super thin quad flat package; no leads; 12 terminals; body 1.6 mm × 1.6 mm × 0.35 mm, 0.4 mm lead pitch. | SOT1355-1 |

## 4.1 Ordering options

**Table 2. Ordering options**

| Type number | Orderable part number | Package | Packing method | Minimum order quantity | Temperature |
|---|---|---|---|---|---|
| PTN5150HX | PTN5150HXMP | X2QFN12 | REEL 13" Q2/T3 *STANDARD MARK SMD DP | 10000 | $T_{amb}$ = −40 °C to +85 °C |


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# 5. Functional diagram

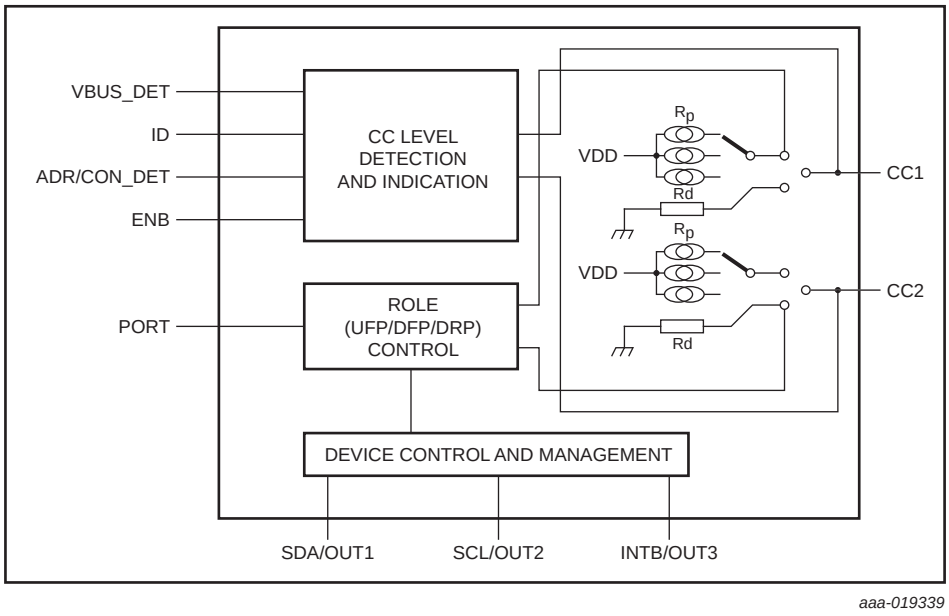
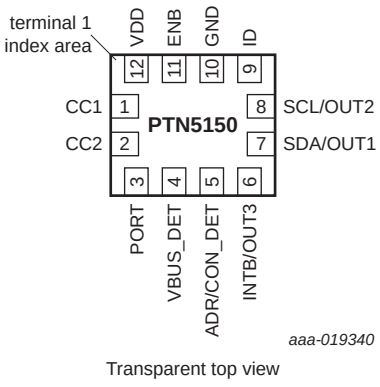



**Fig 1. Functional diagram**

# 6. Pinning information

## 6.1 Pinning




Transparent top view

**Fig 2. Pin configuration**


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## 6.2 Pin description

**Table 3. Pin description**

| Symbol | Pin | Type | Description |
|---|---|---|---|
| 1 | CC1 | I/O | Configure Channels as defined in USB Type-C specification |
| 2 | CC2 | | |
| 3 | PORT | Input | Trinary GPIO Input selection run from VDD<br>PORT= VDD: DFP mode (Rp = 80uA power default for non-I2C mode).<br>PORT= Mid (or floating): DRP mode<br>PORT=GND: UFP mode<br>If ADR = High or Low (I2C mode), PORT input status will be only latched during power up. To change the mode selection, system must write I2C register bit to override mode selection.<br>If ADR = Mid (no- I2C mode). PORT input can be dynamically change. |
| 4 | VBUS_DET | Input | VBUS Detection Pin. (28 V Max Tolerance)<br>Directly tie to VBUS of the USB Type-C receptacle |
| 5 | ADR/CON_DET | I/O | Trinary GPIO Input ADR pin run from VDD<br>• ADR pull up to VDD with 10 kΩ resistor (I2C Enabled with ADDR bit 6 equal to 1, I2C Address 0x7A)<br>• ADR pull down to GND with 10 kΩ resistor. (I2C Enabled with ADDR bit 6 equal to 0, I2C Address 0x3A)<br>• ADR = Mid or floating (Pin 6/7/8) configured as OUT1/2/3 in non-I2C mode<br>Output. This pin will automatically switch from input to CON_DET output in "non-I2C mode or set 09H bit[0] to 0" after TINPUTLATCH<br>• CON_DET = High (Connection Detected)<br>• CON_DET = Low (No Connection) |
| 6 | INTB/OUT3 | O/D output | Interrupt to notify I2C status register changed<br>INTB: (only valid in I2C mode)<br>• Low = Interrupt asserted<br>• Hi-Z = Interrupt de-asserted<br>OUT3: (only valid in non- I2C mode)<br>• Low = Analog Audio Detected<br>• Hi-Z = No Detection |
| 7 | SDA/OUT1 | O/D Input /output | I2C SDA (Open Drain Input & Output)<br>OUT 2 & OUT 1 : (Open Drain Output)<br>0 0 = high current mode<br>1 0 = medium current mode<br>1 1 = default current mode |
| 8 | SCL/OUT2 | O/D Input /output | I2C SCL (Open Drain Input)<br>OUT 2 & OUT 1 : (Open Drain Output)<br>0 0 = high current mode<br>1 0 = medium current mode<br>1 1 = default current mode |
| 9 | ID | O/D output | ID (Open Drain Output)<br>Low = DFP mode detected valid UFP on CC1 or CC2 line. This signal is used to enable OTG mode, requires external pull up resistor. |


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**Table 3. Pin description** *...continued*

| Symbol | Pin | Type | Description |
|---|---|---|---|
| 10 | GND | Power | Ground |
| 11 | ENB | Input | Chip Enable and Disable<br>• Low = Chip Enable<br>• High = Chip Disable to Hiberation mode. Note that I2C register values are lost when ENB is HIGH. |
| 12 | VDD | Power | Power supply |

# 7. Functional description

## 7.1 CC detection and indication block

For USB Type-C solution, two pins on the connector, CC1 and CC2, are used to establish and manage the DFP/UFP connection between a host port and a device port.

A hardware GPIO trinary pin, PORT, is provided to configure PTN5150 in either DFP/DRP/UFP mode alternatively, the PORT input can be override later by override the I2C registers. If the GPIO Trinary ADR input is mid-level or floating (non I2C), PORT input pin can dynamically change at any time to reconfigure the DFP/DRP/UFP. The GPIO trinary input pins should be powered by VDD.

- When PTN5150 is operating under host role, different current modes (high/medium/default) can be configured through I2C register. During initial power up, default current mode is being selected. In order to indicate different current modes, three Rp current sources are being implemented.

**Table 4. Current source implementation for each DFP advertisement**

| DFP advertisement | Current source to VDD | Current source precision |
|---|---|---|
| Default USB Power | 80 μA | ±20 % |
| 1.5 A at 5 V | 180 μA | ±8 % |
| 3.0 A at 5 V | 330 μA | ±8 % |

Internal comparators are constantly monitoring the voltage levels of CC1 and CC2 pins. PTN5150 reports if an UFP (device) or powered cable is connected externally on the CC pins. When no external connection is detected, cable connected bit in the I2C register will be cleared. Any changes in the attach/detach events or Rp current source changes will trigger INTB pin to go LOW.

**Table 5. RD implementation for each UFP advertisement**

| UFP advertisement | RD value | RD accuracy |
|---|---|---|
| UFP mode | 5.1 kΩ | ±10 % |

**Table 6. Voltage range detection for each DFP advertisement**

| DFP advertisement | UFP ($V_{Rd}$) voltage range | Powered cable/adapter $V_{Ra}$ voltage range | No connect ($V_{open}$) voltage range |
|---|---|---|---|
| Default USB Power | 0.25 V to 1.50 V | 0.00 V to 0.15 V | >1.65 V |
| 1.5 A at 5 V | 0.45 V to 1.50 V | 0.00 V to 0.35 V | >1.65 V |
| 3.0 A at 5 V | 0.85 V to 2.45 V | 0.00 V to 0.75 V | >2.75 V |


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- When PTN5150 is operating under device role (UFP), it is able to detect different current modes indicated by external host's pull-up resistors. Internally there is a pull-down resistor (Rd) of 5.1 kΩ on CC1 and CC2 pins. Status of current mode detected is reported in the I2C register. If pin 6/7/8 is configured as OUT1/2/3, OUT1/2 reports the detected Rp pull up current source value as well.

The configuration channel (CC1 or CC2) is used to serve the following purposes in this block

- Detect connection of USB ports, e.g. a DFP (host) or a UFP (device), and establish host or device roles between two connected ports. When there is no power supplied to PTN5150, device role (with internal pull-down resistor Rd active) will be the default configuration.
- Resolve cable orientation and twist connections to establish USB data bus routing.
- Discover optional accessory modes such as audio adapter accessory and debug accessory modes. Resistors (Ra, Rd, Rp, or Open) connected on CC1/CC2 will be reported in the I2C registers, and host controller can configure the external interface accordingly.

## 7.2 ADR/CON_DET output pin

Pin 5 is multiple purpose I/O pin. When device power up, pin 5 is input which latched the input voltage level to configure I2C address. The I2C register offset 09H has default value "1" to disable CON_DET output. After TINPUT_LATCH, pin 5 becomes CON_DET output. When USB Type-C cable attached or detached in either DFP or UFP mode, CON_DET will asserted a signal to notify the system the status. The same attached or detached status also stored in the I2C interrupt register.

For ADR strapping resistor selection, 10 kΩ pull up or pull down resistor is recommended.

## 7.3 VCONN1/VCONN2 power output control

When a USB Type-C system need to support VCONN power in DFP or UFP power accessories mode, the system need to know the orientation to provide VCONN power. PTN5150 provides two bits of VCONN status register 0AH and an interrupt signal to notify system whether VCONN power is detected on VCONN1 or VCONN2 and then turn on discrete PowerFET using via 2 x GPIO. Figure 3 shows the system level implementation of VCONN power with PTN5150.


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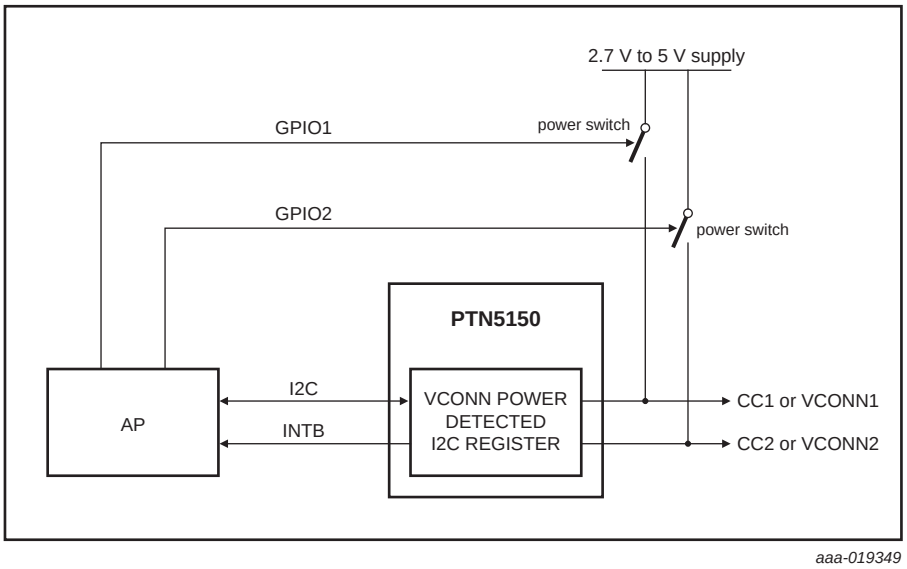



**Fig 3. Schematic connections to turn on/off VCONN1/2 power**

## 7.4 Off state

When PTN5150 is not powered (i.e., VDD=0V), special steps should be done to prevent back-current issues on control pins such PORT or ADR pins when these pins' states are not low. These pins can be controlled through two different ways.

1. pull-up/pull-down resistors - make sure these pull-up resistors' VDD is the same power source as to power PTN5150. When power to PTN5150 is off, power to these pull-up resistors will be off as well.
2. external processor's GPIO - if PTN5150 is turned off when the external processor's power stays on, processor should configure these GPIOs connected to these control pins as output low (< 0.4 V) or tri-state mode (configure GPIOs as input mode). This will make sure no current will be flowing into PTN5150 through these control pins.

## 7.5 I²C-bus

PTN5150 can work with systems with or without I²C-bus. “I2C mode” is defined as ADR pin has external 10 kΩ pull-up or pull-down resistor during power up, and “non-I2C mode” is defined as ADR pin is not connected to any external pull-up or pull-down resistor during power up. When operating in I2C mode, all features of PTN5150 can be configured and accessed through registers. OUT1, OUT2, OUT3 are not available in I2C mode. PORT input will be a one-time latched during power up.

In non-I2C mode, a subset of features can be configured or accessed through these I/O pins:

- PORT input: In non I²C-bus mode, PORT input can be dynamically change.
- CON_DET output: attached/detached notification
- OUT1/OUT2 output: detected Rp current source value
- OUT3: Analog Audio Detect


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## 7.6 I²C-bus programmability

PTN5150 has I²C-bus interface that enables system integrator to program register settings suitable for the application needs. Table 7 describes possible settings for different functions of the device. Although some functions of the device can be configured through external hardware pins (such as PORT), it also allows the system integrator to override the settings by programming the internal registers through I2C.

After power-on, the device samples the hardware pin values (as I2C is not operational yet) and reflects the status in the I2C status registers as default condition.

**Table 7. I2C registers and descriptions**

| Register offset | Register name | Bits | Reset value | Description |
|---|---|---|---|---|
| 01H<br>Read Only | Version ID | [7:3] | 00001 | Device version ID |
| | Vendor ID | [2:0] | 011 | Vendor ID |
| 02H<br>Read/Write | Control | [7:5] | 000 | Reserved |
| | | [4:3] | 00 | Rp Selection (DFP mode)<br>00: 80 μA Default<br>01: 180 μA Medium<br>10: 330 μA High<br>11 Reserved |
| | | [2:1] | PORT pin state | Mode Selection<br>00: Device (UFP Mode)<br>01: Host (DFP Mode)<br>10: Dual Role (DRP Mode)<br>During power up, device will latch the input of PORT input pin to configure UFP/DFP/DRP. After power up, writing to these register bits will overwrite the PORT Mode selection. |
| | | [0] | 0 | Interrupt Mask for detached/attached<br>0: Does not Mask Interrupts<br>1: Mask Interrupts for register offset 03H bit[1:0]. |
| 03H<br>Read Only/Clear on Read | Interrupt Status | [7:2] | 000000 | Reserved |
| | | [1] | 0 | Cable Detach Interrupt<br>0: No Interrupt<br>1: Cable Detached |
| | | [0] | 0 | Cable Attach Interrupt<br>0: No Interrupt<br>1: Cable Attached |


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**Table 7. I2C registers and descriptions** *...continued*

| Register offset | Register name | Bits | Reset value | Description |
|---|---|---|---|---|
| 04H<br>Read Only | CC Status | [7] | 0 | VBUS Detection (UFP mode after valid CC detection)<br>0: VBUS not detected<br>1: VBUS detected |
| | | [6:5] | 00 | Rp Detection (In UFP mode)<br>00: Standby<br>01: Rp = Std USB<br>10: Rp = 1.5A<br>11: Rp = 3.0A |
| | | [4:2] | 000 | Port Attachment Status<br>000: Not Connected<br>001: DFP attached<br>010: UFP attached<br>011: Analog Audio Accessory attached<br>100: Debug Accessory attached<br>101: Reserved<br>110: Reserved<br>111: Reserved |
| | | [1:0] | 00 | CC Polarity<br>00: Cable Not Attached<br>01: CC1 is connected (normal orientation)<br>10: CC2 is connected (reversed orientation)<br>11: Reserved |
| 05H | Reserved | [7:0] | 00000000 | Reserved |
| 06H | Reserved | [7:0] | 00000000 | Reserved |
| 07H | Reserved | [7:0] | 00000000 | Reserved |
| 08H | Reserved | [7:0] | 00000000 | Reserved |
| 09H<br>Read/Write | CON_DET configuration register | [7:1] | 0000000 | Reserved |
| | | [0] | 1 | Disable CON_DET output bit (Read/Write)<br>0: Enable CON_DET output on pin 5<br>1: Disable CON_DET output on pin 5<br>Recommend to disable CON_DET output for system using I2C to access PTN5150 |


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**Table 7. I2C registers and descriptions** *…continued*

| Register offset | Register name | Bits | Reset value | Description |
|---|---|---|---|---|
| 0AH<br>Read Only | VCONN Status register | [7:2] | 000000 | Reserved |
| | | [1:0] | 00 | VCONN Detected Status (Read Only)<br>00: Standby<br>01: VCONN power should be applied on CC1<br>10: VCONN power should be applied on CC2<br>11: Reserved<br>Ra detect happens in all modes. VCONN enable happens autonomously when as DFP (including in DRP mode).<br>Prior to accessing this register, system must write register offset 43H with value of 0xe0 to enable VCONN detected status. If register offset 43H is not set to 0xe0, VCONN detected status read out is always 00. |
| 10H | Reset register | [7:1] | 0000000 | Reserved. |
| | | [0] | 0 | 1: Reset system digital block |
| 11H | Reserved | [7:0] | 00001100 | Reserved. Do not write any other values other than “00001100” (power up setting) to this register |
| 12H | Reserved | [7:0] | 000000 | Reserved. |
| 13H | Reserved | [7:0] | 10100001 | Reserved. Do not write to this register |
| 14H | Reserved | [7:0] | 00011111 | Reserved. Do not write to this register |
| 15H | Reserved | [7:0] | 11001001 | Reserved. Do not write to this register |
| 16H | Reserved | [7:0] | 01010001 | Reserved. Do not write to this register |
| 17H | Reserved | [7:0] | 01010000 | Reserved. Do not write to this register |
| 18H<br>Read/Write | Interrupt Mask register | [7] | 0 | Reserved |
| | | [6] | 0 | Reserved |
| | | [5] | 0 | Reserved |
| | | [4] | 1 | Interrupt Mask for CC1 or CC2 Comparator Change<br>0: Does not Mask Interrupts<br>1: Mask Interrupts |
| | | [3] | 1 | Interrupt Mask for role Change<br>0: Does not Mask Interrupts<br>1: Mask Interrupts |
| | | [2] | 1 | Interrupt Mask for orientation Found<br>0: Does not Mask Interrupts<br>1: Mask Interrupts |
| | | [1] | 1 | Interrupt Mask for debug Accessories Found<br>0: Does not Mask Interrupts<br>1: Mask Interrupts |
| | | [0] | 1 | Interrupt Mask for audio Accessories Found<br>0: Does not Mask Interrupts<br>1: Mask Interrupts |


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**Table 7. I2C registers and descriptions** *…continued*

| Register offset | Register name | Bits | Reset value | Description |
|---|---|---|---|---|
| 19H<br>Read Only/Clear on Read | Interrupt Register status | [7] | 0 | Reserved |
| | | [6] | 0 | Reserved |
| | | [5] | 0 | Reserved |
| | | [4] | 0 | Interrupt Status for Comparator Change<br>0: No interrupt<br>1: When attached as UFP, Change of Rp current advertisement detected. New advertisement is reflected on register offset 04H bit[6:5]. |
| | | [3] | 0 | Interrupt status for role change<br>0: No interrupt<br>1: Role changed detected. New role is reflected on register offset 04H bit[4:2]. |
| | | [2] | 0 | Interrupt status for orientation found<br>0: No interrupt<br>1: Orientation detected on attachment. New orientation is reflected on register offset 04H bit[1:0]. |
| | | [1] | 0 | Interrupt status for debug accessories found<br>0: No interrupt<br>1: Debug Accessory attachment detected. Register offset 04H bit[4:2] should be updated to 3'b100. |
| | | [0] | 0 | Interrupt status for audio accessories found<br>0: No interrupt<br>1: Audio Accessory attachment detected. Register offset 04H bit[4:2] should be updated to 3'b011. |

## 7.7 I²C-bus read and write operations

PTN5150 supports programming of the internal registers through the I²C-bus interface. I²C-bus can support up to 400 kHz data rate. 8-bit device slave address of PTN5150 is defined in combination with ADR pin.

**Table 8. Read/write device slave address**

| Name | Size (Bits) | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Slave address | 8 | 0 | ADR | 1 | 1 | 1 | 0 | 1 | R/W |

Reading/writing the internal registers must be done according to the following protocol. The read protocol contains two phases:

- Command phase
- Data phase

The command phase is an I2C write to PTN5150 that contains a single data byte indicating the internal register address to read out. The data phase is an I2C read operation that contains one byte of data and STOP bit is asserted, starting from the least significant byte.


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The I2C write operation contains only the command phase, which contains 8-bit internal register address, followed by one byte of data to be written to the register, starting from the least significant byte.

It is recommended to use single-byte write/read commands to PTN5150. Incremental address read/write function is not supported. Figure 4 and Figure 5 illustrate the protocol used on the I²C-bus to write and read register inside the device.

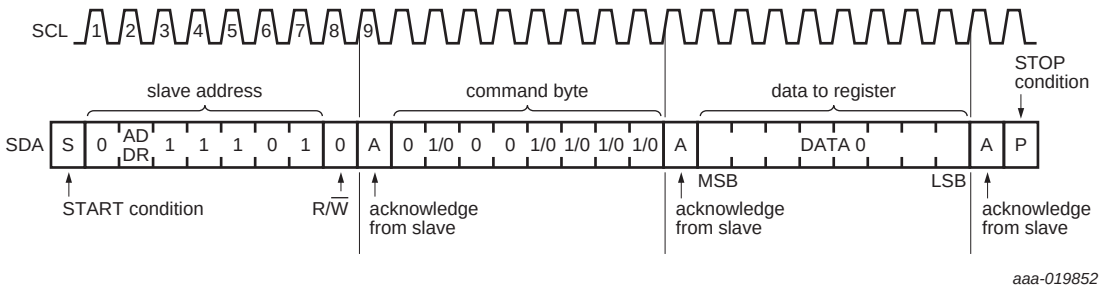



**Fig 4. I²C-bus write sequences**

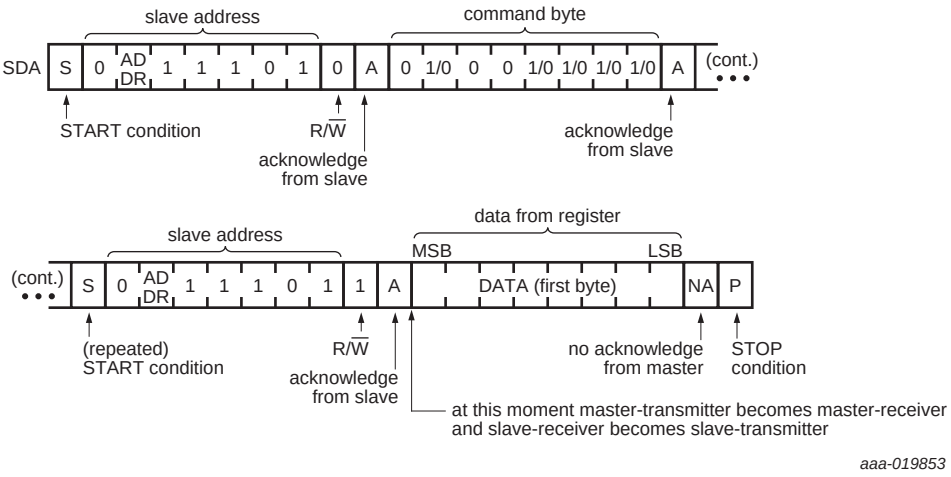



**Fig 5. I²C-bus read sequences**


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# 8. Limiting values

**Table 9. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| VDD[1] | Supply voltage | | –0.5 | +6.0 | V |
| VBUS_DET | VBUS Detect | | –0.5 | +28.0 | V |
| Control pins | PORT, ADR/CON_DET, INTB/OUT3, CC1, CC2, ENB, ID | | –0.5 | VDD +0.3 | V |
| | SCL/OUT2, SDA/OUT1 | | –0.5 | VDD +0.3 | V |
| $T_{stg}$ | Storage temperature | | -65 | 150 | °C |
| $V_{esd}$ | Electrostatic discharge CC1/CC2/VBUS_DET | HBM[2] | - | 7000 | V |
| | All other pins | HBM[2] | - | 2000 | V |
| | All pins | CDM[3] | - | 500 | V |

[1] All voltage values, except differential voltages, are with respect to network ground terminal.

[2] Human Body Model: ANSI/EOS/ESD-S5.1-1994, standard for ESD sensitivity testing, Human Body Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

[3] Charged Device Model: ANSI/EOS/ESD-S5.3-1-1999, standard for ESD sensitivity testing, Charged Device Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

# 9. Recommended operating conditions

**Table 10. Operating conditions**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| VDD | supply voltage | –40 to +85 °C | +2.7 | | +5.5 | V |
| $T_{VDDramp}$ | VDD ramp up time | Time to reach 90% of VDD | - | - | 10 | ms |
| VBUS_DET | VBUS Detect | VBUS Analog Input | 4.0 | 5.0 | 21 | V |
| $V_i$ | input voltage | CMOS inputs (PORT, ADR) | –0.5 | - | VDD+0.3 | V |
| | | I2C inputs (SCL, SDA, ENB) | –0.5 | - | 1.98 | V |
| $T_{amb}$ | ambient temperature | operating in free air | –40 | - | 85 | °C |

# 10. Characteristics

**Table 11. General characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Device role (UFP) Sink CC Detection** | | | | | | |
| Rd | Pull down resistor | UFP mode | 4.59 | 5.10 | 5.61 | kΩ |
| $V_{CLAMPH}$ | High current mode clamp voltage | VDD=0 V | 0.85 | - | 2.18 | V |
| $V_{CLAMPM}$ | Medium current mode clamp voltage | VDD=0 V | 0.45 | - | 1.25 | V |


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**Table 11. General characteristics** *...continued*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CLAMPD}$ | Default current mode clamp voltage | VDD=0 V | 0.25 | - | 1.25 | V |
| $V_{THH}$ | High current mode threshold | UFP mode | 1.16 | 1.23 | 1.31 | V |
| $V_{THM}$ | Medium current mode threshold | UFP mode | 0.61 | 0.66 | 0.70 | V |
| $V_{THD}$ | Default current mode threshold | UFP mode | 0.15 | 0.2 | 0.25 | V |
| **Host role (DFP advertisement) Current source** | | | | | | |
| $I_{PH}$ | Current source | High current source mode (3 A) | 304 | 330 | 356 | µA |
| $I_{PM}$ | Current source | Medium current source mode (1.5 A) | 166 | 180 | 194 | µA |
| $I_{PD}$ | Current source | Default current source mode | 64 | 80 | 96 | µA |
| **VBUS Detect Threshold** | | | | | | |
| $V_{VBUSDET}$ | VBUSDET threshold | No external R | 2.5 | 3.0 | 3.5 | V |
| **Current Consumption** | | | | | | |
| $I_{DD_hibernation}$ | hibernation mode current | VDD = 3.3 V; ENB = high | 2 | 4.5 | 10 | µA |
| $I_{DD_active}$ | active supply current; cable attached | VDD = 3.3 V<br>PORT = high (DFP) | 65 | 100 | 130 | µA |
| | | VDD = 3.3 V<br>PORT = low (UFP) | 5 | 15 | 35 | µA |
| $I_{DD_standby}$ | standby/polling current; no cable attached | VDD = 3.3 V<br>PORT = floating (DRP) | 5 | 15 | 35 | µA |
| | | VDD = 3.3 V<br>PORT = high (DFP) | 5 | 15 | 35 | µA |
| | | VDD = 3.3 V<br>PORT = low (UFP) | 5 | 15 | 35 | µA |
| $T_{CCdebounce}$ | debounce time | time a port shall wait before it can determine it is attached | - | 120 | - | ms |
| $T_{disconnection}$ | disconnection time | time a port shall respond when it is disconnected | - | 1.2 | - | ms |
| $T_{Startup}$ | start-up time | supply voltage valid to $R_p/R_d$ active | - | 25 | - | ms |
| $T_{rcfg}$ | | When selected DFP mode, system overwrite to UFP mode using $I^2C$ or PORT input, the Trcfg delay is measured from disabled Rp to enable Rd. | - | 2 | - | ms |
| | | When selected UFP mode, system overwrite to DFP mode using $I^2C$ or PORT input, the Trcfg delay is measured from to disable Rd and enable Rp. | - | 35 | - | ms |


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**Table 12. PORT control input characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{pu}$ | external pull up resistor | External pull-up resistor is connected to VDD | - | 10 | - | kΩ |
| $R_{pd}$ | external pull down resistor | External pull-down resistor is connected to GND | - | 10 | - | kΩ |
| $V_{IL}$ | Input Low Voltage | | - | - | 0.4 | V |
| $V_{IM}$ | Input Mid level Voltage | | 40%*VDD | 50%*VDD | 60%*VDD | V |
| $V_{IH}$ | Input High Voltage | | 80%*VDD | - | - | V |

**Table 13. ADR/CON_DET input/output characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{pu}$ | external pull up resistor | External pull-up resistor is connected to VDD | - | 10 | - | kΩ |
| $R_{pd}$ | external pull down resistor | External pull-down resistor is connected to GND | - | 10 | - | kΩ |
| $V_{IL}$ | Input Low Voltage | | - | - | 0.4 | V |
| $V_{IM}$ | Input Mid level Voltage | | 40%*VDD | 50%*VDD | 60%*VDD | V |
| $V_{IH}$ | Input High Voltage | | 80%*VDD | - | - | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = 3 mA | 80%*VDD | - | - | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 3 mA | - | - | 20%*VDD | V |

[1] CON_DET output can be enabled or disabled by accessing I2C register offset 09H bit[0]

**Table 14. ENB, SCL and SDA input characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL(MAX)}$ | maximum input voltage low level | | – | - | +0.4 | V |
| $V_{IH(MIN)}$ | minimum input voltage high level | | 1.05 | - | - | V |
| **I2C Fast mode interface pins (SCL, SDA)** | | | | | | |
| $V_{HYS}$ | Hysteresis of Schmitt trigger inputs | | 0.09 | - | - | V |

**Table 15. Open-drain output buffer characteristics (OUT2, OUT1, INTB/OUT3, ID pins)**

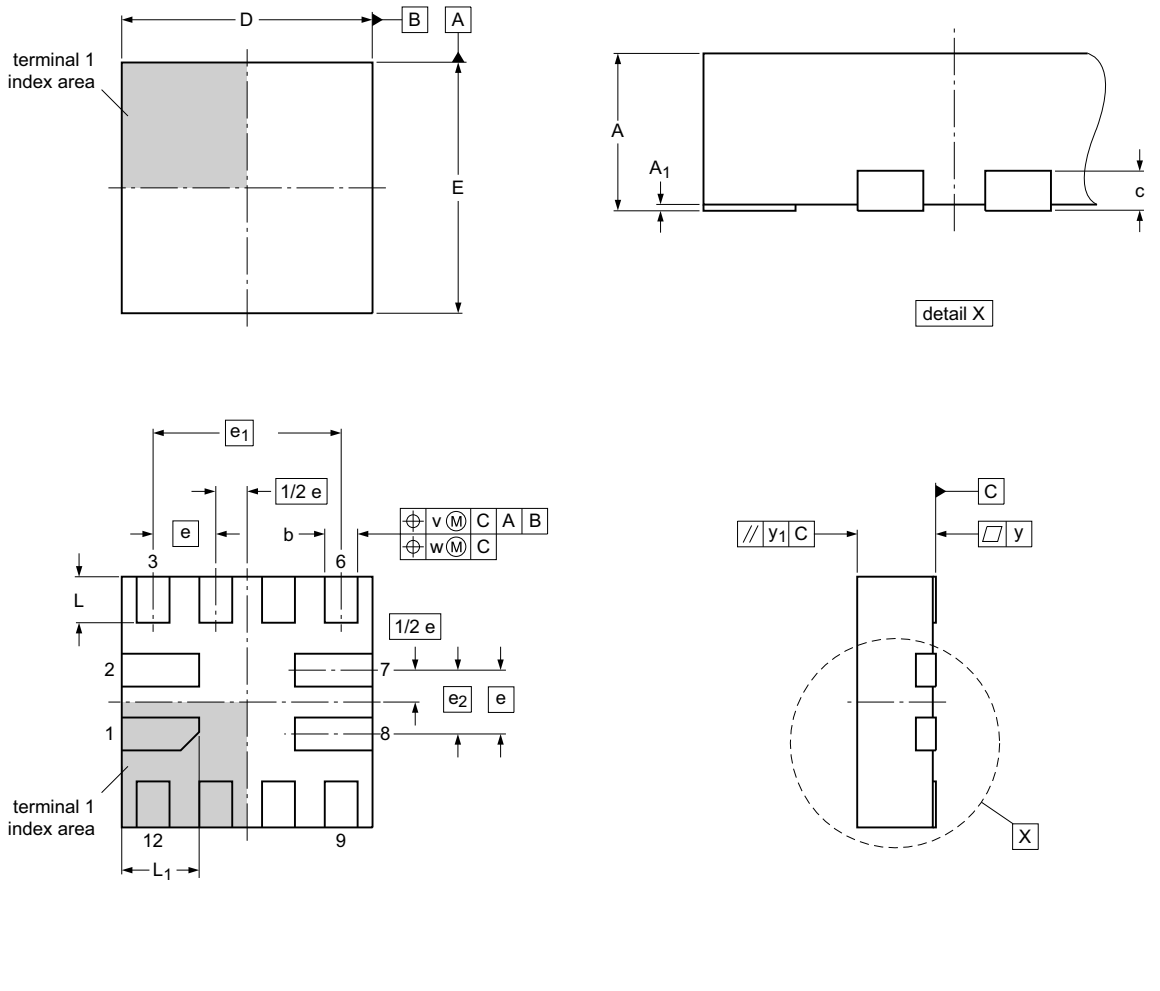
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{OL}$ | low-level output voltage | $I_{OL}$= 3 mA | 0 | - | 0.4 | V |


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# 11. Package outline

**X2QFN12: plastic, super thin quad flat package; no leads; 12 terminals; body 1.6 x 1.6 x 0.35 mm** **SOT1355-1**




Dimensions (mm are the original dimensions)

| Unit | A | $A_1$ | b | c | D | E | e | $e_1$ | $e_2$ | L | $L_1$ | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| max | 0.40 | 0.05 | 0.25 | | 1.65 | 1.65 | | | | 0.4 | 0.6 | | | | |
| mm nom | 0.35 | | 0.20 | 0.127 | 1.60 | 1.60 | 0.4 | 1.2 | 0.4 | 0.3 | 0.5 | 0.07 | 0.05 | 0.05 | 0.05 |
| min | 0.30 | 0.00 | 0.15 | | 1.55 | 1.55 | | | | 0.2 | 0.4 | | | | |

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

*sot1355-1_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT1355-1 | - - - | MO-255 | - - - | | | ~~13-12-23~~ 14-01-13 |

**Fig 6. Package outline X2QFN12 (SOT1355-1)**


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# 12. Packing information

## 12.1 X2QFN12; Reel dry pack, SMD, 13"; Q2/T3 standard product orientation; Orderable part number ending ,528 or MP; Ordering code (12NC) ending 528

### 12.1.1 Packing method

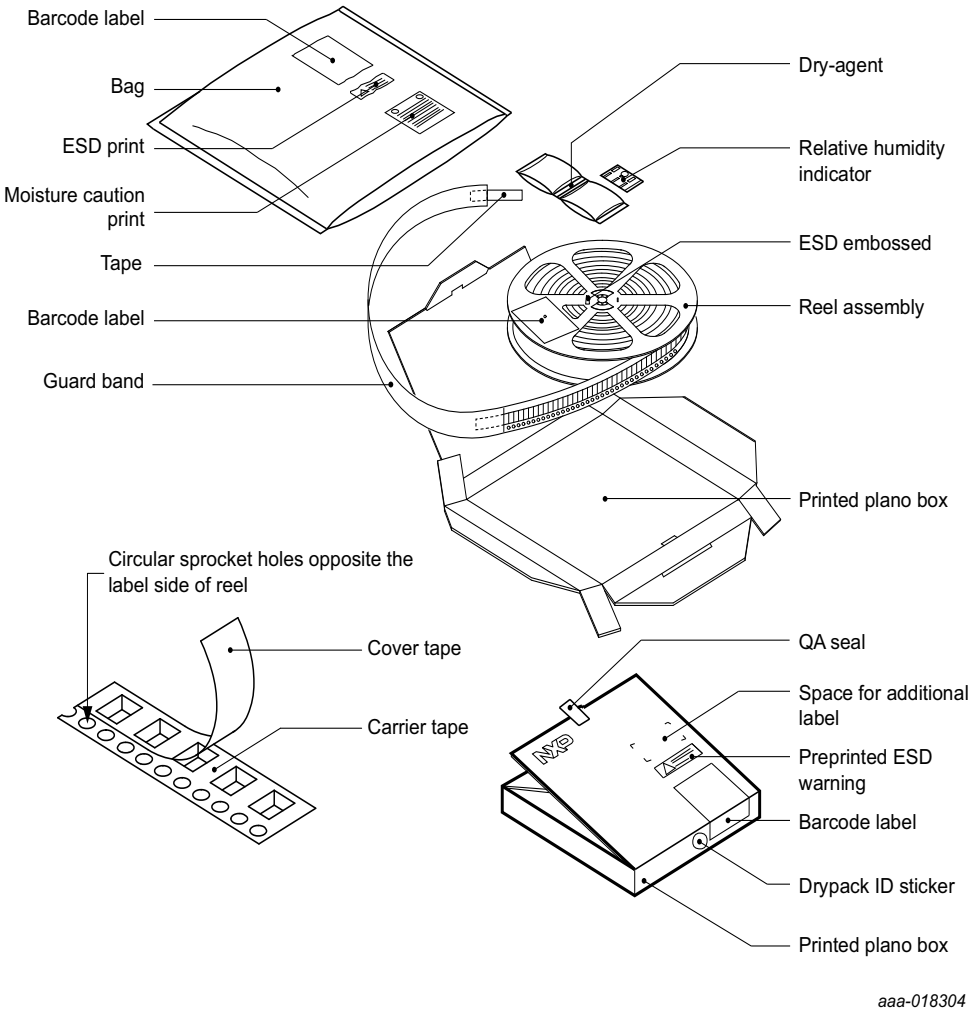



**Fig 7. Reel dry pack for SMD**


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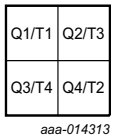
**Table 16. Dimensions and quantities**

| Reel dimensions d × w (mm) [1] | SPQ/PQ (pcs) [2] | Reels per box | Outer box dimensions l × w × h (mm) |
|---|---|---|---|
| 330 × 8 | 10000 | 1 | 342 × 338 × 39 |

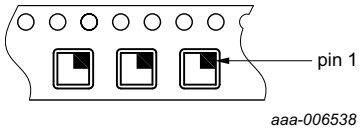
[1] d = reel diameter; w = tape width.

[2] Packing quantity dependent on specific product type.
View ordering and availability details at NXP order portal, or contact your local NXP representative.

### 12.1.2 Product orientation



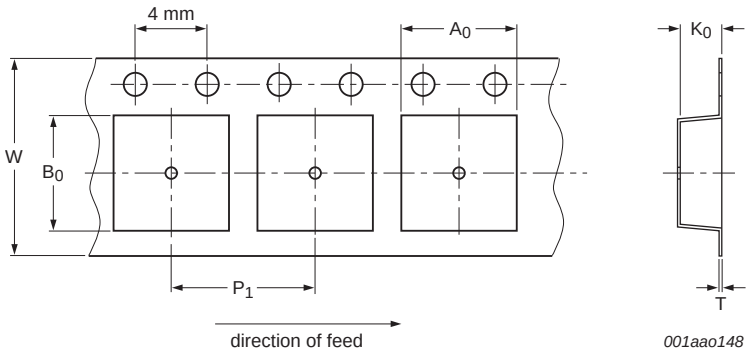

Tape pocket quadrants




Pin 1 is in quadrant Q2/T3

**Fig 8. Product orientation in carrier tape**

### 12.1.3 Carrier tape dimensions




Not drawn to scale.

**Fig 9. Carrier tape dimensions**

**Table 17. Carrier tape dimensions**
*In accordance with IEC 60286-3.*

| $A_0$ (mm) | $B_0$ (mm) | $K_0$ (mm) | T (mm) | $P_1$ (mm) | W (mm) |
|---|---|---|---|---|---|
| 1.85 ± 0.10 | 1.85 ± 0.10 | 0.50 ± 0.05 | 0.25 ± 0.05 | 4.0 ± 0.10 | 8 ± 0.30 |


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### 12.1.4 Reel dimensions

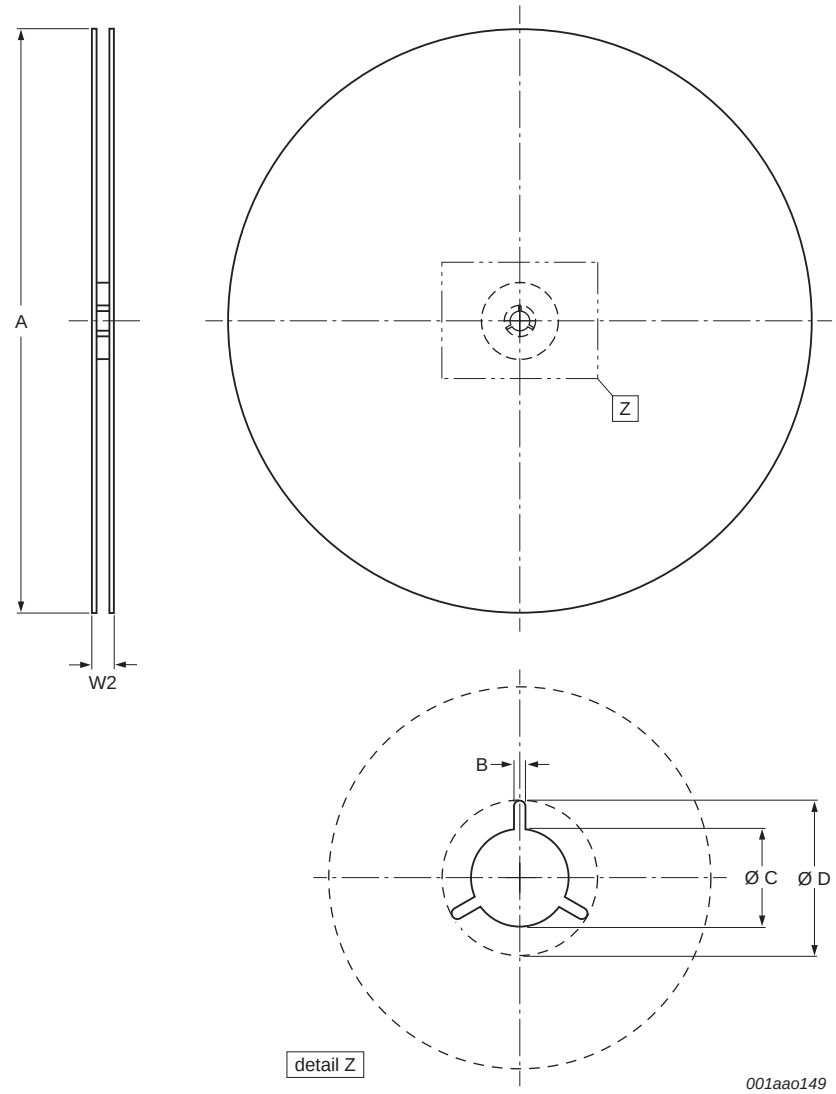



**Fig 10. Schematic view of reel**

**Table 18. Reel dimensions**

*In accordance with IEC 60286-3.*

| A [nom] (mm) | W2 [max] (mm) | B [min] (mm) | C [min] (mm) | D [min] (mm) |
|---|---|---|---|---|
| 330 | 14.4 | 1.5 | 12.8 | 20.2 |


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### 12.1.5 Barcode label

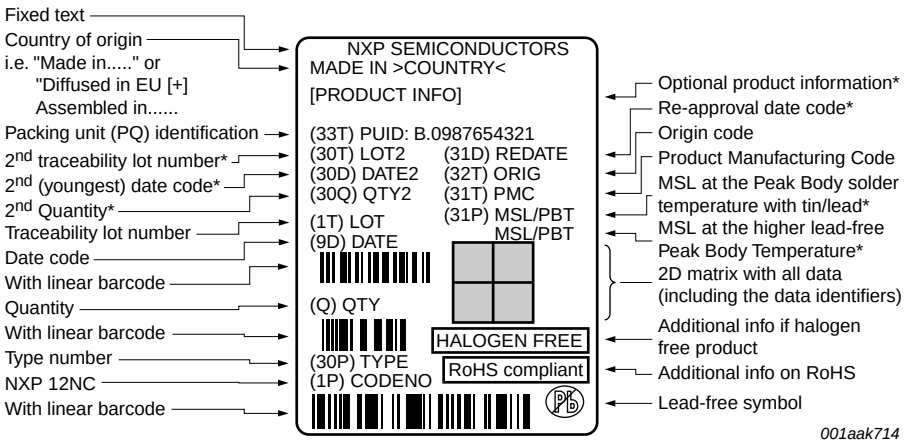



**Fig 11. Example of typical box and reel information barcode label**

**Table 19. Barcode label dimensions**

| Box barcode label<br>l × w (mm) | Reel barcode label<br>l × w (mm) |
|---|---|
| 100 × 75 | 100 × 75 |


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# 13. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

## 13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

## 13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

## 13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities


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## 13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 12) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 20 and 21

**Table 20. SnPb eutectic process (from J-STD-020D)**

| Package thickness (mm) | Package reflow temperature (°C) | |
|---|---|---|
| | Volume ($mm^3$) | |
| | < 350 | ≥ 350 |
| < 2.5 | 235 | 220 |
| ≥ 2.5 | 220 | 220 |

**Table 21. Lead-free process (from J-STD-020D)**

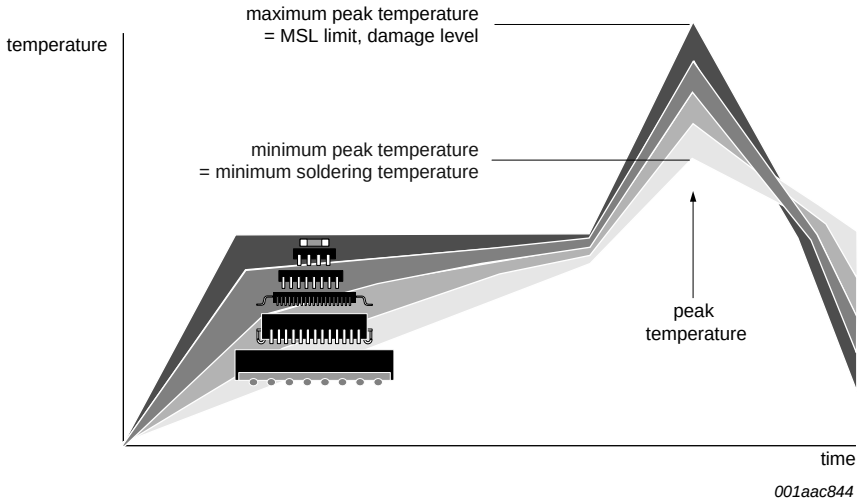
| Package thickness (mm) | Package reflow temperature (°C) | | |
|---|---|---|---|
| | Volume ($mm^3$) | | |
| | < 350 | 350 to 2000 | > 2000 |
| < 1.6 | 260 | 260 | 260 |
| 1.6 to 2.5 | 260 | 250 | 245 |
| > 2.5 | 250 | 245 | 245 |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 12.


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MSL: Moisture Sensitivity Level

**Fig 12. Temperature profiles for large and small components**

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.


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## 14. Soldering: PCB footprints

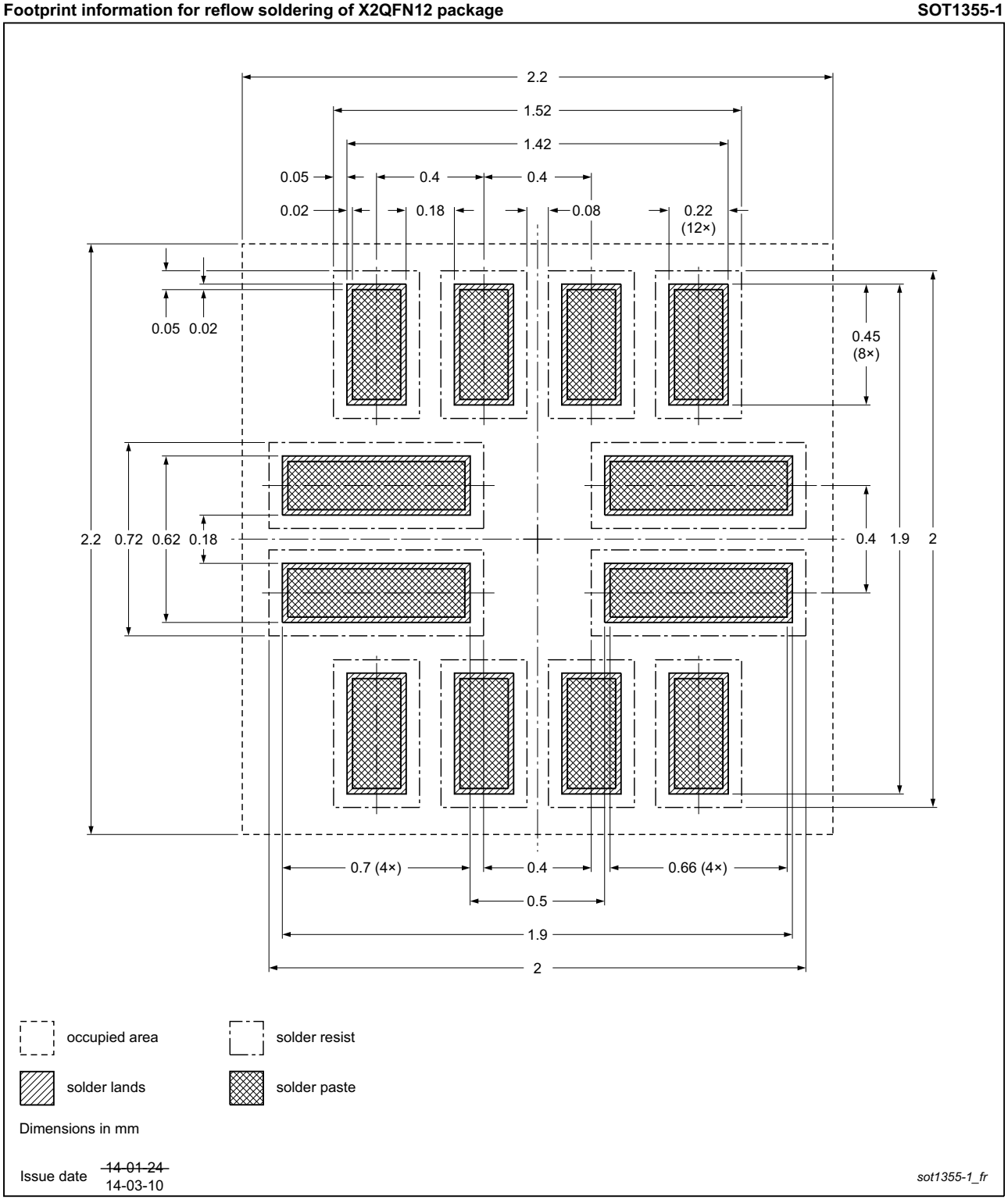



**Fig 13. PCB footprint for SOT1355-1 (X2QFN12); reflow soldering**


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# 15. Revision history

**Table 22. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| PTN5150 v.1.1 | 20161209 | Product data sheet | - | PTN5150 v.1 |
| Modifications: | • Table 2 “Ordering options”: Removed 500 piece MOQ<br>• Added Section 12 “Packing information” | | | |
| PTN5150 v.1 | 20160203 | Product data sheet | - | - |


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| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

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## 18. Contents

**1 General description . . . . . 1**
**2 Features and benefits . . . . . 1**
**3 Applications . . . . . 2**
**4 Ordering information . . . . . 2**
4.1 Ordering options . . . . . 2
**5 Functional diagram . . . . . 3**
**6 Pinning information . . . . . 3**
6.1 Pinning . . . . . 3
6.2 Pin description . . . . . 4
**7 Functional description . . . . . 5**
7.1 CC detection and indication block . . . . . 5
7.2 ADR/CON_DET output pin . . . . . 6
7.3 VCONN1/VCONN2 power output control . . . . . 6
7.4 Off state . . . . . 7
7.5 I²C-bus . . . . . 7
7.6 I²C-bus programmability . . . . . 8
7.7 I²C-bus read and write operations . . . . . 11
**8 Limiting values . . . . . 13**
**9 Recommended operating conditions . . . . . 13**
**10 Characteristics . . . . . 13**
**11 Package outline . . . . . 16**
**12 Packing information . . . . . 17**
12.1 X2QFN12; Reel dry pack, SMD, 13"; Q2/T3 standard product orientation; Orderable part number ending ,528 or MP; Ordering code (12NC) ending 528 . . . . . 17
12.1.1 Packing method . . . . . 17
12.1.2 Product orientation . . . . . 18
12.1.3 Carrier tape dimensions . . . . . 18
12.1.4 Reel dimensions . . . . . 19
12.1.5 Barcode label . . . . . 20
**13 Soldering of SMD packages . . . . . 21**
13.1 Introduction to soldering . . . . . 21
13.2 Wave and reflow soldering . . . . . 21
13.3 Wave soldering . . . . . 21
13.4 Reflow soldering . . . . . 22
**14 Soldering: PCB footprints . . . . . 24**
**15 Revision history . . . . . 25**
**16 Legal information . . . . . 26**
16.1 Data sheet status . . . . . 26
16.2 Definitions . . . . . 26
16.3 Disclaimers . . . . . 26
16.4 Trademarks . . . . . 27
**17 Contact information . . . . . 27**
**18 Contents . . . . . 28**

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