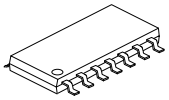
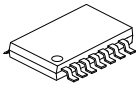
U74AHCT125

CMOS IC

QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS



SOP-14



TSSOP-14

■ DESCRIPTION

The U74AHCT125 is a quadruple bus buffer gates with 3-state output. When $\overline{OE}$ is high, the Y output is in a high-impedance state. When $\overline{OE}$ is low, the device passes noninverted data from the A input to the Y output.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

■ FEATURES

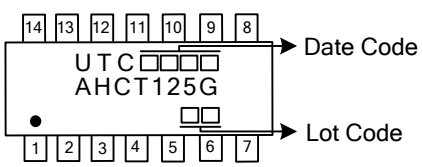
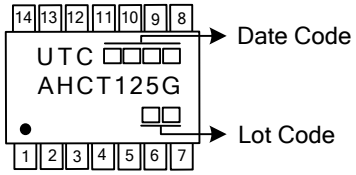
* TTL-Voltage Compatible
* Max t_{PD} of 3.8ns from A to Y at 5V, C_L=15pF
* Low Quiescent Current: I_{CC} = 2 μA (Max) at 5.5V
* ±8 mA Output Driver at 5V

■ ORDERING INFORMATION

Ordering Number	Package	Packing
U74AHCT125G-P14-R	TSSOP-14	Tape Reel
U74AHCT125G-S14-R	SOP-14	Tape Reel

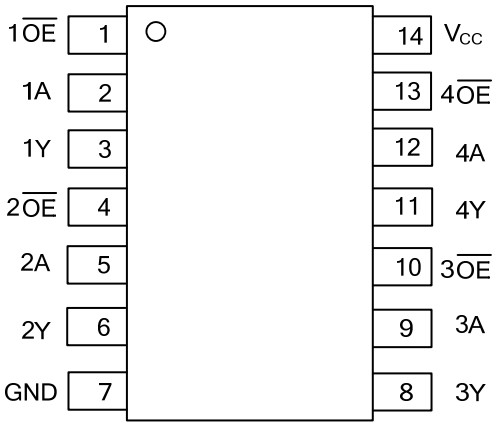
U74AHCT125G-S14-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) P14: TSSOP-14, S14: SOP-14 (3) G: Halogen Free and Lead Free

■ MARKING

SOP-14	TSSOP-14
	

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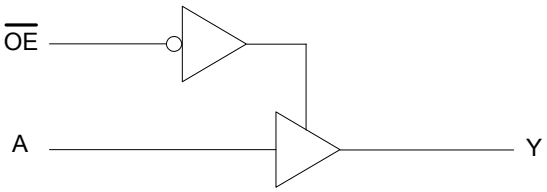
■ PIN CONFIGURATION



■ FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

■ LOGIC DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5~7	V
Input Voltage	V_{IN}	-0.5~7	V
Output Voltage	V_{OUT}	-0.5~V_{CC} +0.5	V
Input Clamp Current (V_{IN}<0)	I_{IK}	-20	mA
Output Clamp Current (V_{OUT}<0, or V_{OUT}>V_{CC})	I_{OK}	±20	mA
Output Current	I_{OUT}	±25	mA
V_{CC} or GND Current	I_{CC}	±50	mA
Storage Temperature	T_{STG}	-65 ~ +150	°C

Note: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING COMDITIONS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	4.5 ~ 5.5	V
High-Level Input Voltage	V_{IH}	2	V
Low-Level Input Voltage	V_{IL}	0.8	V
Input Voltage	V_{IN}	0 ~ 5.5	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
High-level Output Current	I_{OH}	-8	mA
Low-level Output Current	I_{OL}	8	mA
Input Transition Rise or Fall Rate	$\Delta t/\Delta v$	20	ns/V
Operating Temperature	T_A	-40 ~ 85	°C

■ ELECTRICAL CHARACTERISTICS (T_A =25°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Output Voltage	V_{OH}	I_{OH} = -50 μA, V_{CC} = 4.5V	4.4	4.5		V
		I_{OH} = -8 mA, V_{CC} = 4.5V	3.94			
Low-Level Output Voltage	V_{OL}	I_{OH} = 50 μA, V_{CC} = 4.5V			0.1	V
		I_{OH} = 8 mA, V_{CC} = 4.5V			0.36	
Input Leakage Current (A or $\overline{OE}$ input)	$I_{I(LEAK)}$	V_{IN} = 5.5V or GND, V_{CC} = 0 to 5.5V			±0.1	μA
High-impedance state Current	I_{OZ}	V_{OUT} = V_{CC} or GND, V_{CC} = 5.5V			±0.25	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND, I_{OUT} = 0, V_{CC} = 5.5V			2	μA
Additional quiescent supply current	ΔI_{CC}	One input at 3.4V,other inputs at V_{CC} or GND			1.35	mA
Input Capacitance	C_{IN}	V_{IN} = V_{CC} or GND, V_{CC}=5V		4	10	pF
Output Capacitance	C_{OUT}	V_{OUT} = V_{CC} or GND, V_{CC}=5V		15		pF

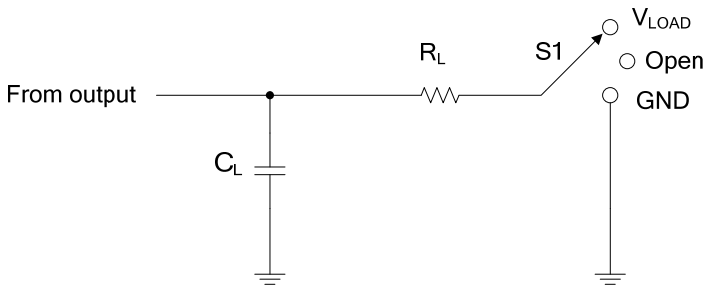
■ SWITCHING CHARACTERISTICS (V_{CC} = 5V ± 0.5V, T_A =25°C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay from Input A to Output Y, t_{PD}	t_{PLH}	C_L=15pF, R_L=1kΩ		3.8	5.5	ns
		C_L=50pF, R_L=1kΩ		5.3	7.5	
	t_{PHL}	C_L=15pF, R_L=1kΩ		3.8	5.5	ns
		C_L=50pF, R_L=1kΩ		5.3	7.5	
Propagation Delay from Input $\overline{OE}$ to Output Y, t_{EN}	t_{PZH}	C_L=15pF, R_L=1kΩ		3.6	5.1	ns
		C_L=50pF, R_L=1kΩ		5.1	7.1	
	t_{PZL}	C_L=15pF, R_L=1kΩ		3.6	5.1	ns
		C_L=50pF, R_L=1kΩ		5.1	7.1	
Propagation Delay from Input $\overline{OE}$ to Output Y, t_{DIS}	t_{PHZ}	C_L=15pF, R_L=1kΩ		4.6	6.8	ns
		C_L=50pF, R_L=1kΩ		6.1	8.8	
	t_{PLZ}	C_L=15pF, R_L=1kΩ		4.6	6.8	ns
		C_L=50pF, R_L=1kΩ		6.1	8.8	

■ OPERATING CHARACTERISTICS (T_A =25°C)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNIT
Power Dissipation Capacitance	C_{PD}	V_{CC} = 5V, f=1MHz, No load	14	pF

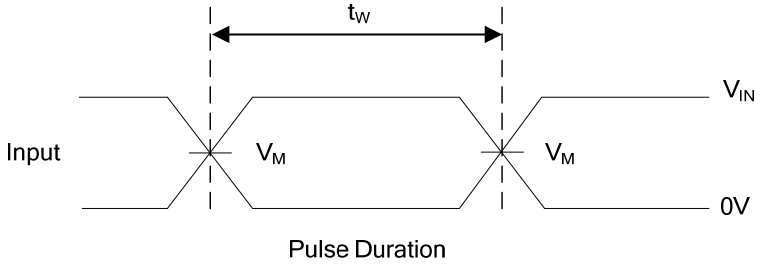
■ TEST CIRCUIT AND WAVEFORMS



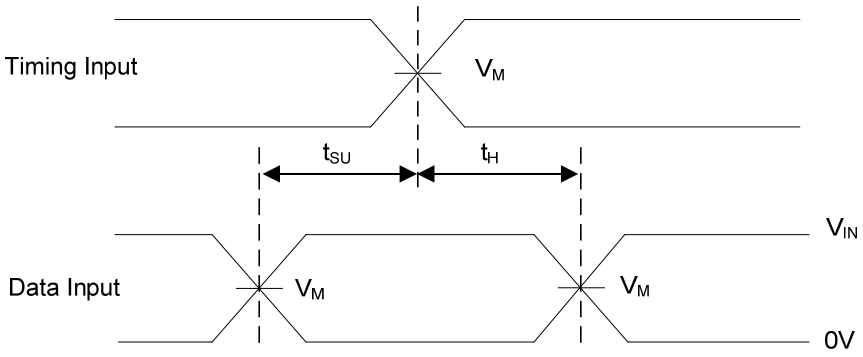
Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	Input		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_{IN}	t_R, t_F					
5V±0.5V	V_{CC}	≤3ns	$V_{CC}/2$	V_{CC}	15pF 50pF	1kΩ	0.5V

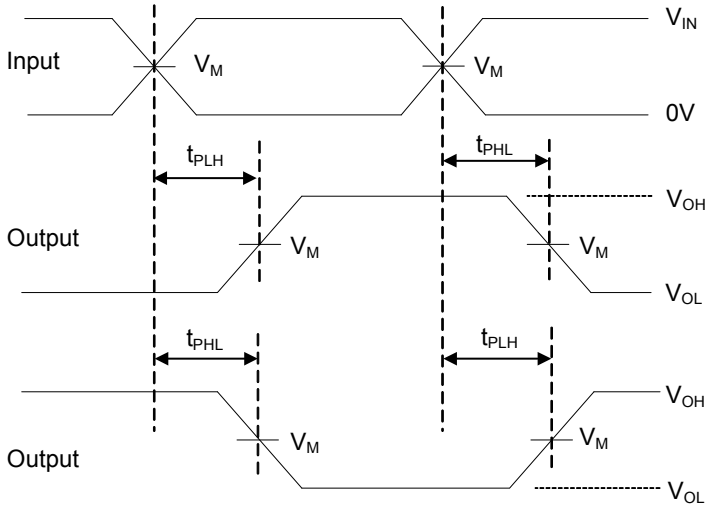


Pulse Duration

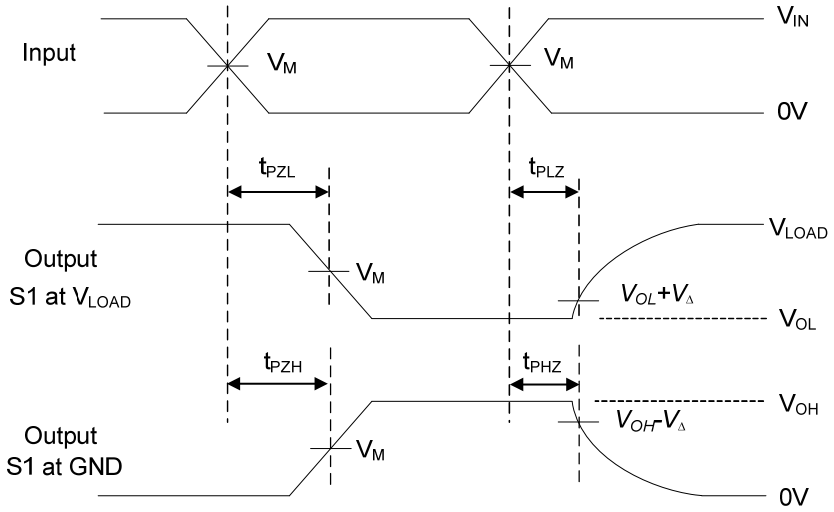


Setup and Hold Times

■ TEST CIRCUIT AND WAVEFORMS(Cont.)



Voltage Waveforms Propagation Delay Times



Voltage Waveforms Enble and Disable Times

Notes: 1. C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: P_{RR} ≤1MHz, Z_O = 50Ω.

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