CY2907

Single-PLL General Purpose EPROM Programmable Clock Generator

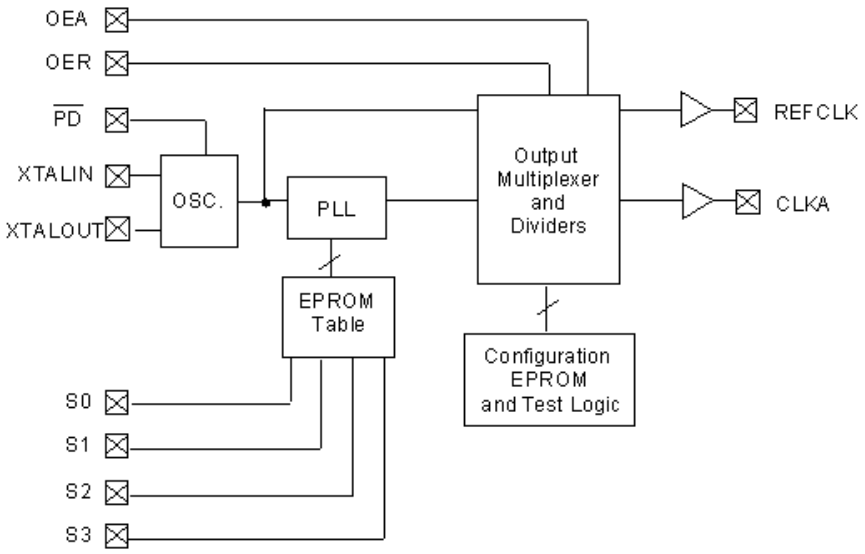
Features

- Single phase locked loop (PLL) architecture
- EPROM programmability
- Factory programmable (CY2907) or field programmable (CY2907F) device options
- Up to two configurable outputs
- Low skew, low jitter, high accuracy outputs
- Power management (power-down, OE)
- Frequency select option
- Configurable 5 V or 3.3 V Operation
- 8-pin or 14-pin SOIC packages

Benefits

- Generates a custom frequency from an external source
- Easy customization and fast turnaround
- Programming support available for all opportunities
- Provides clocking requirements from a single device
- Meets critical industry standard timing requirements
- Supports low power applications
- Up to 16 user selectable frequencies
- Supports industry standard design platforms
- Industry standard packaging saves on board space

Logic Block Diagram



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Pin Configurations

Figure 1. 14-pin SOIC and 8-pin SOIC (Top View)



Pin Description

Name	Pin Number		Description
	14-pin SOIC	8-pin SOIC	
S1	1	5	Frequency select (CLKA) (internal pull-up resistor to V_{DD})
S2	2	NA	Frequency select (CLKA) (internal pull-up resistor to V_{DD})
S3	3	NA	Frequency select (CLKA) (internal pull-up resistor to V_{DD})
V_{SS}	4	2	Ground
V_{SS}	5	NA	Ground
$\overline{PD}$	6	NA	Power-down (active LOW) (internal pull-up resistor to V_{DD})
XTALIN[1]	7	3	Reference crystal input
XTALOUT[1, 2]	8	4	Reference crystal feedback
OER	9	NA	REFCLK output enable (active HIGH) (internal pull-up resistor to V_{DD})
OEA	10	NA	CLKA output enable (active HIGH) (internal pull-up resistor to V_{DD})
CLKA	11	6	Clock output
V_{DD}	12	7	Voltage supply
REFCLK	13	8	Reference clock output (default, can be driven by PLL if desired)
S0	14	1	Frequency select (CLKA) (internal pull-up resistor to V_{DD})

Notes
1. For best accuracy, use a parallel resonant crystal, $C_{LOAD} \approx 17$ pF.
2. Float XTALOUT pin if XTALIN is driven by reference clock (as opposed to crystal).

Functional Description

The CY2907 is a general purpose clock generator designed for use in a wide variety of applications—from graphics to PC peripherals to disk drives. It generates selectable system clock frequencies from a single reference input (crystal or reference clock). The CY2907 is configured with an EPROM array, similar to the other devices in the Cypress EPROM Programmable Clock family, making it easy to customize for any application. Furthermore, the CY2907 is compatible with all industry standard 9107 and 9108 clock synthesizers.

Device Programming

Two versions of the CY2907 are available - Field Programmable and Factory Programmable. Field programmable devices must be programmed before being installed in an application. They are one-time-programmable (OTP). Customers can program small quantities in-house using the Cypress CY3670 programmer. Production quantities are available through Cypress's value-added distribution partners, or by using third party programmers from BP Microsystems, Hi-Lo Systems, and others.

For high volume orders, devices can be factory programmed by Cypress. All requests must be submitted to the local Cypress Field Application Engineer (FAE) or sales representative. After the request is processed, you receive a new part number, samples, and a data sheet with the programmed values. This part number is used for additional sample requests and production orders.

CyberClocks™ Software

CyberClocks is an easy-to-use software application that enables the user to configure any one of the EPROM Programmable Clocks offered by Cypress. You may specify the input frequency, PLL and output frequencies, and different functional options. Note the output frequency ranges in this data sheet when specifying them in CyberClocks to make sure that you stay within the limits. After a configuration is established, you can print the configuration and save programming files in ENT and JED formats.

CyberClocks runs on PCs running the Windows™ operating system, and is available for free download on the Cypress Semiconductor website at www.cypress.com.

Within the CyberClocks application, the CY2907 is found in the CyClocks™ section. Note that the standalone CyberClocks software should not be confused with the CyberClocks Online software, which is a web-based application that is used to configure other programmable clock devices.

Cypress CY3670 Programming Kit

Cypress's CY3670 is a portable programmer that connects to a PC serial port and enables users of CyClocks software to quickly and easily program any of the CY2291F, CY2292F, CY2071AF, and CY2907F devices. An adapter is also required and is ordered separately. The CY3097 is the adapter for the CY2907F8. For the CY2907F14, order adapter CY3098.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Supply voltage ..... –0.5 to +7.0 V

Input voltage ..... –0.5 V to V_{DD} + 0.5 V

Storage temperature (non-condensing).... –65 °C to +150 °C

Max soldering temperature (10 sec)..... +260 °C

Junction temperature..... +150 °C

Static discharge voltage..... > 2000 V (per MIL-STD-883, method 3015)

Operating Conditions[3]

Parameter	Description	Min	Max	Unit
V_{DD}	Supply voltage, 5 V operation	4.5	5.5	V
	Supply voltage, 3.3 V operation	3.0	3.6	V
T_A	Commercial operating temperature, Ambient	0	70	°C
C_L	Maximum capacitive load	–	15	pF
f_{REF}	External reference crystal	10.0	25.0	MHz
	External reference clock[4, 5]	1.0	30.0	MHz

Notes
3. Electrical parameters are guaranteed with these operating conditions.
4. Guaranteed by design, not 100% tested in production.
5. Load = max typical configuration, f_{REF} = 14.318 MHz. Specific configurations may vary. A close approximation of I_{DD} can be derived by the following formula: I_{DD} (mA) = V_{DD} × (6.25 + (0.055 × F_{REF}) + (0.0017 × C_{LOAD} × (F_{CLKA} + REFCLK))). C_{LOAD} is specified in pF and F is specified in MHz.

Electrical Characteristics at 5.0 V Commercial

V_{DD} = 4.5 V to 5.5 V, T_A = 0 °C to +70 °C

Parameter	Description	Test Conditions			Min	Max	Unit
V_{IH}	High-level input voltage	Except crystal inputs			2.0	–	V
V_{IL}	Low-level input voltage	Except crystal inputs			–	0.8	V
V_{OH}[6]	High-level output voltage	V_{DD} = V_{DD} Min.	I_{OH} = –30 mA	CLKA	2.4	–	V
V_{OL}[6]	Low-level output voltage	V_{DD} = V_{DD} Min.	I_{OL} = 10 mA	CLKA	–	0.4	V
I_{OH}[6]	Output high current	V_{OH} = 2.0 V			–	–35	mA
I_{OL}[6]	Output low current	V_{OL} = 0.8 V			22	–	mA
I_{IH}	Input high current	V_{IH} = V_{DD}			–2	2	µA
I_{IL}	Input low current	V_{IL} = 0V			–	20	µA
I_{DD}[7]	Power supply current	$\overline{PD}$ HIGH, CLKA = 50 MHz			–	42	mA
I_{DD}	Power supply current	$\overline{PD}$ LOW, Logic inputs LOW			–	100	µA
I_{DD}	Power supply current	$\overline{PD}$ LOW, Logic inputs HIGH			–	40	µA
R_{PU}[6]	Pull-up resistor	V_{IN} = V_{DD} – 1.0 V			–	700	kΩ

Electrical Characteristics at 3.3 V Commercial

V_{DD} = 3.0 V to 3.6 V, T_A = 0 °C to +70 °C

Parameter	Description	Test Conditions	Min	Max	Unit
V_{IH}	High-level input voltage	Except crystal inputs	0.7 × V_{DD}	–	V
V_{IL}	Low-level input voltage	Except crystal inputs	–	0.2 × V_{DD}	V
V_{OH}[8]	High-level output voltage	CLKA, I_{OH} = –5 mA	0.85 × V_{DD}	–	V
V_{OL}[8]	Low-level output voltage	CLKA, I_{OL} = 6 mA	–	0.1 × V_{DD}	V
I_{OH}[8]	Output high current	V_{OH} = 0.7 × V_{DD}	–	–10	mA
I_{OL}[8]	Output low current	V_{OL} = 0.2 × V_{DD}	15	–	mA
I_{IH}	Input high current	V_{IH} = V_{DD}	–2	2	µA
I_{IL}	Input low current	V_{IL} = 0 V	–	10	µA
I_{DD}[9]	Power supply current	$\overline{PD}$ HIGH, CLKA = 50 MHz	–	40	mA
I_{DD}	Power supply current	$\overline{PD}$ LOW, Logic inputs LOW	–	40	µA
I_{DD}	Power supply current	$\overline{PD}$ LOW, Logic inputs HIGH	–	12	µA
R_{PU}[8]	Pull-up resistor	V_{IN} = V_{DD} – 0.5 V	–	900	kΩ

Notes
6. Guaranteed by design, not 100% tested in production.
7. Load = max. typical configuration, f_{REF} = 14.318 MHz. Specific configurations may vary. A close approximation of I_{DD} can be derived by the following formula: I_{DD} (mA) = V_{DD} × (6.25 + (0.055 × F_{REF}) + (0.0017 × C_{LOAD} × (F_{CLKA} + REFCLK))). C_{LOAD} is specified in pF and F is specified in MHz.
8. Guaranteed by design, not 100% tested in production.
9. Load = max. typical configuration, f_{REF} = 14.318 MHz. Specific configurations may vary. A close approximation of I_{DD} can be derived by the following formula: I_{DD} (mA) = V_{DD} × (6.25 + (0.055 × F_{REF}) + (0.0017 × C_{LOAD} × (F_{CLKA} + REFCLK))). C_{LOAD} is specified in pF and F is specified in MHz.

:

Switching Characteristics at 5.0 V Commercial[10]

Parameter	Output[11]	Description	Test Conditions	Min	Max	Unit
t_R	CLKA	Output rise time 0.8 V to 2.0 V	15 pF load	–	1.40	ns
t_F	CLKA	Output fall time 2.0 V to 0.8 V	15 pF load	–	1.00	ns
t_R	CLKA	Output rise time 20% to 80%	15 pF load	–	3.5	ns
t_F	CLKA	Output fall time 80% to 20%	15 pF load	–	2.5	ns
t_D	CLKA	Duty cycle	15 pF load at 1.4 V	45.0	55.0	%
F_I	XTALIN	Input frequency	Crystal oscillator	10	25	MHz
F_I	XTALIN	Input frequency	External input clock[12]	1	30	MHz
F_O	CLKA	Output frequency	CY2907, 15 pF load	0.5	130.0	MHz
			CY2907F, 15 pF load	0.5	100.0	MHz
t_{JIS}	CLKA	Jitter (one sigma)	20 MHz to 130 MHz	–	150	ps
t_{JIS}	CLKA	Jitter (one sigma)	14 MHz to 20 MHz	–	200	ps
t_{JIS}	CLKA	Jitter (one sigma)	Less than 14 MHz	–	1	%
t_{JAB}	CLKA	Jitter (absolute)	20 MHz to 130 MHz	–250	+ 250	ps
t_{JAB}	CLKA	Jitter (absolute)	14 MHz to 20 MHz	–500	+ 500	ps
t_{JAB}	CLKA	Jitter (absolute)	Less than 14 MHz	–	3	%
t_{PU}		Power-up time		–	18	ms
t_{FT}	CLKA	Transition time	8 MHz to 66.6 MHz	–	13	ms

Switching Characteristics at 3.3 V Commercial[10]

Parameter	Output[11]	Description	Test Conditions	Min	Max	Unit
t_R	CLKA	Output rise time 20% to 80%	15 pF Load	–	3.5	ns
t_F	CLKA	Output fall time 80% to 20%	15 pF Load	–	2.5	ns
t_D	CLKA	Duty cycle	15 pF Load at 1.4 V	40.0	53.0	%
F_I	XTALIN	Input frequency	Crystal Oscillator	10	25	MHz
F_I	XTALIN	Input frequency	External Input Clock[12]	1	30	MHz
F_O	CLKA	Output frequency	CY2907, 15 pF Load	0.5	100.0	MHz
			CY2907F, 15 pF Load	0.5	80.0	MHz
t_{JIS}	CLKA	Jitter (one sigma)	25 MHz to 100 MHz	–	150	ps
t_{JIS}	CLKA	Jitter (one sigma)	14 MHz to 25 MHz	–	200	ps
t_{JIS}	CLKA	Jitter (one sigma)	Less than 14 MHz	–	1	%
t_{JAB}	CLKA	Jitter (absolute)	25 MHz to 120 MHz	–250	+250	ps
t_{JAB}	CLKA	Jitter (absolute)	14 MHz to 25 MHz	–500	+500	ps
t_{JAB}	CLKA	Jitter (absolute)	Less than 14 MHz	–	3	%
t_{PU}		Power-up time		–	18	ms
t_{FT}	CLKA	Transition time	8 MHz to 66.6 MHz	–	13	ms

Notes
10. Guaranteed by design, not 100% tested in production.
11. REFCLK output can also be configured to be driven by the PLL. In that case these characteristics are also valid.
12. Refer to the application note *Crystal Oscillator Topics* when using an external reference clock as an input frequency source.

Switching Waveforms

Figure 2. Frequency Select Change (Transition Time)

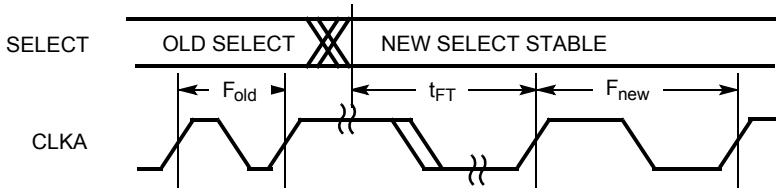


Figure 3. Duty Cycle Timing

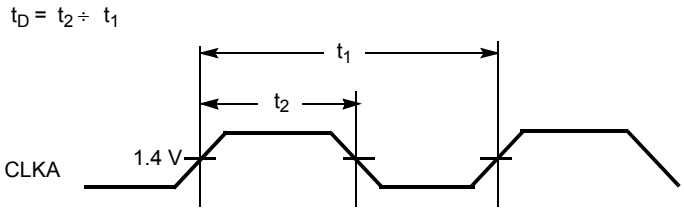
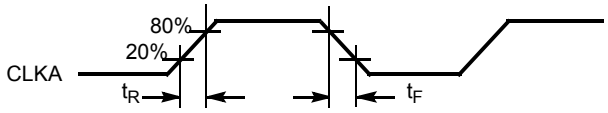
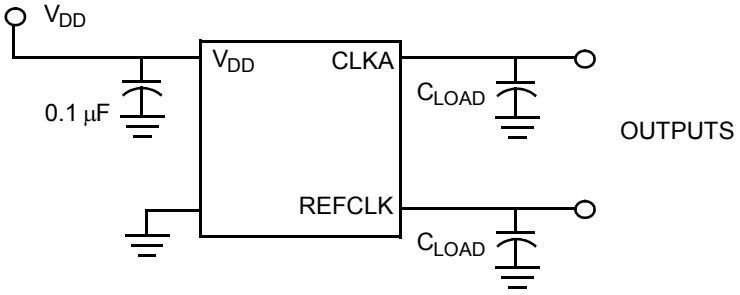


Figure 4. All Outputs Rise/Fall Time



Test Circuit

Figure 5. Test Circuit

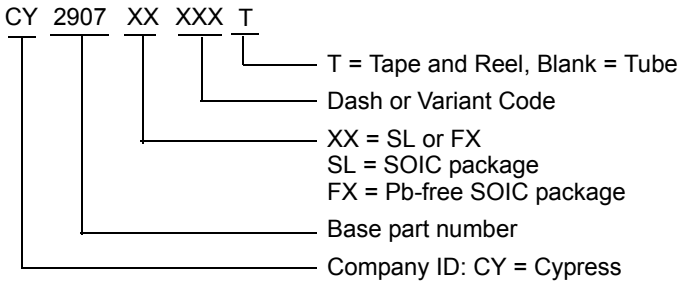


Note: All capacitors should be placed as close to each pin as possible.

Ordering Information

Ordering Code	Package Type	Operating Range
Pb-free		
CY2907FX8[13]	8-pin SOIC	5.0 V/3.3 V, Commercial, Field programmable
CY2907FX8T[13]	8-pin SOIC - Tape and Reel	5.0 V/3.3 V, Commercial, Field programmable
CY2907FX14[13]	14-pin SOIC	5.0 V/3.3 V, Commercial, Field programmable
CY2907FX14T[13]	14-pin SOIC - Tape and Reel	5.0 V/3.3 V, Commercial, Field programmable
Programmer		
CY3670	Cypress FTG programmer	
CY3097	Socket Adapter for CY3670 for programming CY2907FX8	
CY3098	Socket Adapter for CY3670 for programming CY2907FX14	

Ordering Code Definitions



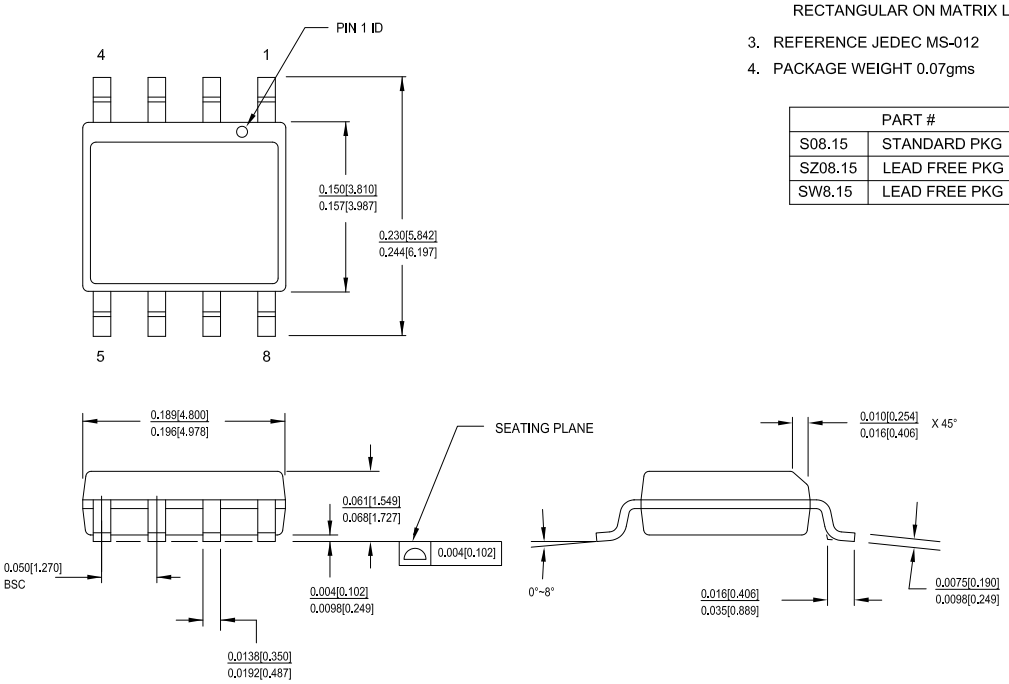
Package Characteristics

Package	θ_{JA} (C/W)	θ_{JC} (C/W)	Transistor Count
8-pin SOIC	170	35	5436
14-pin SOIC	140	31	5436

Note
13. Not for new designs. New designs should use a device other than the CY2907.

Package Diagrams

Figure 6. 8-pin (150-Mil) SOIC

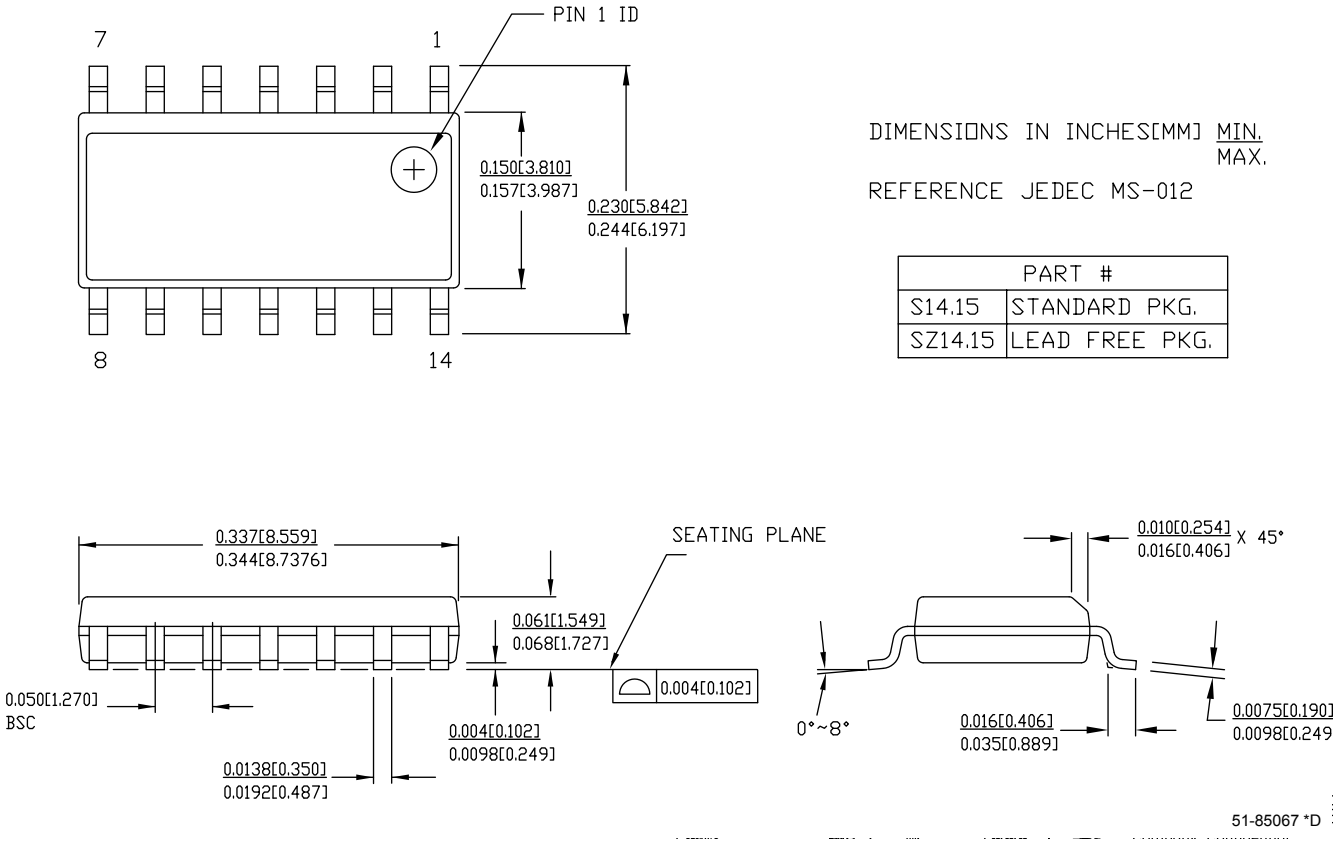


1. DIMENSIONS IN INCHES[MM] MIN.
   MAX.
2. PIN 1 ID IS OPTIONAL,
   ROUND ON SINGLE LEADFRAME
   RECTANGULAR ON MATRIX LEADFRAME
3. REFERENCE JEDEC MS-012
4. PACKAGE WEIGHT 0.07gms

PART #	
S08.15	STANDARD PKG
SZ08.15	LEAD FREE PKG
SW8.15	LEAD FREE PKG

51-85066 *F

Figure 7. 14-pin (150-Mil) SOIC



Acronyms

Acronym	Description
EPROM	erasable programmable read only memory
OE	output enable
PLL	phase-locked loop
SOIC	small-outline integrated circuit
TSSOP	thin-shrink small outline package

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kΩ	kilo ohm
MHz	megahertz
µA	microampere
mA	milliampere
ms	millisecond
mW	milliwatt
ns	nanosecond
%	percent
pF	picofarad
ppm	parts per million
ps	picosecond
V	volt

Document History Page

Document Title: CY2907 Single-PLL General Purpose EPROM Programmable Clock Generator Document Number: 38-07137				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	110246	SZV	12/18/01	Change from Spec number: 38-00505 to 38-07137
*A	1088524	KVM/ KKVTMP	See ECN	Added Pb-free for CY2907F8 and CY2907F14 field programmable devices Updated and added to text on page 2 Applied new template
*B	2715646	KVM/AESA	06/10/09	Removed obsolete part numbers from the ordering information table: CY2907SC-xxx, CY2907SC-xxxT, CY2907SI-xxx, CY2907SI-xxxT, CY2907F8T, CY2907F8I, CY2907F8IT, CY2907F14T, CY2907F14I and CY2907F14IT Added note: “Not for new designs” Removed industrial temperature references: page 1 features list, T_A spec, DC and AC electrical tables Removed Selector Guide table from page 1
*C	2948496	KVM	06/09/10	Updated package diagrams and ordering information table.
*D	3051170	BASH	10/07/2010	Updated Ordering Information and added Ordering Code Definitions. Added Acronyms and Units of Measure. Minor edits.
*E	3155189	BASH	01/27/2011	No technical updates.
*F	3402027	BASH	10/11/2011	Removed the following pruned parts: CY2907SL-262 and CY2907SL-262T from the Ordering Information table. Updated package diagrams.
*G	4047640	CINM	07/02/2013	Updated Package Diagrams: spec 51-85066 – Changed revision from *E to *F. Completing Sunset Review.

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