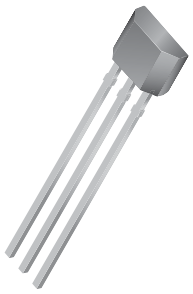
Programmable Linear Hall Effect Sensor ICs with Analog Output Available in a Miniature Thin Profile Surface Mount Package

Features and Benefits

- Customer programmable offset, sensitivity, sensitivity temperature coefficient, and polarity
- Programmability at end-of-line
- Ratiometric sensitivity, quiescent voltage output, and clamps for interfacing with application DAC
- Temperature-stable quiescent voltage output and sensitivity
- Precise recoverability after temperature cycling
- Output voltage clamps provide short circuit diagnostic capabilities
- Wide ambient temperature range: –40°C to 150°C
- Immune to mechanical stress
- Miniature package options

Packages: 3 pin SOT23W (suffix LH), and 3 pin SIP (suffix UA)





Not to scale

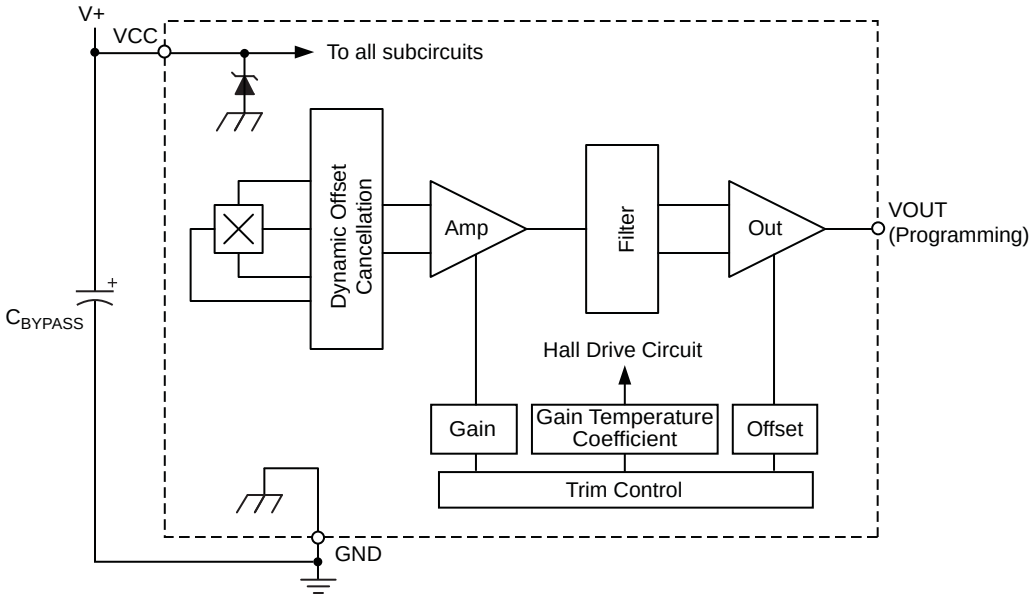
Description

New applications for linear output Hall effect sensing, such as displacement, angular position, and current measurement, require high accuracy in conjunction with small package size. The Allegro® A138x family of programmable linear Hall effect sensor ICs was designed specifically to achieve both goals. These temperature-stable devices are available in a miniature surface mount package (SOT23-W) and an ultramini through-hole single-in-line package. The accuracy of these devices is enhanced via programmability on the output pin for end-of-line optimization without the added complexity and cost of a fully programmable device.

These ratiometric Hall effect devices provide a voltage output that is proportional to the applied magnetic field. Both the quiescent voltage output and magnetic sensitivity are user-adjustable. The quiescent voltage output can be set around 50% of the supply voltage, and the sensitivity adjusted between 2 mV/G and 9 mV/G over the device family. Programming selections also exist for output polarity and temperature compensation. The features of this linear family make it ideal for high accuracy requirements of automotive and industrial applications, and performance is guaranteed over an extended temperature range, –40°C to 150°C.

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Functional Block Diagram



Description (continued)

Each BiCMOS monolithic circuit integrates a Hall element, temperature-compensating circuitry to reduce the intrinsic sensitivity drift of the Hall element, a small-signal high-gain amplifier, a clamped low-impedance output stage, and a proprietary dynamic offset cancellation technique.

The A138x devices are provided in a 3 pin ultramini single-in-line package (UA suffix), and a 3 pin surface mount SOT-23W package (LH suffix).

Selection Guide

Part Number	Packing[1]	Package	T_A (°C)	Internal Bandwidth (kHz)	Sensitivity Range (mV/G)
A1381ELHLT-T	Tape and reel, 3000 pieces/reel	Surface mount	–40 to 85	12	6.00 to 9.00
A1381EUA-T	Bulk bag, 500 pieces/bag	Through hole			
A1381LLHLT-T	Tape and reel, 3000 pieces/reel	Surface mount	–40 to 150		
A1381LUA-T	Bulk bag, 500 pieces/bag	Through hole			
~~A1382ELHLT-T~~[2]	Tape and reel, 3000 pieces/reel	Surface mount	–40 to 85	17	4.00 to 6.25
~~A1382ELHLX-T~~[2]	Tape and reel, 10000 pieces/reel	Surface mount			
~~A1382EUA-T~~[2]	Bulk bag, 500 pieces/bag	Through hole			
~~A1382LLHLT-T~~[2]	Tape and reel, 3000 pieces/reel	Surface mount	–40 to 150		
~~A1382LLHLX-T~~[2]	Tape and reel, 10000 pieces/reel	Surface mount			
~~A1382LUA-T~~[2]	Bulk bag, 500 pieces/bag	Through hole			
A1383ELHLT-T	Tape and reel, 3000 pieces/reel	Surface mount	–40 to 85	21	2.75 to 4.25
A1383EUA-T	Bulk bag, 500 pieces/bag	Through hole			
A1383LLHLT-T	Tape and reel, 3000 pieces/reel	Surface mount	–40 to 150		
A1383LUA-T	Bulk bag, 500 pieces/bag	Through hole			
A1384ELHLT-T	Tape and reel, 3000 pieces/reel	Surface mount	–40 to 85	27	2.00 to 3.00
A1384EUA-T	Bulk bag, 500 pieces/bag	Through hole			
A1384LLHLT-T	Tape and reel, 3000 pieces/reel	Surface mount	–40 to 150		
A1384LUA-T	Bulk bag, 500 pieces/bag	Through hole			

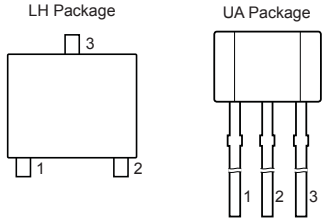
[1]Contact Allegro for additional packing options.

[2]Variants are in production but have been determined to be LAST TIME BUY. This classification indicates that the variant is obsolete and notice has been given. Sale of the variant is currently restricted to existing customer applications. The variant should not be purchased for new design applications because of obsolescence in the near future. Samples are no longer available. Status date change December 10, 2012. Deadline for receipt of LAST TIME BUY orders is May 31, 2013.

Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Forward Supply Voltage	V_{CC}		8	V
Reverse Supply Voltage	V_{RCC}		–0.1	V
Forward Output Voltage	V_{OUT}		28	V
Reverse Output Voltage	V_{ROUT}		–0.1	V
Output Source Current	$I_{OUT(SOURCE)}$	VOUT to GND	2	mA
Output Sink Current	$I_{OUT(SINK)}$	VCC to VOUT	10	mA
Operating Ambient Temperature	T_A	Range E	–40 to 85	°C
		Range L	–40 to 150	°C
Storage Temperature	T_{stg}		–65 to 165	°C
Maximum Junction Temperature	T_J(max)		165	°C

Pin-out Diagrams



Number		Name	Description
LH	UA		
1	1	VCC	Input power supply; use bypass capacitor to connect to ground
3	2	GND	Ground
2	3	VOUT	Output signal; also used for programming

OPERATING CHARACTERISTICS, valid over full operating temperature range, T_A; C_{BYPASS}= 0.1 µF, V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Units
ELECTRICAL CHARACTERISTICS							
Supply Voltage	V_{CC}			4.5	5.0	5.5	V
Supply Current	I_{CC}	No load on VOUT		–	6.9	8	mA
Power-On Time[1]	t_{PO}	A1381	T_A = 25 °C, C_{BYPASS} = open, C_L (of test probe) = 10 pF, Sens = 7.5 mV/G	–	32	–	µs
		A1382	T_A = 25 °C, C_{BYPASS} = open, C_L (of test probe) = 10 pF, Sens = 5.0 mV/G	–	27	–	µs
		A1383	T_A = 25 °C, C_{BYPASS} = open, C_L (of test probe) = 10 pF, Sens = 3.125 mV/G	–	23	–	µs
		A1384	T_A = 25 °C, C_{BYPASS} = open, C_L (of test probe) = 10 pF, Sens = 2.5 mV/G	–	19	–	µs
Delay to Clamp[1]	t_{CLP}	T_A = 25°C, C_L = 10 nF		–	30	–	µs
Supply Zener Clamp Voltage	V_Z	T_A = 25°C, I_{CC} = 11 mA		6	8.3	–	V
Internal Bandwidth	BW_i	A1381	Small signal –3 dB	–	12	–	kHz
		A1382		–	17	–	kHz
		A1383		–	21	–	kHz
		A1384		–	27	–	kHz
Chopping Frequency[2]	f_C	T_A = 25°C		–	170	–	kHz
OUTPUT CHARACTERISTICS							
Noise (peak to peak)	$V_{N(p-p)}$	A1381	T_A=25°C; C_L = 10 nF, Sens = 7.5 mV/G; no external filter	–	34	–	mV
		A1382	T_A=25°C; C_L = 10 nF, Sens = 5.0 mV/G; no external filter	–	27	–	mV
		A1383	T_A=25°C; C_L = 10 nF, Sens = 3.125 mV/G; no external filter	–	20	–	mV
		A1384	T_A=25°C; C_L = 10 nF, Sens = 2.5 mV/G; no external filter	–	18	–	mV
		A138x	T_A=25°C; Sens = 2.5 mV/G; external 2 kHz low pass filter with R = 1.69 kΩ, C = 47 nF	–	4.7	–	mV
DC Output Resistance	R_{OUT}			–	< 1	–	Ω
Output Load Resistance	R_L	VOUT to VCC		4.7	–	–	kΩ
		VOUT to GND		4.7	–	–	kΩ
Output Load Capacitance	C_L	VOUT to GND		–	–	10	nF
Phase Shift[3]	ΔΦ	No load on VOUT, magnetic input signal frequency = 1 kHz, with 1 $V_{(p-p)}$ output signal		–	3	–	deg.
Output Voltage Clamp[4]	$V_{CLP(HIGH)}$	T_A = 25°C, B = 600 G, Sens = 5.0 mV/G, R_L = 10 kΩ (VOUT to GND)		4.35	4.5	4.65	V
	$V_{CLP(LOW)}$	T_A = 25°C, B = –600 G, Sens = 5.0 mV/G, R_L = 10 kΩ (VCC to VOUT)		0.40	0.55	0.70	V
Output Slew Rate	SR	C_L = 10 nF		–	175	–	V/ms

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OPERATING CHARACTERISTICS (continued), valid over full operating temperature range, T_A; C_{BYPASS}= 0.1 µF, V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Units
PRE-PROGRAMMING TARGET[5]							
Pre-Programming Quiescent Voltage Output	$V_{OUT(Q)init}$	B = 0 G, T_A = 25°C		–	2.1	–	V
Pre-Programming Sensitivity	$Sens_{init}$	A1381	T_A = 25°C	–	4.2	–	mV/G
		A1382		–	2.9	–	mV/G
		A1383		–	2.1	–	mV/G
		A1384		–	1.4	–	mV/G
Pre-Programming Sensitivity Temperature Coefficient[6]	$TC_{Sensinit}$	T_A = 150°C		–	–0.05	–	%/°C
QUIESCENT VOLTAGE OUTPUT PROGRAMMING							
Guaranteed Quiescent Voltage Output Range[4,7]	$V_{OUT(Q)}$	B = 0 G, T_A = 25°C		2.3	–	2.6	V
Quiescent Voltage Output Programming Bits				–	6	–	bit
Average Quiescent Voltage Output Step Size[8,9]	$Step_{VOUT(Q)}$	T_A = 25°C		8	11.5	15	mV
Quiescent Voltage Output Programming Resolution[10]	$Err_{PGVOUT(Q)}$	T_A = 25°C		–	$Step_{VOUT(Q)}$ × ±0.5	–	mV
SENSITIVITY PROGRAMMING							
Guaranteed Sensitivity Range[4,11]	Sens	A1381	T_A = 25°C	6.00	–	9.00	mV/G
		A1382		4.00	–	6.25	mV/G
		A1383		2.75	–	4.25	mV/G
		A1384		2.00	–	3.00	mV/G
Sensitivity Programming Bits				–	6	–	bit
Average Sensitivity Step Size[8,9]	$Step_{SENS}$	A1381	T_A = 25°C	90	110	130	µV/G
		A1382		55	75	95	µV/G
		A1383		35	55	75	µV/G
		A1384		28	35	42	µV/G
Sensitivity Programming Resolution[10]	Err_{PGSENS}	T_A = 25°C		–	$Step_{SENS}$ × ±0.5	–	mV/G
SENSITIVITY TC PROGRAMMING							
Guaranteed Sensitivity Temperature Coefficient Range[6]	TC_{Sens}	T_A = 150°C		0.00	–	0.095	%/°C
Sensitivity Temperature Coefficient Programming Bits				–	3	–	bit
Average Sensitivity Temperature Coefficient Step Size[6]	$Step_{TCSENS}$	T_A = 150°C		–	0.03	–	%/°C
Sensitivity Temperature Coefficient Programming Resolution[6]	$Err_{PGTCSENS}$	T_A = 150°C		–	$Step_{TCSENS}$ x ±0.5	–	%/°C
POLARITY PROGRAMMING							
Polarity Programming Bit[12]	POL			–	1	–	bit
LOCK BIT PROGRAMMING							
Overall Programming Lock Bit	LOCK			–	1	–	bit

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OPERATING CHARACTERISTICS (continued), valid over full operating temperature range, T_A; C_{BYPASS}= 0.1 µF, V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
ERROR COMPONENTS						
Linearity Sensitivity Error	Lin_{ERR}		–	±1.5	–	%
Symmetry Sensitivity Error	Sym_{ERR}		–	±1.5	–	%
Ratiometry Quiescent Voltage Output Error[13]	$Rat_{ERRVOUT(Q)}$		–	±1.5	–	%
Ratiometry Sensitivity Error[13]	$Rat_{ERRSens}$		–	±1.5	–	%
Ratiometry Clamp Error[14]	Rat_{ERRCLP}	T_A = 25°C	–	±1.5	–	%
DRIFT CHARACTERISTICS						
Quiescent Voltage Output Drift Through Temperature Range	$\Delta V_{OUT(Q)}$	A1381, T_A = 150°C	–	–	±60	mV
		A1382, T_A = 150°C	–	–	±50	mV
		A1383, T_A = 150°C	–	–	±40	mV
		A1384, T_A = 150°C	–	–	±40	mV
Sensitivity Drift Through Temperature Range[15]	$\Delta Sens_{TC}$		–	±3	–	%
Sensitivity Drift Due to Package Hysteresis[1]	$\Delta Sens_{PKG}$	T_A = 25°C; after temperature cycling	–	±2	–	%

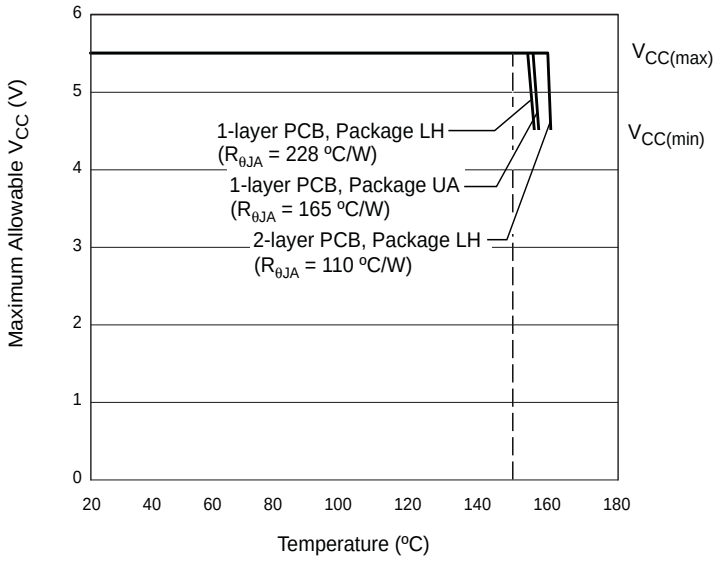
[1]See Characteristic Definitions section.
[2]f_C varies up to approximately ± 20% over the full operating ambient temperature range, T_A, and process.
[3]Unit of measure (phase degrees) in reference to the magnetic input signal.
[4]Sens, $V_{OUT(Q)}$, $V_{CLP(LOW)}$, and $V_{CLP(HIGH)}$ scale with V_{CC} due to ratiometry.
[5]Raw device characteristic values before any programming.
[6]Programmed at 150°C and calculated relative to 25°C.
[7]$V_{OUT(Q)}$(max) is the value available with all programming fuses blown (maximum programming code set). The $V_{OUT(Q)}$ range is the total range from $V_{OUT(Q)init}$ up to and including $V_{OUT(Q)}$(max). See Characteristic Definitions section.
[8]Step size is larger than required, in order to provide for manufacturing spread. See Characteristic Definitions section.
[9]Non-ideal behavior in the programming DAC can cause the step size at each significant bit rollover code to be greater than twice the maximum specified value of $Step_{VOUT(Q)}$, $Step_{SENS}$, or $Step_{TCSENS}$.
[10]Overall programming value accuracy. See Characteristic Definitions section.
[11]Sens(max) is the value available with all programming fuses blown (maximum programming code set). Sens range is the total range from $Sens_{init}$ up to and including Sens(max). See Characteristic Definitions section.
[12]Default polarity is for V_{OUT} voltage to increase with a positive (south polarity) field applied to the branded face of the device.
[13]Percent change from actual value at V_{CC} = 5 V, for a given temperature, over the guaranteed supply voltage operating range.
[14]Percent change from actual value at V_{CC} = 5 V, T_A = 25°C, over the guaranteed supply voltage operating range.
[15]Sensitivity drift from expected value at T_A after programming TC_{SENS}. See Characteristic Definitions section.

THERMAL CHARACTERISTICS may require derating at maximum conditions, see application information

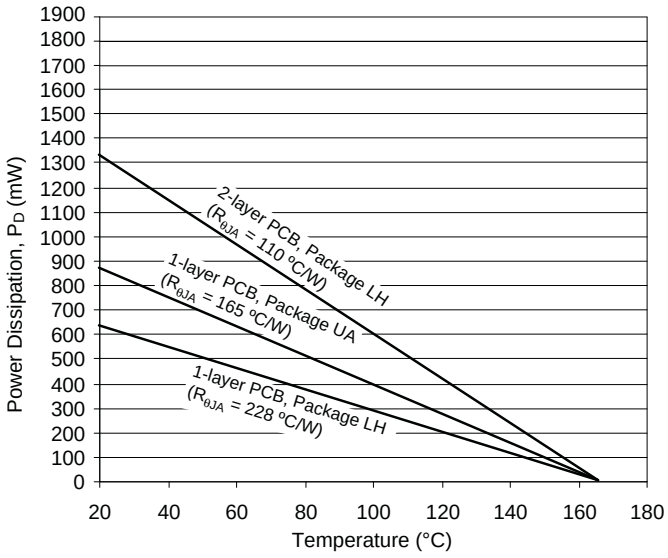
Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	Package LH, 1-layer PCB with copper limited to solder pads	228	ºC/W
		Package LH, 2-layer PCB with 0.463 in.^{2} of copper area each side connected by thermal vias	110	ºC/W
		Package UA, 1-layer PCB with copper limited to solder pads	165	ºC/W

*Additional thermal information available on Allegro website.

Power Derating Curve

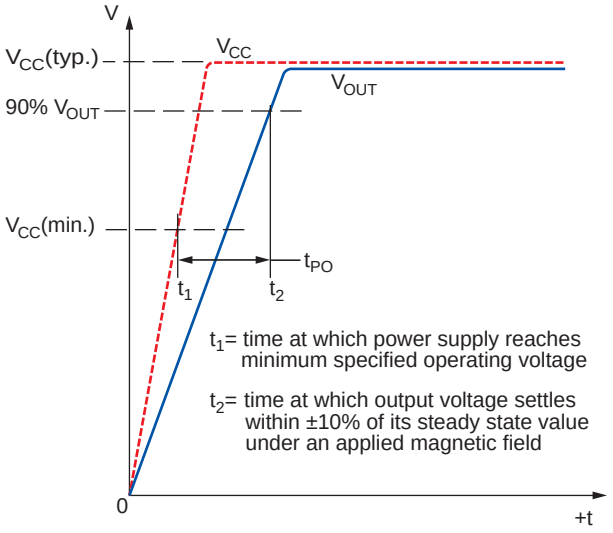


Power Dissipation versus Ambient Temperature

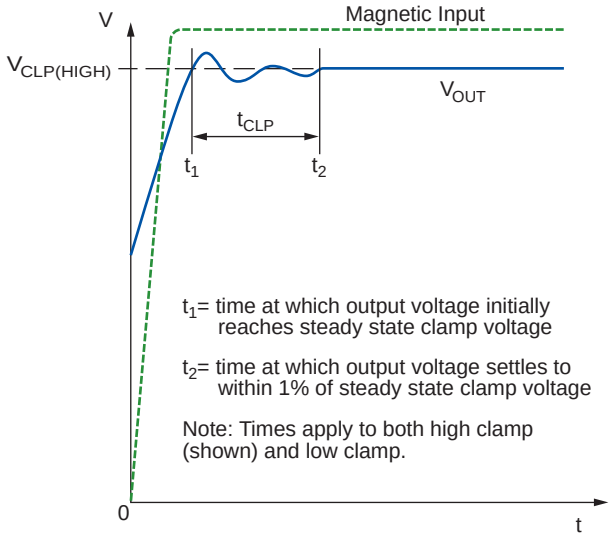


Characteristic Definitions

Power-On Time When the supply is ramped to its operating voltage, the device requires a finite time to power its internal components before responding to an input magnetic field. Power-On Time, t_{PO}, is defined as: the time it takes for the output voltage to settle within ±10% of its steady state value under an applied magnetic field, after the power supply has reached its minimum specified operating voltage, V_{CC}(min), as shown in the following chart.

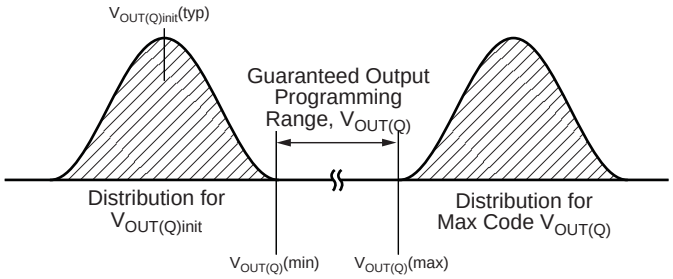


Delay to Clamp A large magnetic input step may cause the clamp to overshoot its steady state value. The Delay to Clamp, t_{CLP}, is defined as: the time it takes for the output voltage to settle within ±1% of its steady state value, after initially passing through its steady state voltage, as shown in the following chart.



Quiescent Voltage Output In the quiescent state (no significant magnetic field: B = 0 G), the output, $V_{OUT(Q)}$, has a constant ratio to the supply voltage, V_{CC}, throughout the entire operating ranges of V_{CC} and ambient temperature, T_A.

Guaranteed Quiescent Voltage Output Range The quiescent voltage output, $V_{OUT(Q)}$, can be programmed around its nominal value of 2.5 V, within the guaranteed quiescent voltage range limits: $V_{OUT(Q)}$(min) and $V_{OUT(Q)}$(max). The available guaranteed programming range for $V_{OUT(Q)}$ falls within the distributions of the initial, $V_{OUT(Q)init}$, and the maximum programming code for setting $V_{OUT(Q)}$, as shown in the following diagram.



Average Quiescent Voltage Output Step Size The average quiescent voltage output step size for a single device is determined using the following calculation:

$$Step_{VOUT(Q)} = \frac{V_{OUT(Q)maxcode} - V_{OUT(Q)init}}{2^n - 1} \cdot \qquad (1)$$

where:

n is the number of available programming bits in the trim range,

$2^n - 1$ is the value of the maximum programming code in the range, and

$V_{OUT(Q)maxcode}$ is the quiescent voltage output at code $2^n - 1$.

Quiescent Voltage Output Programming Resolution The programming resolution for any device is half of its programming step size. Therefore, the typical programming resolution will be:

$$Err_{PGVOUT(Q)}(typ) = 0.5 \times Step_{VOUT(Q)}(typ) \cdot \qquad (2)$$

Quiescent Voltage Output Drift Through Temperature Range Due to internal component tolerances and thermal considerations, the quiescent voltage output, $V_{OUT(Q)}$, may drift from its nominal value over the operating ambient temperature, T_A. For purposes of specification, the Quiescent Voltage Output Drift Through Temperature Range, $\Delta V_{OUT(Q)}$ (mV), is defined as:

$$\Delta V_{OUT(Q)} = V_{OUT(Q)(TA)} - V_{OUT(Q)(25°C)} \quad . \qquad (3)$$

Sensitivity The presence of a south polarity magnetic field, perpendicular to the branded surface of the package face, increases the output voltage from its quiescent value toward the supply voltage rail (assuming that the polarity bit, POL, is in its initial state of logic 0). The amount of the output voltage increase is proportional to the magnitude of the magnetic field applied. Conversely, the application of a north polarity field decreases the output voltage from its quiescent value. This proportionality is specified as the magnetic sensitivity, Sens (mV/G), of the device, and it is defined as:

$$Sens = \frac{V_{OUT(BPOS)} - V_{OUT(BNEG)}}{BPOS - BNEG} \quad , \qquad (4)$$

where BPOS and BNEG are two magnetic fields with opposite polarities.

Guaranteed Sensitivity Range The magnetic sensitivity, Sens, can be programmed around its nominal value, 2.5 to 7.5 mV/G depending on device type, within the sensitivity range limits: Sens(min) and Sens(max). Refer to the Guaranteed Quiescent Voltage Output Range section for a conceptual explanation of how value distributions and ranges are related.

Average Sensitivity Step Size Refer to the Average Quiescent Voltage Output Step Size section for a conceptual explanation.

Sensitivity Programming Resolution Refer to the Quiescent Voltage Output Programming Resolution section for a conceptual explanation.

Sensitivity Temperature Coefficient Device sensitivity changes as temperature changes, with respect to its programmed sensitivity temperature coefficient, TC_{SENS}. TC_{SENS} is programmed at 150°C, and calculated relative to the nominal sensitivity program ming temperature of 25°C. TC_{SENS} (%/°C) is defined as:

$$TC_{Sens} = \left(\frac{Sens_{T2} - Sens_{T1}}{Sens_{T1}} \times 100\%\right)\left(\frac{1}{T2 - T1}\right) \quad , \qquad (5)$$

where T1 is the nominal Sens programming temperature of 25°C, and T2 is the TC_{SENS} programming temperature of 150°C. The ideal value of Sens over the full ambient temperature range, $Sens_{IDEAL(TA)}$, is defined as:

$$Sens_{IDEAL(TA)} = Sens_{T1}\,[100\% + TC_{SENS}\,(T_A - T1)] \qquad (6)$$

Guaranteed Sensitivity Temperature Coefficient Range The magnetic sensitivity temperature coefficient can be programmed within its limits: TC_{Sens}(max) and TC_{Sens}(min). Refer to the Guaranteed Quiescent Voltage Output Range section for a conceptual explanation of how value distributions and ranges are related.

Average Sensitivity Temperature Coefficient Step Size Refer to the Average Quiescent Voltage Output Step Size section for a conceptual explanation.

Sensitivity Temperature Coefficient Programming Resolution Refer to the Quiescent Voltage Output Programming Resolution section for a conceptual explanation.

Sensitivity Drift Through Temperature Range Second order sensitivity temperature coefficient effects cause the magnetic sensitivity, Sens, to drift from its ideal value over the operating ambient temperature range, T_A. For purposes of specification, the sensitivity drift through temperature range, $\Delta Sens_{TC}$, is defined as:

$$\Delta Sens_{TC} = \frac{Sens_{TA} - Sens_{IDEAL(TA)}}{Sens_{IDEAL(TA)}} \times 100\% \quad . \qquad (7)$$

Sensitivity Drift Due to Package Hysteresis Package stress and relaxation can cause the device sensitivity at $T_A = 25°C$ to change during and after temperature cycling.

For purposes of specification, the sensitivity drift due to package hysteresis, $\Delta Sens_{PKG}$, is defined as:

$$\Delta Sens_{PKG} = \frac{Sens_{(25°C)2} - Sens_{(25°C)1}}{Sens_{(25°C)1}} \times 100\% \quad , \qquad (8)$$

where $Sens_{(25°C)1}$ is the programmed value of sensitivity at T_A = 25°C, and $Sens_{(25°C)2}$ is the value of sensitivity at T_A = 25°C, after temperature cycling T_A up to 150°C, down to –40°C, and back to up 25°C.

Linearity Sensitivity Error The 138x family is designed to provide a linear output in response to a ramping applied magnetic field. Consider two magnetic fields, B1 and B2. Ideally, the sensitivity of a device is the same for both fields, for a given supply voltage and temperature. Linearity error is present when there is a difference between the sensitivities measured at B1 and B2.

Linearity Error is calculated separately for the positive (Lin_{ERRPOS}) and negative (Lin_{ERRNEG}) applied magnetic fields. Linearity error (%) is measured and defined as:

$$Lin_{ERRPOS} = \left(1 - \frac{Sens_{BPOS2}}{Sens_{BPOS1}}\right) \times 100\% \quad ,$$

$$Lin_{ERRNEG} = \left(1 - \frac{Sens_{BNEG2}}{Sens_{BNEG1}}\right) \times 100\% \quad , \qquad (9)$$

where:

$$Sens_{Bx} = \frac{|V_{OUT(Bx)} - V_{OUT(Q)}|}{B_x} \quad , \qquad (10)$$

and B_{POSx} and B_{NEGx} are positive and negative magnetic fields, with respect to the quiescent voltage output such that $|B_{POS2}| > |B_{POS1}|$ and $|B_{NEG2}| > |B_{NEG1}|$. Then:

$$Lin_{ERR} = \max(|Lin_{ERRPOS}|, |Lin_{ERRNEG}|) \quad . \qquad (11)$$

Symmetry Sensitivity Error The magnetic sensitivity of an A138x device is constant for any two applied magnetic fields of equal magnitude and opposite polarities.

Symmetry error, Sym_{ERR} (%), is measured and defined as:

$$Sym_{ERR} = \left(1 - \frac{Sens_{BPOS}}{Sens_{BNEG}}\right) \times 100\% \quad , \qquad (12)$$

where $Sens_{Bx}$ is as defined in equation 10, and B_{POS} and B_{NEG} are positive and negative magnetic fields such that $|B_{POS}| = |B_{NEG}|$.

Ratiometry Error The A138x devices feature ratiometric output. This means that the quiescent voltage output, $V_{OUT(Q)}$, magnetic sensitivity, Sens, and clamp voltage, $V_{CLP(HIGH)}$ and $V_{CLP(LOW)}$, are proportional to the supply voltage, V_{CC}. In other words, when the supply voltage increases or decreases by a certain percentage, each characteristic also increases or decreases by the same percentage. Error is the difference between the measured change in the supply voltage relative to 5 V, and the measured change in each characteristic.

The ratiometric error in quiescent voltage output, $Rat_{ERRVOUT(Q)}$ (%), for a given supply voltage, V_{CC}, is defined as:

$$Rat_{ERRVOUT(Q)} = \left(1 - \frac{V_{OUT(Q)(VCC)} / V_{OUT(Q)(5V)}}{V_{CC} / 5\ V}\right) \times 100\% \quad . \qquad (13)$$

The ratiometric error in magnetic sensitivity, $Rat_{ERRSens}$ (%), for a given supply voltage, V_{CC}, is defined as:

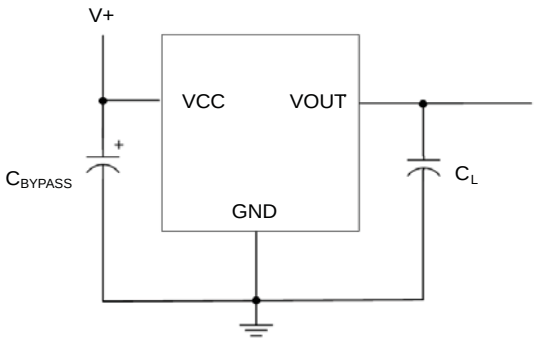
$$Rat_{ERRSens} = \left(1 - \frac{Sens_{(VCC)} / Sens_{(5V)}}{V_{CC} / 5\ V}\right) \times 100\% \quad . \qquad (14)$$

The ratiometric error in the clamp voltages, Rat_{ERRCLP} (%), for a given supply voltage, V_{CC}, is defined as:

$$Rat_{ERRCLP} = \left(1 - \frac{V_{CLP(VCC)} / V_{CLP(5V)}}{V_{CC} / 5\ V}\right) \times 100\% \quad . \qquad (15)$$

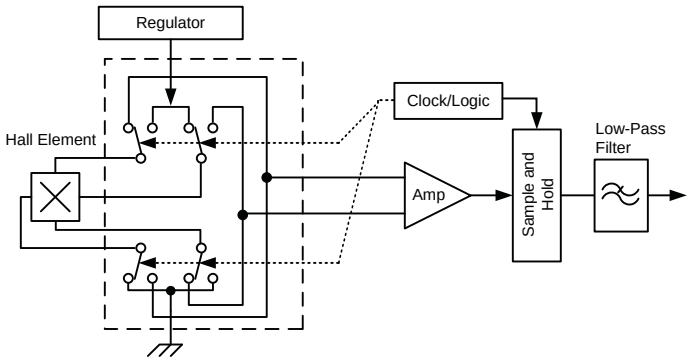
where V_{CLP} is either $V_{CLP(HIGH)}$ or $V_{CLP(LOW)}$.

Typical Application Drawing



Chopper Stabilization Technique

When using Hall-effect technology, a limiting factor for switchpoint accuracy is the small signal voltage developed across the Hall element. This voltage is disproportionally small relative to the offset that can be produced at the output of the Hall element. This makes it difficult to process the signal while maintaining an accurate, reliable output over the specified operating temperature and voltage ranges. Chopper stabilization is a unique approach used to minimize Hall offset on the chip. The patented Allegro technique, namely Dynamic Quadrature Offset Cancellation, removes key sources of the output drift induced by thermal and mechanical stresses. This offset reduction technique is based on a signal modulation-demodulation process. The undesired offset signal is separated from the magnetic field-induced signal in the frequency domain, through modulation. The subsequent demodulation acts as a modulation process for the offset, causing the magnetic field-induced signal to recover its original spectrum at base band, while the DC offset becomes a high-frequency signal. The magnetic-sourced signal then can pass through a low-pass filter, while the modulated DC offset is suppressed. The chopper stabilization technique uses a 170 kHz high frequency clock. For the demodulation process, a sample and hold technique is used, where the sampling is performed at twice the chopper frequency (340 kHz). This high-frequency operation allows a greater sampling rate, which results in higher accuracy and faster signal-processing capability. This approach desensitizes the chip to the effects of thermal and mechanical stresses, and produces devices that have extremely stable quiescent Hall output voltages and Precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process, which allows the use of low-offset, low-noise amplifiers in combination with high-density logic integration and sample-and-hold circuits.



Concept of Chopper Stabilization Technique

Programming Guidelines

Overview

Programming is accomplished by sending a series of input voltage pulses serially through the VOUT pin of the device. A unique combination of different voltage level pulses controls the internal programming logic of the device to select a desired programmable parameter and change its value. There are two programming pulses, referred to as a *high* voltage pulse, V_{PH}, consisting of a $V_{P(LOW)} - V_{P(HIGH)} - V_{P(LOW)}$ sequence and a *mid* voltage pulse, V_{PM}, consisting of a $V_{P(LOW)} - V_{P(MID)} - V_{P(LOW)}$ sequence.

The 138x features Try mode, Blow mode, and Lock mode:

- In Try mode, the value of a single programmable parameter may be set and measured. The parameter value is stored temporarily, and resets after cycling the supply voltage. Note that other parameters cannot be accessed simultaneously in this mode.
- In Blow mode, the value of a single programmable parameter may be permanently set by blowing solid-state fuses internal to the device. Additional parameters may be blown sequentially.
- In Lock mode, a device-level fuse is blown, blocking the further programming of all parameters.

The programming sequence is designed to help prevent the device from being programmed accidentally; for example, as a result of noise on the supply line.

Although any programmable variable power supply can be used to generate the pulse waveforms, Allegro highly recommends using the Allegro Sensor IC Evaluation Kit, available on the Allegro Web site On-line Store. The manual for that kit is available for download free of charge, and provides additional information on programming these devices.

Definition of Terms

Register. The section of the programming logic that controls the choice of programmable modes and parameters.

Bit Field. The internal fuses unique to each register, represented as a binary number. Incrementing the bit field of a particular register causes its programmable parameter to change, based on the internal programming logic.

Key. A series of V_{PM} voltage pulses used to select a register, with a value expressed as the decimal equivalent of the binary value. The LSB of a register is denoted as key 1, or bit 0.

Code. The number used to identify the combination of fuses activated in a bit field, expressed as the decimal equivalent of the binary value. The LSB of a bit field is denoted as code 1, or bit 0.

Addressing. Incrementing the bit field code of a selected register by serially applying a pulse train through the VOUT pin of the device. Each parameter can be measured during the addressing process, but the internal fuses must be blown before the programming code (and parameter value) becomes permanent.

Fuse Blowing. Applying a V_{PH} voltage pulse of sufficient duration at the $V_{P(HIGH)}$ level to permanently set an addressed bit by blowing a fuse internal to the device. Once a bit (fuse) has been blown, it cannot be reset.

Blow Pulse. A V_{PH} voltage pulse of sufficient duration at the $V_{P(HIGH)}$ level to blow the addressed fuse.

Cycling the Supply. Powering-down, and then powering-up the supply voltage. Cycling the supply is used to clear the programming settings in Try mode.

Programming Pulse Requirements, Protocol at T_A = 25°C

Characteristic	Symbol	Notes	Min.	Typ.	Max.	Units
Programming Voltage	$V_{P(LOW)}$	Measured at the VOUT pin.	-	-	5.5	V
	$V_{P(MID)}$		14	15	16	V
	$V_{P(HIGH)}$		26	27	28	V
Programming Current	I_P	Minimum supply current required to ensure proper fuse blowing. In addition, a minimum capacitance, C_{BLOW} = 0.1 µF, must be connected between the VOUT and GND pins during programming to provide the current necessary for fuse blowing.	300	-	-	mA
Pulse Width	$t_{OFF(HIGH)}$	Duration at $V_{P(LOW)}$ level following a $V_{P(HIGH)}$ level.	30	-	-	µs
	$t_{OFF(MID)}$	Duration at $V_{P(LOW)}$ level following a $V_{P(MID)}$ level.	5	-	-	µs
	$t_{ACTIVE(HIGH)}$	Duration of $V_{P(HIGH)}$ level for V_{PH} pulses during key/code selection.	30	-	-	µs
	$t_{ACTIVE(MID)}$	Duration of $V_{P(MID)}$ level for V_{PH} pulses during key/code selection.	15	-	-	µs
	t_{BLOW}	Duration at $V_{P(HIGH)}$ level for fuse blowing.	30	-	-	µs
Pulse Rise Time	t_{Pr}	Rise time required for transitions from $V_{P(LOW)}$ to either $V_{P(MID)}$ or $V_{P(HIGH)}$.	1	-	100	µs
Pulse Fall Time	t_{Pf}	Fall time required for transitions from $V_{P(HIGH)}$ to either $V_{P(MID)}$ to $V_{P(LOW)}$.	1	-	100	µs

Programming Procedures

Parameter Selection

Each programmable parameter can be accessed through a specific register. To select a register, a sequence of voltage pulses consisting of a V_{PH} pulse, a series of V_{PM} pulses, and a V_{PH} pulse (with no V_{CC} supply interruptions) must be applied serially to the VOUT pin. The number of V_{PM} pulses is called the *key*, and uniquely identifies each register. The pulse train used for selection of the first register, key 1, is shown in figure 1.

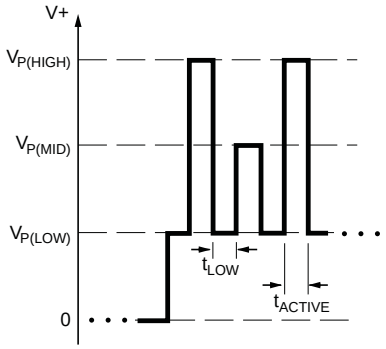


Figure 1. Parameter selection pulse train. This shows the sequence for selecting the register corresponding to key 1, indicated by a single V_{PM} pulse.

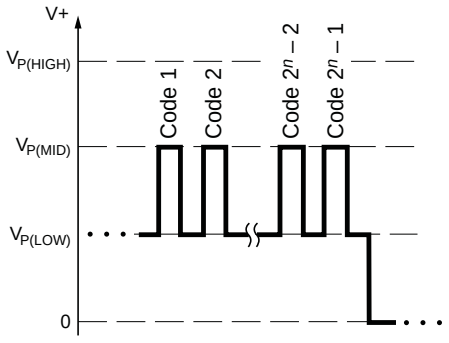


Figure 2. Bit field addressing pulse train. Addressing the bit field by incrementing the code causes the programmable parameter value to change. The number of bits available for a given programming code, *n*, varies among parameters; for example, the bit field for $V_{OUT(Q)}$ has 6 bits available, which allows 63 separate codes to be used.

The A138x has three registers that select among the five programmable parameters:

- Register 1:
  Quiescent voltage output, $V_{OUT(Q)}$
- Register 2:
  Sensitivity, Sens
- Register 3:
  Sensitivity temperature coefficient, TC_{Sens}
  Polarity, POL
  Overall device locking, LOCK

Bit Field Addressing

After a programmable parameter has been selected, a V_{PH} pulse transitions the programming logic into the bit field addressing state. Applying a series of V_{PM} pulses to the VOUT pin of the device, as shown in figure 2, increments the bit field of the selected parameter.

When addressing the bit field, the number of V_{PM} pulses is represented by a decimal number called a *code*. Addressing activates the corresponding fuse locations in the given bit field by incrementing the binary value of an internal DAC. The value of the bit field (and code) increments by one with the falling edge of each V_{PM} pulse, up to the maximum possible code (see the Programming Logic table). As the value of the bit field code increases, the value of the programmable parameter changes.

Measurements can be taken after each pulse to determine if the desired result for the programmable parameter has been reached. Cycling the supply voltage resets all the locations in the bit field that have unblown fuses to their initial states.

Fuse Blowing

After the required code is found for a given parameter, its value can be set permanently by blowing individual fuses in the appropriate register bit field. Blowing is accomplished by applying a V_{PH} pulse, called a *blow pulse*, of sufficient duration at the $V_{P(HIGH)}$ level to permanently set an addressed bit by blowing a fuse internal to the device. Due to power requirements, the fuse for each bit in the bit field must be blown individually. To accomplish this, the code representing the desired parameter value must be translated to a binary number. For example, as shown

in figure 3, decimal code 5 is equivalent to the binary number 101. Therefore bit 2 (code 4) must be addressed and blown, the device power supply cycled, and then bit 0 (code 1) addressed and blown. An appropriate sequence for blowing code 5 is shown in figure 4. The order of blowing bits, however, is not important. Blowing bit 0 first, and then bit 2 is acceptable.

Note: After blowing, the programming is not reversible, even after cycling the supply power. Although a register bit field fuse cannot be reset after it is blown, additional bits within the same register can be blown at any time until the device is locked. For example, if bit 1 (binary 10) has been blown, it is still possible to blow bit 0. The end result would be binary 11 (decimal code 3).

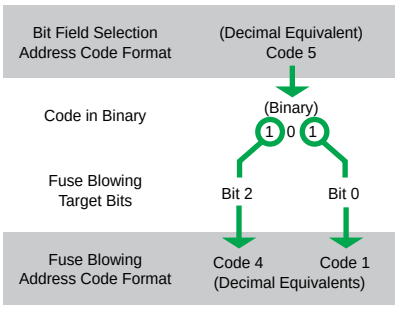


Figure 3. Example of code 5 broken into its binary components, which are code 4 and code 1.

Locking the Device

After the desired code for each parameter is programmed, the device can be locked to prevent further programming of any parameters.

Additional Guidelines

The additional guidelines in this section should be followed to ensure the proper behavior of these devices:

- A 0.1 µF blowing capacitor, C_{BLOW}, must be mounted between the VOUT pin and the GND pin during programming, to ensure enough current is available to blow fuses.
- The C_{BLOW} blowing capacitor must be replaced in the final application with a suitable C_L. (The maximum load capacitance is 10 nF for proper operation.)
- The power supply used for programming must be capable of delivering at least 26 V and 300 mA.
- Be careful to observe the t_{LOW} delay time before powering down the device after blowing each bit.
- The following programming order is recommended:

  1. POL
  2. TC_{SENS}
  3. Sens
  4. $V_{OUT(Q)}$
  5. LOCK (only after all other parameters have been programmed and validated, because this prevents any further programming of the device)

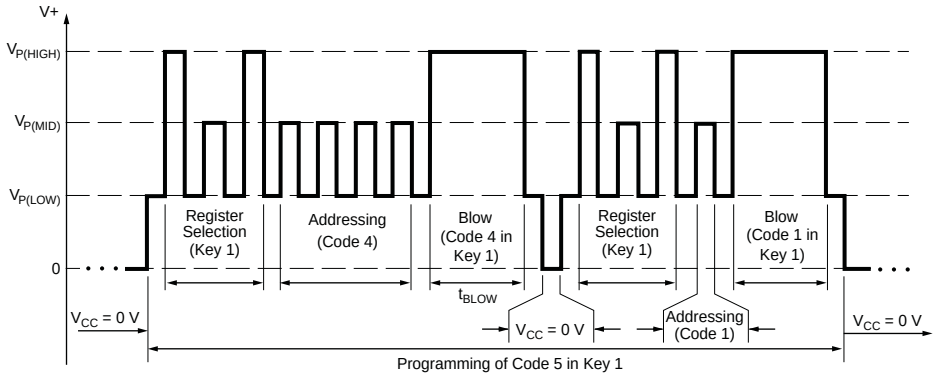


Figure 4. Example of programming pulses applied to the VOUT pin that result in permanent parameter settings. In this example, the register corresponding to key 1 is selected and code 5 is addressed and blown.

Programming Modes

Try Mode

Try mode allows a single programmable parameter to be tested without permanently setting its value. Multiple parameters cannot be tested simultaneously in this mode. After powering the VCC supply, select the desired parameter register and address its bit field. When addressing the bit field, each V_{PM} pulse increments the value of the parameter register, up to the maximum possible code (see Programming Logic table). The addressed parameter value remains stored in the device even after the programming drive voltage is removed from the VOUT pin, allowing the value to be measured. Note that for accurate time measurements, the blow capacitor, C_{BLOW}, should be removed during output voltage measurement.

It is not possible to decrement the value of the register without resetting the parameter bit field. To reset the bit field, and thus the value of the programmable parameter, cycle the supply (V_{CC}) voltage.

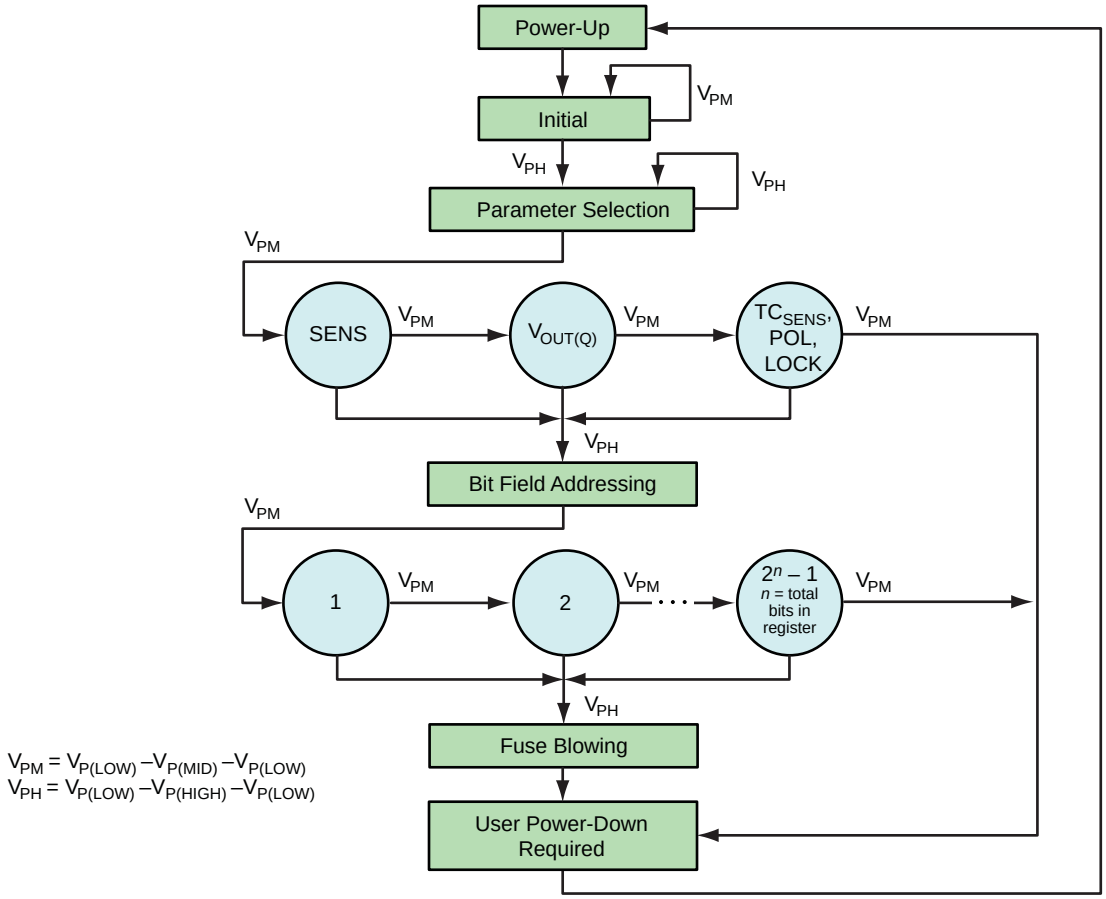
Blow Mode

After the required value of the programmable parameter is found using Try mode, its corresponding code should be blown to make its value permanent. To do this, select the required parameter register, and address and blow each required bit separately (as described in the Fuse Blowing section). The supply must be cycled between blowing each bit of a given code. After a bit is blown, cycling the supply will not reset its value.

Lock Mode

To lock the device, address the LOCK bit and apply a blow pulse with C_{BLOW} in place. After locking the device, no future programming of any parameter is possible.

Programming State Machine



Initial State After system power-up, the programming logic is reset to a known state. This is referred to as the Initial state. All the bit field locations that have intact fuses are set to logic 0. While in the Initial state, any V_{PM} pulses on the VOUT pin are ignored. To enter the Parameter Selection state, apply one V_{PH} pulse on the VOUT pin.

Parameter Selection State This state allows the selection of the parameter register containing the bit fields to be programmed. To select a parameter register, increment through the keys by applying V_{PM} pulses on the VOUT pin. Register keys select among the following programming parameters:

- 1 pulse - Sens
- 2 pulses - $V_{OUT(Q)}$
- 3 pulses - TC_{SENS}, POL, and LOCK

To enter the Bit Field Addressing state, apply one V_{PH} pulse on the VOUT pin.

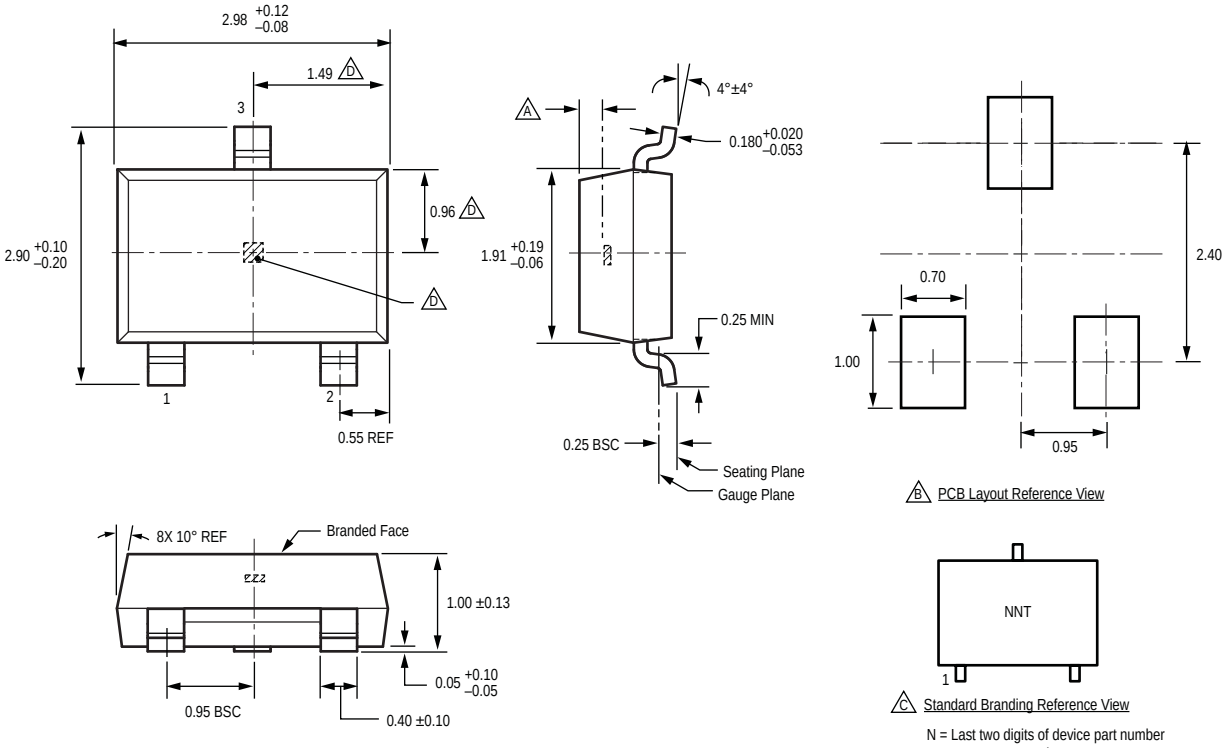
Bit Field Addressing State This state allows the selection of the individual bit fields to be programmed in the selected parameter register (see Programming Logic table). To leave this state, either cycle device power or blow the fuses for the selected code. Note that merely addressing the bit field does not permanently set the value of the selected programming parameter; fuses must be blown to do so.

Fuse Blowing State To blow an addressed bit field, apply a V_{PH} pulse on the VOUT pin. Power to the device should then be cycled before additional programming is attempted. Note: Each bit representing a decimal code must be blown individually (see the Fuse Blowing section).

Programming Logic Table

Programmable Parameter (Register Key)	Bit Field Address		Description
	Binary Format [MSB → LSB]	Decimal Equivalent Code	
Sens (1)	000000	0	Initial value ($Sens_{init}$)
	111111	63	Maximum value of sensitivity (Sens) in range
$V_{OUT(Q)}$ (2)	000000	0	Initial value ($V_{OUT(Q)init}$)
	111111	63	Maximum value of quiescent voltage output ($V_{OUT(Q)}$) in range; B = 0 G
TC_{SENS} , POL, LOCK (3)	000000	0	Initial value of sensitivity temperature coefficient range ($TC_{Sensinit}$)
	000111	7	Maximum value of sensitivity temperature coefficient (TC_{Sens}) in range
	001000	8	POL bit, switches polarity (causes V_{OUT} to increase with a negative [north polarity] field applied to the branded face of the device)
	010000	16	LOCK bit, enables permanent locking of all programming bit fields in the device

Package LH, 3 Pin; (SOT-23W)



N = Last two digits of device part number
T = Temperature code

For Reference Only; not for tooling use (reference dwg. 802840)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

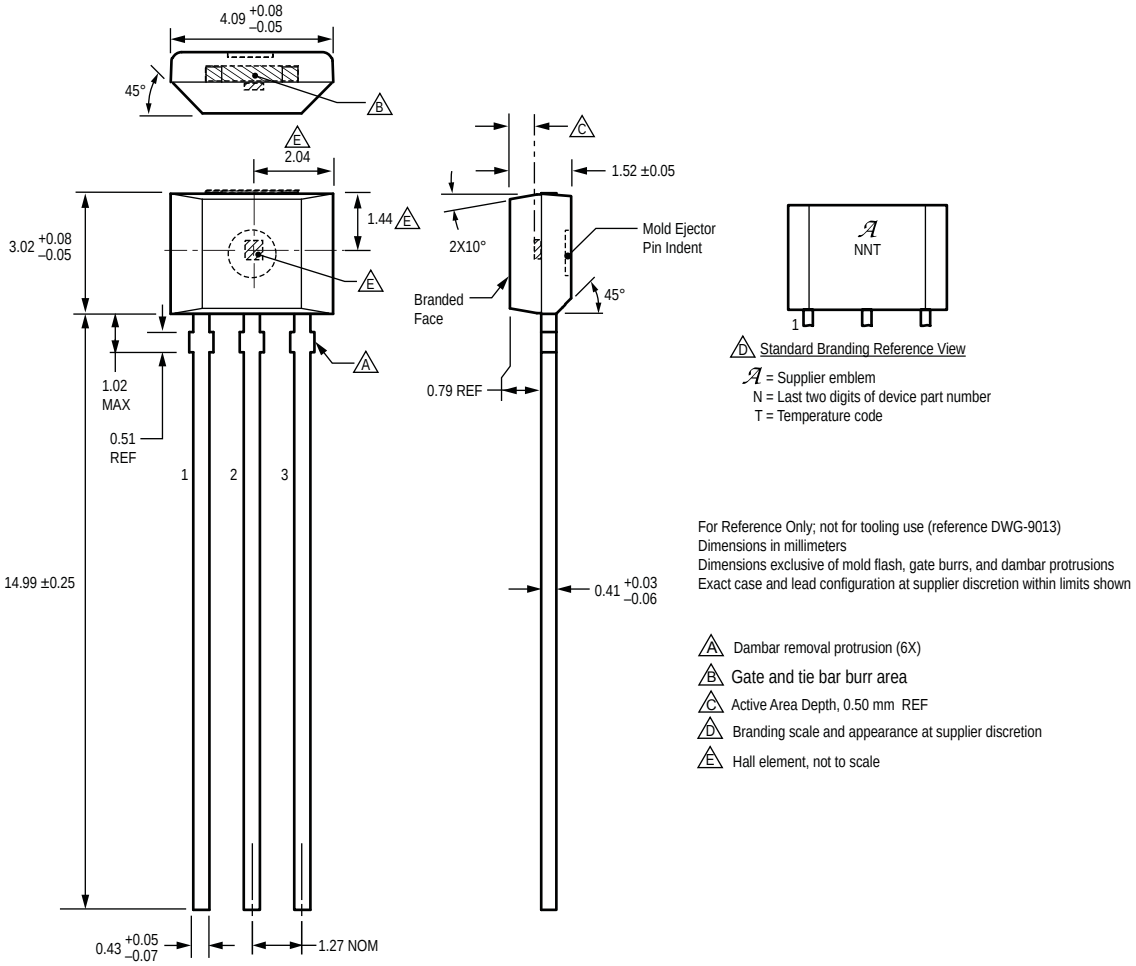
A Active Area Depth, 0.28 mm REF

B Reference land pattern layout
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

C Branding scale and appearance at supplier discretion

D Hall element, not to scale

Package UA, 3-Pin SIP



Please note that there are changes to the existing UA package drawing pending. Please contact the Allegro Marketing department for additional information.

Revision History

Revision	Revision Date	Description of Revision
Rev. 9	December 10, 2012	Update product availability

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