

## 1-Series, 2-Series, 3-Series, and 4-Series Li-Ion Battery Pack Manager

Check for Samples: [bq40z50](#)

### FEATURES

- Fully Integrated 1-Series, 2-Series, 3-Series, and 4-Series Li-Ion or Li-Polymer Cell Battery Pack Manager and Protection
- Next-Generation Patented Impedance Track™ Technology Accurately Measures Available Charge in Li-Ion and Li-Polymer Batteries
- High Side N-CH Protection FET Drive
- Integrated Cell Balancing While Charging or At Rest
- Full Array of Programmable Protection Features
  - Voltage
  - Current
  - Temperature
  - Charge Timeout
  - CHG/DSG FETs
  - AFE
- Sophisticated Charge Algorithms
  - JEITA
  - Enhanced Charging
  - Adaptive Charging
  - Cell Balancing
- Diagnostic Lifetime Data Monitor
- LED Display
- Supports Two-Wire SMBus v1.1 Interface
- SHA-1 Authentication
- Compact Package: 32-Lead QFN

### APPLICATIONS

- Notebook/Netbook PCs
- Medical and Test Equipment
- Portable Instrumentation

### DESCRIPTION

The bq40z50 device, incorporating patented Impedance Track™ technology, is a fully integrated, single-chip, pack-based solution that provides a rich array of features for gas gauging, protection, and authentication for 1-series, 2-series, 3-series, and 4-series cell Li-Ion and Li-Polymer battery packs.

Using its integrated high-performance analog peripherals, the bq40z50 device measures and maintains an accurate record of available capacity, voltage, current, temperature, and other critical parameters in Li-Ion or Li-Polymer batteries, and reports this information to the system host controller over an SMBus v1.1 compatible interface.

The bq40z50 provides software-based 1st- and 2nd-level safety protection against overvoltage, undervoltage, overcurrent, short-circuit current, overload, and overtemperature conditions, as well as other pack- and cell-related faults.

SHA-1 authentication, with secure memory for authentication keys, enables identification of genuine battery packs.

The compact 32-lead QFN package minimizes solution cost and size for smart batteries while providing maximum functionality and safety for battery gauging applications.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Impedance Track is a trademark of Texas Instruments.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### ORDERING INFORMATION

T <sub>A</sub>	PART NUMBER	PACKAGE	PACKAGE DESIGNATOR	PACKAGE MARKING	ORDERING INFORMATION <sup>(1)</sup>	
					TUBE <sup>(2)</sup>	TAPE AND REEL <sup>(3)</sup>
-40°C to 85°C	bq40z50	RSM-32	RSM	bq40z50	bq40z50RSMT	bq40z50RSMR

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of the document, or see the TI website at [www.ti.com](http://www.ti.com).
- (2) A single tube quantity is 50 units.
- (3) A single reel quantity is 2000 units.

### THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>		bq40z50		UNITS
		RSM (QFN)		
		32 Pins		
$\theta_{JA, \text{ High K}}$	Junction-to-ambient thermal resistance <sup>(2)</sup>	47.4		°C/W
$\theta_{JC(\text{top})}$	Junction-to-case(top) thermal resistance <sup>(3)</sup>	40.3		
$\theta_{JB}$	Junction-to-board thermal resistance <sup>(4)</sup>	14.7		
$\psi_{JT}$	Junction-to-top characterization parameter <sup>(5)</sup>	0.8		
$\psi_{JB}$	Junction-to-board characterization parameter <sup>(6)</sup>	14.4		
$\theta_{JC(\text{bottom})}$	Junction-to-case(bottom) thermal resistance <sup>(7)</sup>	3.8		

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](http://www.ti.com/lit/zip/SPR9953).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter,  $\psi_{JT}$ , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter,  $\psi_{JB}$ , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

## TYPICAL IMPLEMENTATION

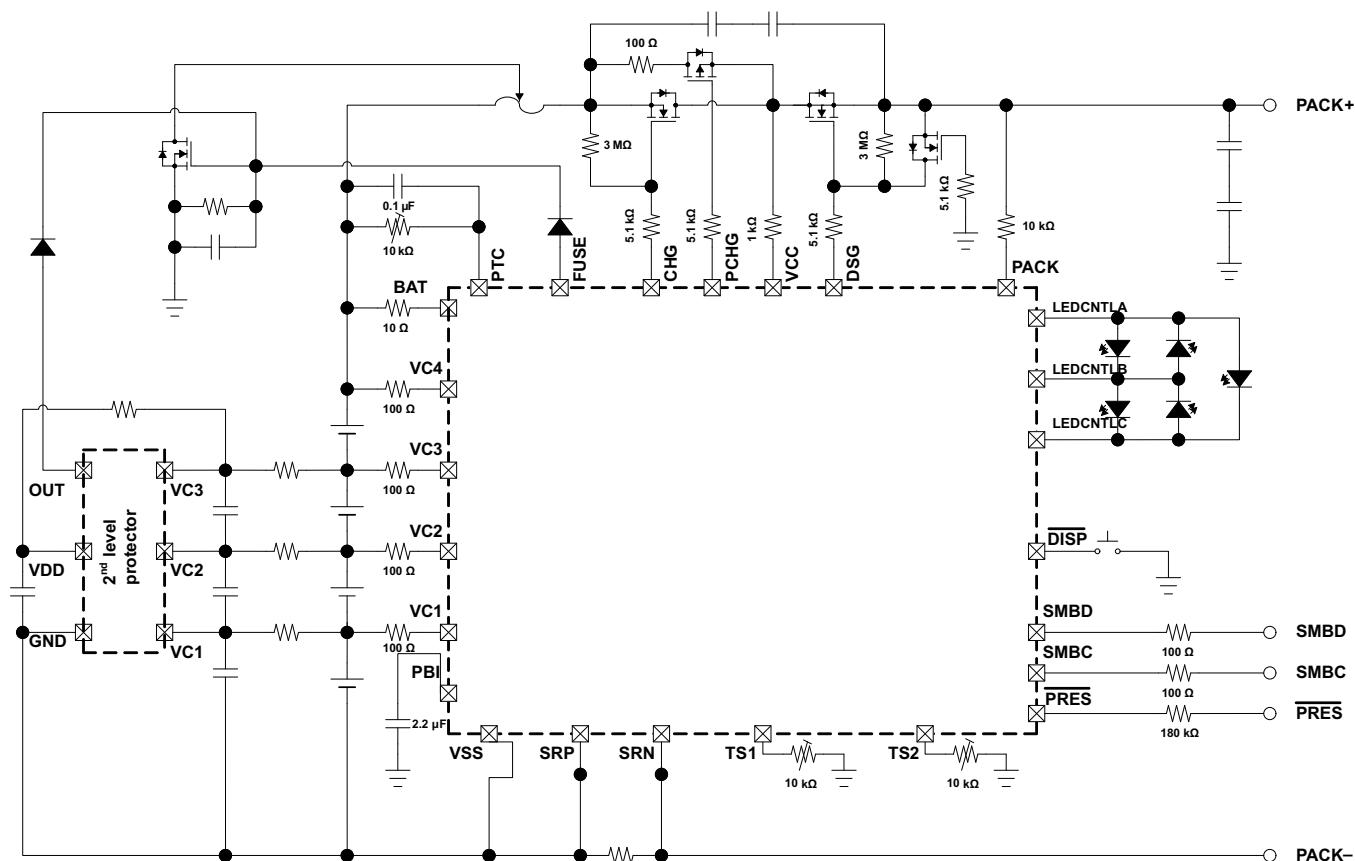


Figure 1. bq40z50 Implementation

## Pinout Diagram

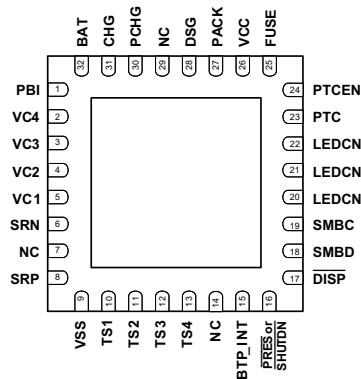


Figure 2. bq40z50 Pinout Diagram

### PIN FUNCTIONS

PIN NAME	PIN NUMBER	TYPE (1)	DESCRIPTION
PBI	1	P	Power supply backup input pin
VC4	2	IA	Sense voltage input terminal for most positive cell, and balance current input for most positive cell

(1) P = Power Connection, O = Digital Output, AI = Analog Input, I = Digital Input, I/OD = Digital Input/Output

**PIN FUNCTIONS (continued)**

PIN NAME	PIN NUMBER	TYPE <sup>(1)</sup>	DESCRIPTION
VC3	3	IA	Sense voltage input terminal for second most positive cell, balance current input for second most positive cell, and return balance current for most positive cell
VC2	4	IA	Sense voltage input terminal for third most positive cell, balance current input for third most positive cell, and return balance current for second most positive cell
VC1	5	IA	Sense voltage input terminal for least positive cell, balance current input for least positive cell, and return balance current for third most positive cell
SRN	6	I	Analog input pin connected to the internal coulomb counter peripheral for integrating a small voltage between SRP and SRN where SRP is the top of the sense resistor.
NC	7	—	Not internally connected. Connect to VSS.
SRP	8	I	Analog input pin connected to the internal coulomb counter peripheral for integrating a small voltage between SRP and SRN where SRP is the top of the sense resistor.
VSS	9	P	Device ground
TS1	10	IA	Temperature sensor 1 thermistor input pin
TS2	11	IA	Temperature sensor 2 thermistor input pin
TS3	12	IA	Temperature sensor 3 thermistor input pin
TS4	13	IA	Temperature sensor 4 thermistor input pin
NC	14	—	Not internally connected.
BTP_INT	15	O	Battery Trip Point (BTP) interrupt output
$\overline{\text{PRES}}$ or $\overline{\text{SHUTDN}}$	16	I	Host system present input for removable battery pack or emergency system shutdown input for embedded pack
$\overline{\text{DISP}}$	17	—	Display control for LEDs
SMBD	18	I/OD	SMBus data pin
SMBC	19	I/OD	SMBus clock pin
LEDCNTLA	20	—	LED display segment that drives the external LEDs depending on the firmware configuration
LEDCNTLB	21	—	LED display segment that drives the external LEDs depending on the firmware configuration
LEDCNTLC	22	—	LED display segment that drives the external LEDs depending on the firmware configuration
PTC	23	IA	Safety PTC thermistor input pin. To disable, connect both PTC and PTCEN to VSS.
PTCEN	24	IA	Safety PTC thermistor enable input pin. Connect to BAT. To disable, connect both PTC and PTCEN to VSS.
FUSE	25	O	Fuse drive output pin
VCC	26	P	Secondary power supply input.
PACK	27	IA	Pack sense input pin
DSG	28	O	NMOS Discharge FET drive output pin
NC	29	—	Not internally connected.
PCHG	30	O	PMOS Precharge FET drive output pin
CHG	31	O	NMOS Charge FET drive output pin
BAT	32	P	Primary power supply input pin

PIN EQUIVALENT DIAGRAMS

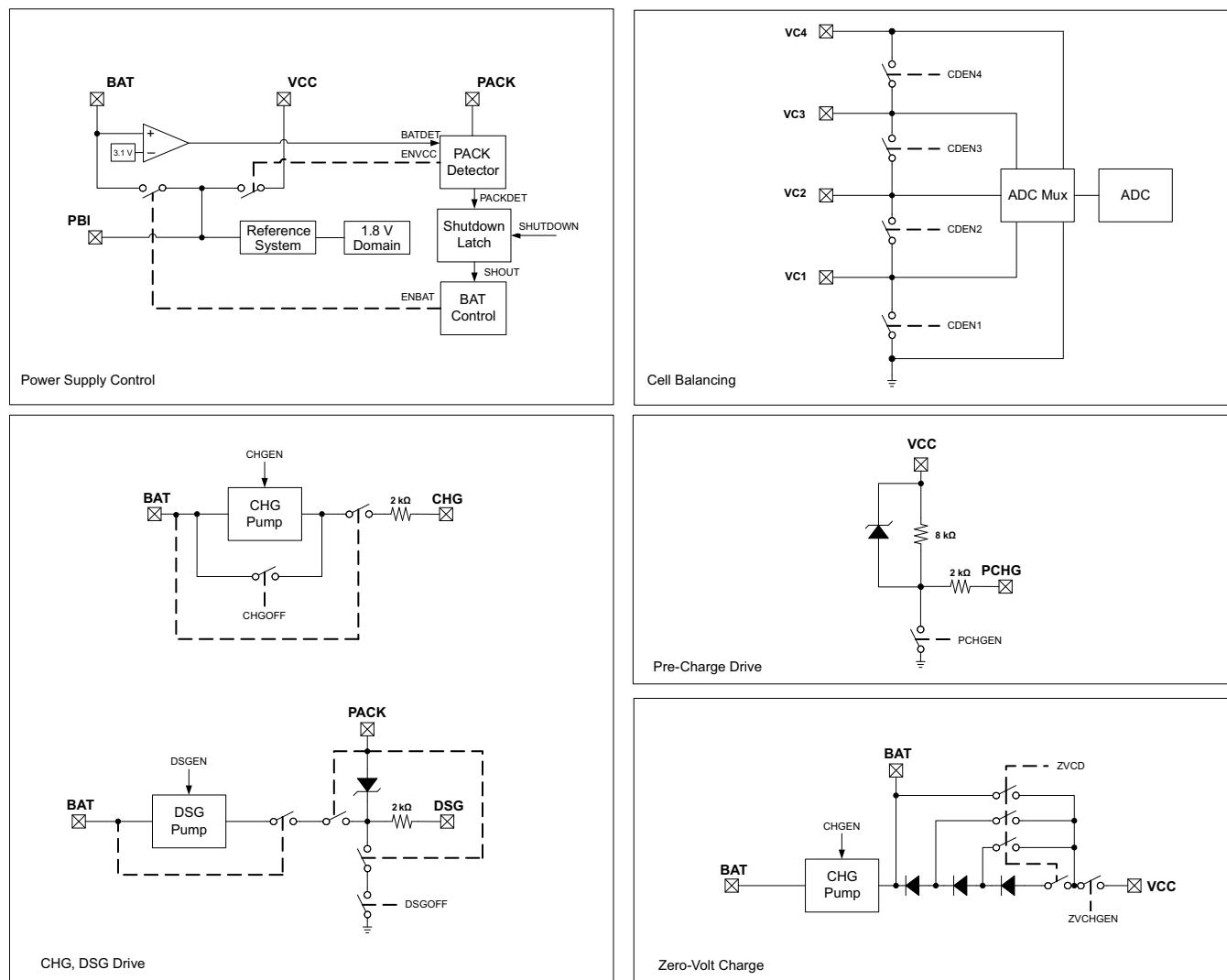


Figure 3. Pin Equivalent Diagram 1

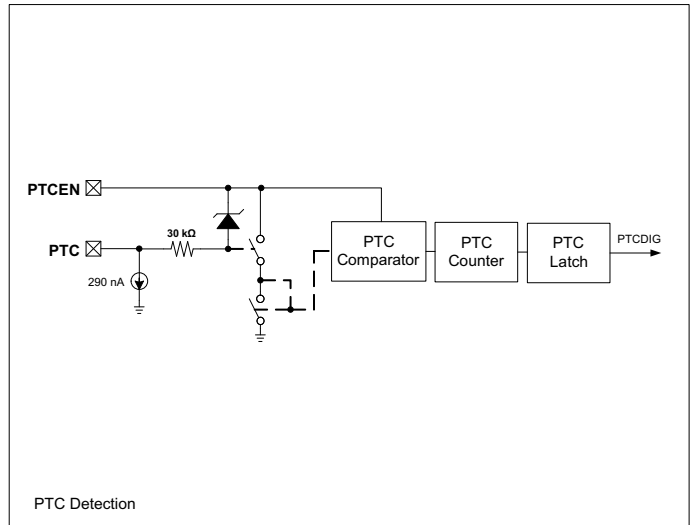
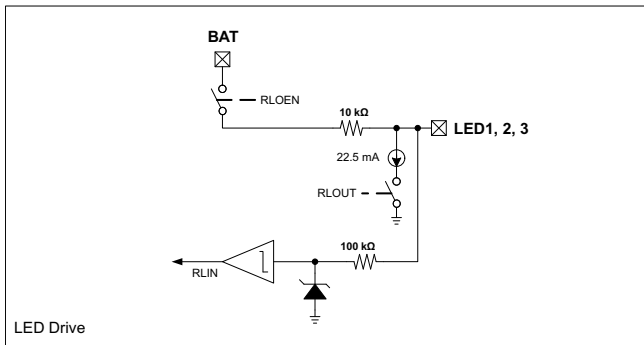
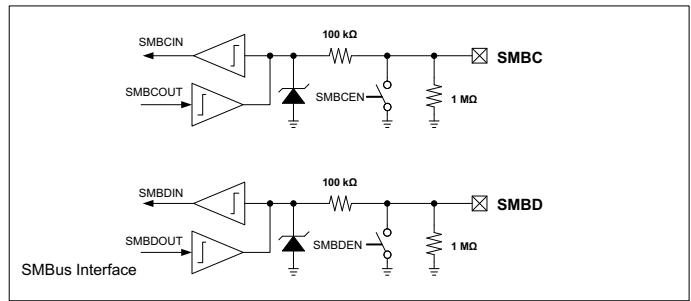
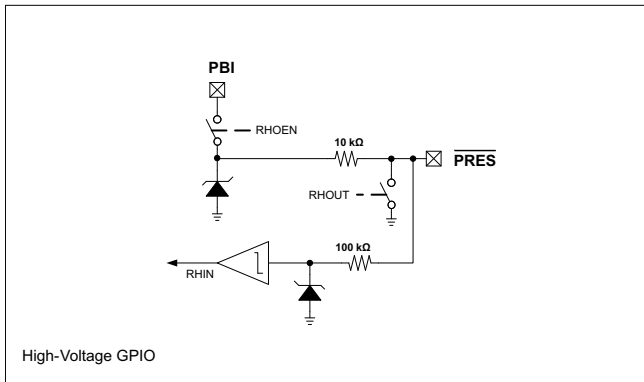
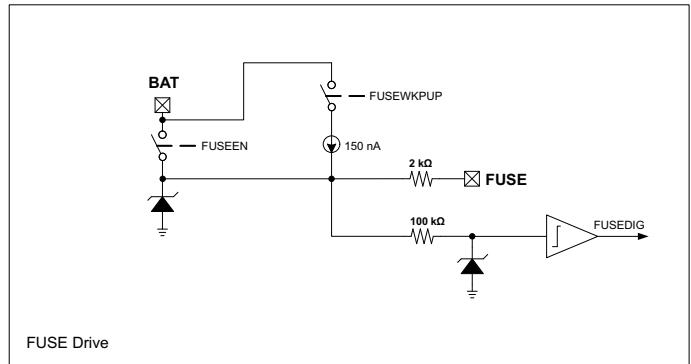
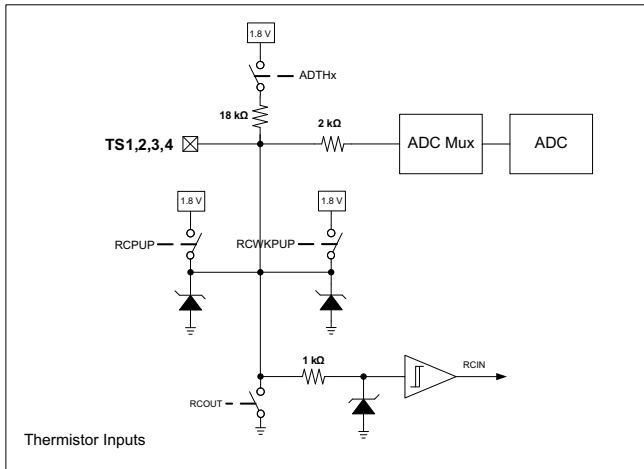


Figure 4. Pin Equivalent Diagram 2

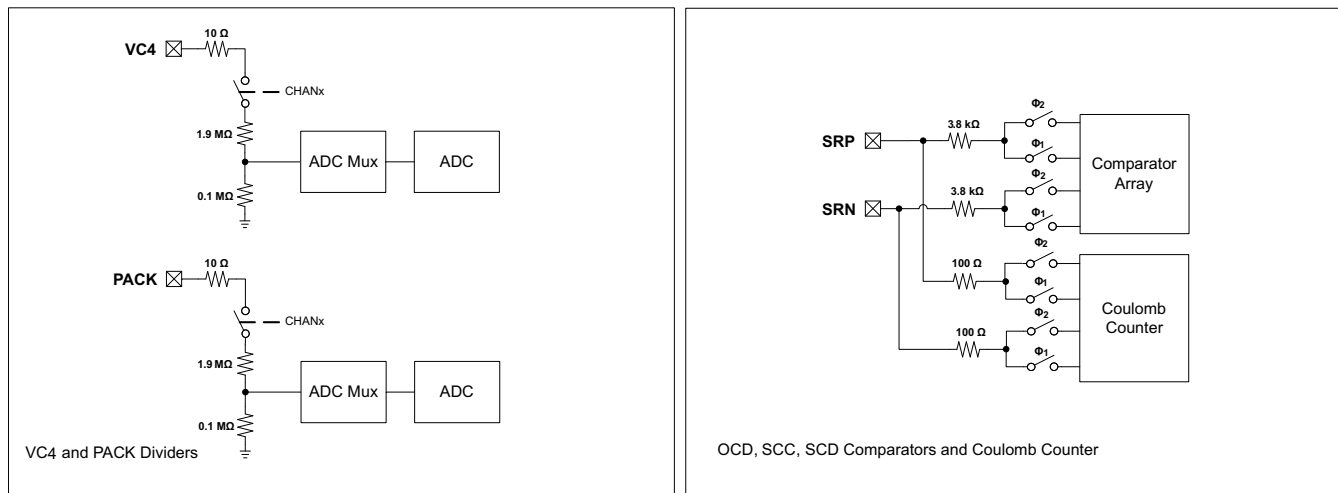


Figure 5. Pin Equivalent Diagram 3

**ABSOLUTE MAXIMUM RATINGS**

Over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

DESCRIPTION	PINS	VALUE
Supply voltage range, V <sub>CC</sub>	BAT, VCC, PBI	-0.3 to 30 V
Input voltage range, V <sub>IN</sub>	PACK, SMBC, SMBD, $\overline{\text{PRES}}$ or $\overline{\text{SHUTDOWN}}$ , BTP_INT, DISP	-0.3 to 30 V
	TS1, TS2, TS3, TS4	-0.3 to V <sub>REG</sub> + 0.3 V
	PTC, PTCEN, LEDCNTLA, LEDCNTLB, LEDCNTLC	-0.3 to V <sub>BAT</sub> + 0.3 V
	SRP, SRN	-0.3 to 0.3 V
	VC4	VC3 - 0.3 to VC3 + 8.5 V, or VSS + 30 V
	VC3	VC2 - 0.3 to VC2 + 8.5 V, or VSS + 30 V
	VC2	VC1 - 0.3 to VC1 + 8.5 V, or VSS + 30 V
Output voltage range, V <sub>O</sub>	CHG, DSG	-0.3 to 32 V
	PCHG, FUSE	-0.3 to 30 V
Maximum VSS current, I <sub>SS</sub>		50 mA
ESD Rating	HBM	2 kV
	CDM	500 V
	MM	200 V
Functional Temperature, T <sub>FUNC</sub>		-40 to 110°C
Storage temperature range, T <sub>STG</sub>		-65 to 150°C
Lead temperature (soldering, 10 s), T <sub>SOLDER</sub>		300°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**RECOMMENDED OPERATING CONDITIONS**

Typical values stated where T<sub>A</sub> = 25°C and VCC = 14.4 V, Min/Max values stated where T<sub>A</sub> = -40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

			MIN	TYP	MAX	UNIT
V <sub>CC</sub>	Supply voltage	BAT, VCC, PBI	2.2		26	V
V <sub>SHUTDOWN-</sub>	Shutdown voltage	V <sub>PACK</sub> < V <sub>SHUTDOWN-</sub>	1.8	2.0	2.2	V

## RECOMMENDED OPERATING CONDITIONS (continued)

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

			MIN	TYP	MAX	UNIT
$V_{\text{SHUTDOWN+}}$	Start-up voltage	$V_{\text{PACK}} > V_{\text{SHUTDOWN-}} + V_{\text{HYS}}$	2.05	2.25	2.45	V
$V_{\text{HYS}}$	Shutdown voltage hysteresis	$V_{\text{SHUTDOWN+}} - V_{\text{SHUTDOWN-}}$	250			mV
$V_{\text{IN}}$	Input voltage range	PACK, SMBC, SMBD, $\overline{\text{PRES}}$ , BTP_IN, $\overline{\text{DISP}}$	26			V
		TS1, TS2, TS3, TS4	$V_{\text{REG}}$			
		PTC, PTCEN, LEDCNTLA, LEDCNTLB, LEDCNTLC	$V_{\text{BAT}}$			
		SRP, SRN	-0.2	0.2		
		VC4	$V_{\text{VC3}}$	$V_{\text{VC3}} + 5$		
		VC3	$V_{\text{VC2}}$	$V_{\text{VC2}} + 5$		
		VC2	$V_{\text{VC1}}$	$V_{\text{VC1}} + 5$		
	VC1	$V_{\text{VSS}}$	$V_{\text{VSS}} + 5$			
$V_{\text{O}}$	Output voltage range	CHG, DSG, PCHG, FUSE	26			V
$C_{\text{PBI}}$	External PBI capacitor		2.2			$\mu\text{F}$
$T_{\text{OPR}}$	Operating temperature		-40	85		$^\circ\text{C}$

## SUPPLY CURRENT

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $20\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT	
$I_{\text{NORMAL}}$	NORMAL mode	CHG on, DSG on, no Flash write			336	$\mu\text{A}$
$I_{\text{SLEEP}}$	SLEEP mode	CHG off, DSG on, no SBS communication			75	$\mu\text{A}$
		CHG off, DSG off, no SBS communication			52	
$I_{\text{SHUTDOWN}}$	SHUTDOWN mode				1.6	$\mu\text{A}$

## POWER SUPPLY CONTROL

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT			
$V_{\text{SWITCHOVER-}}$	BAT to $V_{\text{CC}}$ switchover voltage	$V_{\text{BAT}} < V_{\text{SWITCHOVER-}}$			1.95	2.1	2.2	V
$V_{\text{SWITCHOVER+}}$	$V_{\text{CC}}$ to BAT switchover voltage	$V_{\text{BAT}} > V_{\text{SWITCHOVER-}} + V_{\text{HYS}}$			2.9	3.1	3.25	V
$V_{\text{HYS}}$	Switchover voltage hysteresis	$V_{\text{SWITCHOVER+}} - V_{\text{SWITCHOVER-}}$			1000			mV
$I_{\text{LKG}}$	Input Leakage current	BAT pin, BAT = 0 V, $V_{\text{CC}} = 25\text{ V}$ , PACK = 25 V			1			$\mu\text{A}$
		PACK pin, BAT = 25 V, $V_{\text{CC}} = 0\text{ V}$ , PACK = 0 V			1			
		BAT and PACK pins, BAT = 0 V, $V_{\text{CC}} = 0\text{ V}$ , PACK = 0 V, PBI = 25 V			1			
$R_{\text{PD}}$	Internal pulldown resistance	PACK			30	40	50	k $\Omega$



## AFE POWER-ON RESET

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{\text{REGIT-}}$	Negative-going voltage input	$V_{\text{REG}}$	1.51	1.55	1.59	V
$V_{\text{HYS}}$	Power-on reset hysteresis	$V_{\text{REGIT+}} - V_{\text{REGIT-}}$	70	100	130	mV
$t_{\text{RST}}$	Power-on reset time		200	300	400	$\mu\text{s}$

## AFE WATCHDOG RESET AND WAKE TIMER

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$t_{\text{WDT}}$	AFE watchdog timeout	$t_{\text{WDT}} = 500$	372	500	628	ms
		$t_{\text{WDT}} = 1000$	744	1000	1256	
		$t_{\text{WDT}} = 2000$	1488	2000	2512	
		$t_{\text{WDT}} = 4000$	2976	4000	5024	
$t_{\text{WAKE}}$	AFE wake timer	$t_{\text{WAKE}} = 250$	186	250	314	ms
		$t_{\text{WAKE}} = 500$	372	500	628	
		$t_{\text{WAKE}} = 1000$	744	1000	1256	
		$t_{\text{WAKE}} = 512$	1488	2000	2512	
$t_{\text{FETOFF}}$	FET off delay after reset	$t_{\text{FETOFF}} = 512$	409	512	614	ms

## CURRENT WAKE COMPARATOR

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{\text{WAKE}}$	Wake voltage threshold	$V_{\text{WAKE}} = \pm 0.625\text{ mV}$	$\pm 0.3$	$\pm 0.625$	$\pm 0.9$	mV
		$V_{\text{WAKE}} = \pm 1.25\text{ mV}$	$\pm 0.6$	$\pm 1.25$	$\pm 1.8$	
		$V_{\text{WAKE}} = \pm 2.5\text{ mV}$	$\pm 1.2$	$\pm 2.5$	$\pm 3.6$	
		$V_{\text{WAKE}} = \pm 5\text{ mV}$	$\pm 2.4$	$\pm 5.0$	$\pm 7.2$	
$V_{\text{WAKE(DRIFT)}}$	Temperature drift of $V_{\text{WAKE}}$ accuracy		0.5		%/ $^\circ\text{C}$	
$t_{\text{WAKE}}$	Time from application of current to wake interrupt		700		$\mu\text{s}$	
$t_{\text{WAKE(SU)}}$	Wake comparator startup time		500	1000	$\mu\text{s}$	

## VC1, VC2, VC3, VC4, BAT, PACK

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
K	Scaling factor	VC1–VSS, VC2–VC1, VC3–VC2, VC4–VC3	0.1980	0.2000	0.2020	—
		BAT–VSS, PACK–VSS	0.049	0.050	0.051	
		$V_{\text{REF2}}$	0.490	0.500	0.510	

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{IN}$	Input voltage range	VC1–VSS, VC2–VC1, VC3–VC2, VC4–VC3	–0.2		5	V
		BAT–VSS, PACK–VSS	–0.2		20	
$I_{LKG}$	Input leakage current	VC1, VC2, VC3, VC4, cell balancing off, cell detach detection off, ADC multiplexer off			1	$\mu\text{A}$
$R_{CB}$	Internal cell balance resistance	$R_{DS(ON)}$ for internal FET switch at $2\text{ V} < V_{DS} < 4\text{ V}$			200	$\Omega$
$I_{CD}$	Internal cell detach check current	$VCx > VSS + 0.8\text{ V}$	30	50	70	$\mu\text{A}$

### SMBD, SMBC

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{IH}$	Input voltage high	SMBC, SMBD, $V_{REG} = 1.8\text{ V}$	1.3			V
$V_{IL}$	Input voltage low	SMBC, SMBD, $V_{REG} = 1.8\text{ V}$			0.8	V
$V_{OL}$	Output low voltage	SMBC, SMBD, $V_{REG} = 1.8\text{ V}$ , $I_{OL} = 1.5\text{ mA}$			0.4	V
$C_{IN}$	Input capacitance			5		pF
$I_{LKG}$	Input leakage current				1	$\mu\text{A}$
$R_{PD}$	Pulldown resistance		0.7	1.0	1.3	M $\Omega$

### $\overline{\text{PRES}}$ , BTP\_INT, $\overline{\text{DISP}}$

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{IH}$	High-level input		1.3			V
$V_{IL}$	Low-level input				0.55	V
$V_{OH}$	Output voltage high	$V_{BAT} > 5.5\text{ V}$ , $I_{OH} = -0\text{ }\mu\text{A}$	3.5			V
		$V_{BAT} > 5.5\text{ V}$ , $I_{OH} = -10\text{ }\mu\text{A}$	1.8			
$V_{OL}$	Output voltage low	$I_{OL} = 1.5\text{ mA}$			0.4	V
$C_{IN}$	Input capacitance			5		pF
$I_{LKG}$	Input leakage current				1	$\mu\text{A}$
$R_O$	Output reverse resistance	Between $\overline{\text{PRES}}$ or BTP_INT or $\overline{\text{DISP}}$ and PBI	8			k $\Omega$

### LEDCNTLA, LEDCNTLB, LEDCNTLC

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{IH}$	High-level input		1.45			V
$V_{IL}$	Low-level input				0.55	V
$V_{OH}$	Output voltage high	$V_{BAT} > 3.0\text{ V}$ , $I_{OH} = -22.5\text{ mA}$	$V_{BAT} - 1.6$			V
$V_{OL}$	Output voltage low	$I_{OL} = 1.5\text{ mA}$			0.4	V
$I_{SC}$	High level output current protection		–30	–45	–60	mA
$I_{OL}$	Low level output current	$V_{BAT} > 3.0\text{ V}$ , $V_{OH} = 0.4\text{ V}$	15.75	22.5	29.25	mA

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
$I_{LEDCNTLX}$ Current matching between LEDCNTLX	$V_{BAT} = V_{LEDCNTLX} + 2.5\text{ V}$		+/-1		%
$C_{IN}$ Input capacitance			20		pF
$I_{LKG}$ Input leakage current				1	$\mu\text{A}$
$f_{LEDCNTLX}$ Frequency of LED pattern			124		Hz

## COULOMB COUNTER

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Input voltage range		-0.1		0.1	V
Full scale range		$-V_{REF1}/10$		$V_{REF1}/10$	V
Integral nonlinearity <sup>(1)</sup>	16-bit, best fit over input voltage range		$\pm 5.2$	$\pm 22.3$	LSB
Offset error	16-bit, Post-calibration		$\pm 5$	$\pm 10$	$\mu\text{V}$
Offset error drift	15-bit + sign, Post-calibration		0.2	0.3	$\mu\text{V}/^\circ\text{C}$
Gain error	15-bit + sign, over input voltage range		$\pm 0.2$	$\pm 0.8$	%FSR
Gain error drift	15-bit + sign, over input voltage range			150	PPM/ $^\circ\text{C}$
Effective input resistance		2.5			$\text{M}\Omega$

(1)  $1\text{ LSB} = V_{REF1}/(10 \times 2^N) = 1.215/(10 \times 2^{15}) = 3.71\text{ }\mu\text{V}$

## CC DIGITAL FILTER

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Conversion time	Single conversion		250		ms
Effective resolution	Single conversion	15			Bits

## ADC

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Input voltage range	Internal reference ( $V_{REF1}$ )	-0.2		1	V
	External reference ( $V_{REG}$ )	-0.2		$0.8 \times V_{REG}$	
Full scale range	$V_{FS} = V_{REF1}$ or $V_{REG}$	$-V_{FS}$		$V_{FS}$	V
Integral nonlinearity <sup>(1)</sup>	16-bit, best fit, $-0.1\text{ V}$ to $0.8 \times V_{REF1}$			$\pm 6.6$	LSB
	16-bit, best fit, $-0.2\text{ V}$ to $-0.1\text{ V}$			$\pm 13.1$	
Offset error <sup>(2)</sup>	16-bit, Post-calibration, $V_{FS} = V_{REF1}$		$\pm 67$	$\pm 157$	$\mu\text{V}$
Offset error drift	16-bit, Post-calibration, $V_{FS} = V_{REF1}$		0.6	3	$\mu\text{V}/^\circ\text{C}$
Gain error	16-bit, $-0.1\text{ V}$ to $0.8 \times V_{FS}$		$\pm 0.2$	$\pm 0.8$	%FSR
Gain error drift	16-bit, $-0.1\text{ V}$ to $0.8 \times V_{FS}$			150	PPM/ $^\circ\text{C}$
Effective input resistance		8			$\text{M}\Omega$

(1)  $1\text{ LSB} = V_{REF1}/(2^N) = 1.225/(2^{15}) = 37.4\text{ }\mu\text{V}$  (when  $t_{CONV} = 31.25\text{ ms}$ )

(2) For VC1-VSS, VC2-VC1, VC3-VC2, VC4-VC3, VC4-VSS, PACK-VSS, and  $V_{REF1}/2$ , the offset error is multiplied by (1/ADC multiplexer scaling factor (K)).

## ADC DIGITAL FILTER

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Conversion time	Single conversion		31.25		ms
	Single conversion		15.63		
	Single conversion		7.81		
	Single conversion		1.95		
Resolution	No missing codes	16			Bits
Effective resolution	With sign, $t_{\text{CONV}} = 31.25\text{ ms}$	14	15		Bits
	With sign, $t_{\text{CONV}} = 15.63\text{ ms}$	13	14		
	With sign, $t_{\text{CONV}} = 7.81\text{ ms}$	11	12		
	With sign, $t_{\text{CONV}} = 1.95\text{ ms}$	9	10		

## CHG, DSG FET DRIVE

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Output voltage ratio	$\text{Ratio}_{\text{DSG}} = (V_{\text{DSG}} - V_{\text{BAT}})/V_{\text{BAT}}$ , $2.2\text{ V} < V_{\text{BAT}} < 4.92\text{ V}$ , $10\text{ M}\Omega$ between PACK and DSG	2.133	2.333	2.433	—
	$\text{Ratio}_{\text{CHG}} = (V_{\text{CHG}} - V_{\text{BAT}})/V_{\text{BAT}}$ , $2.2\text{ V} < V_{\text{BAT}} < 4.92\text{ V}$ , $10\text{ M}\Omega$ between BAT and CHG	2.133	2.333	2.433	
$V_{(\text{FETON})}$	$V_{\text{DSG(ON)}} = V_{\text{DSG}} - V_{\text{BAT}}$ , $V_{\text{BAT}} \geq 4.92\text{ V}$ , $10\text{ M}\Omega$ between PACK and DSG, $V_{\text{BAT}} = 18\text{ V}$	10.5	11.5	12	V
	$V_{\text{CHG(ON)}} = V_{\text{CHG}} - V_{\text{BAT}}$ , $V_{\text{BAT}} \geq 4.92\text{ V}$ , $10\text{ M}\Omega$ between BAT and CHG, $V_{\text{BAT}} = 18\text{ V}$	10.5	11.5	12	
$V_{(\text{FETOFF})}$	$V_{\text{DSG(OFF)}} = V_{\text{DSG}} - V_{\text{PACK}}$ , $10\text{ M}\Omega$ between PACK and DSG	-0.4		0.4	V
	$V_{\text{CHG(OFF)}} = V_{\text{CHG}} - V_{\text{BAT}}$ , $10\text{ M}\Omega$ between BAT and CHG	-0.4		0.4	
$t_{\text{R}}$	$V_{\text{DSG}}$ from 0% to 35% $V_{\text{DSG(ON)(TYP)}}$ , $V_{\text{BAT}} \geq 2.2\text{ V}$ , $C_{\text{L}} = 4.7\text{ nF}$ between DSG and PACK, $5.1\text{ k}\Omega$ between DSG and $C_{\text{L}}$ , $10\text{ M}\Omega$ between PACK and DSG		200	500	$\mu\text{s}$
	$V_{\text{CHG}}$ from 0% to 35% $V_{\text{CHG(ON)(TYP)}}$ , $V_{\text{BAT}} \geq 2.2\text{ V}$ , $C_{\text{L}} = 4.7\text{ nF}$ between CHG and BAT, $5.1\text{ k}\Omega$ between CHG and $C_{\text{L}}$ , $10\text{ M}\Omega$ between BAT and CHG		200	500	
$t_{\text{F}}$	$V_{\text{DSG}}$ from $V_{\text{DSG(ON)(TYP)}}$ to $1\text{ V}$ , $V_{\text{BAT}} \geq 2.2\text{ V}$ , $C_{\text{L}} = 4.7\text{ nF}$ between DSG and PACK, $5.1\text{ k}\Omega$ between DSG and $C_{\text{L}}$ , $10\text{ M}\Omega$ between PACK and DSG		40	300	$\mu\text{s}$
	$V_{\text{CHG}}$ from $V_{\text{CHG(ON)(TYP)}}$ to $1\text{ V}$ , $V_{\text{BAT}} \geq 2.2\text{ V}$ , $C_{\text{L}} = 4.7\text{ nF}$ between CHG and BAT, $5.1\text{ k}\Omega$ between CHG and $C_{\text{L}}$ , $10\text{ M}\Omega$ between BAT and CHG		40	200	

## PCHG FET DRIVE

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{(\text{FETON})}$	Output voltage, PCHG on $V_{\text{PCHG(ON)}} = V_{\text{VCC}} - V_{\text{PCHG}}$ , $10\text{ M}\Omega$ between $V_{\text{CC}}$ and PCHG	6	7	8	V
$V_{(\text{FETOFF})}$	Output voltage, PCHG off $V_{\text{PCHG(OFF)}} = V_{\text{VCC}} - V_{\text{PCHG}}$ , $10\text{ M}\Omega$ between $V_{\text{CC}}$ and PCHG	-0.4		0.4	V
$t_{\text{R}}$	Rise time $V_{\text{PCHG}}$ from 10% to 90% $V_{\text{PCHG(ON)(TYP)}}$ , $V_{\text{VCC}} \geq 8\text{ V}$ , $C_{\text{L}} = 4.7\text{ nF}$ between PCHG and $V_{\text{CC}}$ , $5.1\text{ k}\Omega$ between PCHG and $C_{\text{L}}$ , $10\text{ M}\Omega$ between $V_{\text{CC}}$ and CHG		40	200	$\mu\text{s}$

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
$t_F$ Fall time	$V_{PCHG}$ from 90% to 10% $V_{PCHG(ON)(TYP)}$ , $V_{CC} \geq 8\text{ V}$ , $C_L = 4.7\text{ nF}$ between PCHG and $V_{CC}$ , $5.1\text{ k}\Omega$ between PCHG and $C_L$ , $10\text{ M}\Omega$ between $V_{CC}$ and CHG		40	200	$\mu\text{s}$

## FUSE DRIVE

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{OH}$ Output voltage high	$V_{BAT} \geq 8\text{ V}$ , $C_L = 1\text{ nF}$ , $I_{AFEFUSE} = 0\text{ }\mu\text{A}$	6	7	8.65	V
	$V_{BAT} < 8\text{ V}$ , $C_L = 1\text{ nF}$ , $I_{AFEFUSE} = 0\text{ }\mu\text{A}$	$V_{BAT} - 0.1$		$V_{BAT}$	
$V_{IH}$ High-level input		1.5	2.0	2.5	V
$I_{AFEFUSE(PU)}$ Internal pullup current	$V_{BAT} \geq 8\text{ V}$ , $V_{AFEFUSE} = V_{SS}$		150	330	nA
$R_{AFEFUSE}$ Output impedance		2	2.6	3.2	k $\Omega$
$C_{IN}$ Input capacitance			5		pF
$t_{DELAY}$ Fuse trip detection delay		128		256	$\mu\text{s}$
$t_{RISE}$ Fuse output rise time	$V_{BAT} \geq 8\text{ V}$ , $C_L = 1\text{ nF}$ , $V_{OH} = 0\text{ V}$ to $5\text{ V}$		5	20	$\mu\text{s}$

## INTERNAL TEMPERATURE SENSOR

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{TEMP}$ Internal temperature sensor voltage drift	$V_{TEMPPP}$	-1.9	-2.0	-2.1	mV/ $^\circ\text{C}$
	$V_{TEMPPP} - V_{TEMPN}$ , assured by design	0.177	0.178	0.179	

## TS1, TS2, TS3, TS4

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{IN}$ Input voltage range	TS1, TS2, TS3, TS4, $V_{BIAS} = V_{REF1}$	-0.2		$0.8 \times V_{REF1}$	V
	TS1, TS2, TS3, TS4, $V_{BIAS} = V_{REG}$	-0.2		$0.8 \times V_{REG}$	
$R_{NTC(PU)}$ Internal pullup resistance	TS1, TS2, TS3, TS4	14.4	18	21.6	k $\Omega$
$R_{NTC(DRIFT)}$ Resistance drift over temperature	TS1, TS2, TS3, TS4	-360	-280	-200	PPM/ $^\circ\text{C}$

## PTC, PTCEN

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
$R_{PTC(TRIP)}$ PTC trip resistance		1.2	2.5	3.95	M $\Omega$

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{\text{PTC(TRIP)}}$	PTC trip voltage	$V_{\text{PTC(TRIP)}} = V_{\text{PTCEN}} - V_{\text{PTC}}$	200	500	890	mV
$I_{\text{PTC}}$	Internal PTC current bias	$T_A = -40^\circ\text{C}$ to $110^\circ\text{C}$	200	290	350	nA
$t_{\text{PTC(DELAY)}}$	PTC delay time	$T_A = -40^\circ\text{C}$ to $110^\circ\text{C}$	40	80	145	ms

## INTERNAL 1.8-V LDO

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{\text{REG}}$	Regulator voltage		1.6	1.8	2.0	V
$\Delta V_{\text{O(TEMP)}}$	Regulator output over temperature	$\Delta V_{\text{REG}}/\Delta T_A$ , $I_{\text{REG}} = 10\text{ mA}$		$\pm 0.25$		%
$\Delta V_{\text{O(LINE)}}$	Line regulation	$\Delta V_{\text{REG}}/\Delta V_{\text{BAT}}$ , $V_{\text{BAT}} = 10\text{ mA}$	-0.6		0.5	%
$\Delta V_{\text{O(LOAD)}}$	Load regulation	$\Delta V_{\text{REG}}/\Delta I_{\text{REG}}$ , $I_{\text{REG}} = 0\text{ mA}$ to $10\text{ mA}$	-1.5		1.5	%
$I_{\text{REG}}$	Regulator output current limit	$V_{\text{REG}} = 0.9 \times V_{\text{REG(NOM)}}$ , $V_{\text{IN}} > 2.2\text{ V}$	20			mA
$I_{\text{SC}}$	Regulator short-circuit current limit	$V_{\text{REG}} = 0 \times V_{\text{REG(NOM)}}$	25	40	55	mA
$\text{PSRR}_{\text{REG}}$	Power supply rejection ratio	$\Delta V_{\text{BAT}}/\Delta V_{\text{REG}}$ , $I_{\text{REG}} = 10\text{ mA}$ , $V_{\text{IN}} > 2.5\text{ V}$ , $f = 10\text{ Hz}$		40		dB
$V_{\text{SLEW}}$	Slew rate enhancement voltage threshold	$V_{\text{REG}}$	1.58	1.65		V

## HIGH-FREQUENCY OSCILLATOR

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$f_{\text{HFO}}$	Operating frequency			16.78		MHz
$f_{\text{HFO(ERR)}}$	Frequency error	$T_A = -20^\circ\text{C}$ to $70^\circ\text{C}$ , includes frequency drift	-2.5	$\pm 0.25$	2.5	%
		$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$ , includes frequency drift	-3.5	$\pm 0.25$	3.5	
$t_{\text{HFO(SU)}}$	Start-up time	$T_A = -20^\circ\text{C}$ to $85^\circ\text{C}$ , oscillator frequency within $\pm 3\%$ of nominal			4	ms
		oscillator frequency within $\pm 3\%$ of nominal			100	$\mu\text{s}$

## LOW-FREQUENCY OSCILLATOR

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$f_{\text{LFO}}$	Operating frequency			262.144		kHz
$f_{\text{LFO(ERR)}}$	Frequency error	$T_A = -20^\circ\text{C}$ to $70^\circ\text{C}$ , includes frequency drift	-1.5	$\pm 0.25$	1.5	%
		$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$ , includes frequency drift	-2.5	$\pm 0.25$	2.5	
$f_{\text{LFO(FAIL)}}$	Failure detection frequency		30	80	100	kHz

## VOLTAGE REFERENCE 1

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{REF1}$ Internal reference voltage	$T_A = 25^\circ\text{C}$ , after trim	1.21	1.215	1.22	V
$V_{REF1(DRIFT)}$ Internal reference voltage drift	$T_A = 0^\circ\text{C}$ to $60^\circ\text{C}$ , after trim	±50			PPM/°C
	$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$ , after trim	±80			

## VOLTAGE REFERENCE 2

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{REF2}$ Internal reference voltage	$T_A = 25^\circ\text{C}$ , after trim	1.22	1.225	1.23	V
$V_{REF2(DRIFT)}$ Internal reference voltage drift	$T_A = 0^\circ\text{C}$ to $60^\circ\text{C}$ , after trim	±50			PPM/°C
	$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$ , after trim	±80			

## INSTRUCTION FLASH

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Data retention		10			Years
Flash programming write cycles		1000			Cycles
$t_{PROGWORD}$ Word programming time	$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$	40			µs
$t_{MASSERASE}$ Mass-erase time	$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$	40			ms
$t_{PAGEERASE}$ Page-erase time	$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$	40			ms
$I_{FLASHREAD}$ Flash-read current	$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$	2			mA
$I_{FLASHWRITE}$ Flash-write current	$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$	5			mA
$I_{FLASHERASE}$ Flash-erase current	$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$	15			mA

## DATA FLASH

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Data retention		10			Years
Flash programming write cycles		20000			Cycles
$t_{PROGWORD}$ Word programming time	$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$	40			µs
$t_{MASSERASE}$ Mass-erase time	$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$	40			ms
$t_{PAGEERASE}$ Page-erase time	$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$	40			ms
$I_{FLASHREAD}$ Flash-read current	$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$	1			mA
$I_{FLASHWRITE}$ Flash-write current	$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$	5			mA
$I_{FLASHERASE}$ Flash-erase current	$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$	15			mA

## OCD, SCC, SCD1, SCD2 CURRENT PROTECTION THRESHOLDS

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{\text{OCD}}$	OCD detection threshold voltage range	$V_{\text{OCD}} = V_{\text{SRP}} - V_{\text{SRN}}$ , AFE PROTECTION CONTROL[RSNS] = 1	-16.6		-100	mV
		$V_{\text{OCD}} = V_{\text{SRP}} - V_{\text{SRN}}$ , AFE PROTECTION CONTROL[RSNS] = 0	-8.3		-50	
$\Delta V_{\text{OCD}}$	OCD detection threshold voltage program step	$V_{\text{OCD}} = V_{\text{SRP}} - V_{\text{SRN}}$ , AFE PROTECTION CONTROL[RSNS] = 1		-5.56		mV
		$V_{\text{OCD}} = V_{\text{SRP}} - V_{\text{SRN}}$ , AFE PROTECTION CONTROL[RSNS] = 0		-2.78		
$V_{\text{SCC}}$	SCC detection threshold voltage range	$V_{\text{SCC}} = V_{\text{SRP}} - V_{\text{SRN}}$ , AFE PROTECTION CONTROL[RSNS] = 1	44.4		200	mV
		$V_{\text{SCC}} = V_{\text{SRP}} - V_{\text{SRN}}$ , AFE PROTECTION CONTROL[RSNS] = 0	22.2		100	
$\Delta V_{\text{SCC}}$	SCC detection threshold voltage program step	$V_{\text{SCC}} = V_{\text{SRP}} - V_{\text{SRN}}$ , AFE PROTECTION CONTROL[RSNS] = 1		22.2		mV
		$V_{\text{SCC}} = V_{\text{SRP}} - V_{\text{SRN}}$ , AFE PROTECTION CONTROL[RSNS] = 0		11.1		
$V_{\text{SCD1}}$	SCD1 detection threshold voltage range	$V_{\text{SCD1}} = V_{\text{SRP}} - V_{\text{SRN}}$ , AFE PROTECTION CONTROL[RSNS] = 1	-44.4		-200	mV
		$V_{\text{SCD1}} = V_{\text{SRP}} - V_{\text{SRN}}$ , AFE PROTECTION CONTROL[RSNS] = 0	-22.2		-100	
$\Delta V_{\text{SCD1}}$	SCD1 detection threshold voltage program step	$V_{\text{SCD1}} = V_{\text{SRP}} - V_{\text{SRN}}$ , AFE PROTECTION CONTROL[RSNS] = 1		-22.2		mV
		$V_{\text{SCD1}} = V_{\text{SRP}} - V_{\text{SRN}}$ , AFE PROTECTION CONTROL[RSNS] = 0		-11.1		
$V_{\text{SCD2}}$	SCD2 detection threshold voltage range	$V_{\text{SCD2}} = V_{\text{SRP}} - V_{\text{SRN}}$ , AFE PROTECTION CONTROL[RSNS] = 1	-44.4		-200	mV
		$V_{\text{SCD2}} = V_{\text{SRP}} - V_{\text{SRN}}$ , AFE PROTECTION CONTROL[RSNS] = 0	-22.2		-100	
$\Delta V_{\text{SCD2}}$	SCD2 detection threshold voltage program step	$V_{\text{SCD2}} = V_{\text{SRP}} - V_{\text{SRN}}$ , AFE PROTECTION CONTROL[RSNS] = 1		-22.2		mV
		$V_{\text{SCD2}} = V_{\text{SRP}} - V_{\text{SRN}}$ , AFE PROTECTION CONTROL[RSNS] = 0		-11.1		
$V_{\text{OFFSET}}$	OCD, SCC, and SCDx offset error	Post-trim	-2.5		2.5	mV
$V_{\text{SCALE}}$	OCD, SCC, and SCDx scale error	No trim	-10		10	%
		Post-trim	-5		5	

## OCD, SCC, SCD1, SCD2 CURRENT PROTECTION TIMING

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$t_{\text{OCD}}$	OCD detection delay time		1		31	ms
$\Delta t_{\text{OCD}}$	OCD detection delay time program step			2		ms
$t_{\text{SCC}}$	SCC detection delay time		0		915	$\mu\text{s}$
$\Delta t_{\text{SCC}}$	SCC detection delay time program step			61		$\mu\text{s}$



Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$t_{\text{SCD1}}$	SCD1 detection delay time	AFE PROTECTION CONTROL[SCDDx2] = 0	0		915	$\mu\text{s}$
		AFE PROTECTION CONTROL[SCDDx2] = 1	0		1850	
$\Delta t_{\text{SCD1}}$	SCD1 detection delay time program step	AFE PROTECTION CONTROL[SCDDx2] = 0		61		$\mu\text{s}$
		AFE PROTECTION CONTROL[SCDDx2] = 1		121		
$t_{\text{SCD2}}$	SCD2 detection delay time	AFE PROTECTION CONTROL[SCDDx2] = 0	0		458	$\mu\text{s}$
		AFE PROTECTION CONTROL[SCDDx2] = 1	0		915	
$\Delta t_{\text{SCD2}}$	SCD2 detection delay time program step	AFE PROTECTION CONTROL[SCDDx2] = 0		30.5		$\mu\text{s}$
		AFE PROTECTION CONTROL[SCDDx2] = 1		61		
$t_{\text{DETECT}}$	Current fault detect time	$V_{\text{SRP}} - V_{\text{SRN}} = V_T - 3\text{ mV}$ for OCD, SCD1, and SC2, $V_{\text{SRP}} - V_{\text{SRN}} = V_T + 3\text{ mV}$ for SCC			160	$\mu\text{s}$
$t_{\text{ACC}}$	Current fault delay time accuracy	Max delay setting	-10		10	%

## SMBus

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$f_{\text{SMB}}$	SMBus operating frequency	SLAVE mode, SMBC 50% duty cycle	10		100	kHz
$f_{\text{MAS}}$	SMBus master clock frequency	MASTER mode, no clock low slave extend		51.2		kHz
$t_{\text{BUF}}$	Bus free time between start and stop		4.7			$\mu\text{s}$
$t_{\text{HD(START)}}$	Hold time after (repeated) start		4.0			$\mu\text{s}$
$t_{\text{SU(START)}}$	Repeated start setup time		4.7			$\mu\text{s}$
$t_{\text{SU(STOP)}}$	Stop setup time		4.0			$\mu\text{s}$
$t_{\text{HD(DATA)}}$	Data hold time		300			ns
$t_{\text{SU(DATA)}}$	Data setup time		250			ns
$t_{\text{TIMEOUT}}$	Error signal detect time		25		35	ms
$t_{\text{LOW}}$	Clock low period		4.7			$\mu\text{s}$
$t_{\text{HIGH}}$	Clock high period		4.0		50	$\mu\text{s}$
$t_{\text{R}}$	Clock rise time	10% to 90%			1000	ns
$t_{\text{F}}$	Clock fall time	90% to 10%			300	ns
$t_{\text{LOW(SEXT)}}$	Cumulative clock low slave extend time				25	ms
$t_{\text{LOW(MEXT)}}$	Cumulative clock low master extend time				10	ms

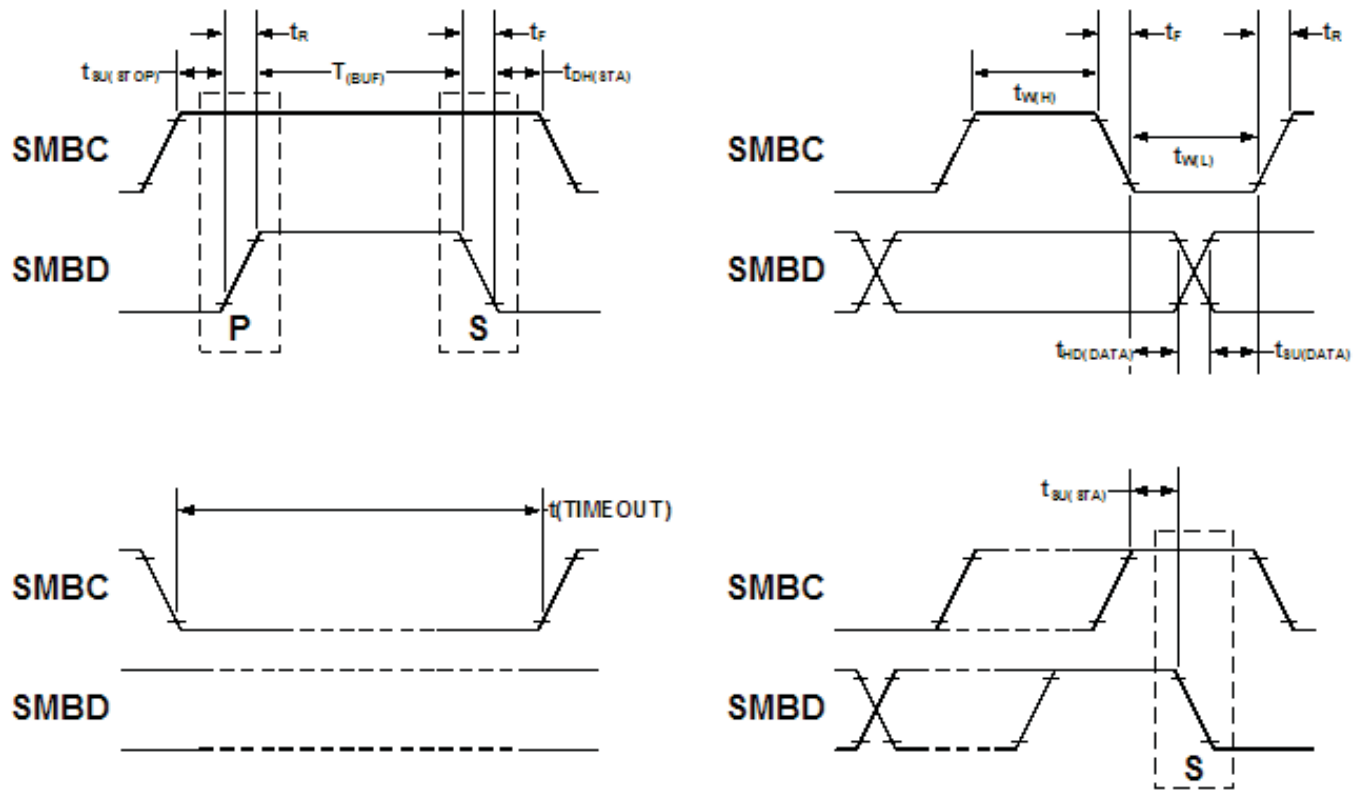


Figure 6. SMBus Timing Diagram

**SMBus XL**

Typical values stated where  $T_A = 25^{\circ}\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  and  $V_{CC} = 2.2\text{ V}$  to  $26\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT	
$f_{\text{SMBXL}}$	SMBus XL operating frequency	SLAVE mode		40	400	kHz
$t_{\text{BUF}}$	Bus free time between start and stop	4.7				$\mu\text{s}$
$t_{\text{HD(START)}}$	Hold time after (repeated) start	4.0				$\mu\text{s}$
$t_{\text{SU(START)}}$	Repeated start setup time	4.7				$\mu\text{s}$
$t_{\text{SU(STOP)}}$	Stop setup time	4.0				$\mu\text{s}$
$t_{\text{TIMEOUT}}$	Error signal detect time	5		20		ms
$t_{\text{LOW}}$	Clock low period			20		$\mu\text{s}$
$t_{\text{HIGH}}$	Clock high period			20		$\mu\text{s}$

## FEATURE SET

### Primary (1st Level) Safety Features

The bq40z50 supports a wide range of battery and system protection features that can easily be configured. The primary safety features include:

- Cell Overvoltage Protection
- Cell Undervoltage Protection
- Cell Undervoltage Protection Compensated
- Overcurrent in Charge Protection
- Overcurrent in Discharge Protection
- Overload in Discharge Protection
- Short Circuit in Charge Protection
- Short Circuit in Discharge Protection
- Overtemperature in Charge Protection
- Overtemperature in Discharge Protection
- Undertemperature in Charge Protection
- Undertemperature in Discharge Protection
- Overtemperature FET protection
- Precharge Timeout Protection
- Host Watchdog Timeout Protection
- Fast Charge Timeout Protection
- Overcharge Protection
- Overcharging Voltage Protection
- Overcharging Current Protection
- Over Precharge Current Protection

### Secondary (2nd Level) Safety Features

The secondary safety features of the bq40z50 can be used to indicate more serious faults via the FUSE pin. This pin can be used to blow an in-line fuse to permanently disable the battery pack from charging or discharging. The secondary safety features provide protection against:

- Safety Overvoltage Permanent Failure
- Safety Undervoltage Permanent Failure
- Safety Overtemperature Permanent Failure
- Safety FET Overtemperature Permanent Failure
- Qmax Imbalance Permanent Failure
- Impedance Imbalance Permanent Failure
- Capacity Degradation Permanent Failure
- Cell Balancing Permanent Failure
- Fuse Failure Permanent Failure
- PTC Permanent Failure
- Voltage Imbalance at Rest Permanent Failure
- Voltage Imbalance Active Permanent Failure
- Charge FET Permanent Failure
- Discharge FET Permanent Failure
- AFE Register Permanent Failure
- AFE Communication Permanent Failure
- Second Level Protector Permanent Failure
- Instruction Flash Checksum Permanent Failure
- Open Cell Connection Permanent Failure

- Data Flash Permanent Failure
- Open Thermistor Permanent Failure

## Charge Control Features

The bq40z50 charge control features include:

- Supports JEITA temperature ranges. Reports charging voltage and charging current according to the active temperature range
- Handles more complex charging profiles. Allows for splitting the standard temperature range into two sub-ranges and allows for varying the charging current according to the cell voltage
- Reports the appropriate charging current needed for constant current charging and the appropriate charging voltage needed for constant voltage charging to a smart charger using SMBus broadcasts
- Reduces the charge difference of the battery cells in fully charged state of the battery pack gradually using a voltage-based cell balancing algorithm during charging. A voltage threshold can be set up for cell balancing to be active. This prevents fully charged cells from overcharging and causing excessive degradation and also increases the usable pack energy by preventing premature charge termination.
- Supports pre-charging/zero-volt charging
- Supports charge inhibit and charge suspend if battery pack temperature is out of temperature range
- Reports charging fault and also indicates charge status via charge and discharge alarms

## Gas Gauging

The bq40z50 uses the Impedance Track algorithm to measure and calculate the available capacity in battery cells. The bq40z50 accumulates a measure of charge and discharge currents and compensates the charge current measurement for the temperature and state-of-charge of the battery. The bq40z50 estimates self-discharge of the battery and also adjusts the self-discharge estimation based on temperature. The device also has TURBO BOOST mode support, which enables the bq40z50 to provide the necessary data for the MCU to determine what level of peak power consumption can be applied without causing a system reset or transient battery voltage level spike to trigger termination flags. See the *bq40z50 Technical Reference Manual (SLUUA43)* for further details.

## Battery Trip Point (BTP)

Required for WIN8 OS, the battery trip point (BTP) feature indicates when the RSOC of a battery pack has depleted to a certain value set in a DF register. This feature allows a host to program two capacity-based thresholds that govern the triggering of a BTP interrupt on the BTP\_INT pin and the setting or clearing of the *OperationStatus[BTP\_INT]* on the basis of *RemainingCapacity()*.

An internal weak pull-up is applied when the BTP feature is active. Depending on the system design, an external pull-up may be required to be put on the BTP\_INT pin. See [PRES](#), [BTP\\_INT](#), [DISP](#) for details.

## Lifetime Data Logging Features

The bq40z50 offers lifetime data logging for several critical battery parameters. The following parameters are updated every 10 hours if a difference is detected between values in RAM and data flash:

- Maximum and Minimum Cell Voltages
- Maximum Delta Cell Voltage
- Maximum Charge Current
- Maximum Discharge Current
- Maximum Average Discharge Current
- Maximum Average Discharge Power
- Maximum and Minimum Cell Temperature
- Maximum Delta Cell Temperature
- Maximum and Minimum Internal Sensor Temperature
- Maximum FET Temperature
- Number of Safety Events Occurrences and the Last Cycle of the Occurrence
- Number of Valid Charge Termination and the Last Cycle of the Valid Charge Termination

- Number of Qmax and Ra Updates and the Last Cycle of the Qmax and Ra Updates
- Number of Shutdown Events
- Cell Balancing Time for Each Cell  
(This data is updated every 2 hours if a difference is detected.)
- Total FW Runtime and Time Spent in Each Temperature Range  
(This data is updated every 2 hours if a difference is detected.)

## Authentication

The bq40z50 supports authentication by the host using SHA-1.

## LED Display

The bq40z50 can drive a 3-, 4-, or 5- segment LED display for remaining capacity indication and/or a permanent fail (PF) error code indication.

## Power Modes

The bq40z50 supports three power modes to reduce power consumption:

- In NORMAL mode, the bq40z50 performs measurements, calculations, protection decisions, and data updates in 250-ms intervals. Between these intervals, the bq40z50 is in a reduced power stage.
- In SLEEP mode, the bq40z50 performs measurements, calculations, protection decisions, and data updates in adjustable time intervals. Between these intervals, the bq40z50 is in a reduced power stage. The bq40z50 has a wake function that enables exit from SLEEP mode when current flow or failure is detected.
- In SHUTDOWN mode, the bq40z50 is completely disabled.

## Configuration

### Oscillator Function

The bq40z50 fully integrates the system oscillators and does not require any external components to support this feature.

### System Present Operation

The bq40z50 checks the  $\overline{\text{PRES}}$  pin periodically (1 s). If  $\overline{\text{PRES}}$  input is pulled to ground by the external system, the bq40z50 detects this as system present.

### Emergency Shutdown

For battery maintenance, the emergency shutdown feature enables a push button action connecting the  $\overline{\text{SHUTDN}}$  pin to shutdown an embedded battery pack system before removing the battery. A high-to-low transition of the  $\overline{\text{SHUTDN}}$  pin signals the bq40z50 to turn off both CHG and DSG FETs, disconnecting the power from the system to safely remove the battery pack. The CHG and DSG FETs can be turned on again by another high-to-low transition detected by the  $\overline{\text{SHUTDN}}$  pin or when a data flash configurable timeout is reached.

### 1-Series, 2-Series, 3-Series, or 4-Series Cell Configuration

In a 1-series cell configuration, VC4 is shorted to VC, VC2 and VC1. In a 2-series cell configuration, VC4 is shorted to VC3 and VC2. In a 3-series cell configuration, VC4 is shorted to VC3.

### Cell Balancing

The device supports cell balancing by bypassing the current of each cell during charging or at rest. If the device's internal bypass is used, up to 10 mA can be bypassed and multiple cells can be bypassed at the same time. Higher cell balance current can be achieved by using an external cell balancing circuit. In external cell balancing mode, only one cell at a time can be balanced.

The cell balancing algorithm determines the amount of charge needed to be bypassed to balance the capacity of all cells.

## BATTERY PARAMETER MEASUREMENTS

### Charge and Discharge Counting

The bq40z50 uses an integrating delta-sigma analog-to-digital converter (ADC) for current measurement, and a second delta-sigma ADC for individual cell and battery voltage and temperature measurement.

The integrating delta-sigma ADC measures the charge/discharge flow of the battery by measuring the voltage drop across a small-value sense resistor between the SRP and SRN pins. The integrating ADC measures bipolar signals from  $-0.1\text{ V}$  to  $0.1\text{ V}$ . The bq40z50 detects charge activity when  $V_{SR} = V_{(SRP)} - V_{(SRN)}$  is positive, and discharge activity when  $V_{SR} = V_{(SRP)} - V_{(SRN)}$  is negative. The bq40z50 continuously integrates the signal over time, using an internal counter. The fundamental rate of the counter is  $0.26\text{ nVh}$ .

### Voltage

The bq40z50 updates the individual series cell voltages at 0.25-second intervals. The internal ADC of the bq40z50 measures the voltage, and scales and calibrates it appropriately. This data is also used to calculate the impedance of the cell for the Impedance Track gas gauging.

### Current

The bq40z50 uses the SRP and SRN inputs to measure and calculate the battery charge and discharge current using a  $1\text{-m}\Omega$  to  $3\text{-m}\Omega$  typ. sense resistor.

### Temperature

The bq40z50 has an internal temperature sensor and inputs for four external temperature sensors. All five temperature sensor options can be individually enabled and configured for cell or FET temperature usage. Two configurable thermistor models are provided to allow the monitoring of cell temperature in addition to FET temperature, which use a different thermistor profile.

### Communications

The bq40z50 uses SMBus v1.1 with MASTER mode and packet error checking (PEC) options per the SBS specification.

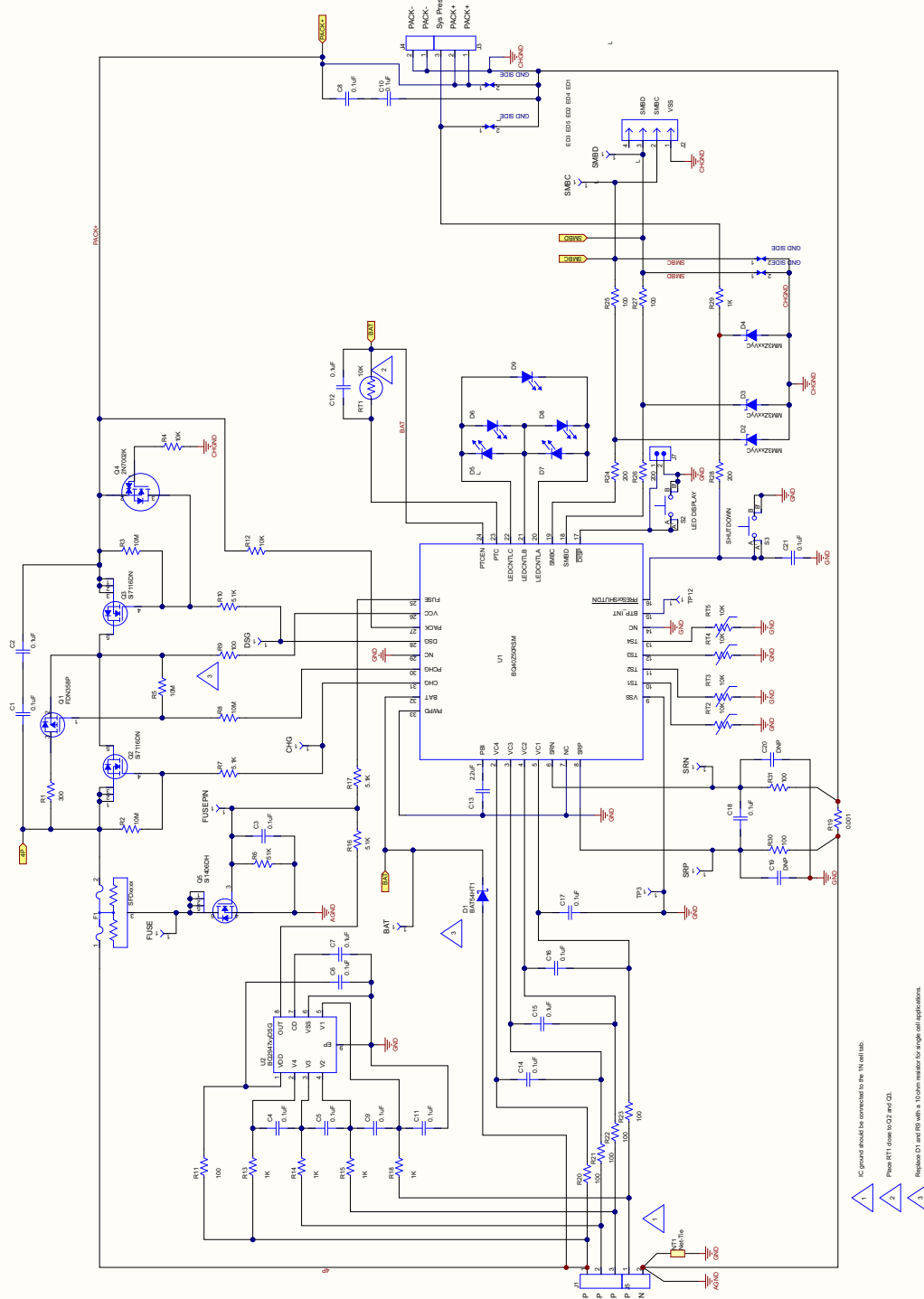
### SMBus On and Off State

The bq40z50 detects an SMBus off state when SMBC and SMBD are low for two or more seconds. Clearing this state requires that either SMBC or SMBD transition high. The communication bus will resume activity within  $1\text{ ms}$ .

### SBS Commands

See the *bq40z50 Technical Reference Manual* ([SLUUA43](#)) for further details.

APPLICATION SCHEMATIC



- 1 IC ground should be connected to the IN cell tab.
- 2 Place RT1 close to C12 and C1.
- 3 Replace D1 and R9 with a 100nm resistor for single cell applications.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ40Z50RSMR	ACTIVE	VQFN	RSM	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ40Z50	<a href="#">Samples</a>
BQ40Z50RSMT	ACTIVE	VQFN	RSM	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ40Z50	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ40Z50RSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ40Z50RSMT	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

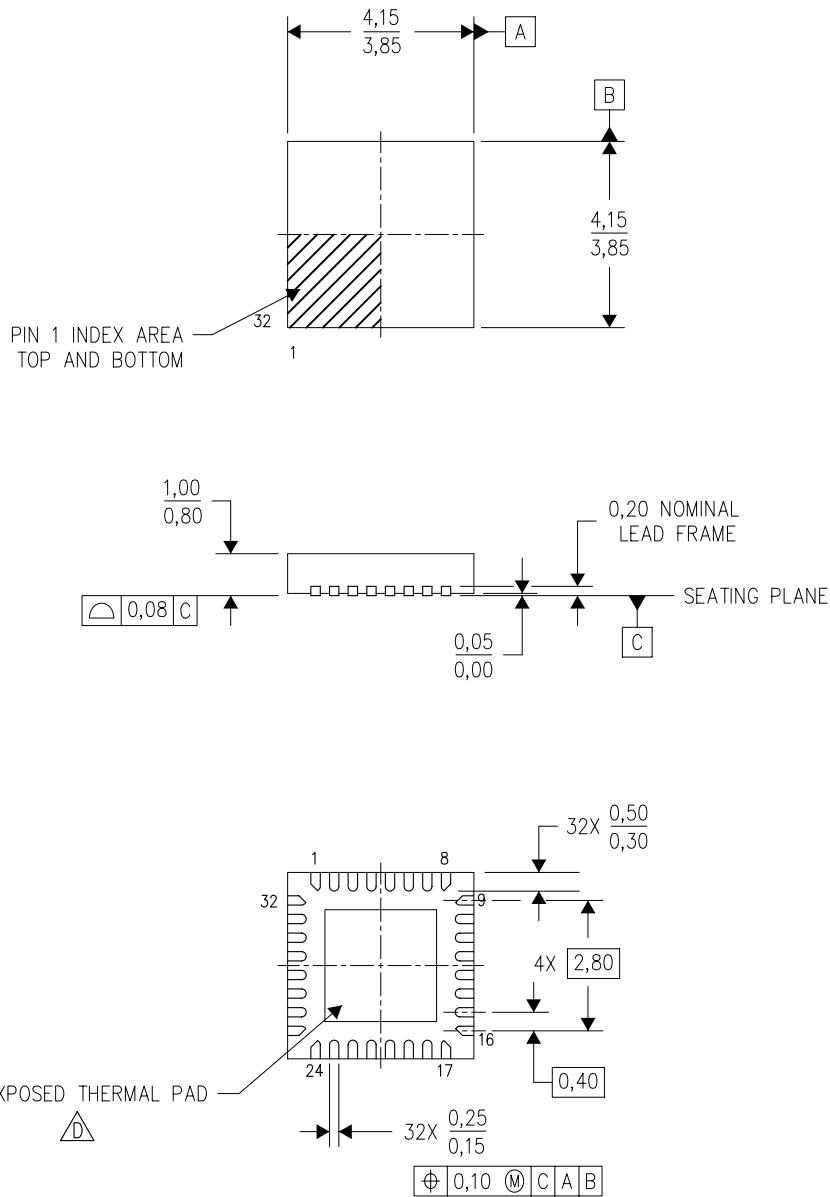
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal


Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ40Z50RSMR	VQFN	RSM	32	3000	367.0	367.0	35.0
BQ40Z50RSMT	VQFN	RSM	32	250	210.0	185.0	35.0

RSM (S-PVQFN-N32)

PLASTIC QUAD FLATPACK NO-LEAD



4207560/B 03/10

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) Package configuration.
  -  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

RSM (S-PVQFN-N32)

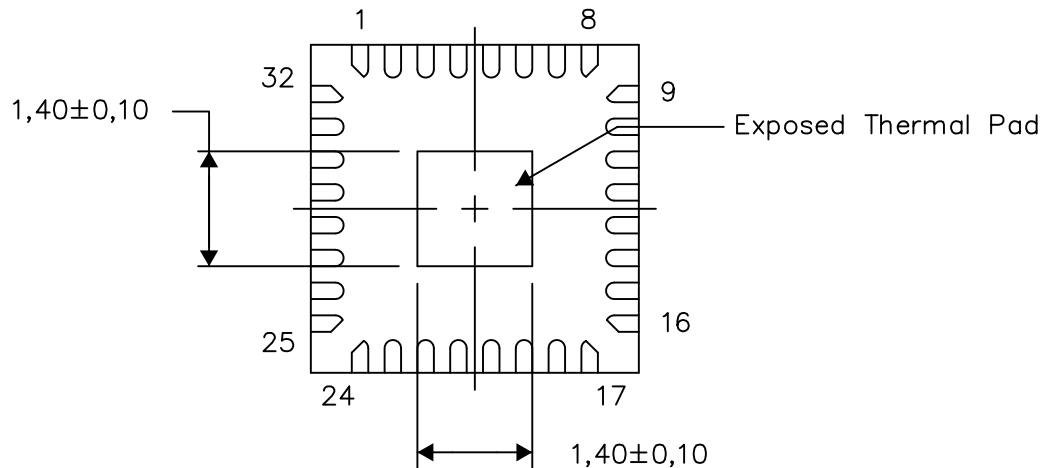
PLASTIC QUAD FLATPACK NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4207868-3/H 04/13

NOTE: All linear dimensions are in millimeters

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