Integrated Circuit Systems, Inc.

ICS9161A

Dual Programmable Graphics Frequency Generator

General Description

The **ICS9161A** is a fully programmable graphics clock generator. It can generate user-specified clock frequencies using an externally generated input reference or a single crystal. The output frequency is programmed by entering a 24-bit digital word through the serial port. Two fully user-programmable phase-locked loops are offered in a single package. One PLL is designed to drive the memory clock, while the second drives the video clock. The outputs may be changed on-the-fly to any desired frequency between 390 kHz and 120 MHz. The **ICS9161A** is ideally suited for any design where multiple or varying frequencies are required.

This part is ideal for graphics applications. It generates low jitter, high speed pixel clocks. It can be used to replace multiple, expensive high speed crystal oscillators. The flexibility of the device allows it to generate non-standard graphics clocks.

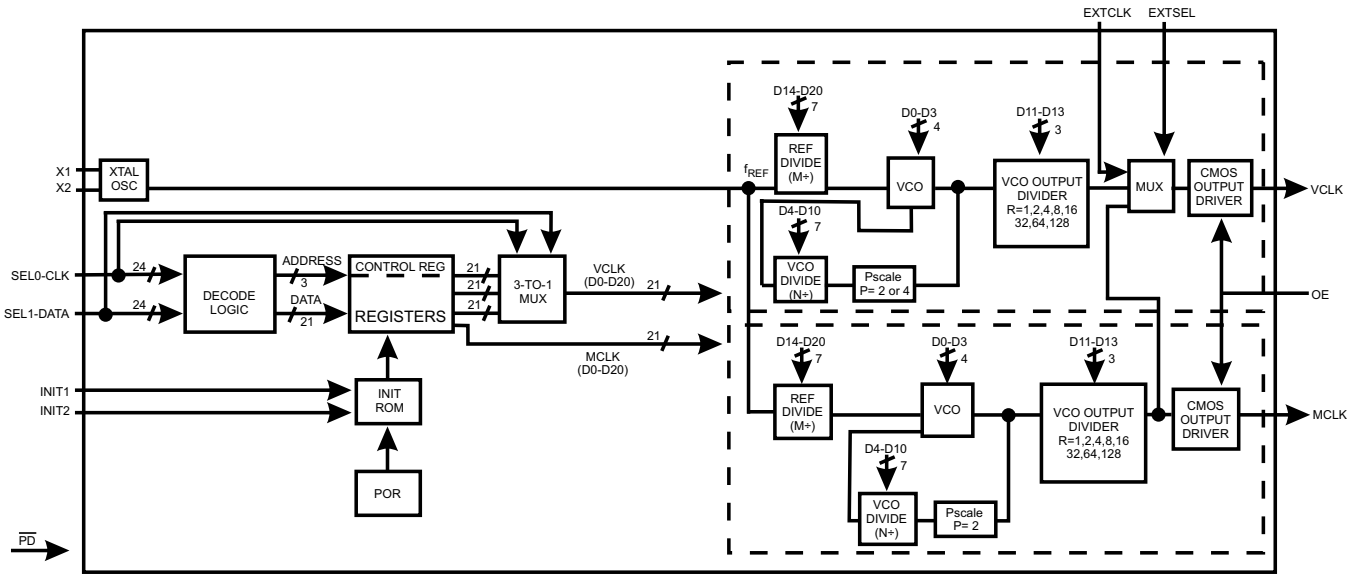
The **ICS9161A** is also ideal in disk drives. It can generate zone clocks for constant density recording schemes. The low profile, 16-pin SOIC or PDIP package and low jitter outputs are especially attractive in board space critical disk drives.

The leader in the area of multiple output clocks on a single chip, ICS has been shipping graphics frequency generators since October, 1990, and is constantly improving the phase-locked loop. The **ICS9161A** incorporates a patented fourth generation PLL that offers the best jitter performance available.

Features

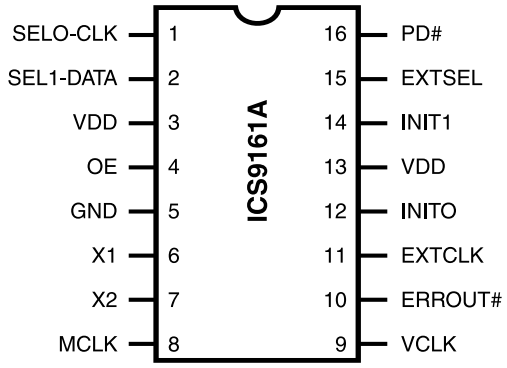
- Pin-for-pin and function compatible with ICD2061A
- Dual programmable graphics clock generator
- Memory and video clocks are individually programmable on-the-fly
- Ideal for designs where multiple or varying frequencies are required
- Increased frequency resolution from optional pre-divide by 2 on the M counter
- Output enable feature available for tristating outputs
- Independent clock outputs range from 390 kHz to 120 MHz for VDD >4.75V
- Power-down capabilities
- Low power, high speed 0.8µ CMOS technology
- Glitch-free transitions
- Available in 16-pin, 300-mil SOIC or PDIP package

Block Diagram



ICS reserves the right to make changes in the device data identified in this publication without further notice. ICS advises its customers to obtain the latest version of all device data to verify that any information being relied upon by the customer is current and accurate.

Pin Configuration



16-Pin 300- mil SOIC or PDIP

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	SEL0-CLK	IN	Clock input in serial programming mode. Clock select pin in operating mode. Has internal pull-down to GND.
2	SEL1-DATA	IN	Data input in serial programming mode. Clock select pin in operating mode. Has internal pull-down to GND.
3	AVDD	PWR	Power.
4	OE	IN	Tristates outputs when low. Has internal pull-up to VDD.
5	GND	PWR	Ground.
6	X1	IN	Crystal input. This input includes XTAL load capacitance and feedback bias for the crystal.
7	X2	OUT	Crystal output which includes internal XTAL load capacitance.
8	MCLK	OUT	Memory clock output.
9	VCLK	OUT	Video clock output.
10	ERROUT#	OUT	Output low signals an error in the serially programmed word.
11	EXTCLK	IN	External clock input. Has internal pull-up to VDD.
12	INIT0	IN	Selects initial power-up conditions, LSB. Has internal pull-down to GND.
13	VDD	PWR	Power.
14	INIT1	IN	Selects initial power-up conditions, MSB. Has internal pull-down to GND.
15	EXTSEL	IN	Selects external clock input (EXTCLK) as VCLK output. Has internal pull-up to VDD.
16	PD#	IN	Power-down pin, active low. Has internal pull-up to VDD.

Register Definitions

The register file consists of the following six registers:

Register Addressing

Address (A2 - A0)	Register	Definition
000	REG0	Video Clock Register 1
001	REG1	Video Clock Register 2
010	REG2	Video Clock Register 3
011	MREG	Memory Register
100	PWRDWN	Divisor for Power-down mode
110	CNTL REG	Control Register

The **ICS9161A** places the three video clock registers and the memory clock register in a known state upon power-up. The registers are initialized based on the state of the INIT1 and INIT0 pins at application of power to the device. The INIT pins must ramp up with VDD if a logical 1 on either pin is required. These input pins are internally pulled down and will default to a logical 0 if left unconnected.

The registers are initialized as follows:

Register Initialization

INIT1	INIT0	MREG	REG0	REG1	REG2
0	0	32.500	25.175	28.322	28.322
0	1	40.000	25.175	28.322	28.322
1	0	50.350	40.000	28.322	28.322
1	1	56.644	40.000	50.350	50.350

Register Selection

When the **ICS9161A** is operating, the video clock output is controlled with a combination of the SEL0, SEL1, PD# and OE pins. The video clock is also multiplexed to an external clock (EXTCLK) which can be selected with the EXTSEL pin. The VCLK Selection Table shows how VCLK is selected.

VCLK Selection

OE	PD#	EXTSEL	SEL1	SEL0	VCLK
0	x	x	x	x	Tristate
1	0	x	x	x	Forced High
1	1	x	0	0	REG0
1	1	x	0	1	REG1
1	1	0	1	0	EXTCLK
1	1	1	1	x	REG2
1	1	x	1	1	REG2

As seen in the VCLK Selection table, OE acts to tristate the output. The PD# pin forces the VCLK signal high while powering down the part. The EXTCLK pin will only be multiplexed in when EXTSEL and SEL0 are logic 0 and SEL1 is a logic 1.

The memory clock outputs are controlled by PD# and OE as follows:

MCLK Selection

OE	PD#	MCLK
0	x	Tristate
1	1	MREG
1	0	PWRDWN

The Clock Select pins SEL0 and SEL1 have two purposes. In serial programming mode, these pins act as the clock and data pins. New data bits come in on SEL1 and these bits are clocked in by a signal on SEL0. While these pins are acquiring new information, the VCLK signal remains unchanged. When SEL0 and SEL1 are acting as register selects, a time-out interval is required to determine whether the user is selecting a new register or wants to program the part. During this initial time-out, the VCLK signal remains at its previous frequency. At the end of this time-out interval, a new register is selected. A second time-out interval is required to allow the VCO to settle to its new value. During this period of time, typically 5ms, the input reference signal is multiplexed to the VCLK signal.

When MCLK or the active VCLK register is being re-programmed, then the reference signal is multiplexed glitch-free to the output during the first time-out interval. A second time-Register out interval is also required to allow the VCO to settle. During this period, the reference signal is multiplexed to the appropriate output signal.

Control Register Definitions

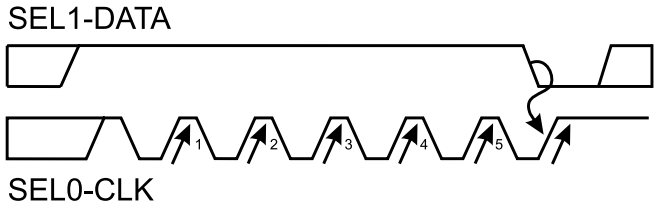
The control register allows the user to adjust various internal options. The register is defined as follows:

Bit	Bit Name	Default Value	Description
21	C5	0	This bit determines which power-down mode the PD# pin will implement. Power-down mode 1, C5=0, forces the MCLK signals to be a function of the power-down register. Power-down mode 2, C5=1, turns off the crystal and disables all outputs.
20	C4	0	This bit determines which clock is multiplexed to VCLK during frequency changes. C4=0 multiplexes the reference frequency to the VCLK output. C4=1 multiplexes MCLK to the VCLK output for applications where the graphics controller cannot run as slow as $f_{REF.}$
19	C3	0	This bit determines the length of the time-out interval. The time-out interval is derived from the MCLK VCO. If this VCO is programmed to certain extremes, the time-out interval may be too short. C3=0, normal time-out. C3=1, doubled time-out interval.
18	C2	0	Reserved, must be set to 0.
17	C1	1	This bit adjusts the duty cycle. C1=0 causes a 1ns decrease in output high time. C1=1 causes no adjustment. If the load capacitance is high, the adjustment can bring the duty cycle closer to 50%.
16	C0	0	Reserved, must be set to 0.
15	NS2	0	Acts on register 2. NS2=0 prescales the N counter by 2. NS2=1 prescales the P counter value to 4.
14	NS1	0	Acts on register 1. NS1=0 prescales the N counter by 2. NS1=1 prescales the P counter value to 4.
13	NS0	0	Acts on register 0. NS1=0 prescales the N counter by 2. NS0=1 prescales the P counter value to 4.

Serial Programming Architecture

The pins SEL0 and SEL1 perform the dual functions of selecting registers and serial programming. In serial programming mode, SEL0 acts as a clock pin while SEL1 acts as the data pin. **The ICS9161A-01** may not be serially programmed when in power-down mode.

In order to program a particular register, an unlocking sequence must occur. The unlocking sequence is detailed in the following timing diagram:



The unlock sequence consists of at least five low-to-high transitions of CLK while data is high, followed immediately by a single low-to-high transition while data is low. Following this unlock sequence, data can be loaded into the serial data register. This programming must include the start bit, shown in Figure 1.

Following any transition of CLK or DATA, the watchdog timer is reset and begins counting. The watchdog timer ensures that successive rising edges of CLK and DATA do not violate the time-out specification of 2ms. If a time-out occurs, the lock mechanism is reset and the data in the serial data register is ignored.

Since the VCLK registers are selected by the SEL0 and SEL1 pins, and since any change in their state may affect the output frequency, new data input on the selection bits is only permitted to pass through the decode logic after the watchdog timer has timed out. This delay of SEL0 or SEL1 data permits a serial program cycle to occur without affecting the current register selection.

Serial Data Register

The serial data is clocked into the serial data register in the order described in Figure 1 below (Serial Data Timing).

The serial data is sent as follows: An individual data bit is sampled on the rising edge of CLK. The complement of the data bit must be sampled on the previous falling edge of CLK. The setup and hold time requirements must be met on both CLK edges. For specifics on timing, see the timing diagrams on pages 10, 11 and 12.

The bits are shifted in this order: a start bit, 21 data bits, 3 address bits (which designate the desired register), and a stop bit. A total of 24 bits must always be loaded into the serial data register or an error is issued. Following the entry of the last data bit, a stop bit or load command is issued by bringing DATA high and toggling CLK high-to-low and low-to-high. The unlocking mechanism then resets itself following the load. Only after a time-out period are the SEL0 and SEL1 pins allowed to return to a register selection function.

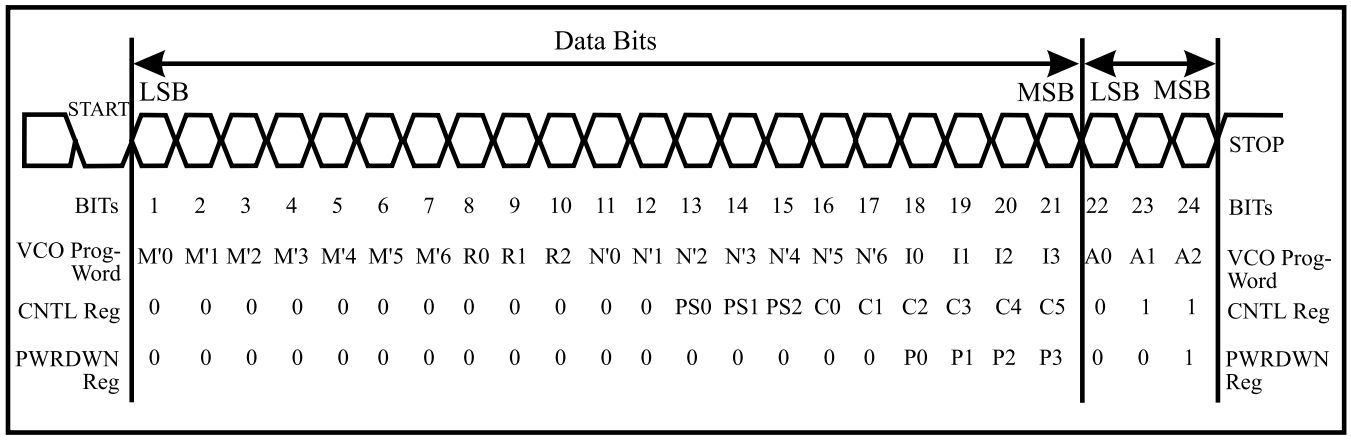


Figure 1: Serial Data Timing

The serial data register is exactly 24 bits long, enough to accept the data being sent. The stop bit acts as a load command that passes the contents of the Serial Data Register into the register indicated by the three address bits. If a stop bit is not received after the serial register is full, and more data is sent, all data in the register is ignored and an error issued. If correct data is received, then the unlocking mechanism re-arms, all data in the serial data register is ignored, and an error is issued.

ERROUT# Operation

Any error in programming the **ICS9161A** is signaled by ERROUT#. When the pin goes low, an error has been detected. It stays low until the next unlock sequence. The signal is invoked for any of the following errors: incorrect start bit, incorrect data encoding, incorrect length of data word, and incorrect stop bit.

Programming the ICS9161A

The **ICS9161A** has a wide operating range, but it is recommended that it is operated within the following limits:

$3.15V < V_{DD} < 5.25V$	V_{DD} supply voltage
$1\ MHz < F_{REF} < 60\ MHz$	F_{REF}=Input Reference Frequency
$200\ kHz < F_{REF/M} < 5\ MHz$	M=Reference divide 3 to 129
$50\ MHz < F_{VCO} < 120\ MHz$	F_{VCO}=VCO output frequency
$F_{CLK} \leq 120\ MHz$	F_{CLK}=output frequency

The frequency of the programmable oscillator FVCO is determined by the following fields:

Field	# of Bits
Index (I)	4
N counter value (N')	7
Mux (R)	3
M counter value (M')	7

Where the least significant bit is the last bit of M and the most significant bit is the first bit of I.

The equations used to determine the oscillator frequency are:

$N=N' + 3\ M=M' + 2$
$F_{VCO}=Prescale \bullet N/M \bullet F_{REF}$
where $3 \leq M \leq 129$ and $4 \leq N \leq 130$
and prescale=2 or 4, as set in the control register
(Where N is the VCO divider & M is the reference divider)

The value of F_{VCO} must remain between 50 MHz and 120 MHz. As a result, for output frequencies below 50 MHz, F_{VCO} must be brought into range. To achieve this, an output divisor is selected by setting the values of the Mux Field (R) as follows:

Output Divisor

R	Divisor
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

Unlike the ICD2061A, the **ICS9161A'**s VCO does not require tuning to place it in certain ranges. The **ICS9161A**'s VCO will operate from 50 MHz to 120 MHz without adjusting the VCO gain. However, to maintain compatibility, the I bits are programmed as in the ICD2061A.

These bits are dummy bits except for the following two cases:

Index Field (I)

I	VCLK F_{VCO}	MCLK F_{VCO}
1110	Turn off VCLK	50 - 120 MHz
1111	Mux MCLK to VLCK	50 - 120 MHz

When the index field is set to 1111, VCLK is turned off and both channels run from the same MCLK VCO. This is done in an effort to reduce jitter, which may increase when VCOs run at 2^n multiples of one another. If the two outputs have to be multiples of one another, it is best to mux MCLK over to the output of the VCLK VCO and to power-down the VCLK VCO. The multiplexed frequency will be divided down by the correct divisor (M) and output on VCLK.

Power Management Issues

Power-down mode 1

The **ICS9161A** contains a mechanism to reduce the quiescent power when stand-by operation is desired. Power-down mode 1 is invoked by polling PD# low and having the proper CNTL register bit set to zero. In this mode, VCOs are shut down, the VCLK output is forced high, and the MCLK output is set to a user-defined low frequency value to refresh dynamic RAM.

The power-down MCLK value is determined by the following equation:

$$MCLK_{PD} = F_{REF}/(\text{PWRDWN register divisor value})$$

The power-down register divisor is determined according to the 4-bit word programmed into the PWRDWN register (see table below).

Power-down mode 2

When there is no need for any output during power-down, an alternate mode is available which will completely shut down all outputs and the reference oscillator, but still preserves all register contents. Power-down mode 2 in invoked by first programming the power-down bit in the CNTL register and then pulling the PD# pin low.

The PD# pin

The PD# pin has a standard internal pull-up resistor during normal operation. When the chip goes into power-down mode 1 or 2, the normal pull-up resistor is dynamically switched to a weak pull-up, which reduces power consumption. If the PD# pin is allowed to float after it has been pulled down, the weak pull-up will bring the signal high and allow the device to resume operation.

Power-Down Register Table

PWRDWN bits				PWRDWN	Power-down	MCLKPD
P3	P2	P1	P0	Register Value	Divisor	(f_{REF}=14.31818)
0	0	0	0	0	n/a	n/a
0	0	0	1	1	32	447.4 kHz
0	0	1	0	2	30	477.3 kHz
0	0	1	1	3	28	511.4 kHz
0	1	0	0	4	26	550.7 kHz
0	1	0	1	5	24	596.6 kHz
0	1	1	0	6	22	650.8 kHz
0	1	1	1	7	20	715.9 kHz
1	0	0	0	8 (default)	18	795.5 kHz
1	0	0	1	9	16	894.9 kHz
1	0	1	0	A	14	1.02 MHz
1	0	1	1	B	12	1.19 MHz
1	1	0	0	C	10	1.43 MHz
1	1	0	1	D	8	1.79 MHz
1	1	1	0	E	6	2.39 MHz
1	1	1	1	F	4	3.58 MHz

Absolute Maximum Ratings

VDD referenced to GND 7V
Operating temperature under bias (T_{OPER}) ..... 0°C to 70°C
Storage temperature ..... -40°C to +150°C
Max. soldering temperature (10 sec) (T_{SOL}) ..... +260°C
Voltage on I/O pins referenced to GND ..... GND -0.5V to VDD +0.5V
Junction temperature (T_j) ..... +125°C
Power dissipation ..... 0.35 Watts

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics at 5.0V

V_{DD} = +5V ± 5%, 0°C ≤ $T_{AMBIENT}$ ≤ +70°C

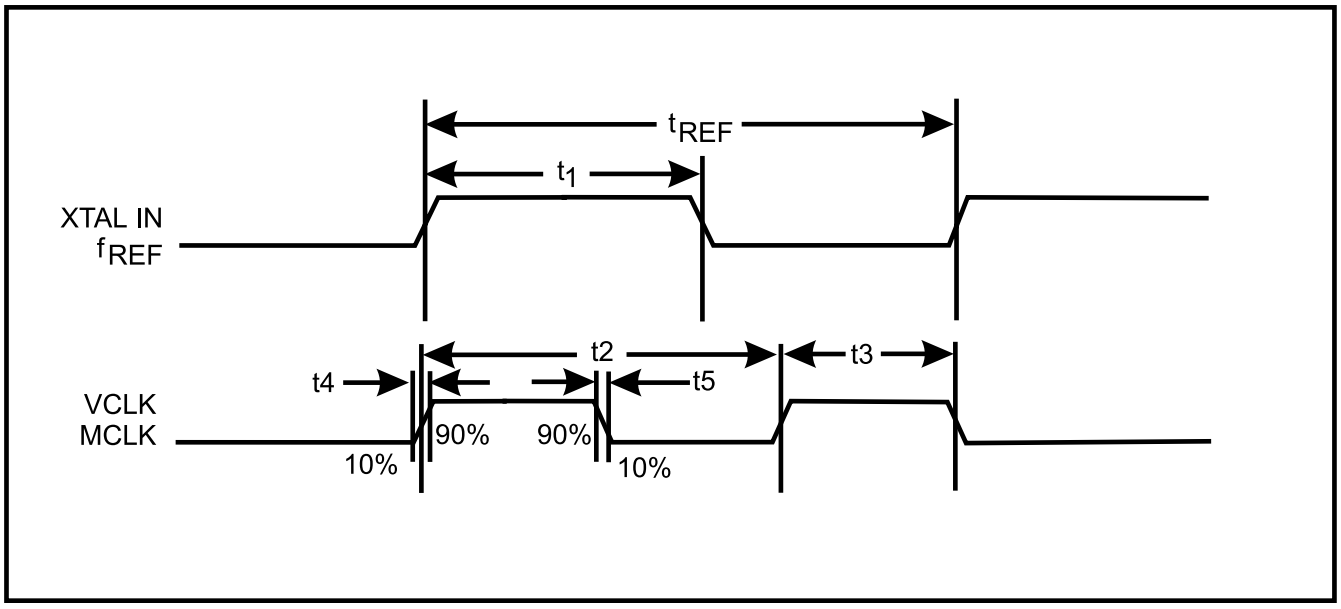
DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
High level input voltage	V_{IH}		2.0	-	-	V
Low level input voltage	V_{IL}		-	-	0.8	V
High level CMOS output voltage[1]	V_{OH}	I_{OH}=-4mA	3.84	-	-	V
Low level output voltage[1]	V_{OL}	I_{OL}=4mA	-	-	0.4	V
Input high current	I_{IH}	V_{DD}=V_{IH}=5.25V for pull-downs	-	-	100	µA
Input low current	I_{IL}	V_{IL}=0V for pull-ups	-250	-	-	µA
Output leakage current	I_{OZ}	(tristate)	-10	-	10	µA
Power supply current	I_{DD}		15	-	65	mA
Power supply current (typical)	I_{DD-TYP}	@60 MHz	-	35	-	mA
Analog power supply current	I_{ADD}		-	-	20	mA
Power-down current (Mode 1)	I_{PD1}		-	6	7.5	mA
Power-down current (Mode 2)	I_{PD2}		-	25	50	µA
Input capacitance[1]	C_{IN}		-	-	10	pF

Note
1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

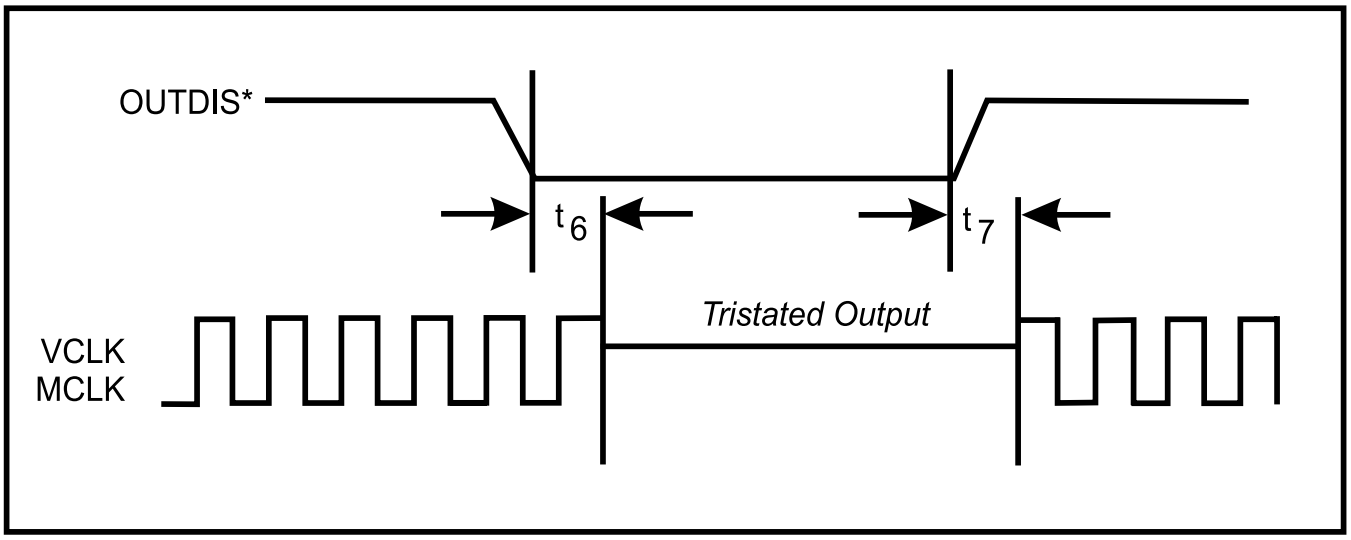
Electrical Characteristics at 5.0V (continued)

AC Characteristics						
DESCRIPTION	NAME	SYMBOL	MIN	TYP	MAX	UNITS
Reference oscillator value[2]	Reference frequency	f_{REF}	1	14.31818	60	MHz
$1/f_{REF}$	Reference period	t_{REF}	16.6	69.8408	1000	ns
Duty cycle for the input oscillator defined as t_1/t_{REF}	Input duty cycle	t_1	25%	-	75%	-
Output oscillator values	Output clock periods	t_2	8.33 (120 MHz)	-	2564 (390 kHz)	ns
Duty cycle for the output oscillators[3]	Output duty cycle	t_3	45%	-	55%	-
Rise time for the output oscillators into a 25pF load	Rise times	t_4	-	-	3	ns
Fall time for the output oscillators into a 25pF load	Fall times	t_5	-	-	3	ns
Old frequency output	freq1 output	t_{freq1}	-	-	-	-
New frequency output	freq2 output	t_{freq2}	-	-	-	-
Time clock output remains high while output muxes to reference frequency	f_{REF} mux time	t_A	0.5 t_{REF}	-	1.5t_{REF}	ns
Interval for serial programming and for VCO changes to settle[4]	Time-out interval	$t_{time-out}$	2	5	10	ms
Time clock output remains high while output muxes to new frequency value	t_{freq2}muxtime	t_B	0.5 t_{REF}	1.5 t_{REF}	-	ns
Time for the output oscillators to go into tristate mode after OUTDIS-signal assertion	Tristate	t_6	-	25	-	ns
Time for the output oscillators to recover from tristate mode after OUTDIS-signal goes high	CLK valid	t_7	-	12	-	ns
Time for power-down mode of operation to take effect	Power-down	t_8	-	25	-	ns
Time for recovery from power-down mode to a valid CLK	Power-up	t_9	-	12	-	ns
Time for MCLK to go high after PWRDWN is asserted high	MCLKOUT high	t_{10}	0	-	t_{PWRDWN}	ns
Delay of MCLK prior to f_{MCLK} signal at output	MCLKOUT delay	t_{11}	0.5 t_{MCLK}	-	1.5 t_{MCLK}	ns
Clock period of serial clock		t_{serclk}	2 • t_{REF}	-	2	ms
Set-up time		t_{SU}	20	-	-	ns
Hold time		t_{HD}	10	-	-	ns
Load command		t_{ldcmd}	0	-	t_1+30	ns

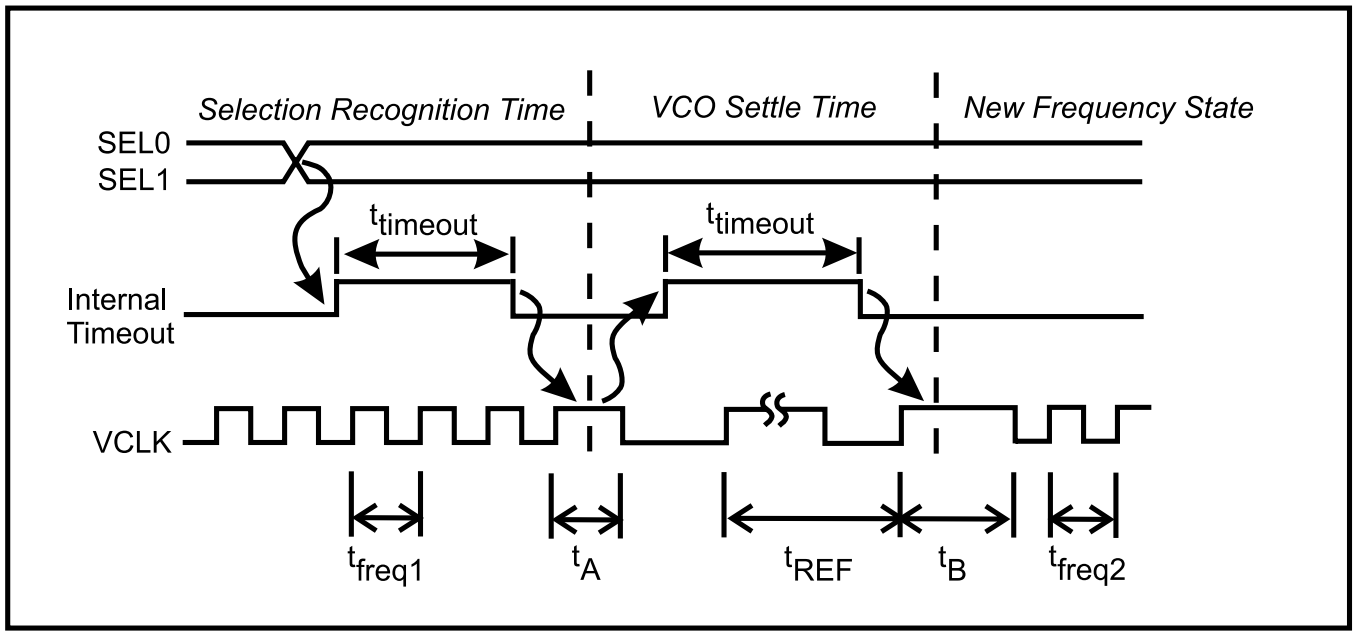
Notes:
1. Parameter guaranteed by design and characterization. Not 100% tested in production.
2. For reference frequencies other than 14.81818 MHz, the pre-loaded ROM frequencies will shift proportionally.
3. Duty cycle is measured at CMOS threshold levels. At 5 volts, V_{TH}=2.5 volts.
4. If the interval is too short, see the time-out interval section in the control register definition.



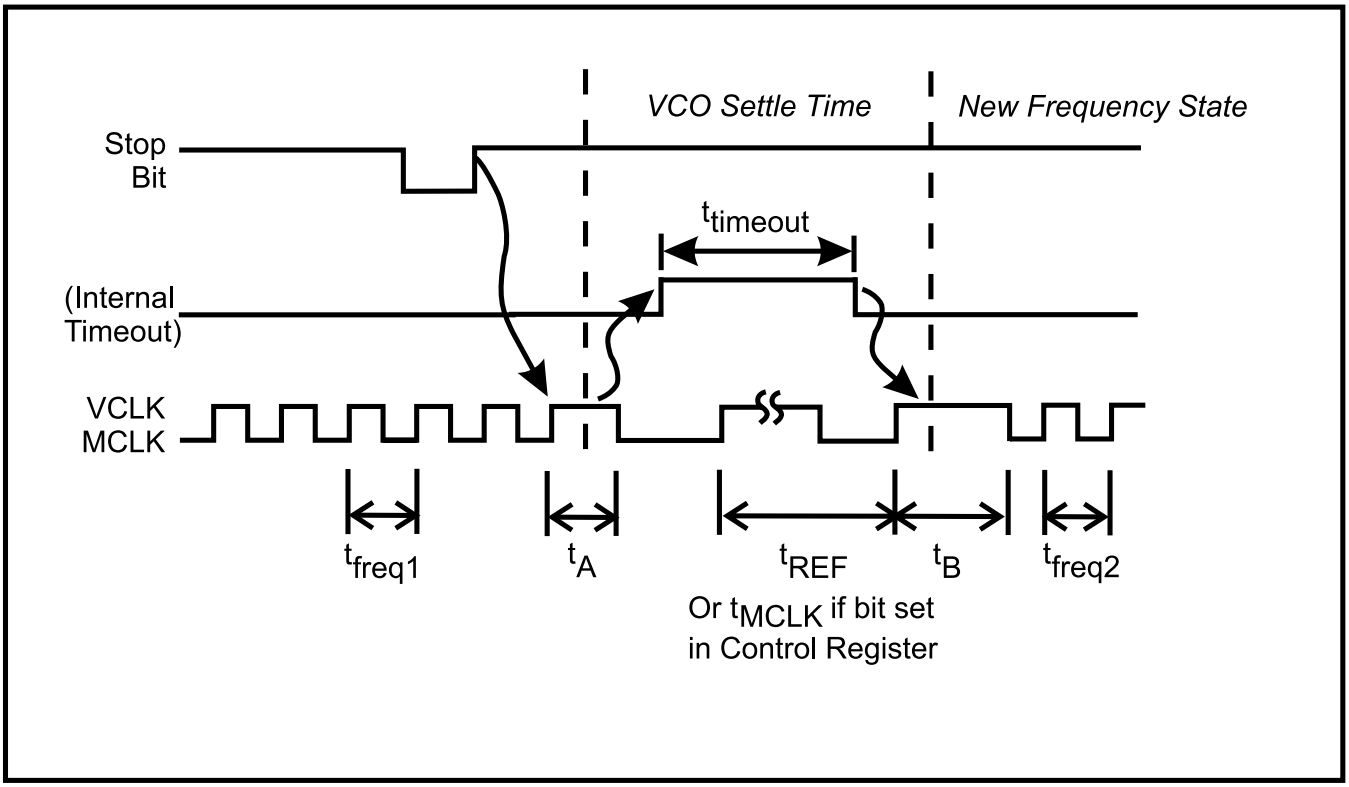
Rise and Fall Times



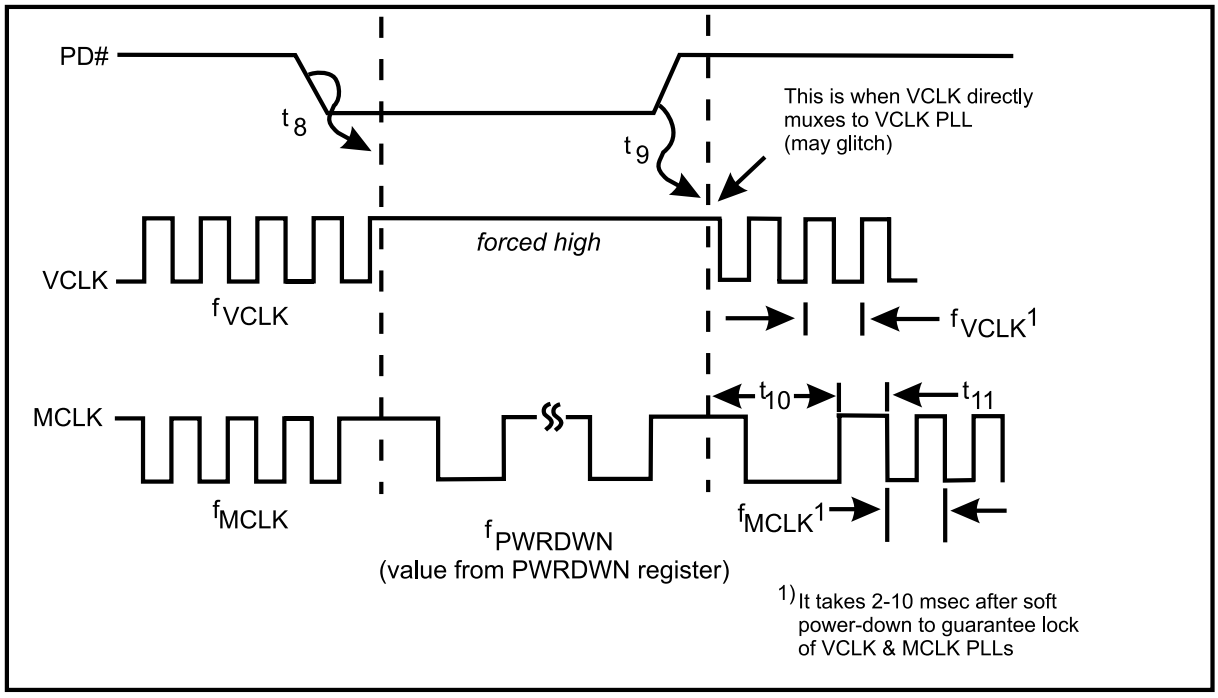
Tristated Timing



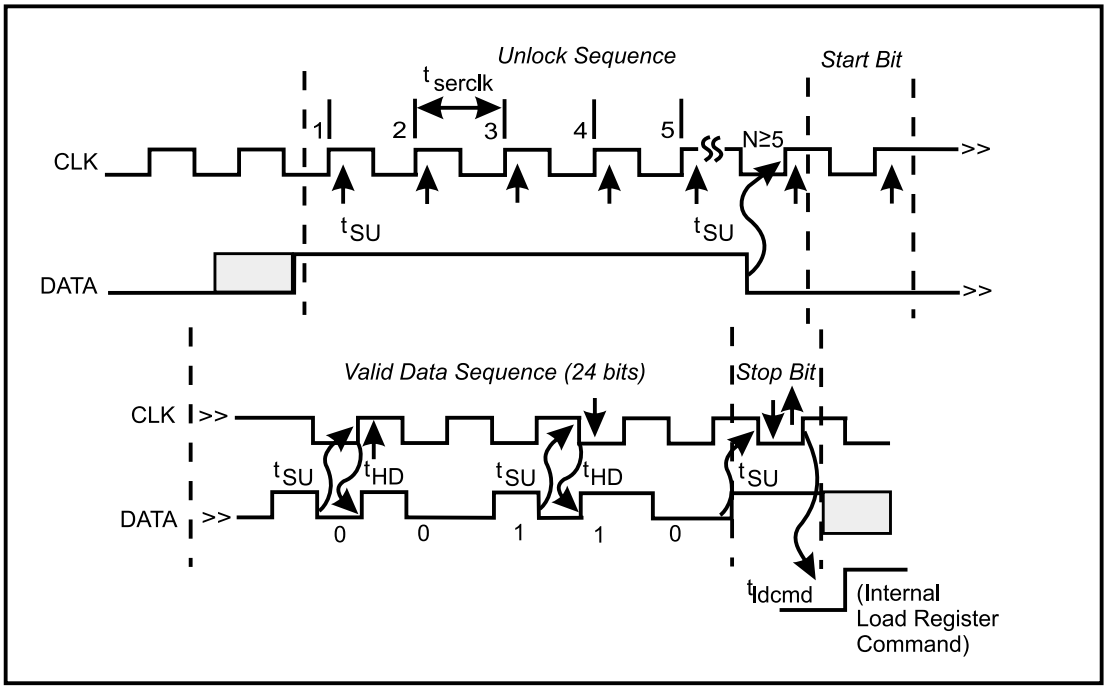
Selection Timing



MCLK and Active VCLK Register Programming Timing



Soft Power-Down Timing (Mode 2)



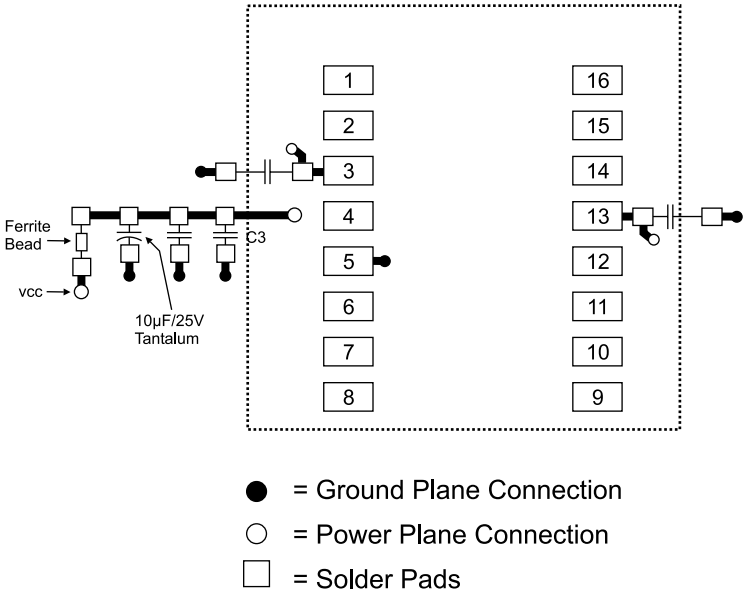
Serial Programming Timing

General Layout Precautions:

1) Use a ground plane on the top layer of the PCB in all areas not used by traces.
2) Make all power traces and vias as wide as possible to lower inductance.

Notes:

1) All clock outputs should have series terminating resistor. Not shown in all places to improve readibility of diagram.
2) 47 ohm / 56pf RC termination should be used on all over 50MHz outputs.
3) Optional crystal load capacitors are recommended.



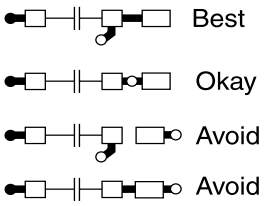
Capacitor Values:

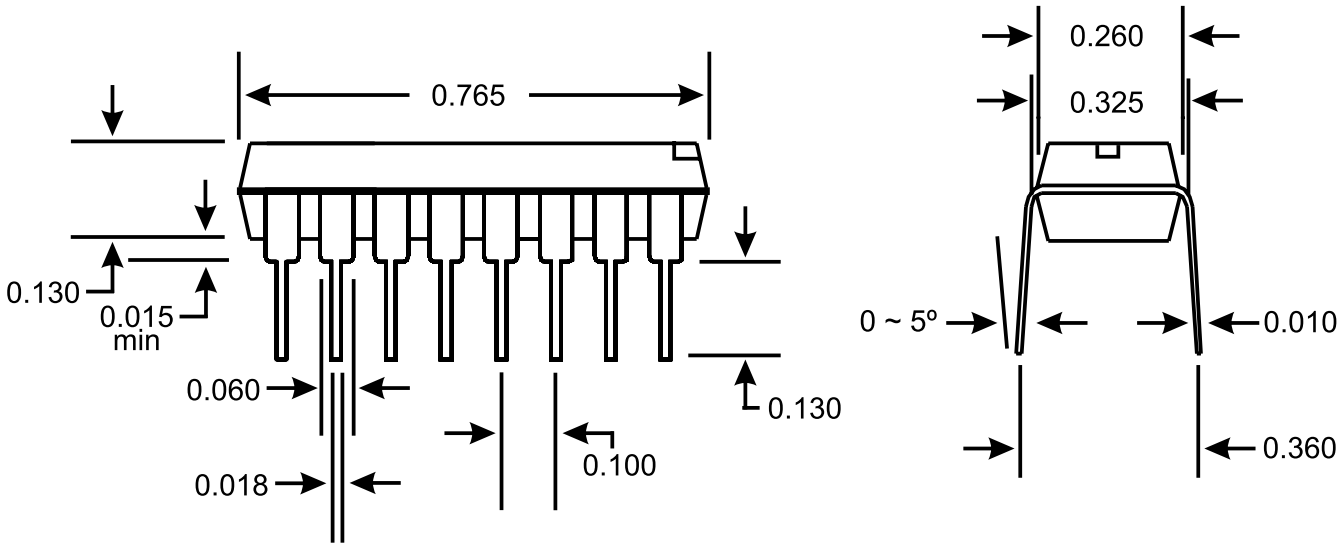
C1, C2 : Crystal load values determined by user

C3 : 100pF ceramic

All unmarked capacitors are 0.01µF ceramic

Connections to VDD:





16-Pin PDIP Package

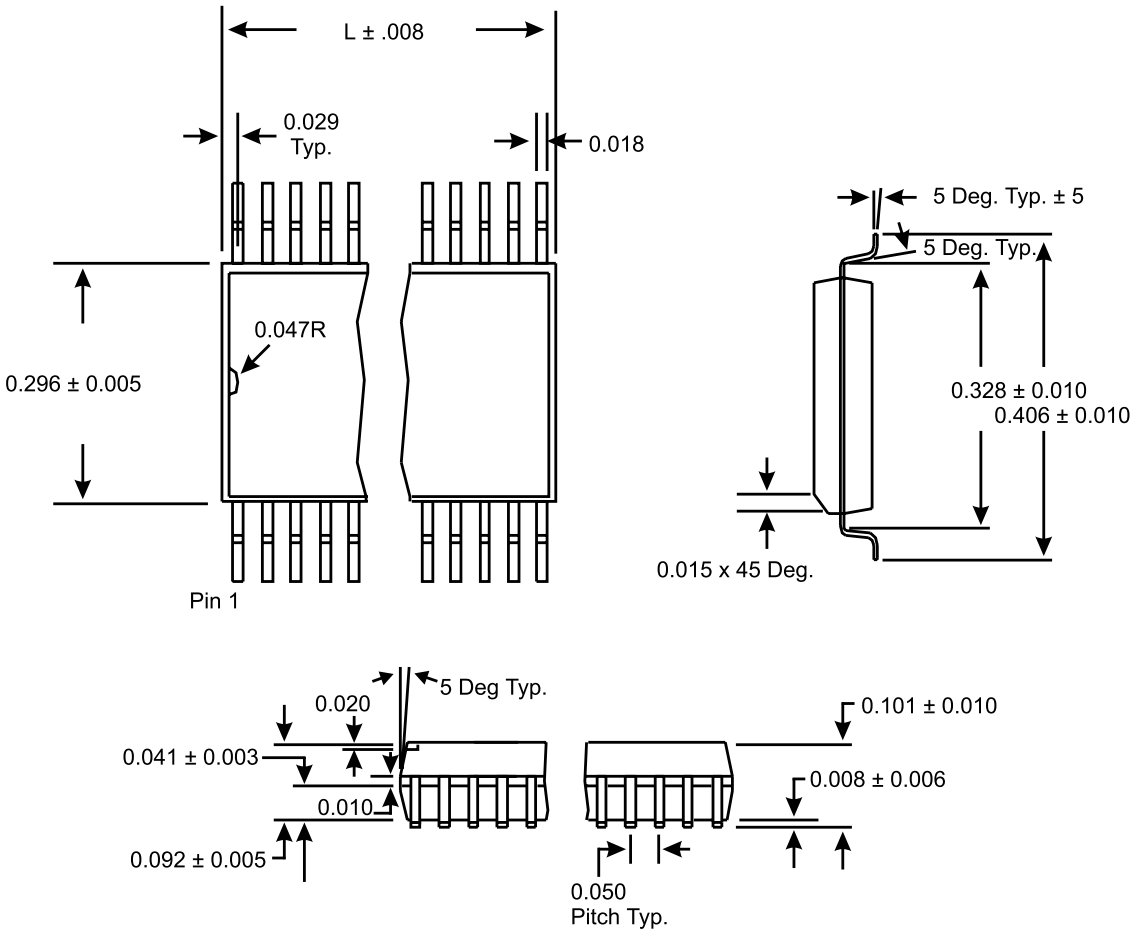
Ordering Information

ICS9161A-01CN16

Example:

ICS XXXX- PPP M X#W

- **Lead Count & Package Width**
  Lead Count=1, 2 or 3 digits
  W=.3" SOIC or .6" DIP; None=Standard Width
- **Package Type**
  N=DIP (Plastic)
- **Pattern Number (2 or 3 digit number for parts with ROM code patterns, if applicable)**
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV=Standard Device



LEAD COUNT	16L
DIMENSION L	0.404

SOIC Package (wide body)

Ordering Information

ICS9161A-01CW16

Example:

ICS XXXX- PPP M X#W

Lead Count & Package Width
Lead Count=1, 2 or 3 digits
W=.3" SOIC or .6" DIP; None=Standard Width

Package Type
W=SOIC

Pattern Number (2 or 3 digit number for parts with ROM code patterns, if applicable)

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV = Standard Device

ICS reserves the right to make changes in the device data identified in this publication without further notice. ICS advises its customers to obtain the latest version of all device data to verify that any information being relied upon by the customer is current and accurate.