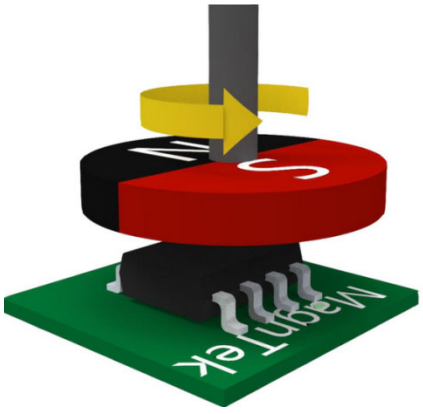
MT6501

Magnetic Angle Position Sensor

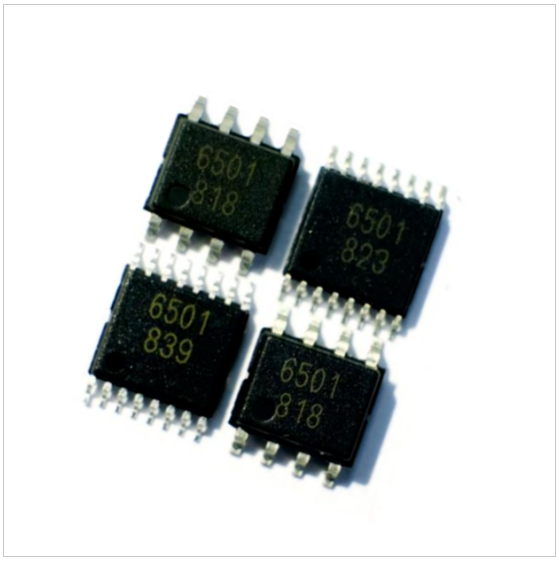
Features and Benefits

- Based on advanced AMR Sensing Technology with 0°~360° Full Range Angle Sensing
- Contactless Angle Measurement
- Programmable Measurement Range
- Programmable Linear Transfer Characteristic
- Selectable Analog (Ratio metric), PWM (Pulse Width Modulation) or Switch Output (SWO)
- 12bit DAC/PWM Resolution
- 1-Wire Program Interface
- 3-Wire SPI Interface
- Over-Voltage and Over-Current Protection
- Single Channel SOP-8 and Dual Channel (Redundant) TSSOP-16 RoHS Compliant 2011/65/EU



Applications

- Absolute Linear Position Sensor
- Steering Wheel Position Sensor
- Steering Angle Sensor for EPS
- Pedal Position Sensor
- Throttle Position Sensor
- Contactless Potentiometer



General Description

The MagnTek rotary position sensor MT6501 is an IC based on advanced AMR magnetic sensing technology. The sensor contains two Wheatstone bridges formed by a magnet field sensing element array. A rotating magnetic field in the x-y sensor plane delivers two sinusoidal output signals indicating the angle (α) between the sensor and the magnetic field direction. Within a homogeneous field in the x-y plane, the output signals are relatively independent of the physical placement in the z direction (air gap).

The sensor is only sensitive to the magnetic field direction as the sensing element output is specially designed to be independent from the magnet field strength. This allows the device to be less sensitive to magnet variations, stray magnetic fields, air gap changes and off-axis misalignment.

This contactless system measures the absolute angle of a diametrically magnetized on-axis magnet. It is especially suitable for applications such as contactless potentiometer, steering angle sensor and etc.

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1. 1 SOP-8 Package

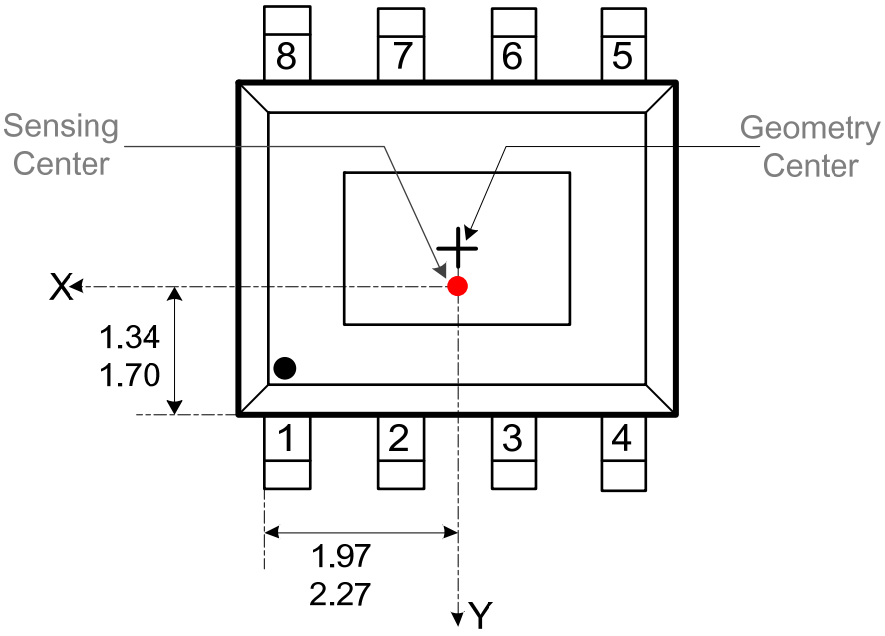


Figure 1: Pin Configuration for SOP-8 Package

Pin List

Name	Number	Type	Description
VDD	1	Supply	5V Supply
CSN/T0	2	Digital I/O	Chip Select for SPI or Test0
SWO/T1	3	Digital I/O	Switch Output or Test1
SCK	4	Digital Input	SPI Clock
OUT	5	Analog Output	Analog Output, PWM Output, OWI I/O
SDAT/T2	6	Digital I/O	SPI Data or Test2
T3	7	Digital I/O	Test3
VSS	8	Ground	Ground

Family Members

Part Number	Description
MT6501CT-ADD	SOP-8 package, tube pack (100pcs/tube) or tape & reel pack (3000pcs/reel)

1. 2 TSSOP-16 Package

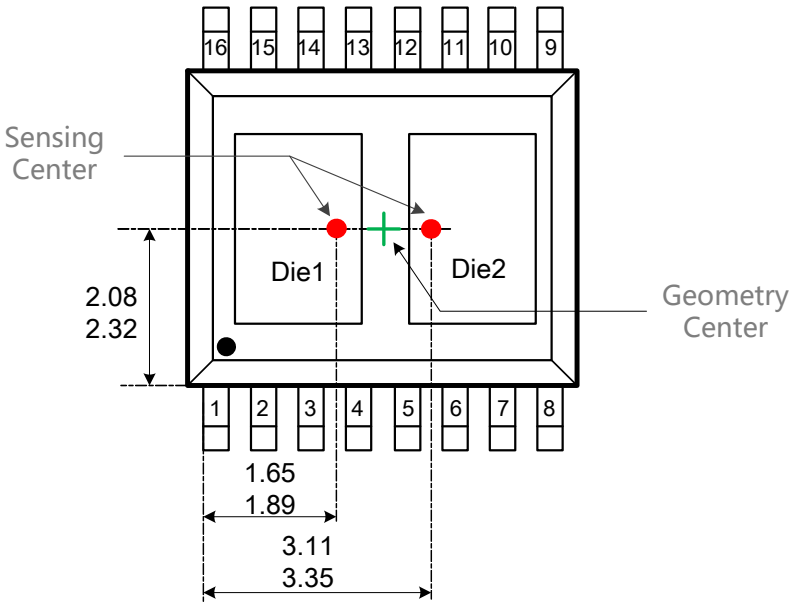


Figure 2: Pin Configuration for TSSOP-16 Package

Pin List

Name	Number	Type	Description
T3_1	1	Digital I/O	Die1 Test3
VSS_1	2	Ground	Die1 Ground
VDD_1	3	Supply	Die1 5V Supply
CSN_1/T0_1	4	Digital I/O	Die1 SPI Enable or Test0
SWO_2/T1_2	5	Digital I/O	Die2 Switch Output or Test1
OUT_2	6	Analog Output	Die2 Analog or PWM Output, OWI I/O
SCK_2	7	Digital Input	Die2 SPI Clock
SDAT_2/T2_2	8	Digital I/O	Die2 SPI Data or Test2
T3_2	9	Digital I/O	Die2 Test3
VSS_2	10	Ground	Die2 Ground
VDD_2	11	Supply	Die2 5V Supply
CSN_2/T0_2	12	Digital I/O	Die2 SPI Enable or Test0
SWO_1/T1_1	13	Digital I/O	Die1 Switch Output or Test1
SCK_1	14	Digital Input	Die1 SPI Clock
OUT_1	15	Analog Output	Die1 Analog or PWM Output, OWI I/O
SDAT_1/T2_1	16	Digital I/O	Die1 SPI Data or Test2

Family Members

Part Number	Description
MT6501GT-ADD	TSSOP-16 package, tube pack (100pcs/tube) or tape & reel pack (3000pcs/reel)

2. Functional Description

The MT6501 is manufactured in a CMOS standard process and uses advanced AMR magnet sensing technology to sense the magnetic field distribution across the surface of the chip. The integrated magnetic sensing element array delivers a voltage representation of the magnetic field at the surface of the IC. Figure 3 shows a simplified block diagram of the chip, consisting of the magnetic sensing element realized by two interleaved Wheatstone bridges to generate cosine and sine signals, gain stages, analog-to-digital converters (ADC) for signal conditioning, a digital signal processing (DSP) unit for angle calculation and digital-to-analog convert (DAC) to generate linear voltage output. Other supporting blocks such as LDO, NVM and etc. are also included.

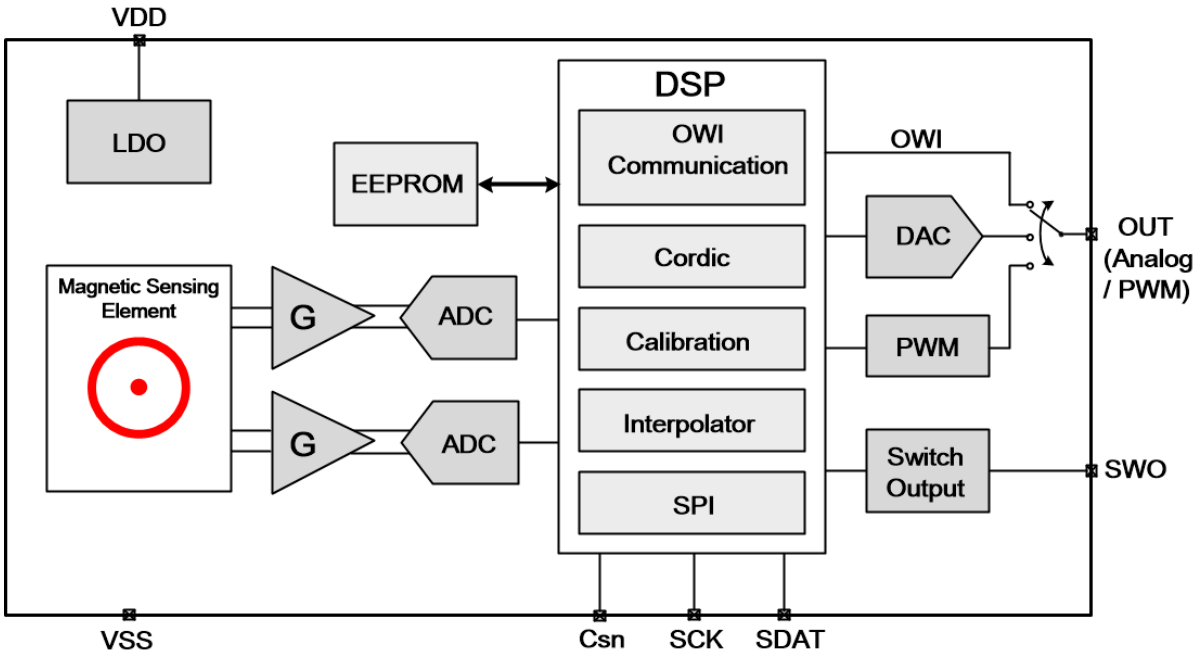


Figure 3: Block Diagram

3. Absolute Maximum Ratings (Non-Operating)

Name	Notes	Min.	Max.	Unit
DC Voltage at Pin VDD	-	-30	30	V
DC Voltage at Pin Out	-0.3		18	V
Output Current	-50		30	mA
Storage Temperature	-	-40	150	℃
Magnetic Flux Density	-		±1	T
Electrostatic Discharge (HBM)	-		±3.5	KV

4. Electrical Characteristics

Operation conditions: Ta=-40 to 150℃, VDD=4.5~5.5V unless otherwise noted.

Symbol	Parameter	Conditions/Notes	Min.	Typ.	Max.	Unit
VDD	Supply Voltage	-	4.5	5.0	5.5	V
IDD	Supply Current	Single Die (SOP-8)	-	6	9	mA
		Dual Die (TSSOP-16)	-	12	18	mA
Timing Specification						
ΔFS	Clock Frequency Variation	Over all VDD and Ta	-10	-	10	%
FR	Analog Output Refresh Rate	Slow Mode	-	4	-	KHz
		Fast Mode	-	8	-	
FPWM	PWM Frequency (Programmable)	-40~150℃	-8%	122 /244 /488 /976	+8%	Hz
TSTEP	Step Response Time (Exclude Slew Rate Effect)	Slow Mode, Filter=Max.	-	-	1400	us
		Slow Mode, Filter=Min.	-	-	1000	
		Fast Mode, Filter=Min.	-	-	600	
TSU	Start-up Cycle (Exclude Slew Rate Effect)	Slow Mode	-	-	15	ms
		Fast Mode	-	-	10	
Analog Output Specification						
IOUT	Output Current	Analog Output Mode	-15	-	15	mA
ISHORT	Output Short Current	Vout=0V	-	-	25	mA
		Vout=VDD	-	-	25	
RL	Output Load	Pull-down to Ground	5	-	-	KΩ
		Pull-up to VDD	1	-	-	
VSAT_LO	Analog Output Low Saturation Level	Pull-up RL≥1KΩ	-	2	4	%VDD
VSAT_HI	Analog Output High Saturation Level	Pull-down RL≥5KΩ	95	97	-	%VDD
CLAMP_LO	Output Clamp Low Level	Programmable	2	-	-	%VDD
CLAMP_HIGH	Output Clamp High Level	Programmable	-	-	98	%VDD
SR	Analog Output Slew Rate	CL≤10nF	-	500	-	V/ms
		CL≤100nF	-	100	-	
Digital Output Specification						
PWM_VOL	PWM Output Low Level	Open-drain (Iout=10mA)	-	-	7	%VDD
GPIO_VOL	GPIO Output Low Level	Push-pull (Iout=5mA)	-	-	5	%VDD
GPIO_VOH	GPIO Output High Level	Push-pull (Iout=5mA)	90	-	-	%VDD

Symbol	Parameter	Conditions/Notes	Min.	Typ.	Max.	Unit
TRISE	Digital Output Rising Time	Push-pull (R_L=10KΩ, C_L=10nF)	-	3.0	-	us
TFALL	Digital Output Falling Time	Push-pull (R_L=10KΩ, C_L=10nF)	-	1.8	-	us
Accuracy Specification						
INL	Integral Non-Linearity	Typical, See Figure 4	-1	-	1	Deg.
INL_TD	Integral Non-Linearity Temperature Drift	Full Temperature Range	-0.5	-	0.5	Deg.
ANG_NOI	Input-referred Noise (Excluding DAC Noise)	Slow Mode, Filter=Min.	-	0.01	0.02	Deg.-rms
ERM	Radiometric Error of Analog Output	Note [1]	-0.1	-	0.1	%VDD
DAC_RES	DAC Resolution	-	-	12	-	Bit
DAC_FS	DAC Full Scale	-	99	-	-	%VDD
DAC_FS_TD	DAC Full Scale Temperature Drift	Full Temperature Range	-0.3	-	0.3	%VDD
DAC_OS	DAC Output Offset	-	-0.5	-	0.5	%VDD
DAC_OS_TD	DAC Output Offset Temperature Drift	Full Temperature Range	-0.25	-	0.25	%VDD
DAC_NOI	DAC Output Noise (RMS)		-	-	0.03	%VDD

Note [1]: The analog output is by design ratiometric, i.e. it is proportional to the supply voltage VDD. The ratiometric error is calculated as follows.

$$\mathrm{ERM} = [\frac{Vout(V_{DD})}{V_{DD}} - \frac{Vout(5\mathrm{V})}{5V}] \cdot 100\%$$

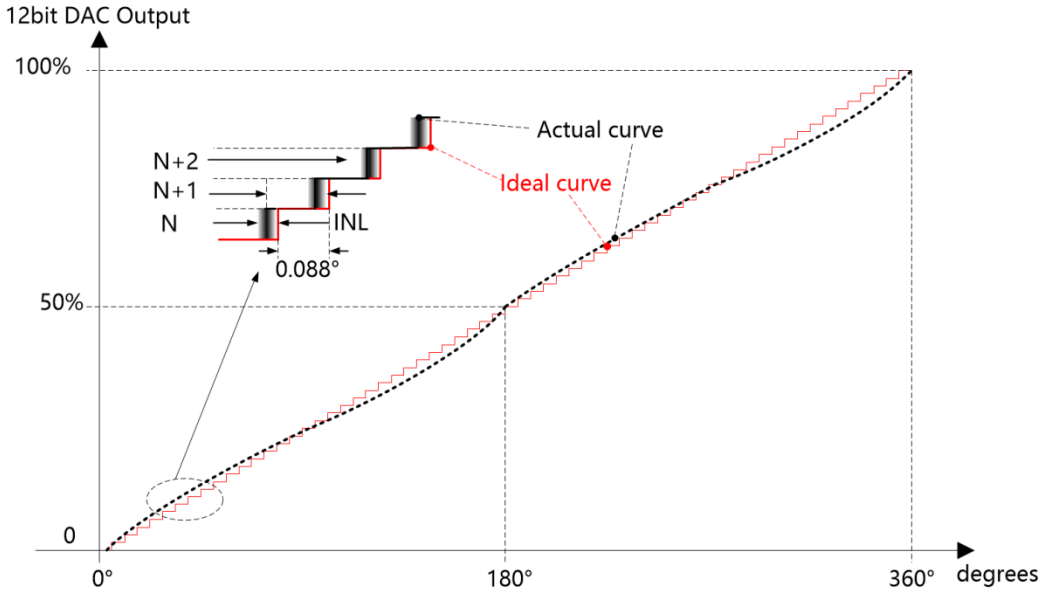


Figure 4: Drawing illustrating of INL

5. Magnetic Input Specifications

Operation conditions: Ta=-40 to 150℃, VDD=4.5~5.5V unless otherwise noted, two-pole cylindrical diametrically magnetized source.

Symbol	Parameter	Conditions/Notes	Min.	Typ.	Max.	Unit
Dmag	Diameter of Magnet	Recommended magnet: Ø8mm x 2.5mm for cylindrical magnets	-	8.0	-	mm
Tmag	Thickness of Magnet		-	2.5	-	mm
Bpk	Magnetic Input Field Amplitude	Measure at the IC surface	300	-	10000	Guass
AG	Air Gap	Magnetic to IC surface distance	-	-	3.0	mm
RS	Rotation Speed		-	-	300	RPM
TCmag1	Recommended magnet material and temperature drift coefficient	NdFeB (Neodymium Iron Boron)	-	-0.12	-	%/℃
TCmag2		SmCo (Samarium Cobalt)	-	-0.035	-	

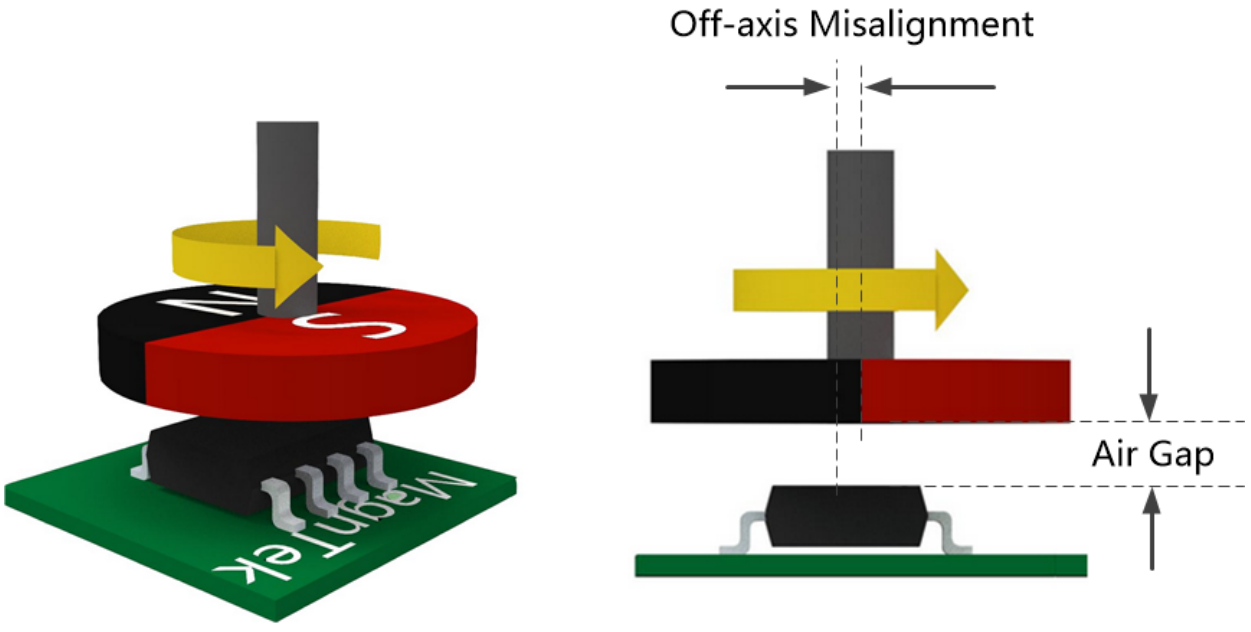


Figure 5: Magnet Arrangement

6. Description of End-User Programmable Items

6.1 Output Mode

The output of MT6501 is defined by the 'Output Mode' and 'Switch Output Enable' parameter.

Output @Pin.5 of SOP-8 Package (Pin.6 & Pin.16 of TSSOP-16 Package)

Parameter	Value	Description
Output Mode	0	Analog Output with C_{LMAX}=330nf
	1	PWM Open-drain Output (NMOS)

Output @Pin.3 of SOP-8 Package (Pin.5 & Pin.13 of TSSOP-16 Package)

Parameter	Value	Description
Switch Output Enable	0	Switch Output Mode Disabled
	1	Switch Output Mode Enabled

6.1.1 Analog Output Mode

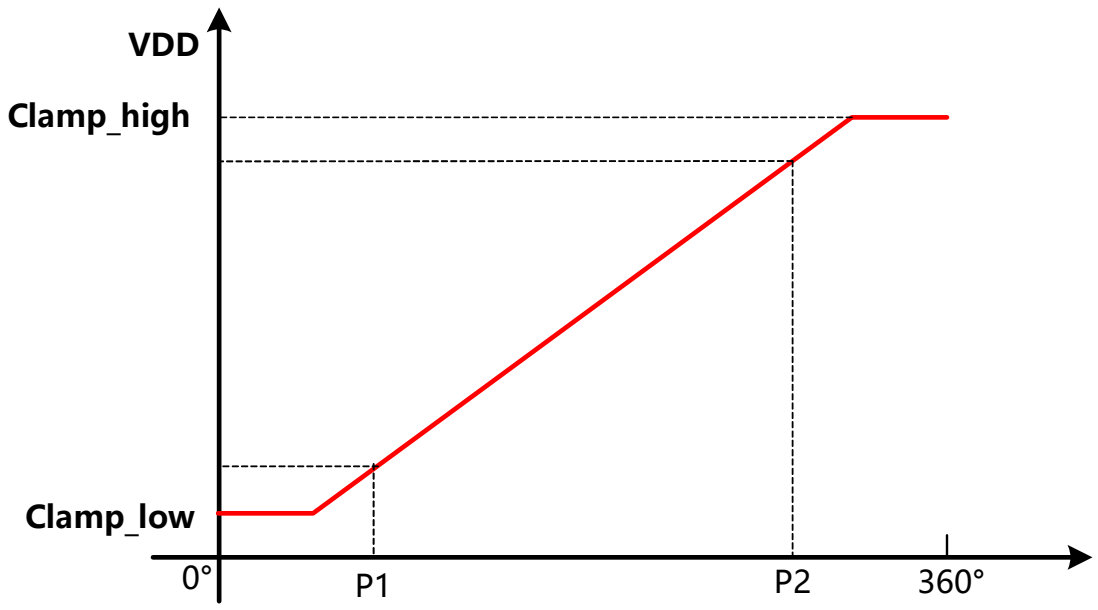


Figure 6: Analog Output

6.1.2 PWM Output Mode

When PWM mode is enabled, the output signal is a digital signal with Pulse-Width-Modulation as shown in Figure 7. PWM is an NMOS open-drain output, so an external pull up resistor (1KΩ~5KΩ) is necessary. The PWM signal has the resolution of 12 bit and with programmable frequency and polarity.

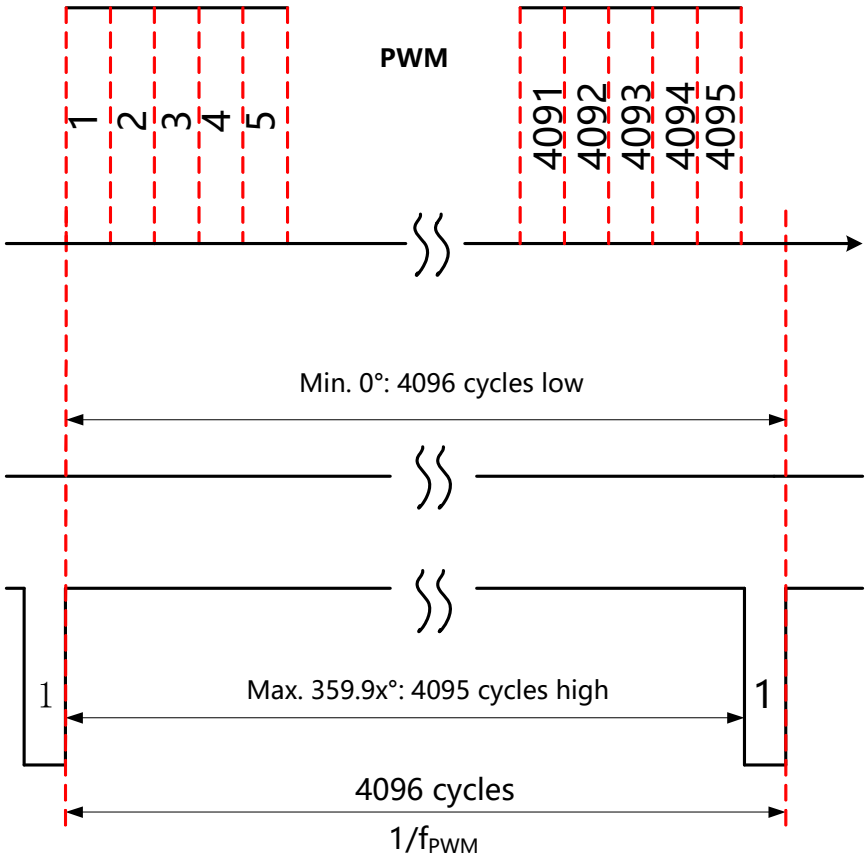


Figure 7: PWM Output

The 'PWM_POL' parameter

Parameter	Value	Description
PWM Polarity	0	High Level Valid
	1	Low Level Valid

The 'PWM_FREQ' parameter

Parameter	Value	Min.	Typ. (Hz)	Max.
FPWM (PWM Frequency)	0	-8% (Note[2])	122	+8% (Note[2])
	1		244	
	2		488	
	3		977	

Note[2] The Min. /Max. PWM frequency is due to chip to chip variation and temperature drift.

6.1.3 Switch Output Mode

When Switch Output Mode of the MT6501 is enabled, the output signal is a digital signal with the switch point selected by 'SW_OP' parameter and hysteresis selected by 'SW_HYS' parameter. Switch output could be enabled with Analog or PWM output at the same time.

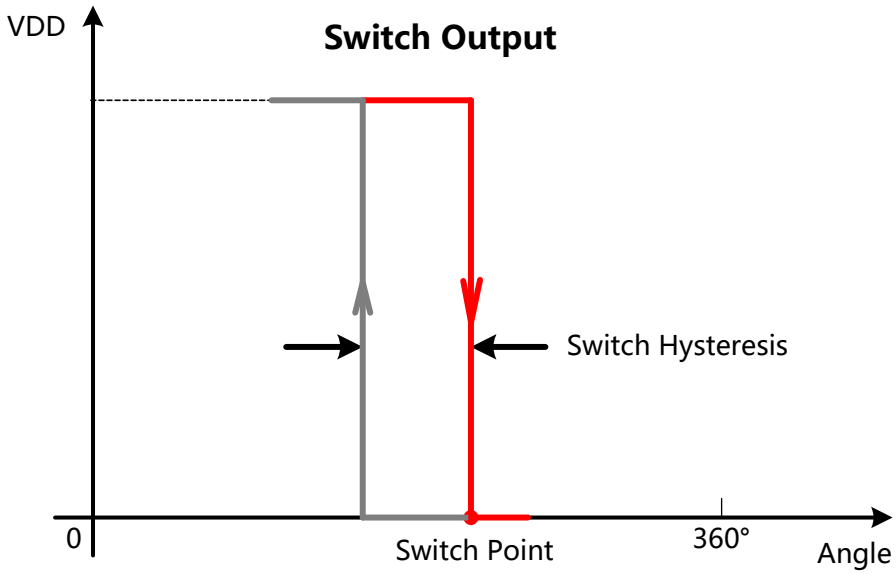


Figure 8: Switch Output

The 'SW_OP' parameter

Parameter	Value	Description
Switching Point	12 bit	9 bit integer and 3 bit decimal for degrees (<360°)

The 'SW_HYS' parameter

Parameter	Value	Description
Switch Hysteresis	6 bit	4 bit integer and 2 bit decimal for degrees

The 'SW_POL' parameter

Parameter	Value	Description
Switch Output Polarity	0	Low Level above SW_OP
	1	High Level above SW_OP

6.2 Programmable Output Transfer Characteristic

The analog output transfer function of MT6501 could be user programmed. It could be defined by 'Clamp_high', 'Clamp_low' and '4-Point' parameters.

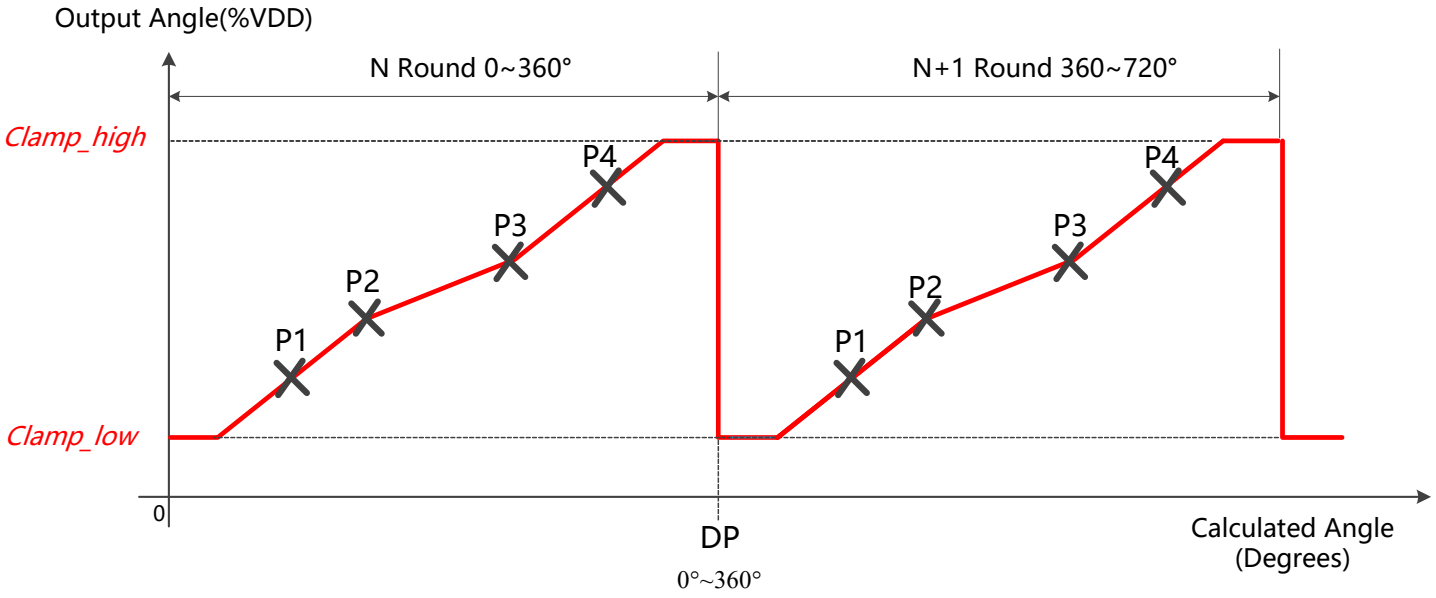


Figure 9: Output Transfer Function

The Discontinuity Point (DP) could be programmed and used as the reference point for angular measurements, it could be programmed between 0~360°.

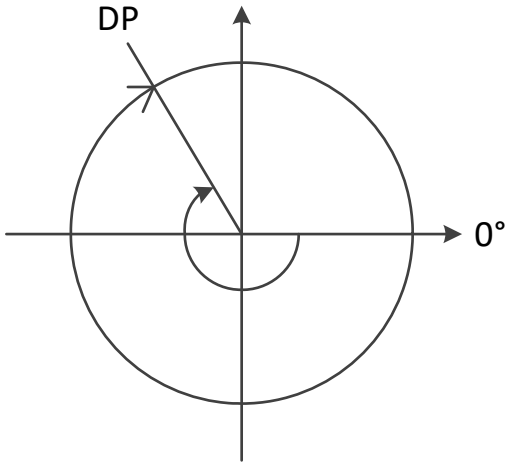


Figure 10: DP Position

The 'DP' parameter

Parameter	Value	Description
Discontinuity Point	12 bit	9 bit integer and 3 bit decimal for degrees (<360°)

6.2.1 4-Point Transfer Function and Parameters

The '4-Point' parameter could be programmed for special output shapes or for better linearity.

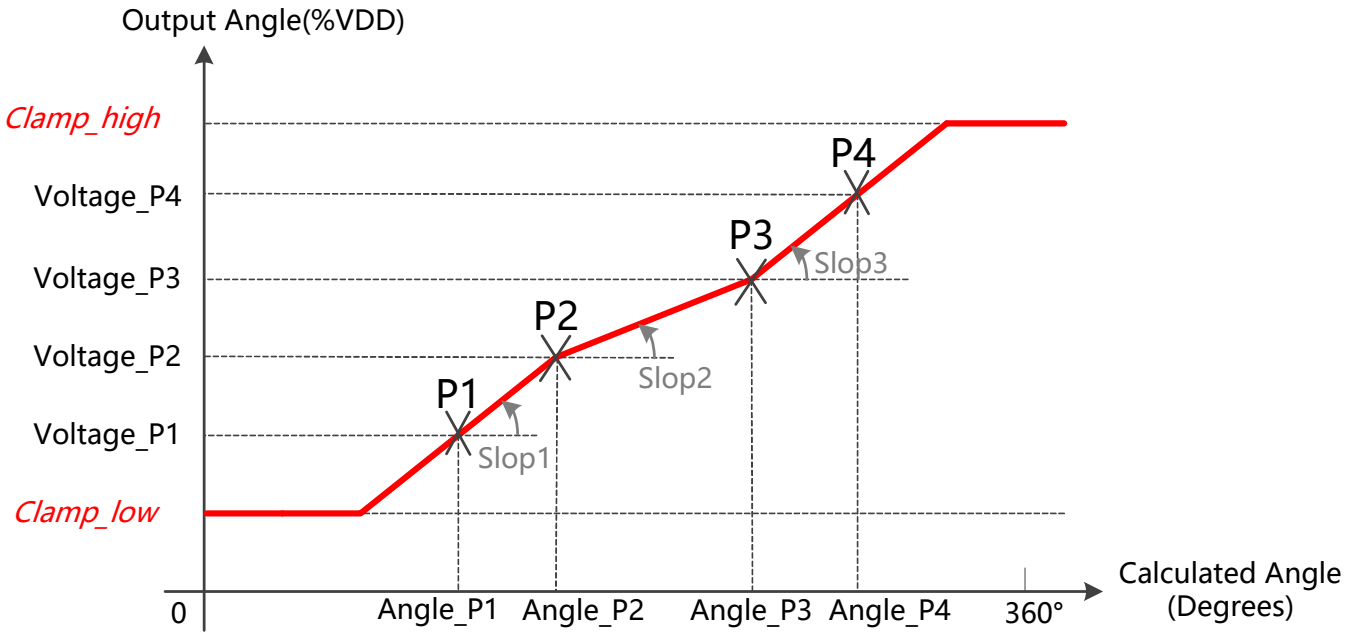


Figure 11: 4-Points Programmable Output Transfer Function

The '4-Point' parameter

Parameter	Value	Description
Angle_P1~Angle_P4	12 bit	9 bit integer and 3 bit decimal for degrees (<360°)
Voltage_P1~Voltage_P4	12 bit	12 bit data represent 0~100% VDD

6.2.2 Clamping Parameters

The clamping levels are two independent values to limit the analog output voltage range. Both the parameters have 12 bits data with the resolution of 0.024%VDD.

The 'Clamp_high', 'Clamp_low' parameter

Parameter	Value	Description
Clamp_high	12 bit	12 bit data represent 0~100% VDD
Clamp_low	12 bit	12 bit data represent 0~100% VDD

7. 3-Wire SPI Interface

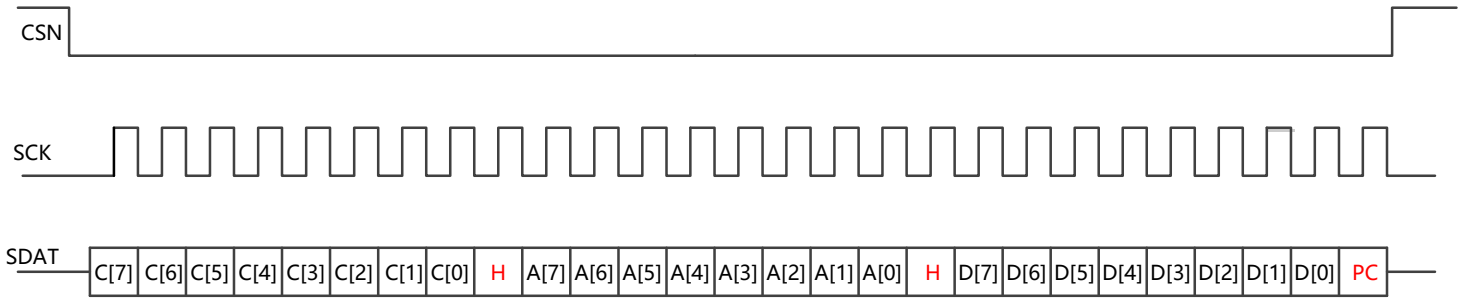


Figure 12: 3-Wire SPI Timing

SPI data transfer starts when CSN is pulled low and stops when it is pulled high. SCK is the serial port clock and it is controlled by the SPI master, it is limited to 512KHz. SDAT is the serial port data input and output, and it is driven at the falling edge of SCK and should be captured at the rising edge of SCK.

C[7:0]: Read or Write command byte
C[7:0]=0xA5, Master writes data to MT6501
C[7:0]=0xAF, Master reads data from MT6501
A[7:0]: Register Address
D[7:0]: Data
PC: Parity Check Bit. MT6501 sends out 8 bit data and an extra parity check bit, but MT6501 does not check the PC bit from master

For SDAT (Pin.6), when as data output, it is default NMOS open-drain output, an external pull-up resistor is needed.

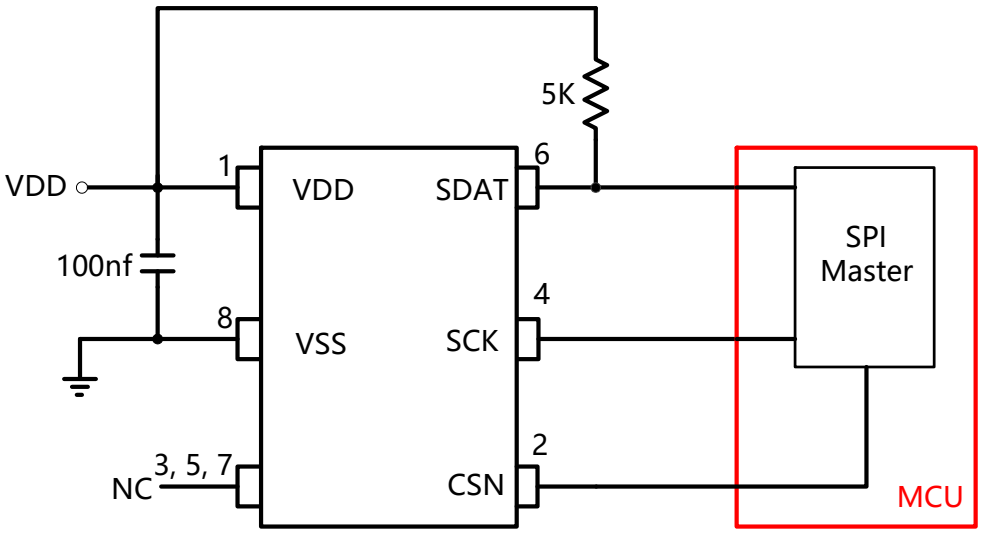


Figure 13: Reference Application Circuit for SPI

8. Recommended Application Diagrams

Figure 14 shows the reference circuit for typical applications that use the analog or PWM output.

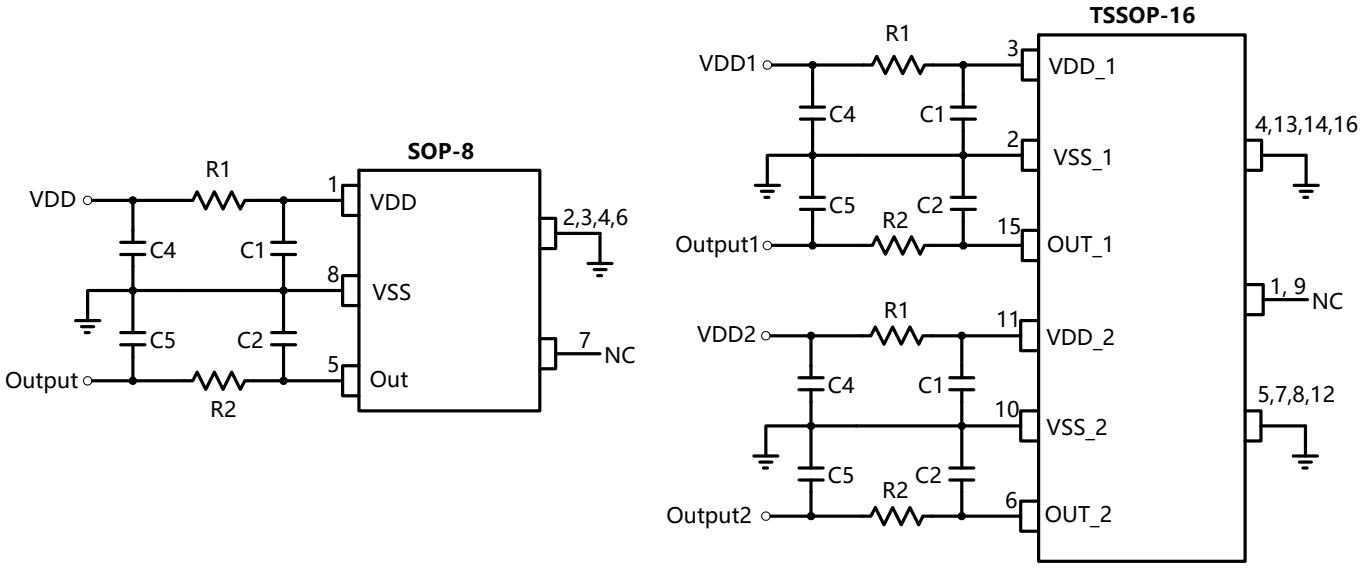


Figure 14: Reference Application Circuit for Analog Interface

Compact PCB Routing		
C1, C2	10nf	Analog Output Mode (No C4, C5, R1, R2)
C1	100nf	PWM Output Mode (No C4, C5, R1, R2)
C2	4.7nf	
Optimal EMC Performance		
C1, C2	10nf	Close to IC Terminals
C4	100nf	Analog Output Mode, close to connector
C5	10nf	
C4	100nf	PWM Output Mode, close to connector
C5	4.7nf	
R1	10 Ω	Increased Ratiometry Error, Recommend for PWM Output Mode
R2	50 Ω	Recommend for PWM Output Mode

For applications that use Switch Output Mode, the reference circuit in Figure 15 is recommended.

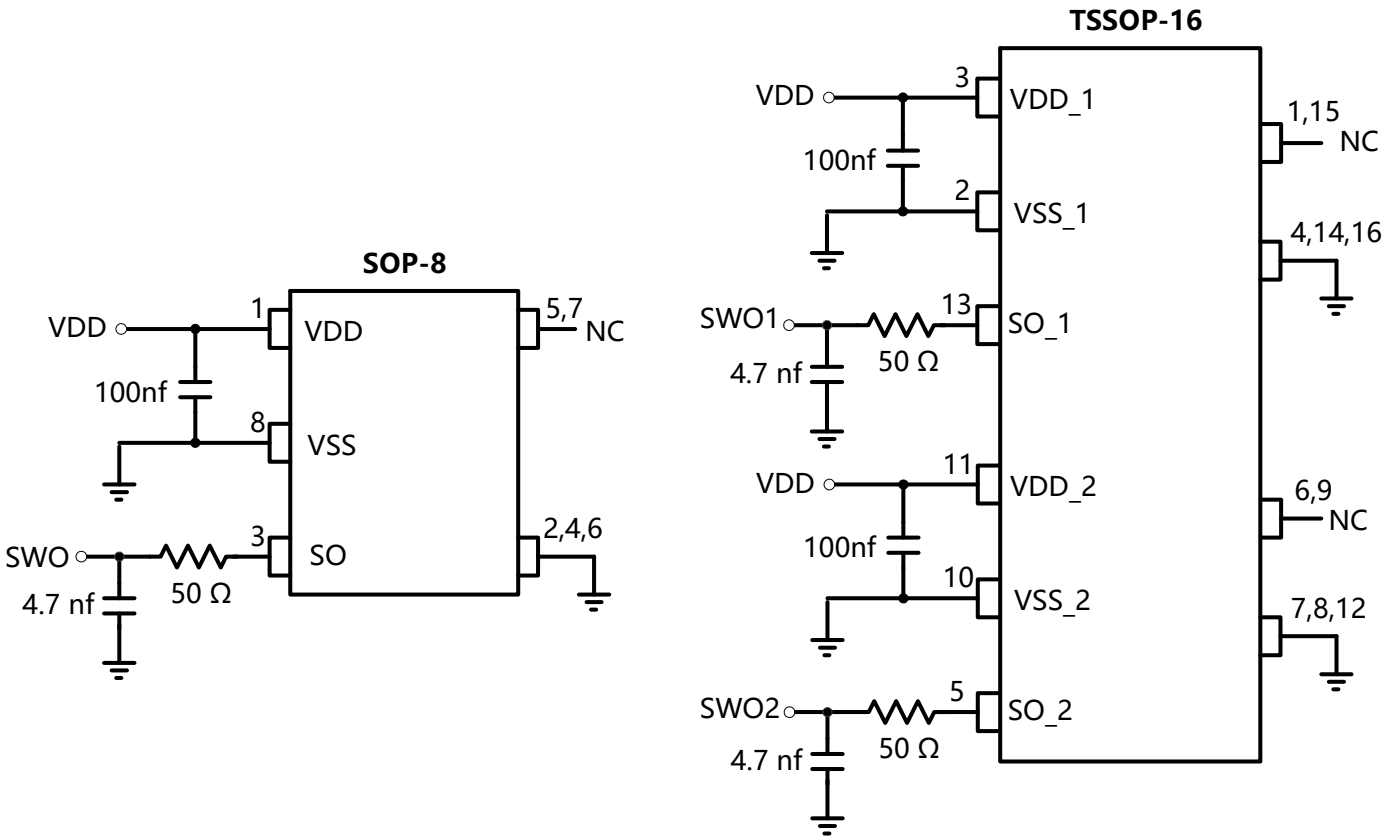


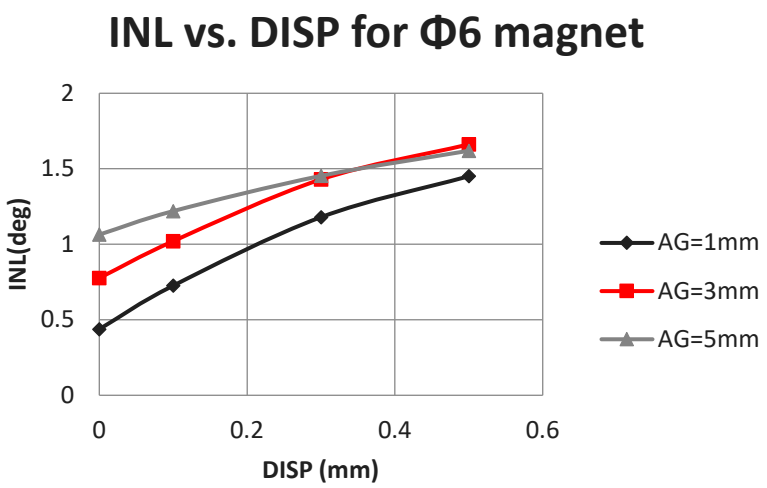
Figure 15: Reference Application Circuit for Switch Output

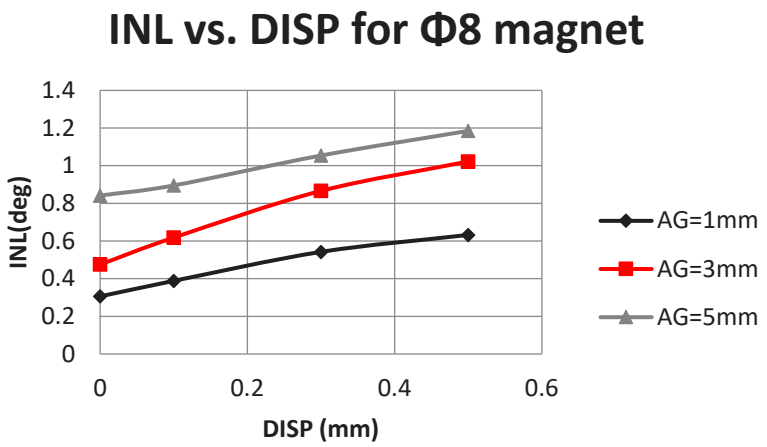
9. EEPROM Endurance

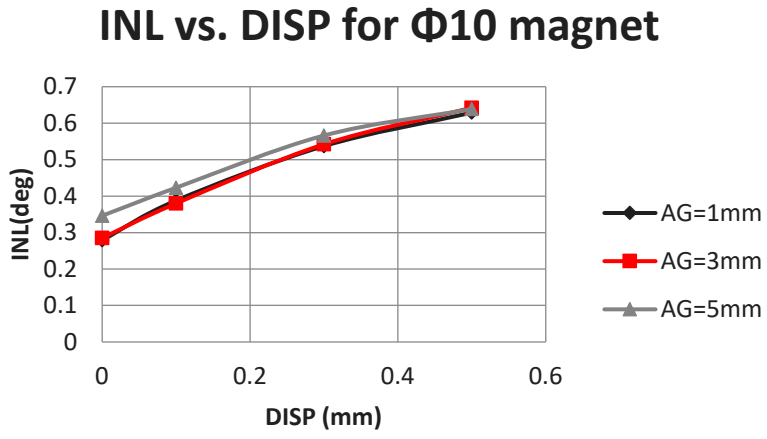
The EEPROM in MT6501 is used for calibration and trimming data storage, it is qualified to guarantee an endurance of minimum 1000 write/erase cycles at 125℃ for engineering purpose.

10. Magnet Placement

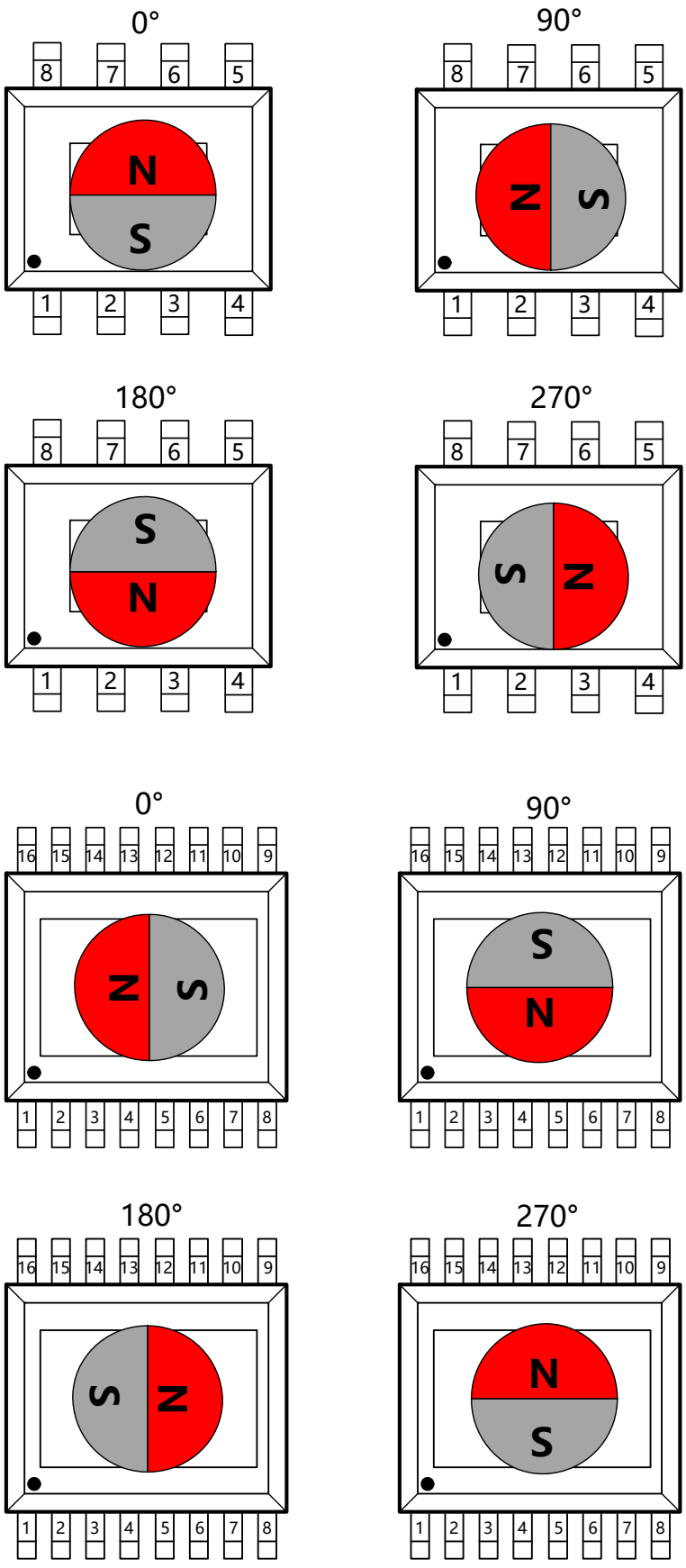
It is required that the magnet' s center axis be aligned with the sensing element center of MT6501 with the air-gap as small as possible. Any misalignment introduces additional angle error and big air-gap also weakens the magnet field which could be sensed by the device. Magnets with larger diameter are more tolerant to DISP (off-axis misalignment) and big AG (air-gap between Magnet and device).





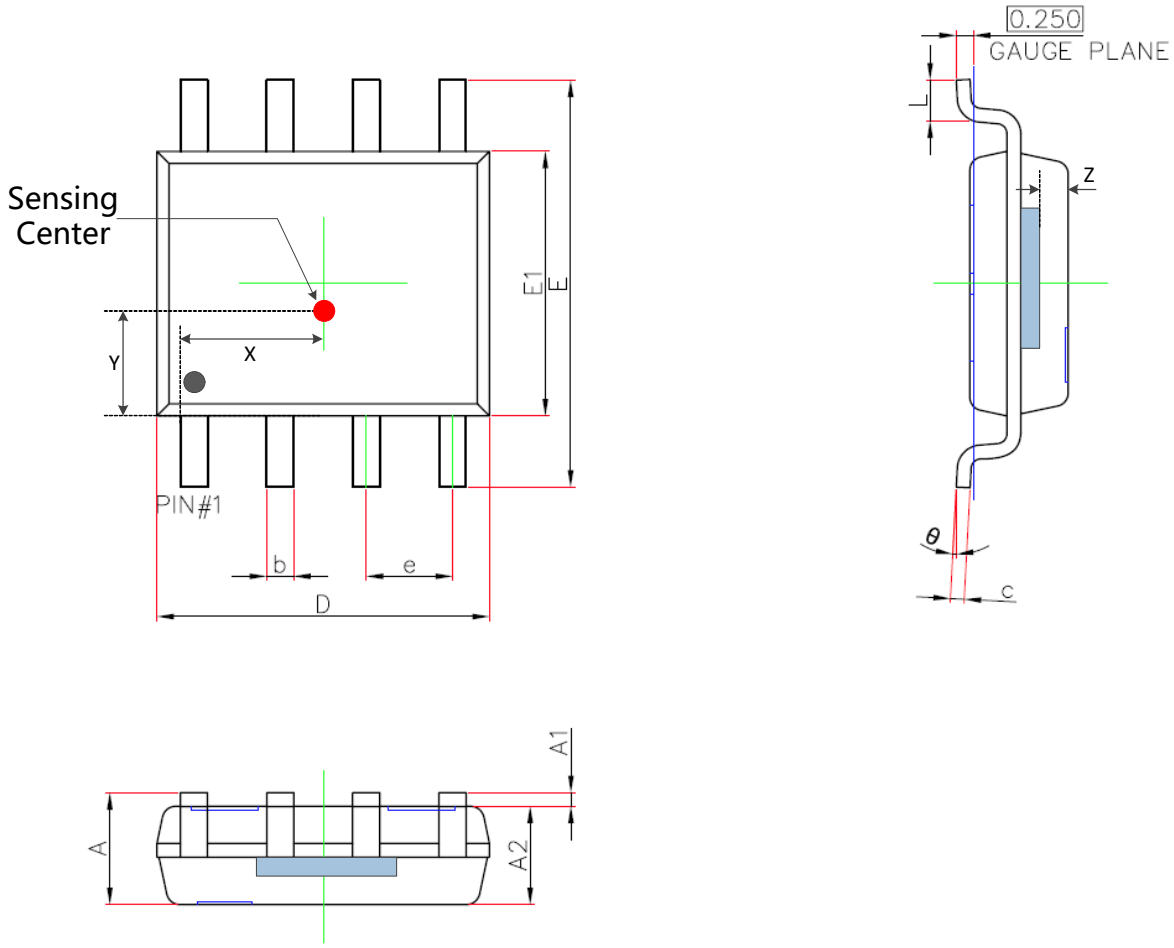


11. Mechanical Angle Direction



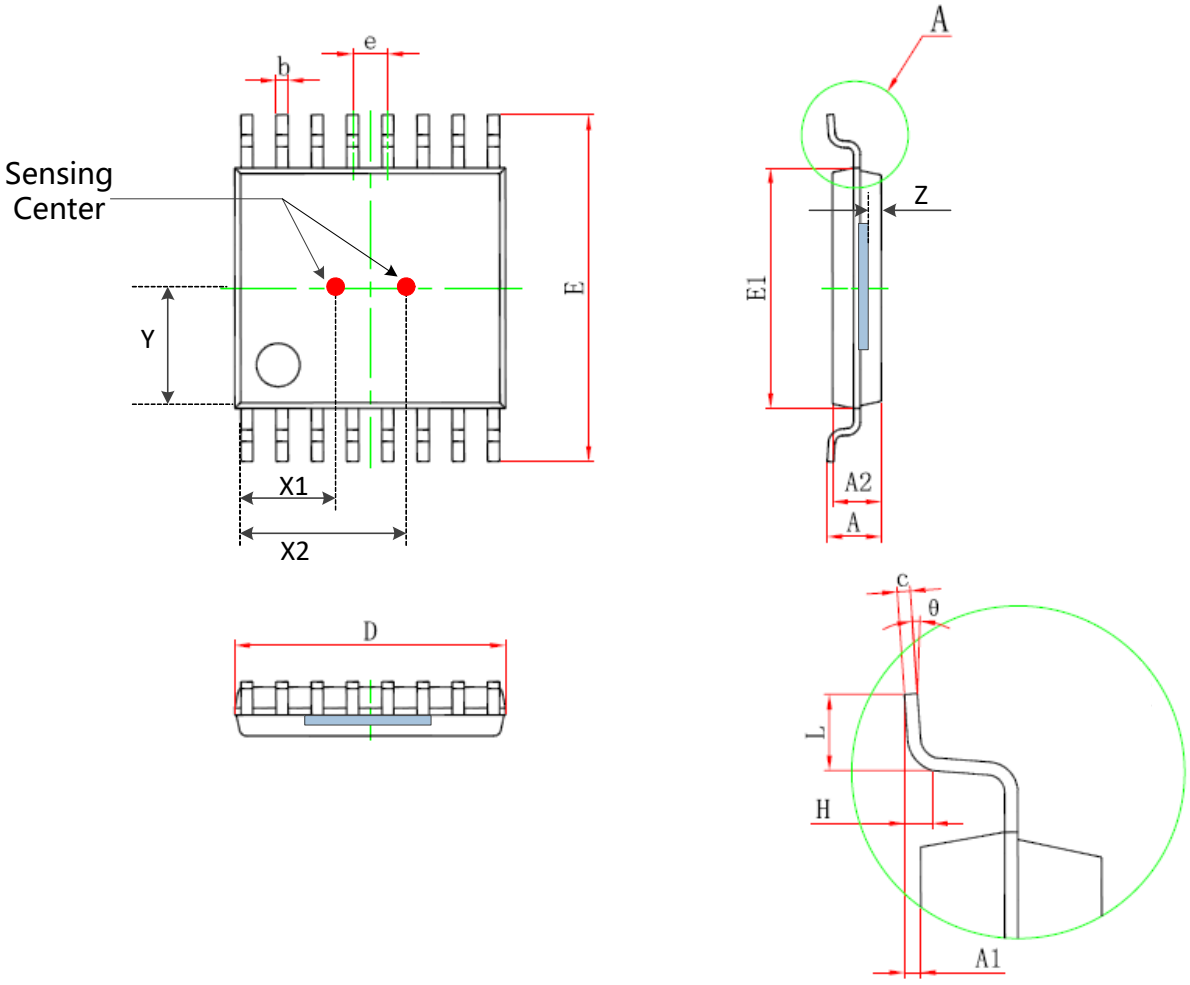
12. Package Information

12.1 SOP-8 Package



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270(BSC)		0.050(BSC)	
L	0.400	0.800	0.016	0.031
θ	0°	8°	0°	8°
X	1.97	2.27	0.078	0.089
Y	1.34	1.70	0.053	0.067
Z	0.42	0.62	0.016	0.024

12.2 TSSOP-16 Package



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
D	4.900	5.100	0.193	0.201
E	6.250	6.550	0.246	0.258
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	4.300	4.500	0.169	0.177
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.25 (TYP)		0.01 (TYP)	
θ	1°	7°	1°	7°
X1	1.650	1.890	0.065	0.074
X2	3.110	3.350	0.122	0.132
Y	2.080	2.320	0.081	0.093
Z	0.210	0.370	0.016	0.024

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14. Revision History

Revision Number	Date	Comments
1.0	2018.03	Initial Release
1.1	2019.09	Update FPWM Min./Max. Range
1.2	2019.12	Update
1.3	2020.02	Update
1.4	2020.05	Update SPI Output Mode and EMC reference