

## Normally – OFF Silicon Carbide Junction Transistor

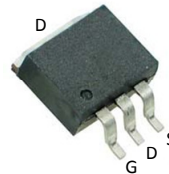
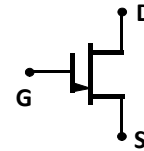
$V_{DS}$	=	1200 V
$R_{DS(ON)}$	=	120 m $\Omega$
$I_D$ ( $T_c = 25^\circ\text{C}$ )	=	25 A
$h_{FE}$ ( $T_c = 25^\circ\text{C}$ )	=	80

### Features

- 175 °C Maximum Operating Temperature
- Gate Oxide Free SiC Switch
- Exceptional Safe Operating Area
- Excellent Gain Linearity
- Temperature Independent Switching Performance
- Low Output Capacitance
- Positive Temperature Coefficient of  $R_{DS,ON}$
- Suitable for Connecting an Anti-parallel Diode

### Package

- RoHS Compliant


**TO-263**


### Advantages

- Compatible with Si MOSFET/IGBT Gate Drive ICs
- > 20  $\mu\text{s}$  Short-Circuit Withstand Capability
- Lowest-in-class Conduction Losses
- High Circuit Efficiency
- Minimal Input Signal Distortion
- High Amplifier Bandwidth

### Applications

- Down Hole Oil Drilling, Geothermal Instrumentation
- Hybrid Electric Vehicles (HEV)
- Solar Inverters
- Switched-Mode Power Supply (SMPS)
- Power Factor Correction (PFC)
- Induction Heating
- Uninterruptible Power Supply (UPS)
- Motor Drives

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### Section I: Absolute Maximum Ratings

Parameter	Symbol	Conditions	Value	Unit	Notes
Drain – Source Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}$	1200	V	
Continuous Drain Current	$I_D$	$T_c = 25^\circ\text{C}$	25	A	Fig. 17
Continuous Drain Current	$I_D$	$T_c = 155^\circ\text{C}$	10	A	Fig. 17
Continuous Gate Current	$I_G$		1.3	A	
Turn-Off Safe Operating Area	RBSOA	$T_{VJ} = 175^\circ\text{C}$ , Clamped Inductive Load	$I_{D,max} = 10$ @ $V_{DS} \leq V_{DSmax}$	A	Fig. 19
Short Circuit Safe Operating Area	SCSOA	$T_{VJ} = 175^\circ\text{C}$ , $I_G = 1\text{ A}$ , $V_{DS} = 800\text{ V}$ , Non Repetitive	>20	$\mu\text{s}$	
Reverse Gate – Source Voltage	$V_{SG}$		30	V	
Reverse Drain – Source Voltage	$V_{SD}$		25	V	
Power Dissipation	$P_{tot}$	$T_c = 25^\circ\text{C} / 155^\circ\text{C}$ , $t_p > 100\text{ ms}$	170 / 22	W	Fig. 16
Storage Temperature	$T_{stg}$		-55 to 175	$^\circ\text{C}$	

**Section II: Static Electrical Characteristics**

Parameter	Symbol	Conditions	Value			Unit	Notes
			Min.	Typical	Max.		
<b>A: On State</b>							
Drain – Source On Resistance	$R_{DS(ON)}$	$I_D = 10\text{ A}, T_J = 25\text{ °C}$		120		mΩ	Fig. 5
		$I_D = 10\text{ A}, T_J = 125\text{ °C}$		164			
		$I_D = 10\text{ A}, T_J = 175\text{ °C}$		208			
Gate On Voltage	$V_{GS,ON}$	$I_D = 10\text{ A}, V_{DS} = 30\text{ V}, T_J = 25\text{ °C}$		3.5		V	Fig. 4
		$I_D = 10\text{ A}, V_{DS} = 30\text{ V}, T_J = 175\text{ °C}$		3.2			
DC Current Gain	$h_{FE}$	$V_{DS} = 5\text{ V}, I_D = 10\text{ A}, T_J = 25\text{ °C}$		80		–	Fig. 5
		$V_{DS} = 5\text{ V}, I_D = 10\text{ A}, T_J = 125\text{ °C}$		56			
		$V_{DS} = 5\text{ V}, I_D = 10\text{ A}, T_J = 175\text{ °C}$		50			
<b>B: Off State</b>							
Drain Leakage Current	$I_{DSS}$	$V_{DS} = 1200\text{ V}, V_{GS} = 0\text{ V}, T_J = 25\text{ °C}$		1		μA	Fig. 6
		$V_{DS} = 1200\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ °C}$		1			
		$V_{DS} = 1200\text{ V}, V_{GS} = 0\text{ V}, T_J = 175\text{ °C}$		10			
Gate Leakage Current	$I_{SG}$	$V_{SG} = 20\text{ V}, T_J = 25\text{ °C}$		20		nA	
<b>C: Thermal</b>							
Thermal resistance, junction - case	$R_{thJC}$			0.88		°C/W	Fig. 20

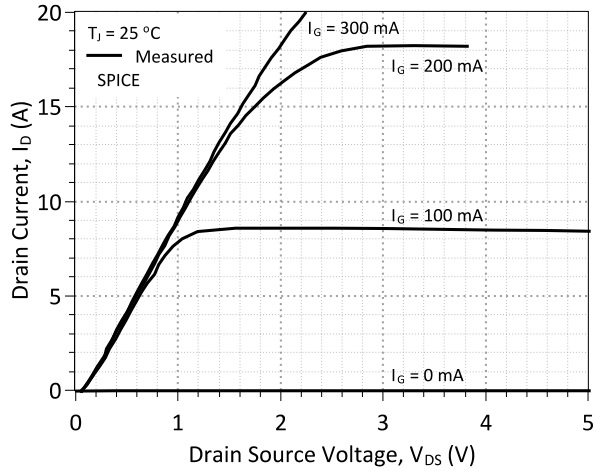
**Section III: Dynamic Electrical Characteristics**

Parameter	Symbol	Conditions	Value			Unit	Notes
			Min.	Typical	Max.		
<b>A: Capacitance and Gate Charge</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 800\text{ V}, f = 1\text{ MHz}$		1403		pF	Fig. 9
Reverse Transfer/Output Capacitance	$C_{rss}/C_{oss}$	$V_{DS} = 800\text{ V}, f = 1\text{ MHz}$		30		pF	Fig. 9
Output Capacitance Stored Energy	$E_{OSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 800\text{ V}, f = 1\text{ MHz}$		9		μJ	Fig. 10
Effective Output Capacitance, time related	$C_{oss,tr}$	$I_D = \text{constant}, V_{GS} = 0\text{ V}, V_{DS} = 0\dots 800\text{ V}$		55		pF	
Effective Output Capacitance, energy related	$C_{oss,er}$	$V_{GS} = 0\text{ V}, V_{DS} = 0\dots 800\text{ V}$		40		pF	
Gate-Source Charge	$Q_{GS}$	$V_{GS} = -5\dots 3\text{ V}$		11		nC	
Gate-Drain Charge	$Q_{GD}$	$V_{GS} = 0\text{ V}, V_{DS} = 0\dots 800\text{ V}$		44		nC	
Gate Charge - Total	$Q_G$			55		nC	
<b>B: Switching<sup>1</sup></b>							
Internal Gate Resistance – zero bias	$R_{G(INT-ZERO)}$	$f = 1\text{ MHz}, V_{AC} = 50\text{ mV}, V_{DS} = 0\text{ V}, V_{GS} = 0\text{ V}, T_J = 175\text{ °C}$		2.6		Ω	
Internal Gate Resistance – ON	$R_{G(INT-ON)}$	$V_{GS} > 2.5\text{ V}, V_{DS} = 0\text{ V}, T_J = 175\text{ °C}$		0.19		Ω	
Turn On Delay Time	$t_{d(on)}$	$T_J = 25\text{ °C}, V_{DS} = 800\text{ V},$		15		ns	
Fall Time, $V_{DS}$	$t_f$	$I_D = 10\text{ A}, \text{Resistive Load}$		18		ns	Fig. 11, 13
Turn Off Delay Time	$t_{d(off)}$	Refer to Section V for additional driving information.		22		ns	
Rise Time, $V_{DS}$	$t_r$			13		ns	Fig. 12, 14
Turn On Delay Time	$t_{d(on)}$			14		ns	
Fall Time, $V_{DS}$	$t_f$	$T_J = 175\text{ °C}, V_{DS} = 800\text{ V},$		18		ns	Fig. 11
Turn Off Delay Time	$t_{d(off)}$	$I_D = 10\text{ A}, \text{Resistive Load}$		33		ns	
Rise Time, $V_{DS}$	$t_r$			11		ns	Fig. 12
Turn-On Energy Per Pulse	$E_{on}$	$T_J = 25\text{ °C}, V_{DS} = 800\text{ V},$		181		μJ	Fig. 11, 13
Turn-Off Energy Per Pulse	$E_{off}$	$I_D = 10\text{ A}, \text{Inductive Load}$		16		μJ	Fig. 12, 14
Total Switching Energy	$E_{tot}$	Refer to Section V.		197		μJ	
Turn-On Energy Per Pulse	$E_{on}$			192		μJ	Fig. 11
Turn-Off Energy Per Pulse	$E_{off}$	$T_J = 175\text{ °C}, V_{DS} = 800\text{ V},$		11		μJ	Fig. 12
Total Switching Energy	$E_{tot}$	$I_D = 10\text{ A}, \text{Inductive Load}$		203		μJ	

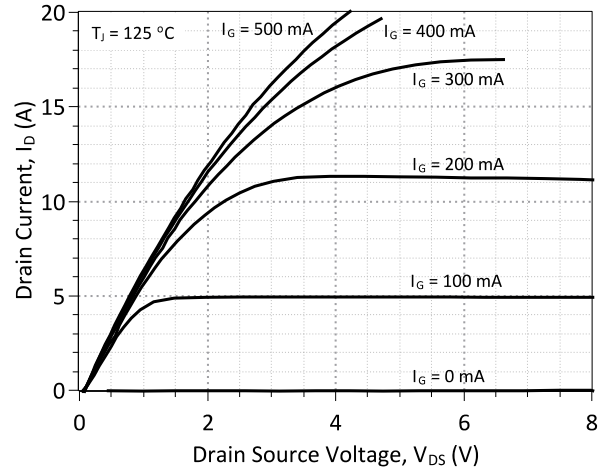
<sup>1</sup> – All times are relative to the Drain-Source Voltage  $V_{DS}$

**Section IV: Figures**

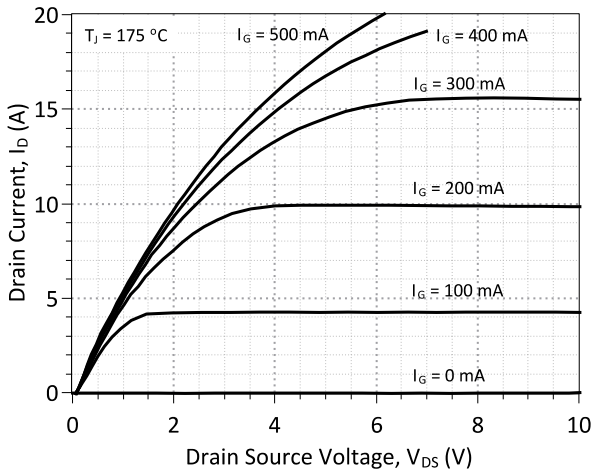
**A: Static Characteristic Figures**



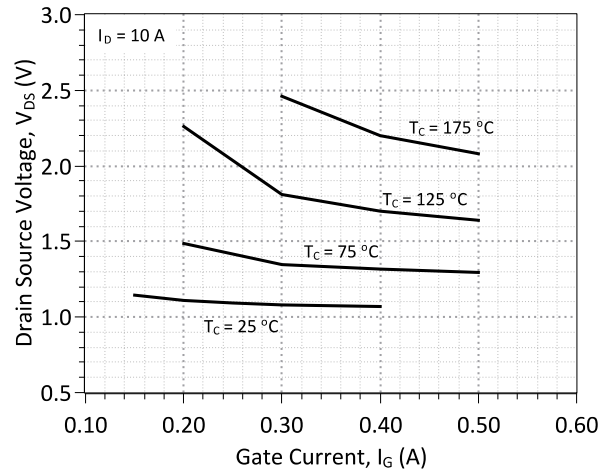
**Figure 1: Typical Output Characteristics at 25 °C**



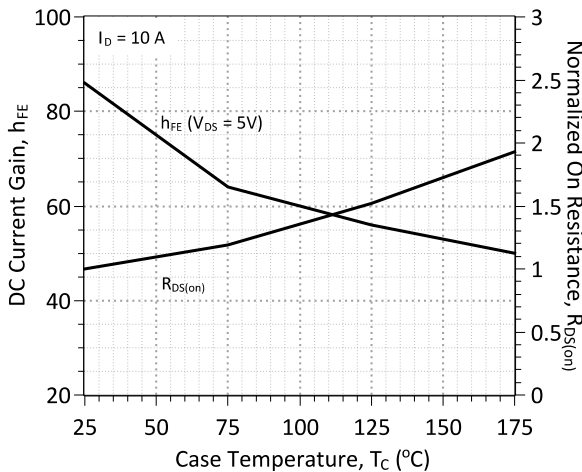
**Figure 2: Typical Output Characteristics at 125 °C**



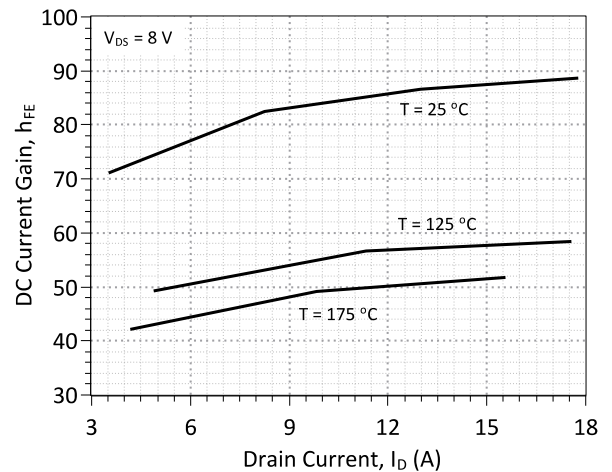
**Figure 3: Typical Output Characteristics at 175 °C**



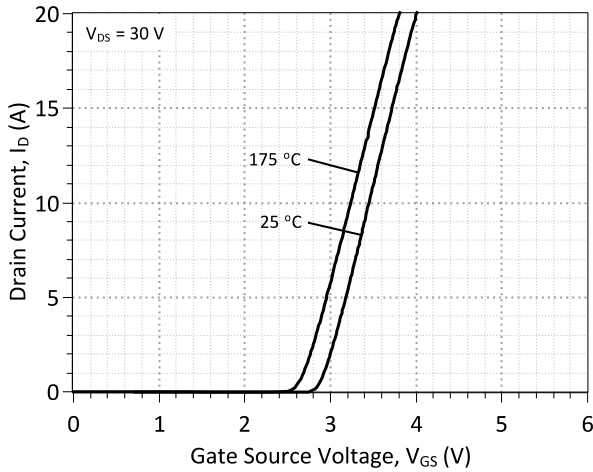
**Figure 4: Drain-Source Voltage vs. Gate Current**



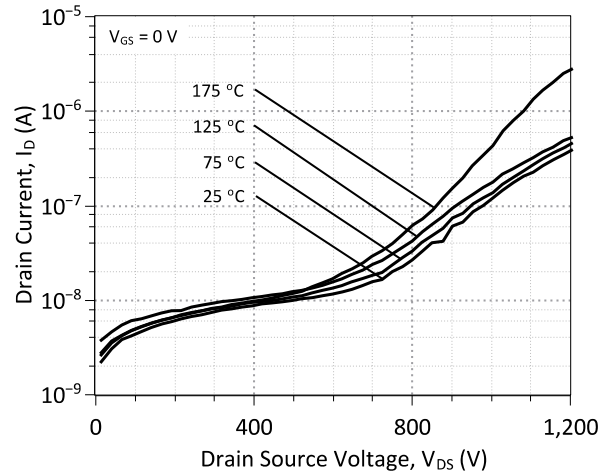
**Figure 5: DC Current Gain and Normalized On-Resistance vs. Temperature**



**Figure 6: DC Current Gain vs. Drain Current**

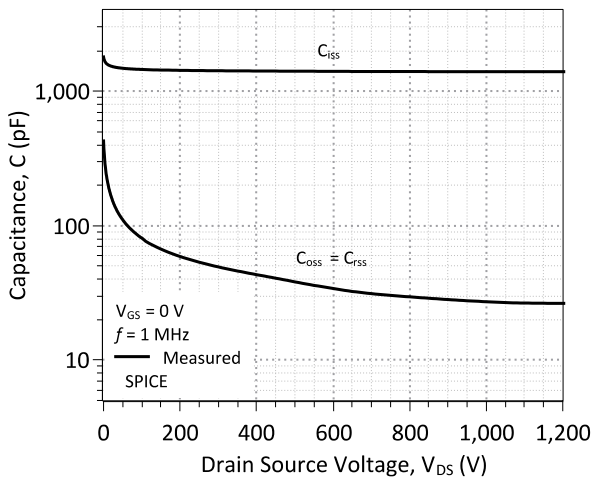


**Figure 7: Typical Transfer Characteristics**

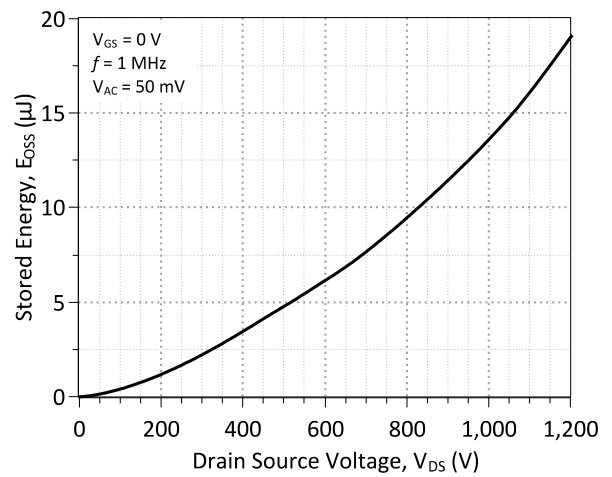


**Figure 8: Typical Blocking Characteristics**

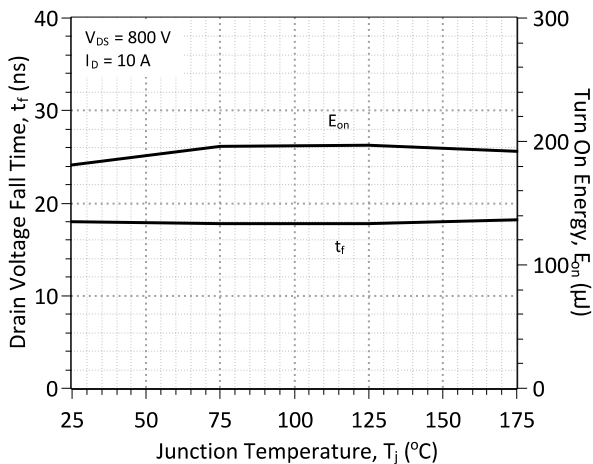
**B: Dynamic Characteristic Figures**



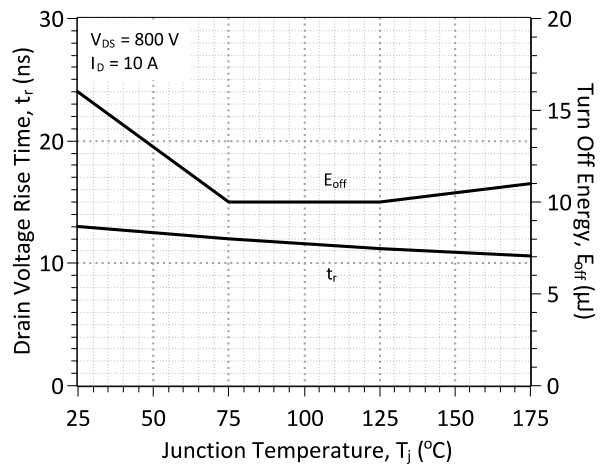
**Figure 9: Input, Output, and Reverse Transfer Capacitance**



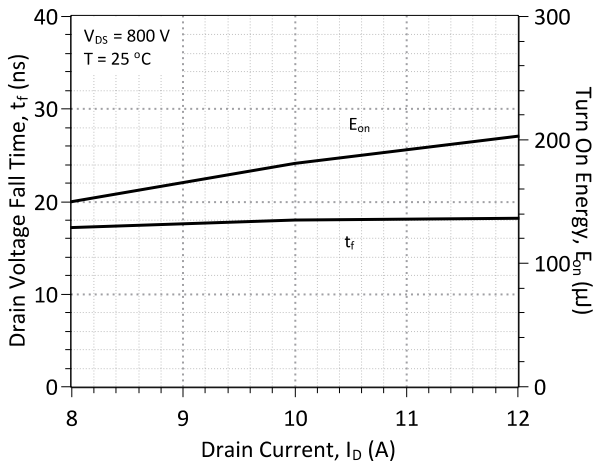
**Figure 10: Output Capacitance Stored Energy**



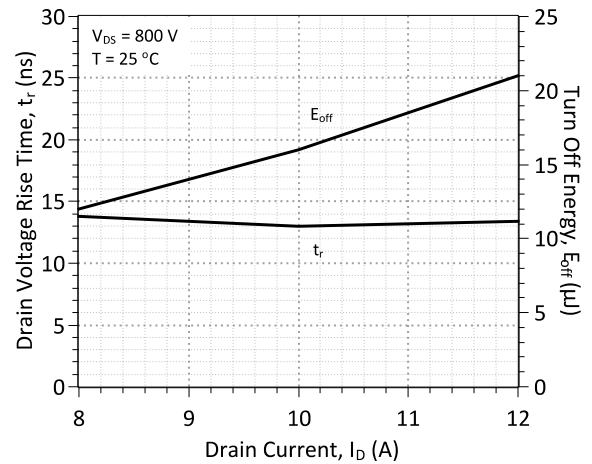
**Figure 11: Typical Switching Times and Turn On Energy Losses vs. Temperature**



**Figure 12: Typical Switching Times and Turn Off Energy Losses vs. Temperature**

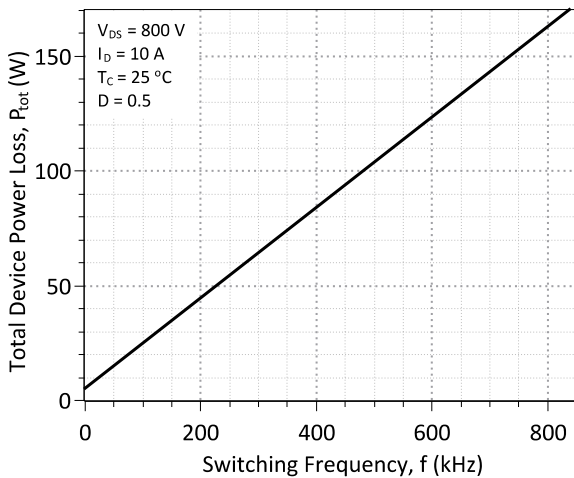


**Figure 13: Typical Switching Times and Turn On Energy Losses vs. Drain Current**

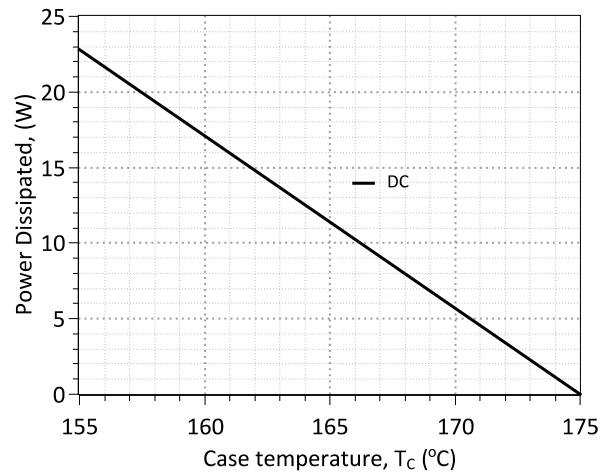


**Figure 14: Typical Switching Times and Turn Off Energy Losses vs. Drain Current**

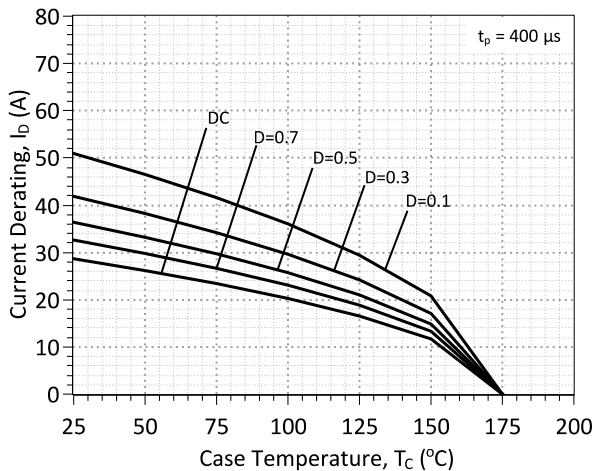
**C: Device Derating Figures**



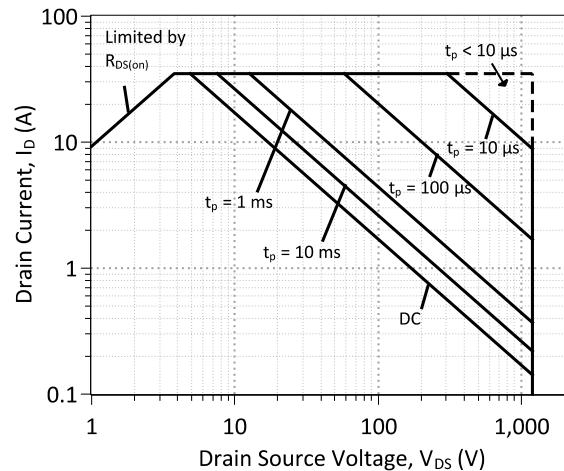
**Figure 15: Typical Hard Switched Device Power Loss vs. Switching Frequency<sup>2</sup>**



**Figure 16: Power Derating Curve**



**Figure 17: Drain Current Derating vs. Temperature**



**Figure 18: Forward Bias Safe Operating Area at T<sub>c</sub> = 25 °C**

<sup>2</sup> – Representative values based on device conduction and switching loss. Actual losses will depend on gate drive conditions, device load, and circuit topology.

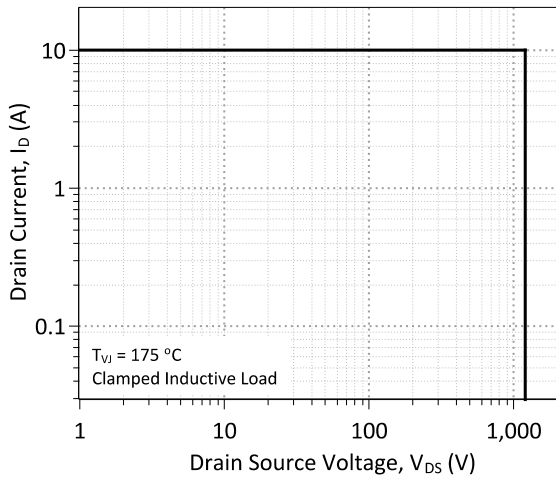


Figure 19: Turn-Off Safe Operating Area

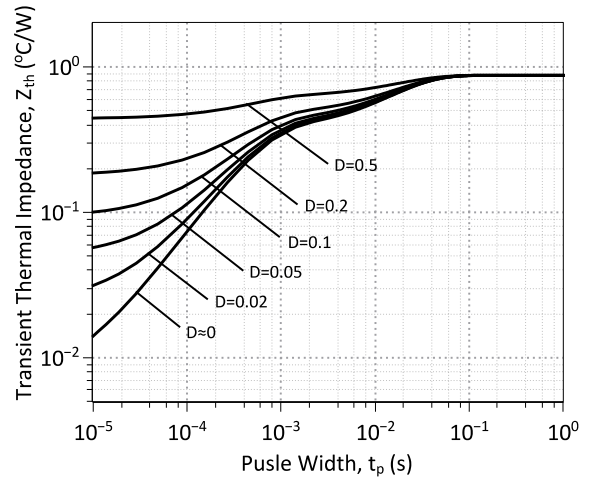


Figure 20: Transient Thermal Impedance

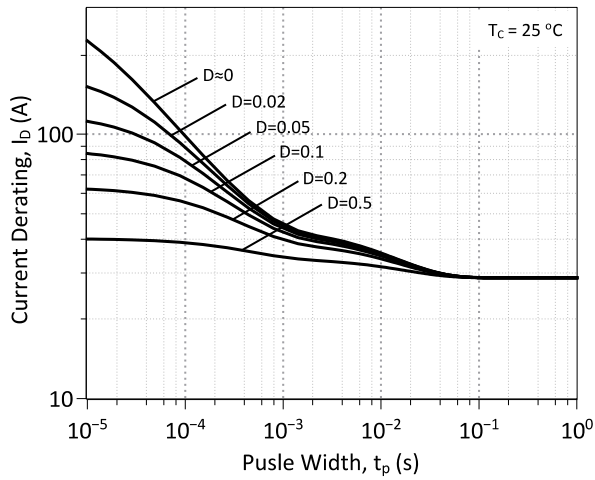
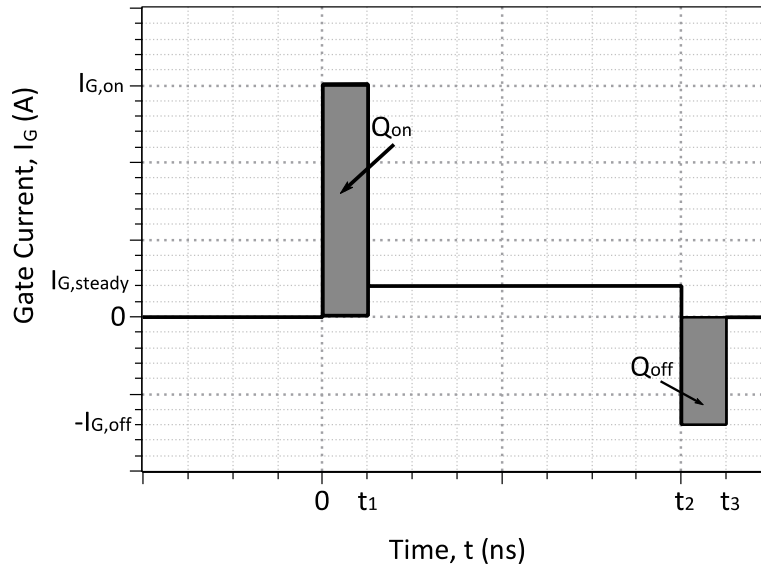


Figure 21: Drain Current Derating vs. Pulse Width

**Section V: Driving the GA10JT12-263**
**A: Gate Drive Theory of Operation**

The SJT transistor is a current controlled transistor which requires a positive gate current for turn-on as well as to remain in on-state. An ideal gate current waveform for ultra-fast switching of the SJT, while maintaining low gate drive losses, is shown in Figure 22.



**Figure 22: Idealized Gate Current Waveform**

**A:1: Gate Currents,  $I_{G,pk}/-I_{G,pk}$  and Voltages during Turn-On and Turn-Off**

An SJT is rapidly switched from its blocking state to on-state, when the necessary gate charge,  $Q_G$ , for turn-on is supplied by a burst of high gate current,  $I_{G,on}$ , until the gate-source capacitance,  $C_{GS}$ , and gate-drain capacitance,  $C_{GD}$ , are fully charged.

$$I_{G,on} * t_1 \geq Q_{gs} + Q_{gd}$$

As an example, an  $I_{G,pk} \geq 2.5$  A is required to achieve a 18 ns  $V_{DS}$  fall time for a 800 V switching transition, due to the gate-drain charge,  $Q_{GD}$  of 44 nC for the GA10JT12-263. The  $I_{G,pk}$  pulse should ideally terminate, when the drain voltage falls to its on-state value, in order to avoid unnecessary drive losses during the steady on-state. In practice, the rise time of the  $I_{G,on}$  pulse is affected by the parasitic inductances,  $L_{par}$  in the TO-263 package and drive circuit. A voltage developed across the parasitic inductance in the source path,  $L_s$ , can de-bias the gate-source junction, when high drain currents begin to flow through the device. The applied gate voltage should be maintained high enough, above the  $V_{GS,ON}$  (see Figure 7) level to counter these effects.

A high negative peak current,  $-I_{G,off}$  is recommended at the start of the turn-off transition, in order to rapidly sweep out the injected carriers from the gate, and achieve rapid turn-off. While satisfactory turn off can be achieved with  $V_{GS} = 0$  V, a negative gate voltage  $V_{GS}$  may be used in order to speed up the turn-off transition.

**A:2: Steady On-State**

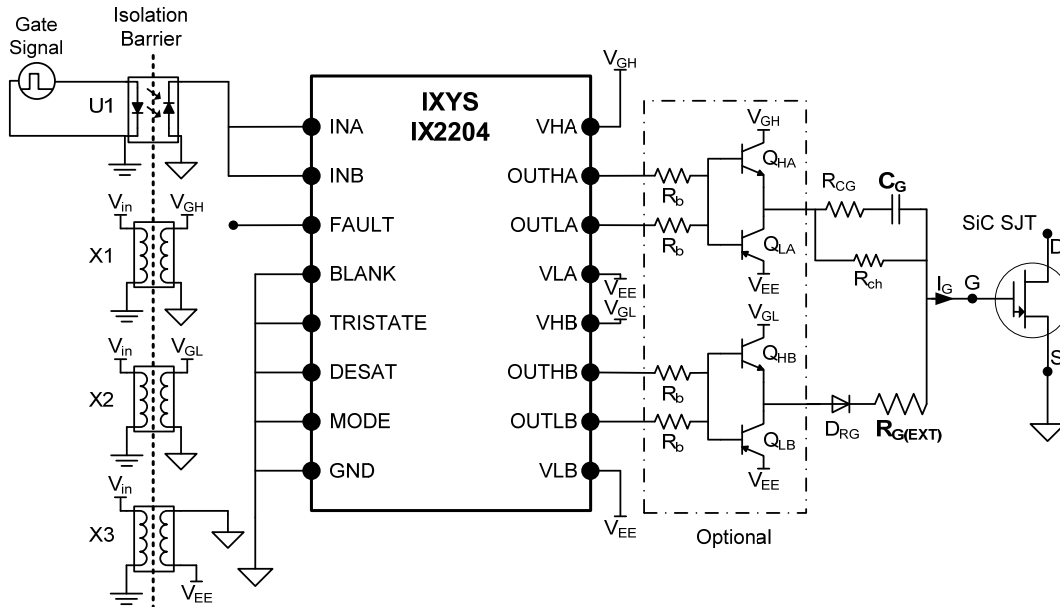
After the device is turned on,  $I_G$  may be advantageously lowered to  $I_{G,steady}$  for reducing unnecessary gate drive losses. The  $I_{G,steady}$  is determined by noting the DC current gain,  $h_{FE}$ , of the device from Figures 5 and 6.

The desired  $I_{G,steady}$  is determined by the peak device junction temperature  $T_J$  during operation, drain current  $I_D$ , DC current gain  $h_{FE}$ , and a 50 % safety margin to ensure operating the device in the saturation region with low on-state voltage drop by the equation:

$$I_{G,steady} \approx \frac{I_D}{h_{FE}(T, I_D)} * 1.5$$

**B: Gate Drive Implementation Examples**
**B:1: Using the IXYS IX2204 Gate Driver**

The IXYS IX2204 is a dual output gate drive integrated circuit which can be used to drive an SJT transistor by supplying the required gate drive current  $I_G$  in a low-power gate drive solution. This configuration features an external gate capacitor,  $C_G$ , which creates the brief current peak  $I_{G,on}$  during device turn-on and  $I_{G,off}$  during turn-off for fast switching and an external gate resistor  $R_{G(EXT)}$  to set the continuous gate current  $I_{G,steady}$  required for the device to remain on. This configuration is shown in Figure 23 with further details provided below.



**Figure 23: Gate drive configuration using an IXYS IX2204 gate drive IC.**

**Table 1: Recommended Component List for implementing the IX2204 based Gate Drive for the GA10JT12-263**

Reference	Component	Description	Suggested Part
$R_{G(EXT)}$	Gate Resistance, External	2.2 $\Omega$ , 2 W	CRM2512-JW-2R2ELF
$C_G$	Gate Capacitance	10 nF	C1812C103J1GACTU
$R_{CG}$	Damping Resistor	1.0 $\Omega$ , 0.5 W	ERJ-1TYJ1R0U
$D_{RG}$	Silicon Schottky Diode	40 V, 2 A	SS24T3G
$R_b$	BJT Base Resistor	1.0 $\Omega$ , 0.5 W	ERJ-1TYJ1R0U
$Q_{HA}, Q_{HB}$	Current Boost NPN	40 V, 8 A, Silicon NPN BJT	MJD44H11
$Q_{LA}, Q_{LB}$	Current Boost PNP	40 V, 8 A, Silicon PNP BJT	MJD45H11
U1	Signal Isolator	Opto-Isolator –or– Transformer Isolator	ACPL-4800 / ADUM3210
X1	DC/DC Converter, $V_{GH}$ Supply	$V_{OUT} = +20$ V, $V_{IN} = +12$ V, 2 W, $V_{ISO} = 5.2$ kV	MGJ2D122005SC
X2	DC/DC Converter, $V_{GL}$ Supply	$V_{OUT} = +5$ V, $V_{IN} = +12$ V, 3 W, $V_{ISO} = 3.0$ kV	MEV3S1205SC
X3	DC/DC Converter, $V_{EE}$ Supply	$V_{OUT} = -5$ V, $V_{IN} = +12$ V, 2 W, $V_{ISO} = 5.2$ kV	MGJ2D122005SC

**B:2: Voltage Supply Selection**

The IX2204 gate drive design requires three supply voltages  $V_{GH}$ ,  $V_{GL}$ , and  $V_{EE}$  (listed in Table 2) optionally supplied through DC/DC converters. During device turn-on,  $V_{GH}$  charges the external capacitor  $C_G$  thereby delivering the narrow width, high current pulse  $I_{G,on}$  to the SJT gate and charges the SJT's internal terminal capacitances  $C_{GD}$  and  $C_{GS}$ . For a given level of parasitic inductance in the gate circuit and SJT package, the rise time of  $I_{G,on}$  is controlled by the choice of  $V_{GH}$  and  $C_G$ . During the steady on-state,  $V_{GL}$  in combination with the internal and external gate resistances provides a continuous gate current for the GA05JT12-263 to remain on. The  $V_{EE}$  supply sets the gate negative during turn-off and steady off-state for faster switching and to avoid spurious turn-on which may be caused by external circuit noise. The power rating of the voltage supplies should be adequate to meet the gate drive power requirements as determined by

$$P_{min,VGH} = \frac{1}{2} C_G V_{GH}^2 f_{sw}$$

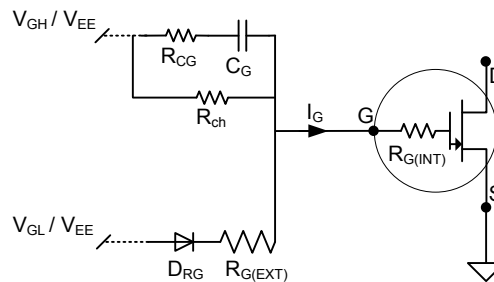
$$P_{min,VEE} = \frac{1}{2} C_G V_{EE}^2 f_{sw}$$

$$P_{min,VGL} = V_{GL} I_{G,cont} D$$



**Table 2: IX2204 Gate Drive Example Component List**

Symbol	Parameter	Values	
		Range	Typical
V <sub>GH</sub>	Supply Voltage, Driver Output A	15 – 20	+ 20.0
V <sub>GL</sub>	Supply Voltage, Driver Output B	5.0 – 7.0	+ 5.0
V <sub>EE</sub>	Negative Supply Voltage	-10 – GND	- 5.0

**B:3: Gate Capacitor C<sub>G</sub> Selection**

**Figure 24: Primary gate drive circuit passive components with series gate resistance Schottky rectifier.**

An external gate capacitor C<sub>G</sub> connected directly to the device gate pin delivers the positive current peak I<sub>G,on</sub> during device turn-on and the negative current peak I<sub>G,off</sub> during turn-off. A low value resistor R<sub>CG</sub> is connected in series with C<sub>G</sub> to damp potential high-frequency oscillation. A high value resistor R<sub>ch</sub> in parallel with C<sub>G</sub> sets the SJT gate to a defined potential (-V<sub>EE</sub>) during steady off-state.

At device turn-on, C<sub>G</sub> is pulled to V<sub>GH</sub> which produces a transient peak of gate voltage and current. This current peak rapidly charges the internal SJT C<sub>GS</sub> and C<sub>GD</sub> capacitances. A Schottky diode, D<sub>RG</sub>, in series with R<sub>G(EXT)</sub> blocks any C<sub>G</sub> induced current from draining out through R<sub>G(EXT)</sub>, and ensures that all of the charge within C<sub>G</sub> flows only into the device gate, allowing for an ultra-fast device turn-on. During steady on-state, a potential of V<sub>GH</sub> - V<sub>GS</sub> = V<sub>GH</sub> - 3 V is across C<sub>G</sub>. When the device is turned off, C<sub>G</sub> is pulled to negative V<sub>EE</sub> and V<sub>GS</sub> is pulled to a transient peak of V<sub>GS,turn-off</sub> = V<sub>EE</sub> - (V<sub>GH</sub> - 3 V), this induces the negative current peak I<sub>G,off</sub> out of the gate which discharges the SJT internal capacitances.

**B:4: External Gate Resistor R<sub>G(EXT)</sub> Selection**

An external gate resistor R<sub>G(EXT)</sub> connected directly to the SJT gate pin acts to deliver a continuous current I<sub>G,steady</sub> during steady on-state. The gate current is determined by:

$$I_{G,steady} = \frac{V_{GL} - V_{GS(FWD)} - V_{Sch}}{R_{G(EXT)} + R_{G(INT)}}$$

The on-state gate-source voltage V<sub>GS(FWD)</sub> can be approximated to 3 V and the Schottky on-state voltage V<sub>Sch</sub> can be approximated to 0.3 V which simplifies the equation to:

$$I_{G,steady} = \frac{V_{GL} - 3.3V}{R_{G(EXT)} + R_{G(INT)}}$$

The desired I<sub>G,steady</sub> is determined by the peak device junction temperature T<sub>J</sub> during operation, drain current I<sub>D</sub>, DC current gain β, and a 50 % safety margin to avoid operating the device in saturation. I<sub>G,steady</sub> may also be approximated from the temperature dependent on-state curves of the device in Figures 1 – 3, provided that a 50 % increase is given.

**Table 3: Passive Output Component List**

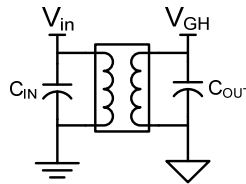
Symbol	Parameter	Values		Units
		Range	Typical	
C <sub>G</sub>	Gate Capacitor, External	5 – 20	10	nF
R <sub>CG</sub>	Damping Resistor of Gate Capacitor	0.5 – 2.0	1.0	Ω
R <sub>ch</sub>	Charging Resistor	500 – 10k	1k	Ω
R <sub>G(EXT)</sub>	Gate Resistor, External	0.5 – 10	3.0	Ω
R <sub>G(INT-ON)</sub>	Gate Resistance, Internal, On-State	0.05 – 0.2	0.19	Ω
D <sub>RG</sub>	Schottky Diode of Gate Resistor	--	--	

**B:5: Optional Gate Current Boost Network**

An optional output totem-pole network may be attached to the IX2204 output pins as shown in Figure 23 using either silicon BJTs (shown) or MOSFETs. This configuration allows the IX2204 to directly drive the BJT bases or MOSFET gates and not supply the full peak and steady state gate current entering the SJT gate. The primary gate current delivery device is transferred to the discrete components which have higher power dissipation ratings than the IX2204.

**B:6: Voltage Supply Isolation**

The DC/DC supply voltage converters are suggested to provide isolation at a minimum of twice the working  $V_{DS}$  on the SJT transistor during off-state to provide adequate protection to circuitry external to the gate drive circuit. Suggested DC/DC converters have an isolation of 3.0 kV or greater. Alternatively, DC/DC converter galvanic isolation may be bypassed and direct connection of variable voltage supplies may be done, this may be convenient during testing and prototyping but carries risk and is not suggested for extended usage.



**Figure 25: Typical DC/DC converter configuration**

**B:7: Signal Isolation**

The gate supply signal is suggested to be isolated to twice the working  $V_{DS}$  on the SJT during off-state to provide adequate protection to circuitry external to the gate drive circuit. This may be done using opto or galvanic isolation techniques.

**B:8: Additional Features**

The IX2204 has additional functionality available which is unused in the given configuration. Desaturation detection and fault status monitoring may be implemented by un-grounding the DESAT, BLANK, and TRISTATE pins and configuring them as recommended in the IX2204 datasheet, available from IXYS. Active miller clamping is also available on other gate drive ICs which may also be desired in some SJT switching applications but is not required, refer to specific gate drive IC datasheets for more information.

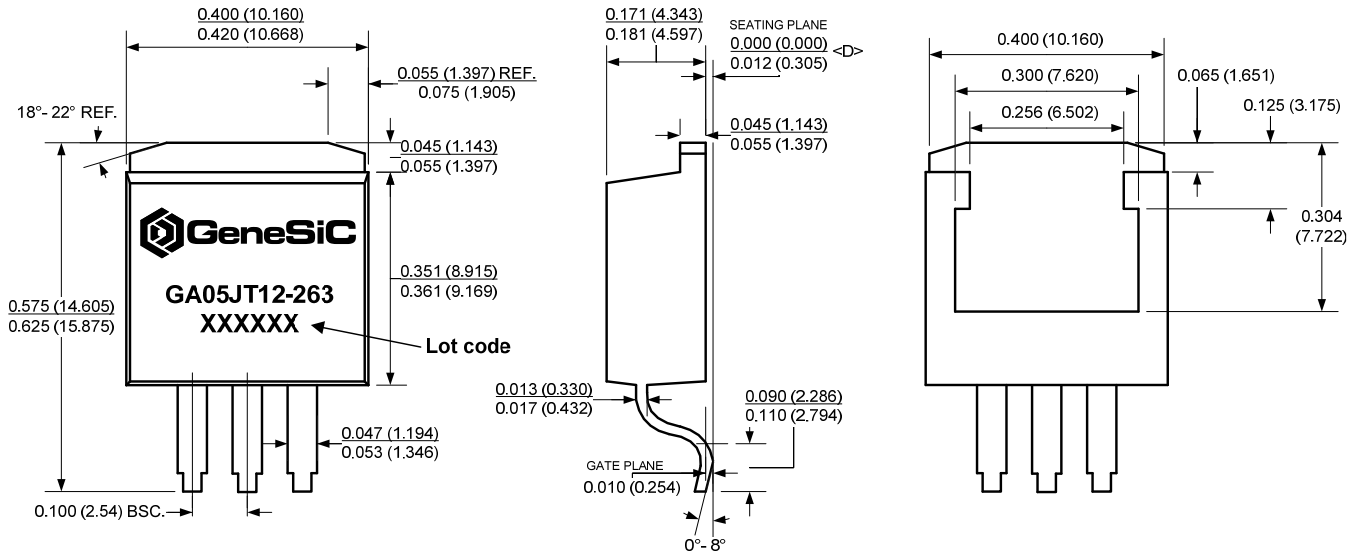
**C: Alternative Gate Drive ICs**

The SJT transistor may be driven similarly to silicon IGBTs or MOSFETs in which a gate driver IC is used to supply positive gate current peaks to the device at turn-on and negative current peaks at turn-off. Table 4 features a partial list of alternative gate drive ICs which may be used; specific product information should be obtained from the individual product manufacturers.

**Table 4: Additional Commercial Gate Drivers Compatible with GA10JT12-263**

Manufacturer	Part Number	Features					Number of Outputs
		Optical Signal Isolation	Desaturation Detection	Active Miller Gate Clamping <sup>3</sup>	High Side Capability		
Avago Tech.	HCPL-316J	✓	✓	–	✓	1	
Avago Tech.	HCPL-322J	✓	✓	✓	✓	1	
IXYS	IXD_604	–	–	–	✓	2	
IXYS	IXD_614	–	–	–	✓	1	
Micrel	MIC4452YN	–	–	–	✓	1	
Microsemi	LX4510	–	–	–	✓	1	
Texas Instruments	UCC27322	–	–	–	✓	1	

<sup>3</sup> – Active Miller Gate Clamping recommended for  $V_{EE} = \text{GND}$  switching applications as SJT and/or output BJT secondary gate discharge path.

**Section VI: Package Dimensions**
**TO-263**
**PACKAGE OUTLINE**

**NOTE**

1. CONTROLLED DIMENSION IS INCH. DIMENSION IN BRACKET IS MILLIMETER.
2. DIMENSIONS DO NOT INCLUDE END FLASH, MOLD FLASH, MATERIAL PROTRUSIONS

**Revision History**

Date	Revision	Comments	Supersedes
2014/08/25	0	Initial release	

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**Section VII: SPICE Model Parameters**

This is a secure document. Please copy this code from the SPICE model PDF file on our website ([http://www.genesicsemi.com/images/products\\_sic/sjt/GA10JT12-263\\_SPICE.pdf](http://www.genesicsemi.com/images/products_sic/sjt/GA10JT12-263_SPICE.pdf)) into LTSPICE (version 4) software for simulation of the GA10JT12-263.

```
*      MODEL OF GeneSiC Semiconductor Inc.
*
*      $Revision:   2.0           $
*      $Date:      25-AUG-2014   $
*
*      GeneSiC Semiconductor Inc.
*      43670 Trade Center Place Ste. 155
*      Dulles, VA 20166
*
*      COPYRIGHT (C) 2014 GeneSiC Semiconductor Inc.
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*
*      These models are provided "AS IS, WHERE IS, AND WITH NO WARRANTY
*      OF ANY KIND EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED
*      TO ANY IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A
*      PARTICULAR PURPOSE."
*      Models accurate up to 2 times rated drain current.
*
.model GA10JT12 NPN
+ IS      5.00E-47
+ ISE     1.26E-28
+ EG      3.23
+ BF      85
+ BR      0.55
+ IKF     5000
+ NF      1
+ NE      2
+ RB      4.67
+ IRB     0.001
+ RBM     0.16
+ RE      0.005
+ RC      0.099
+ CJC     427.39E-12
+ VJC     3.1004
+ MJC     0.4752
+ CJE     1373E-12
+ VJE     10.6442
+ MJE     0.21376
+ XTI     3
+ XTB     -1.27
+ TRC1    6.8E-3
+ VCEO    1200
+ ICRATING 10
+ MFG     GeneSiC_Semiconductor
*
*      End of GA10JT12 SPICE Model
```