# Dual, 2MSPS, 12-Bit, 2 + 2 or 3 + 3 Channel, Simultaneous Sampling ANALOG-TO-DIGITAL CONVERTER

**Check for Samples: ADS7863**

## FEATURES

- **Four Fully- or Six Pseudo-Differential Inputs**
- **SNR: 71dB, THD: –81dB**
- **Programmable and Buffered Internal 2.5V Reference**
- **Flexible Power-Down Features**
- **Variable Power-Supply Ranges: 2.7V to 5.5V**
- **Low-Power Operation: 45mW at 5V**
- **Operating Temperature Range: –40°C to +125°C**
- **Pin-Compatible with ADS7861 and ADS8361 (SSOP package)**

## APPLICATIONS

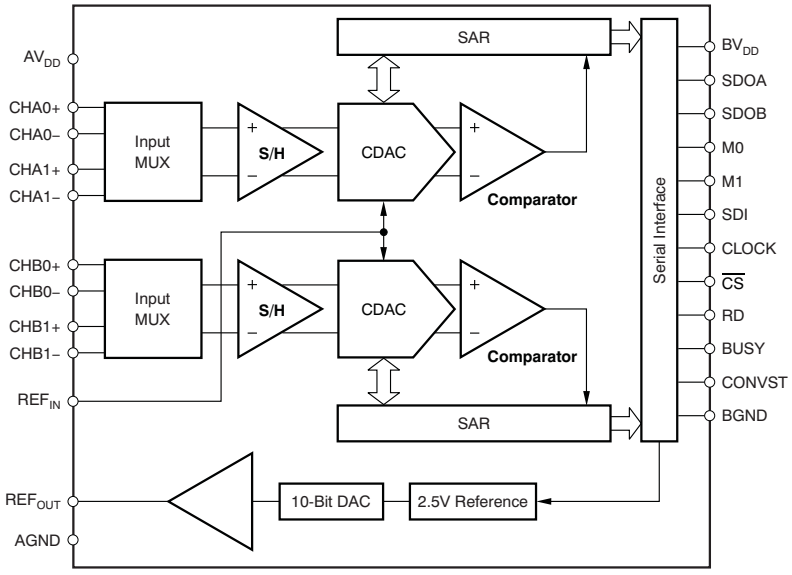
- **Motor Control**
- **Multi-Axis Positioning Systems**
- **Three-Phase Power Control**

## DESCRIPTION

The ADS7863 is a dual, 12-bit, 2MSPS, analog-to-digital converter (ADC) with four fully differential or six pseudo-differential input channels grouped into two pairs for high-speed, simultaneous signal acquisition. Inputs to the sample-and-hold (S/H) amplifiers are fully differential and are maintained differential to the input of the ADC. This architecture provides excellent common-mode rejection of 72dB at 100kHz, which is a critical performance characteristic in noisy environments.

The ADS7863 is pin-compatible with the ADS7861, but offers additional features such as a programmable reference output, flexible supply voltage (2.7V to 5.5V for $AV_{DD}$ and $BV_{DD}$), a pseudo-differential input multiplexer with three channels per ADC, and several power-down features.

The ADS7863 is offered in an SSOP-24 and a 4x4mm QFN-24 package. It is specified over the extended operating temperature range of –40°C to +125°C.




**Functional Block Diagram**

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ORDERING INFORMATION(1)

| PRODUCT | PACKAGE-LEAD | PACKAGE DESIGNATOR | ORDERING NUMBER |
|---|---|---|---|
| ADS7863I | SSOP-24 | DBQ | ADS7863IDBQ |
| | | | ADS7863IDBQR |
| | 4×4 QFN-24 | RGE | ADS7863IRGET |
| | | | ADS7863IRGER |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at ti.com.

## ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

| | | ADS7863 | UNIT |
|---|---|---|---|
| Supply voltage, $AV_{DD}$ to AGND | | –0.3 to +6 | V |
| Supply voltage, $BV_{DD}$ to BGND | | –0.3 to +6 | V |
| Supply voltage, $BV_{DD}$ to $AV_{DD}$ | | 1.5 × $AV_{DD}$ | V |
| Analog and reference input voltage with respect to AGND | | AGND – 0.3 to $AV_{DD}$ + 0.3 | V |
| Digital input voltage with respect to BGND | | BGND – 0.3 to $BV_{DD}$ + 0.3 | V |
| Ground voltage difference \|AGND – BGND\| | | 0.3 | V |
| Input current to any pin except supply pins | | –10 to +10 | mA |
| Maximum virtual junction temperature, $T_J$ | | +150 | °C |
| ESD ratings: | Human body model (HBM), JEDEC standard 22, test method A114-C.01, all pins | ±4000 | V |
| | Charged device model (CDM), JEDEC standard 22, test method C101, all pins | ±1500 | V |

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.


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## RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range, unless otherwise noted.

| PARAMETER | | ADS7863 MIN | ADS7863 NOM | ADS7863 MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage, $AV_{DD}$ to AGND | | 2.7 | 5.0 | 5.5 | V |
| Supply voltage, $BV_{DD}$ to BGND | Low voltage levels | 2.7 | | 3.6 | V |
| | 5V logic levels | 4.5 | 5.0 | 5.5 | |
| Reference input voltage on $REF_{IN}$ | | 0.5 | 2.5 | 2.525 | V |
| Analog differential input voltage (CHXX+) – (CHXX–) | | $-V_{REF}$ | | $+V_{REF}$ | V |
| Operating ambient temperature range, $T_A$ | | –40 | | +125 | °C |

## DISSIPATION RATINGS

| PACKAGE | DERATING FACTOR ABOVE $T_A$ = +25°C | $T_A \le$ +25°C POWER RATING | $T_A$ = +70°C POWER RATING | $T_A$ = +85°C POWER RATING | $T_A$ = +125°C POWER RATING |
|---|---|---|---|---|---|
| SSOP-24 | 10mW/°C | 1250mW | 800mW | 650mW | 250mW |
| QFN-24 (4mm × 4mm) | 22mW/°C | 2740mW | 1750mW | 1420mW | 540mW |

## THERMAL CHARACTERISTICS(1)

Over operating free-air temperature range, unless otherwise noted.

| PARAMETER | | | SSOP-24 | QFN-24 | UNIT |
|---|---|---|---|---|---|
| $\theta_{JA}$ | Junction-to-air thermal resistance | Low-K thermal resistance | 99.8 | 45.6 | °C/W |
| | | High-K thermal resistance | 61.0 | 33.1 | |
| $\theta_{JC}$ | Junction-to-case thermal resistance | | 23.3 | 35 | °C/W |
| $P_{DISS}$ | Device power dissipation at $AV_{DD}$ = 5V and $BV_{DD}$ = 3.3V | | 45.3 | 45.3 | mW |

(1) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface-mount packages.

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## ELECTRICAL CHARACTERISTICS

At $T_A$ = –40°C to +125°C, entire power-supply range, $V_{REF}$ = 2.5V (internal), $f_{CLK}$ = 32MHz, and $t_{DATA}$ = 2MSPS, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | ADS7863 | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP(1) | MAX | |
| **RESOLUTION** | | | 12 | | | Bits |
| **ANALOG INPUT** | | | | | | |
| FSR | Full-scale differential input range | (CHxx+) – (CHxx–) | $–V_{REF}$ | | $+V_{REF}$ | V |
| $V_{IN}$ | Absolute input voltage | CHxx+ or CHxx+ to AGND | –0.1 | | $AV_{DD}$ + 0.1 | V |
| $C_{IN}$ | Input capacitance | CHxx+ or CHxx– to AGND | | 2 | | pF |
| $C_{ID}$ | Differential input capacitance | | | 4 | | pF |
| $I_{IL}$ | Input leakage current | | –1 | | +1 | nA |
| CMRR | Common-mode rejection ratio | Both ADCs, dc to 100kHz | | 72 | | dB |
| **DC ACCURACY** | | | | | | |
| INL | Integral nonlinearity | –40°C < $T_A$ < +125°C | –1.25 | ±0.6 | +1.25 | LSB |
| | | –40°C < $T_A$ < +85°C | –1 | ±0.5 | +1 | LSB |
| DNL | Differential nonlinearity | | –1 | ±0.5 | +1 | LSB |
| $V_{OS}$ | Input offset error | | –3 | ±0.5 | +3 | LSB |
| $V_{OS}$ match | | | –3 | ±0.5 | +3 | LSB |
| $dV_{OS}/dT$ | Input offset thermal drift | | | ±3 | | µV/°C |
| $G_{ERR}$ | Gain error | Referred to voltage at REFIN | –0.5 | | +0.5 | % |
| $G_{ERR}$ match | | | –0.5 | ±0.1 | +0.5 | % |
| $G_{ERR}/dT$ | Gain error thermal drift | Referred to voltage at REFIN | | ±1 | | ppm/°C |
| PSRR | Power-supply rejection ratio | $AV_{DD}$ = 5.5V | | 70 | | dB |
| **AC ACCURACY** | | | | | | |
| SINAD | Signal-to-noise + distortion | $V_{IN}$ = $5V_{PP}$ at 100kHz | 69.8 | 71 | | dB |
| SNR | Signal-to-noise ratio | $V_{IN}$ = $5V_{PP}$ at 100kHz | 70 | 71.5 | | dB |
| THD | Total harmonic distortion | $V_{IN}$ = $5V_{PP}$ at 100kHz | | –81 | –76 | dB |
| SFDR | Spurious-free dynamic range | $V_{IN}$ = $5V_{PP}$ at 100kHz | 76 | 84 | | dB |
| **SAMPLING DYNAMICS** | | | | | | |
| $t_{CONV}$ | Conversion time per ADC | 1MHz < $f_{CLK}$ ≤ 32MHz | 16 | | | $t_{CLK}$ |
| $t_{ACQ}$ | Acquisition time | | 2 | | | $t_{CLK}$ |
| $t_{DATA}$ | Data rate | 1MHz < $f_{CLK}$ ≤ 32MHz | 62.5 | | 2000 | kSPS |
| $t_A$ | Aperture delay | | | | 6 | ns |
| $t_A$ match | | | | 50 | | ps |
| $t_{AJIT}$ | Aperture jitter | | | 50 | | ps |
| $f_{CLK}$ | Clock frequency on CLOCK | | 1 | | 32 | MHz |
| $T_{CLK}$ | Clock period | | 31.25 | | 1000 | ns |
| **INTERNAL VOLTAGE REFERENCE** | | | | | | |
| Resolution | Reference output DAC resolution | | 10 | | | Bits |
| $V_{REFOUT}$ | Reference output voltage | Over 20%...100% DAC range | $0.2V_{REFOUT}$ | | $V_{REFOUT}$ | V |
| | | DAC = 0x3FF, –40°C < $T_A$ < +125°C | 2.485 | 2.500 | 2.515 | V |
| | | DAC = 0x3FF at +25°C | 2.495 | 2.500 | 2.505 | V |
| $dV_{REFOUT}/dT$ | Reference voltage drift | | | ±10 | | ppm/°C |
| $DNL_{DAC}$ | DAC differential nonlinearity | | –9.76 | ±2.44 | 9.76 | mV |
| | | | –4 | ±1 | 4 | LSB |
| $INL_{DAC}$ | DAC integral nonlinearity | | –9.76 | ±1.22 | 9.76 | mV |
| | | | –4 | ±0.5 | 4 | LSB |
| $V_{OSDAC}$ | DAC offset error | $V_{REFOUT}$ = 0.5V | –9.76 | ±2.44 | 9.76 | mV |
| | | | –4 | ±1 | 4 | LSB |

(1) All typical values at $T_A$ = +25°C.


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## ELECTRICAL CHARACTERISTICS (continued)

At $T_A$ = –40°C to +125°C, entire power-supply range, $V_{REF}$ = 2.5V (internal), $f_{CLK}$ = 32MHz, and $t_{DATA}$ = 2MSPS, unless otherwise noted.

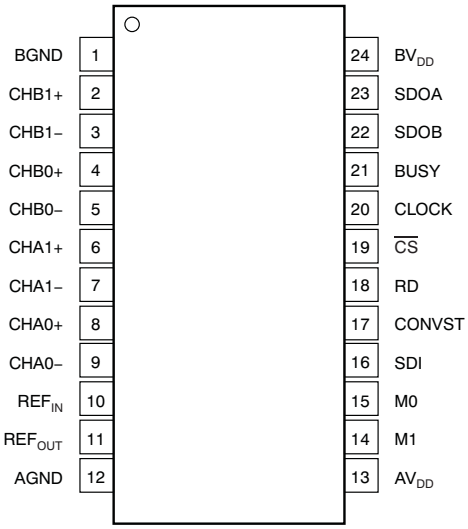
| PARAMETER | | TEST CONDITIONS | ADS7863 MIN | ADS7863 TYP(1) | ADS7863 MAX | UNIT |
|---|---|---|---|---|---|---|
| **INTERNAL VOLTAGE REFERENCE, continued** | | | | | | |
| PSRR | Power-supply rejection ratio | | | 73 | | dB |
| $I_{REFOUT}$ | Reference output dc current | | –2 | | +2 | mA |
| $I_{REFSC}$ | Reference output short-circuit current(2) | | | 50 | | mA |
| $t_{REFON}$ | Reference output settling time | | | 0.5 | | ms |
| **VOLTAGE REFERENCE INPUT** | | | | | | |
| $V_{REF}$ | Reference input voltage range | | 0.5 | | 2.525 | V |
| $I_{REF}$ | Reference input current | | | 50 | | µA |
| $C_{REF}$ | Reference input capacitance | | | 10 | | pF |
| **DIGITAL INPUTS** | | | | | | |
| Logic family | | | CMOS with Schmitt-Trigger | | | |
| $V_{IH}$ | High-level input voltage | | 0.7 × $BV_{DD}$ | | $BV_{DD}$ + 0.3 | V |
| $V_{IL}$ | Low-level input voltage | | –0.3 | | 0.3 × $BV_{DD}$ | V |
| $I_{IN}$ | Input current | $V_{IN}$ = $BV_{DD}$ to BGND | –50 | | +50 | nA |
| $C_{IN}$ | Input capacitance | | | 5 | | pF |
| **DIGITAL OUTPUTS** | | | | | | |
| Logic family | | | | CMOS | | |
| $V_{OH}$ | High-level output voltage | $BV_{DD}$ = 4.5V, $I_{OH}$ = –100µA | $BV_{DD}$ – 0.2 | | | V |
| $V_{OL}$ | Low-level output voltage | $BV_{DD}$ = 4.5V, $I_{OH}$ = 100µA | | | 0.2 | V |
| $I_{OZ}$ | High-impedance-state output current | | –50 | | +50 | nA |
| $C_{OUT}$ | Output capacitance | | | 5 | | pF |
| $C_{LOAD}$ | Load capacitance | | | | 30 | pF |
| **POWER SUPPLY** | | | | | | |
| $AV_{DD}$ | Analog supply voltage | $AV_{DD}$ to AGND | 2.7 | 5.0 | 5.5 | V |
| $BV_{DD}$ | Buffer I/O supply voltage | $BV_{DD}$ to BGND | 2.7 | 3.0 | 5.5 | V |
| $AI_{DD}$ | Analog supply current | $AV_{DD}$ = 2.7V | | 4.5 | 6 | mA |
| | | $AV_{DD}$ = 5.0V | | 6.5 | 8 | |
| | | $AV_{DD}$ = 2.7V, NAP power-down | | 1.1 | 1.5 | |
| | | $AV_{DD}$ = 5.0V, NAP power-down | | 1.4 | 2.0 | |
| | | $AV_{DD}$ = 2.7V, deep power-down | | | 0.001 | |
| | | $AV_{DD}$ = 5.0V, deep power-down | | | 0.001 | |
| $BI_{DD}$ | Buffer I/O supply current | $BV_{DD}$ = 2.7V, $C_{LOAD}$ = 10pF | | 0.5 | 1.3 | mA |
| | | $BV_{DD}$ = 3.3V, $C_{LOAD}$ = 10pF | | 0.9 | 1.6 | |
| $P_{DISS}$ | Power dissipation | $AV_{DD}$ = 2.7V, $BV_{DD}$ = 2.7V | | 13.5 | 19.7 | mW |
| | | $AV_{DD}$ = 5.0V, $BV_{DD}$ = 3.3V | | 35.5 | 45.3 | |

(2) Reference output current is not limited internally.

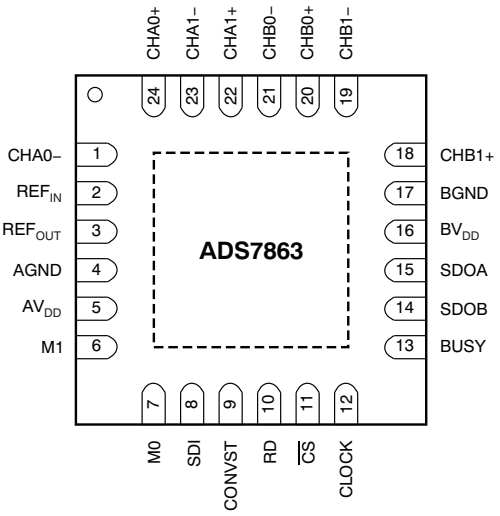
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## DEVICE INFORMATION

**ADS7863IDBQ**
**SSOP-24 (DBQ)**
**(TOP VIEW)**




**ADS7863IRGE**
**4 x 4 QFN-24 (RGE)**
**(TOP VIEW)**

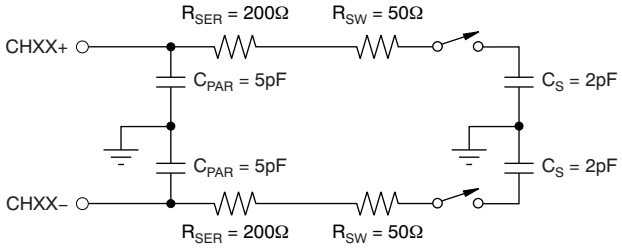



## PIN DESCRIPTIONS

| PIN NUMBER | | NAME | DESCRIPTION |
|---|---|---|---|
| SSOP | QFN | | |
| 1 | 17 | BGND | Buffer I/O ground. Connect to digital ground plane. |
| 2 | 18 | CHB1+ | Noninverting analog input channel B1 |
| 3 | 19 | CHB1– | Inverting analog input channel B1 |
| 4 | 20 | CHB0+ | Noninverting analog input channel B0 |
| 5 | 21 | CHB0– | Inverting analog input channel B0 |
| 6 | 22 | CHA1+ | Noninverting analog input channel A1 |
| 7 | 23 | CHA1– | Inverting analog input channel A1 |
| 8 | 24 | CHA0+ | Noninverting analog input channel A0 |
| 9 | 1 | CHA0– | Inverting analog input channel A0 |
| 10 | 2 | $REF_{IN}$ | Reference voltage input. A ceramic capacitor of 470nF (min) is required at this terminal. |
| 11 | 3 | $REF_{OUT}$ | Reference voltage output. The programmable internal voltage reference output is available on this pin. |
| 12 | 4 | AGND | Analog ground. Connect to analog ground plane. |
| 13 | 5 | $AV_{DD}$ | Analog power supply, 2.7V to 5.5V. Decouple to AGND with a 1μF ceramic capacitor. |
| 14 | 6 | M1 | Mode pin 1. Selects between the SDOx digital outputs (see Table 8). |
| 15 | 7 | M0 | Mode pin 0. Selects between analog input channels (see Table 8). |
| 16 | 8 | SDI | Serial data input. This pin allows the additional features of the ADS7863 to be used but can also be used in ADS7861-compatible manner. |
| 17 | 9 | CONVST | Conversion start. The ADC switches from the sample into the hold mode on the rising edge of CONVST, independent of the status of CLOCK. The conversion itself starts with the next rising edge of CLOCK. |
| 18 | 10 | RD | Read data. Synchronization pulse for the SDOx outputs and SDI input. RD only triggers when $\overline{CS}$ is low. |
| 19 | 11 | $\overline{CS}$ | Chip select. When low, the SDOx outputs are active; when high, the SDOx outputs 3-state. |
| 20 | 12 | CLOCK | External clock input |
| 21 | 13 | BUSY | ADC busy indicator. BUSY goes high when the inputs are in hold mode and returns to low after the conversion has been finished. |
| 22 | 14 | SDOB | Serial data output for converter B. Data are valid on the falling edge of CLOCK. |
| 23 | 15 | SDOA | Serial data output for converter A. When M1 is high, both SDOA and SDOB are active. Data are valid on the falling edge of CLOCK. |
| 24 | 16 | $BV_{DD}$ | Buffer I/O supply, 2.7V to 5.5V. Decouple to BGND with a 1μF ceramic capacitor. |


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## Equivalent Input Circuit




## TIMING CHARACTERISTICS

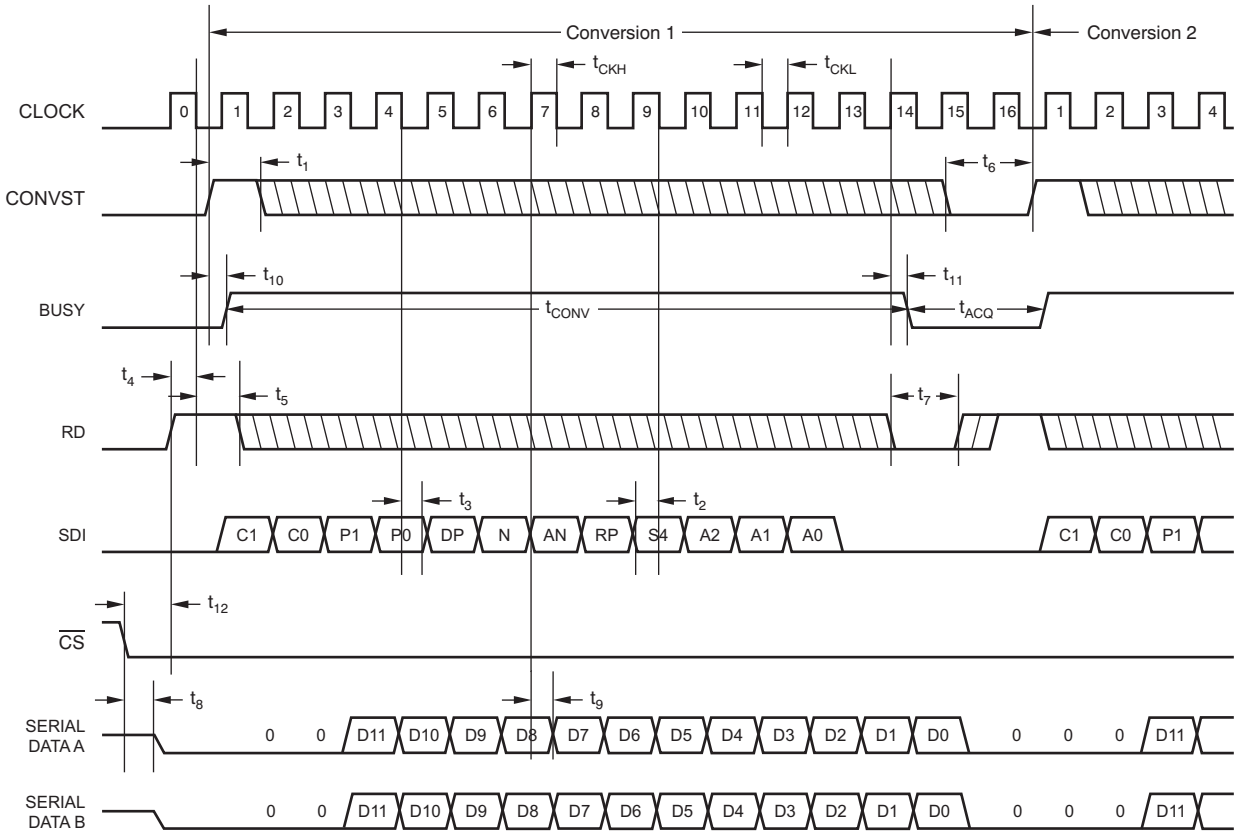
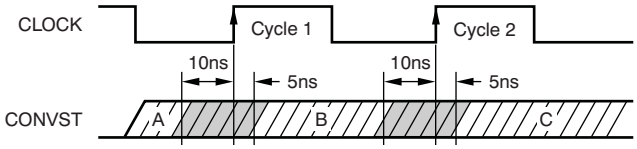



**Figure 1. Detailed Timing Diagram (Mode I)**

## TIMING CHARACTERISTICS (continued)




NOTE: All CONVST commands that occur more than 10ns before the rising edge of cycle '1' of the external clock (Region 'A') initiate a conversion on the rising edge of cycle '1'. All CONVST commands that occur 5ns after the rising edge of cycle '1' or 10ns before the rising edge of cycle 2 (Region 'B') initiate a conversion on the rising edge of cycle '2'. All CONVST commands that occur 5ns after the rising edge of cycle '2' (Region 'C') initiate a conversion on the rising edge of the next clock period.
The CONVST pin should never be switched from LOW to HIGH in the region 10ns prior to the rising edge of the CLOCK and 5ns after the rising edge (gray areas). If CONVST is toggled in this gray area, the conversion could begin on either the same rising edge of the CLOCK or the following edge.

**Figure 2. CONVST Timing**

## TIMING REQUIREMENTS(1)

Over recommended operating free-air temperature range at –40°C to +125°C, $AV_{DD}$ = 5V, and $BV_{DD}$ = 2.7V to 5V, unless otherwise noted.

| SYMBOL | PARAMETER | COMMENTS | ADS7863 MIN | ADS7863 MAX | UNIT |
|---|---|---|---|---|---|
| $t_{CONV}$ | Conversion time | $f_{CLOCK}$ = 32MHz | 406.25 | | ns |
| $t_{ACQ}$ | Acquisition time | $f_{CLOCK}$ = 32MHz | 62.5 | | ns |
| $f_{CLOCK}$ | CLOCK frequency | See Figure 1 | 1 | 32 | MHz |
| $t_{CLOCK}$ | CLOCK period | See Figure 1 | 31.25 | 1000 | ns |
| $t_{CKL}$ | CLOCK low time | See Figure 1 | 9.4 | | ns |
| $t_{CKH}$ | CLOCK high time | See Figure 1 | 9.4 | | ns |
| $t_1$ | CONVST high time | See Figure 1 | 20 | | ns |
| $t_2$ | SDI setup time to CLOCK falling edge | See Figure 1 | 10 | | ns |
| $t_3$ | SDI hold time to CLOCK falling edge | See Figure 1 | 5 | | ns |
| $t_4$ | RD high setup time to CLOCK falling edge | See Figure 1 | 10 | | ns |
| $t_5$ | RD high hold time to CLOCK falling edge | See Figure 1 | 5 | | ns |
| $t_6$ | CONVST low time | See Figure 1 | 1 | | $t_{CLOCK}$ |
| $t_7$ | RD low time relative to CLOCK falling edge | See Figure 1 | 1 | | $t_{CLOCK}$ |
| $t_8$ | $\overline{CS}$ low to SDOx valid | See Figure 1 | 13 | | ns |
| $t_9$ | CLOCK rising edge to DATA valid delay (MIN = minimum hold time of current data; MAX = maximum delay to new data valid) | See Figure 1, 2.7V ≤ $BV_{DD}$ ≤ 3.6V | 4 | 11 | ns |
| | | See Figure 1, 4.5V ≤ $BV_{DD}$ ≤ 5.5V | 3 | 9 | ns |
| $t_{10}$ | CONVST rising edge to BUSY high delay(2) | See Figure 1 | 3 | | ns |
| $t_{11}$ | CLOCK rising edge to BUSY low delay | See Figure 1 | 3 | | ns |
| $t_{12}$ | $\overline{CS}$ low to RD high delay | See Figure 1 | 10 | | ns |

(1) All input signals are specified with $t_R = t_F$ = 1.5ns (10% to 90% of $BV_{DD}$) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
(2) Not applicable in auto-NAP power-down mode.


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## TYPICAL CHARACTERISTICS

Over entire supply voltage range, $V_{REF}$ = 2.5V (internal), $f_{CLK}$ = 32MHz, and $t_{DATA}$ = 2MSPS, unless otherwise noted.

**INTEGRAL NONLINEARITY vs DATA RATE**

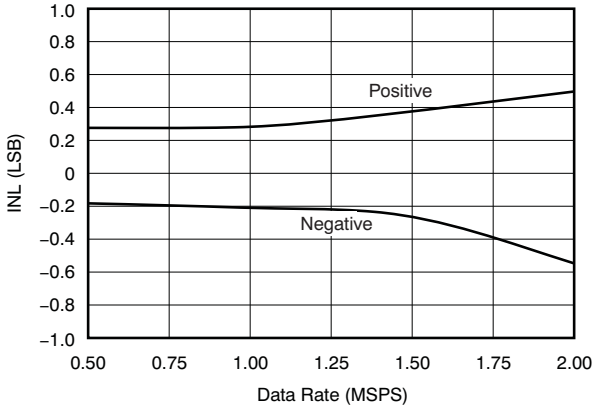



**Figure 3.**

**INTEGRAL NONLINEARITY vs TEMPERATURE**

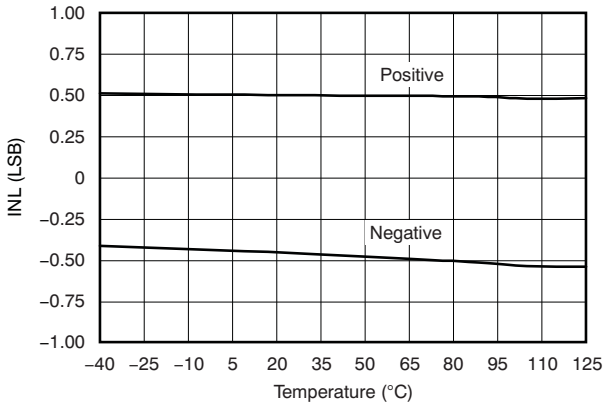



**Figure 4.**

**INTEGRAL NONLINEARITY vs CODE**

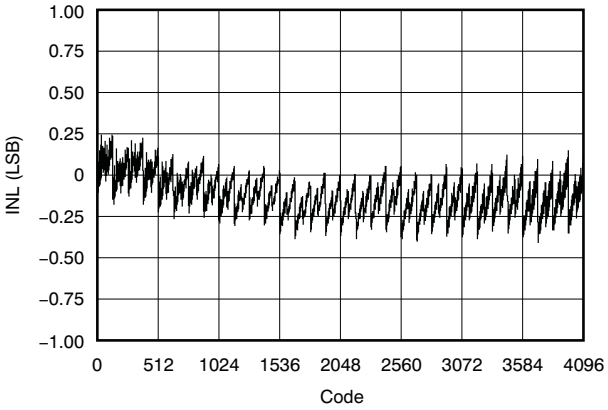



**Figure 5.**

**DIFFERENTIAL NONLINEARITY vs CODE**

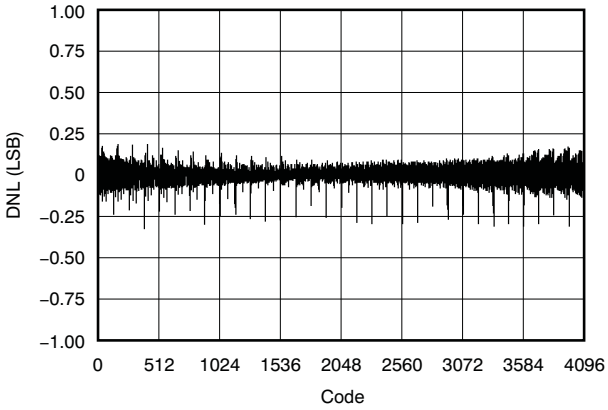



**Figure 6.**

**DIFFERENTIAL NONLINEARITY vs DATA RATE**

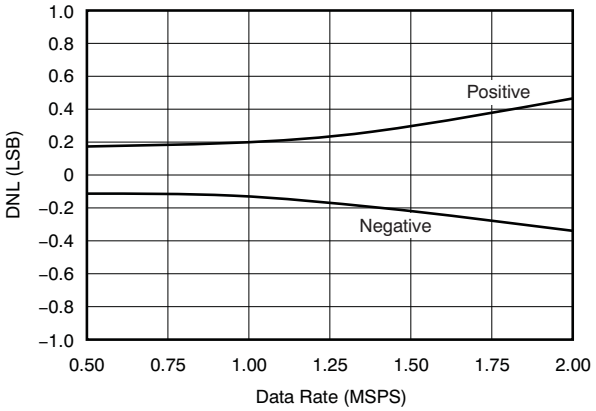



**Figure 7.**

**DIFFERENTIAL NONLINEARITY vs TEMPERATURE**

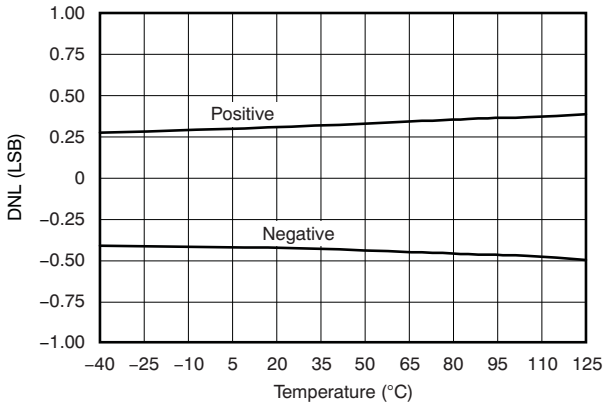



**Figure 8.**

## TYPICAL CHARACTERISTICS (continued)

Over entire supply voltage range, $V_{REF}$ = 2.5V (internal), $f_{CLK}$ = 32MHz, and $t_{DATA}$ = 2MSPS, unless otherwise noted.

**OFFSET ERROR AND OFFSET MATCH vs ANALOG SUPPLY VOLTAGE**

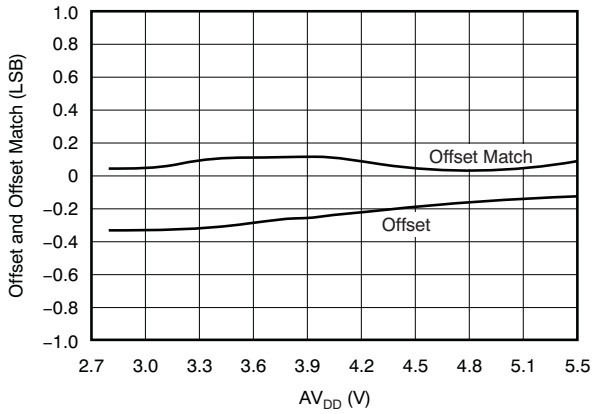



**Figure 9.**

**OFFSET ERROR AND OFFSET MATCH vs TEMPERATURE**

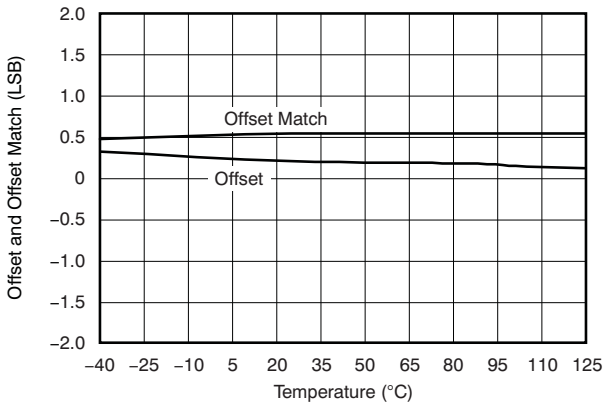



**Figure 10.**

**GAIN ERROR AND GAIN MATCH vs ANALOG SUPPLY VOLTAGE**

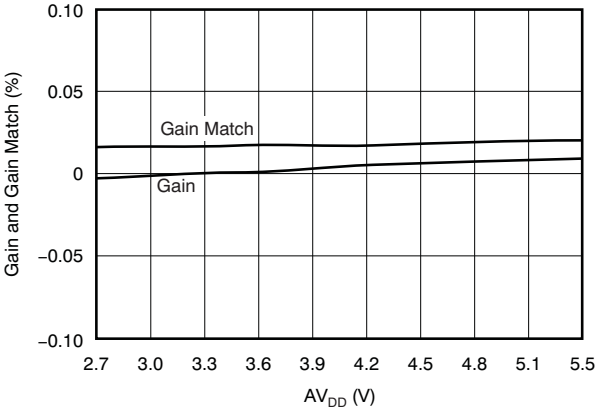



**Figure 11.**

**GAIN ERROR AND GAIN MATCH vs TEMPERATURE**

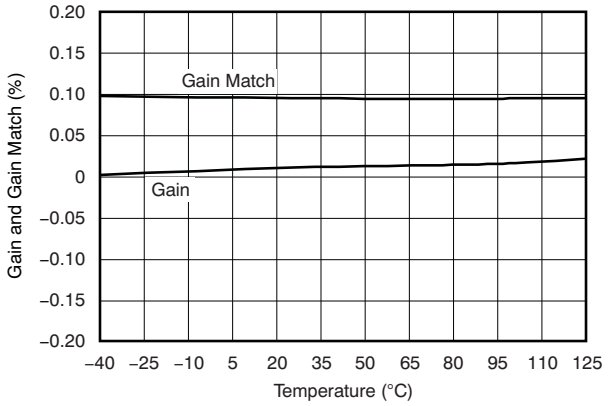



**Figure 12.**

**COMMON-MODE REJECTION RATIO vs ANALOG SUPPLY VOLTAGE**

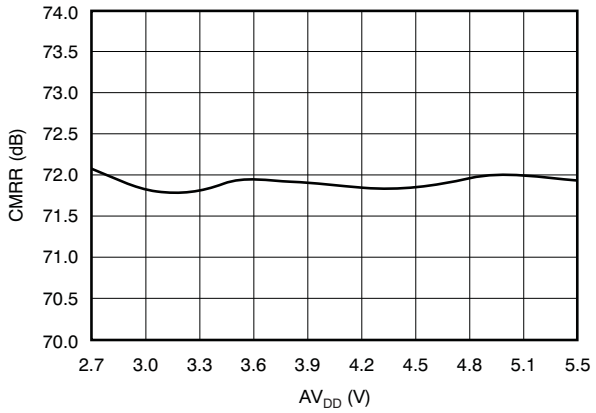



**Figure 13.**

**COMMON-MODE REJECTION RATIO vs TEMPERATURE**

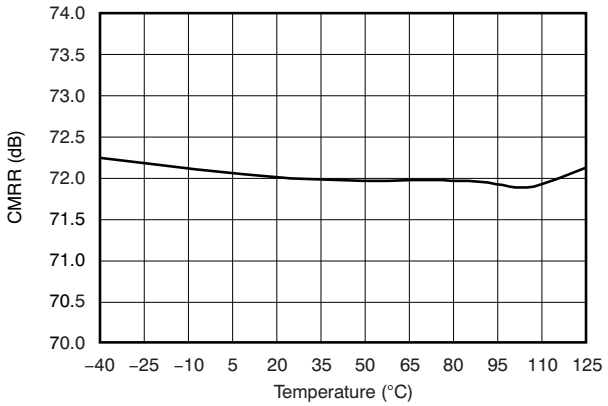



**Figure 14.**


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## TYPICAL CHARACTERISTICS (continued)

Over entire supply voltage range, $V_{REF}$ = 2.5V (internal), $f_{CLK}$ = 32MHz, and $t_{DATA}$ = 2MSPS, unless otherwise noted.

**FREQUENCY SPECTRUM**
**(4096 Point FFT; $f_{IN}$ = 100kHz)**

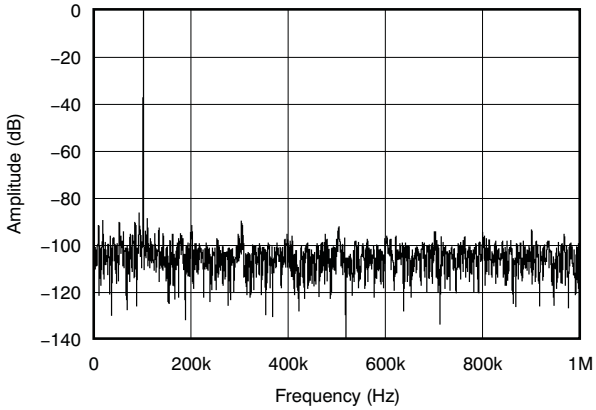



**Figure 15.**

**FREQUENCY SPECTRUM**
**(4096 Point FFT; $f_{IN}$ = 100kHz, $f_{SAMPLE}$ = 1.5MSPS)**

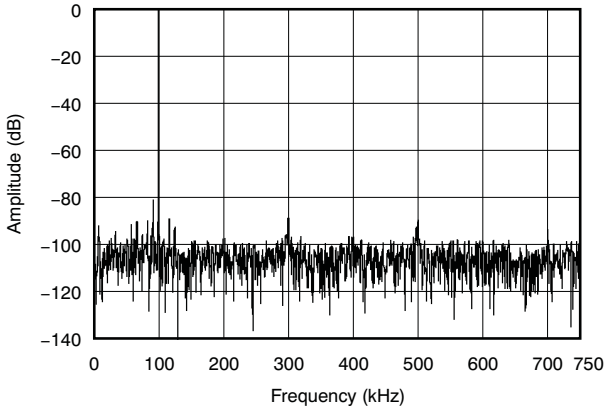



**Figure 16.**

**SIGNAL-TO-NOISE RATIO AND DISTORTION**
**vs INPUT SIGNAL FREQUENCY**

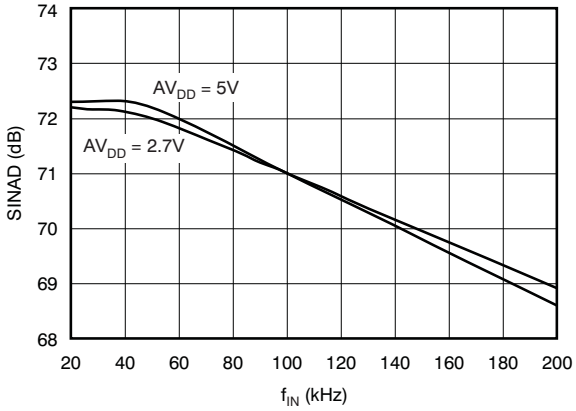



**Figure 17.**

**SIGNAL-TO-RATIO AND DISTORTION**
**vs TEMPERATURE**

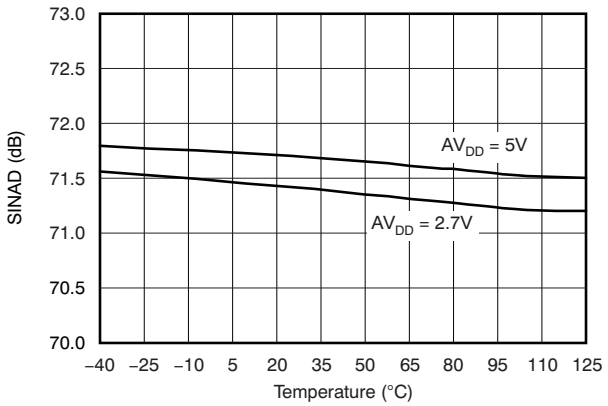



**Figure 18.**

**SIGNAL-TO-NOISE RATIO**
**vs INPUT SIGNAL FREQUENCY**

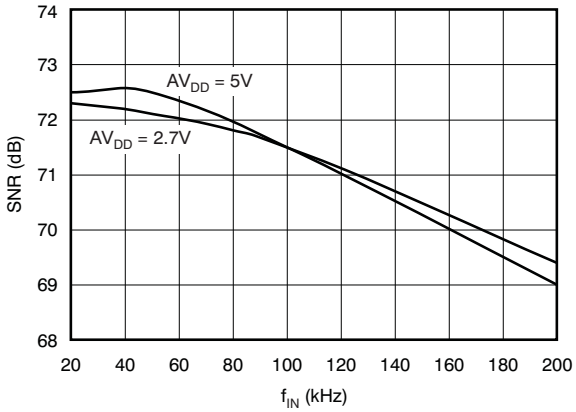



**Figure 19.**

**SIGNAL-TO-NOISE RATIO vs TEMPERATURE**

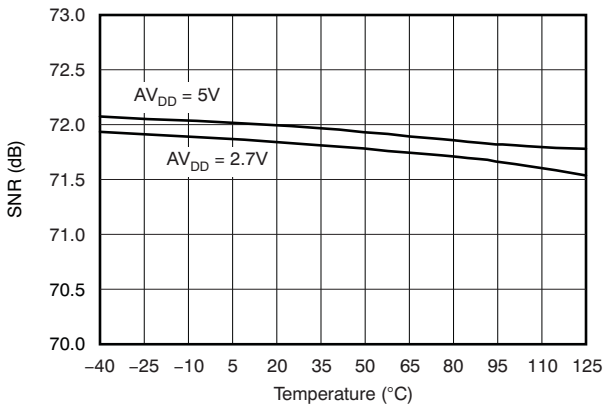



**Figure 20.**

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## TYPICAL CHARACTERISTICS (continued)

Over entire supply voltage range, $V_{REF}$ = 2.5V (internal), $f_{CLK}$ = 32MHz, and $t_{DATA}$ = 2MSPS, unless otherwise noted.

**TOTAL HARMONIC DISTORTION vs INPUT SIGNAL FREQUENCY**

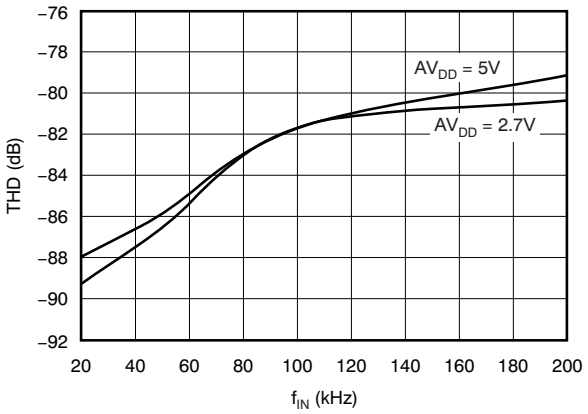



**Figure 21.**

**TOTAL HARMONIC DISTORTION vs TEMPERATURE**

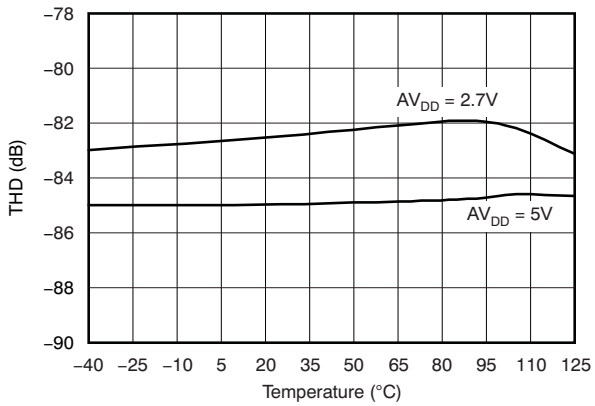



**Figure 22.**

**SPURIOUS-FREE DYNAMIC RANGE vs INPUT SIGNAL FREQUENCY**

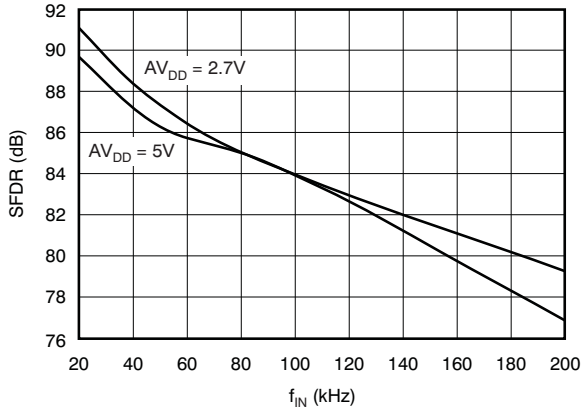



**Figure 23.**

**SPURIOUS-FREE DYNAMIC RANGE vs TEMPERATURE**

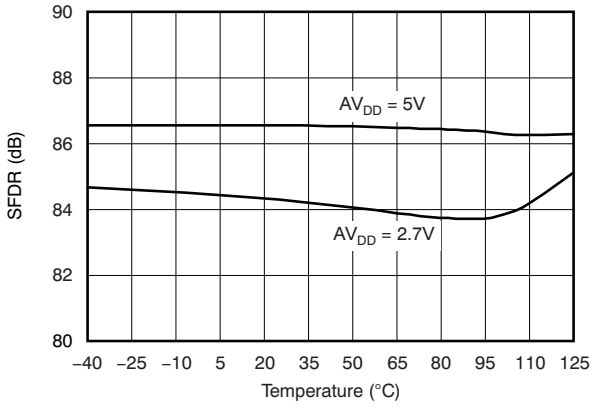



**Figure 24.**

**ANALOG SUPPLY CURRENT vs TEMPERATURE**

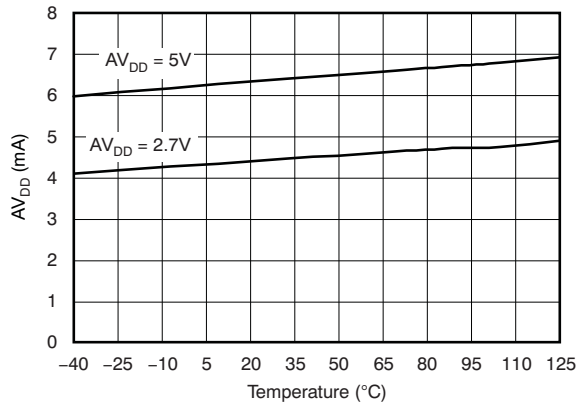



**Figure 25.**

**DIGITAL SUPPLY CURRENT vs TEMPERATURE**

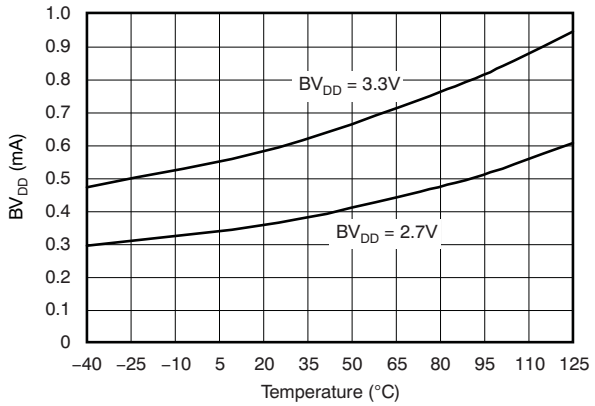



**Figure 26.**


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## TYPICAL CHARACTERISTICS (continued)

Over entire supply voltage range, $V_{REF}$ = 2.5V (internal), $f_{CLK}$ = 32MHz, and $t_{DATA}$ = 2MSPS, unless otherwise noted.

**ANALOG SUPPLY CURRENT vs DATA RATE (Auto-NAP Mode)**

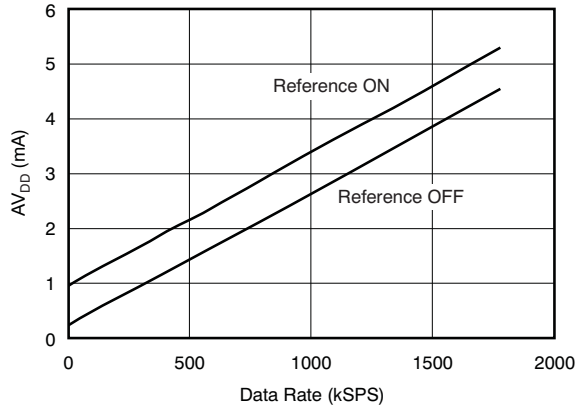



**Figure 27.**

**ANALOG SUPPLY CURRENT vs TEMPERATURE (Auto-NAP Mode)**

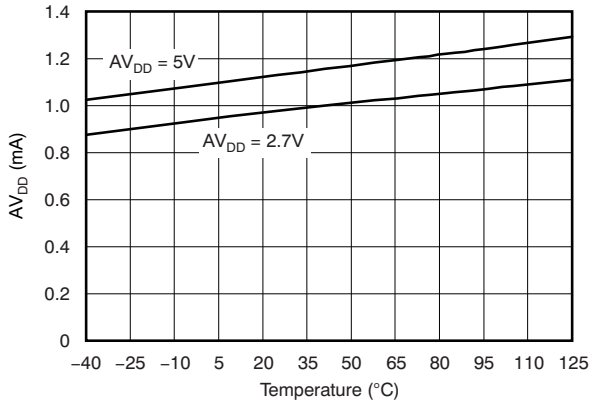



**Figure 28.**

**ANALOG SUPPLY CURRENT vs DATA RATE (Deep Power-Down Mode)**

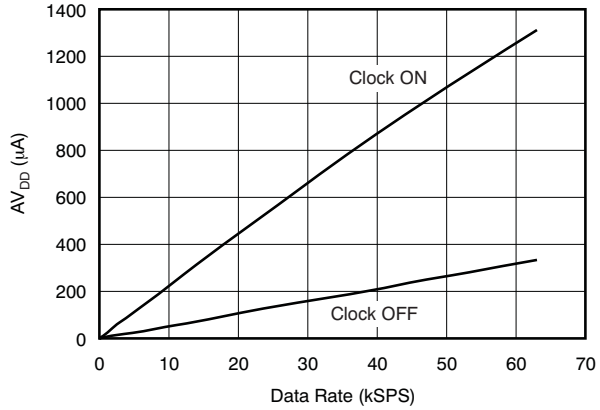



**Figure 29.**

**REFERENCE OUTPUT VOLTAGE vs TEMPERATURE**

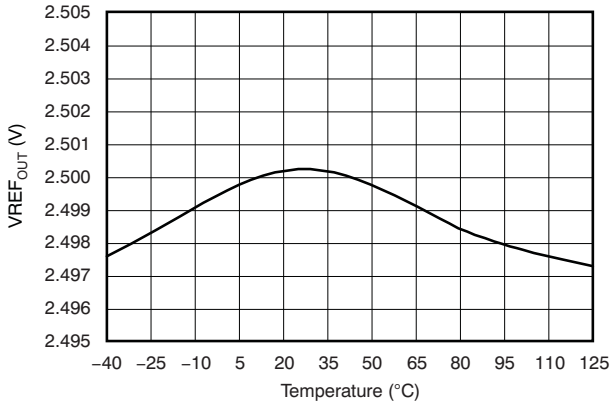



**Figure 30.**

# APPLICATIONS INFORMATION

## GENERAL DESCRIPTION

The ADS7863 includes two 12-bit analog-to-digital converters (ADCs) that operate based on the successive-approximation register (SAR) principle. The ADCs sample and convert simultaneously. Conversion time can be as low as 406.25ns. Adding the acquisition time of 62.5ns and an additional clock cycle for setup/hold time requirements and skew results in a maximum conversion rate of 2MSPS.

Each ADC has a fully differential, 2:1 multiplexer front-end. In many common applications, all negative input signals remain at the same constant voltage (for example, 2.5V). In this type of application, the multiplexer can be used in a pseudo-differential 3:1 mode, where CHx0– functions as a common-mode input and the remaining three inputs (CHx0+, CHx1–, and CHx1+) operate as separate inputs referred to the common-mode input.

The ADS7863 also includes a 2.5V internal reference. The reference drives a 10-bit digital-to-analog converter (DAC), allowing the voltage at the $REF_{OUT}$ pin to be adjusted via the serial interface in 2.44mV steps. A low-noise operational amplifier with unity gain buffers the DAC output voltage and drives the $REF_{OUT}$ pin.

The ADS7863 offers a serial interface that is compatible with the ADS7861. However, instead of the A0 pin of the ADS7861 that controls the channel selection, the ADS7863 offers a serial data input (SDI) pin that supports additional functions described in the Digital section of this data sheet (see also the *ADS7861 Compatibility* section).

## ANALOG

This section addresses the analog input circuit, the ADCs, and the reference design of the device.

### Analog Inputs

Each ADC is fed by an input multiplexer; see Figure 31. Each multiplexer is either used in a fully-differential 2:1 configuration (as described in Table 1) or a pseudo-differential 3:1 configuration (as shown in Table 2). The channel selection is performed using bits C1 and C0 in the SDI register (see also the Serial Data Input section).

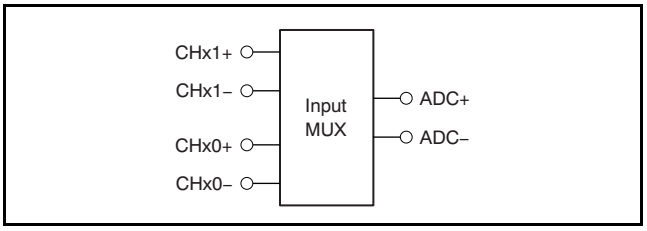



**Figure 31. Input Multiplexer Configuration**

The input path for the converter is fully differential and provides a common-mode rejection of 72dB at 100kHz. The high CMRR also helps suppress noise in harsh industrial environments.

**Table 1. Fully Differential 2:1 Multiplexer Configuration**

| C1 | C0 | ADC+ | ADC– |
|---|---|---|---|
| 0 | 0 | CHx0+ | CHx0– |
| 1 | 1 | CHx1+ | CHx1– |

**Table 2. Pseudo-Differential 3:1 Multiplexer Configuration**

| C1 | C0 | ADC+ | ADC– |
|---|---|---|---|
| 0 | 0 | CHx0+ | CHx0– |
| 0 | 1 | CHx1– | CHx0– |
| 1 | 0 | CHx1+ | CHx0– |

Each of the 2pF sample-and-hold capacitors (shown as $C_S$ in the Equivalent Input Circuit) is connected via switches to the multiplexer output. Opening the switches holds the sampled data during the conversion process. After finishing the conversion, both capacitors are pre-charged for the duration of one clock cycle to the voltage present at the $REF_{IN}$ pin. After the pre-charging, the multiplexer outputs are connected to the sampling capacitors again. The voltage at the analog input pin is usually different from the reference voltage; therefore, the sample capacitors must be charged to within one-half LSB for 12-bit accuracy during the acquisition time $t_{ACQ}$ (see the Timing Characteristics).

Acquisition time is indicated with the BUSY signal being held low. It starts by closing the input switches (after finishing the previous conversion and pre-charging) and finishes with the rising edge of the CONVST signal. If the ADS7863 operates at full speed, the acquisition time is typically 62.5ns.


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The minimum –3dB bandwidth of the driving operational amplifier can be calculated as shown in Equation 1, with *n* = 12 being the resolution of the ADS7863:

$$f_{-3dB} = \frac{\ln(2) \times (n + 1)}{2\pi \times t_{ACQ}} \quad (1)$$

With $t_{ACQ}$ = 62.5ns, the minimum bandwidth of the driving amplifier is 23MHz. The required bandwidth can be lower if the application allows a longer acquisition time.

A gain error occurs if a given application does not fulfill the settling requirement shown in Equation 1. As a result of precharging the capacitors, linearity and THD are not directly affected, however.

The OPA365 from Texas Instruments is recommended as a driver; in addition to offering the required bandwidth, it provides a low offset and also offers excellent THD performance.

The phase margin of the driving operational amplifier is usually reduced by the ADC sampling capacitor. A resistor placed between the capacitor and the amplifier limits this effect; therefore, an internal 200Ω resistor ($R_{SER}$) is placed in series with the switch. The switch resistance ($R_{SW}$) is typically 50Ω (see Equivalent Input Circuit).

The differential input voltage range of the ADC is $\pm V_{REF}$, the voltage at the $REF_{IN}$ pin.

It is important to keep the voltage to all inputs within the 0.3V limit below AGND and above $AV_{DD}$ while not allowing dc current to flow through the inputs. Current is only necessary to recharge the sample-and-hold capacitors.

### Analog-to-Digital Converter (ADC)

The ADS7863 includes two SAR-type, 2MSPS, 12-bit ADCs (shown in the functional block diagram on the front page of this data sheet).

#### *CONVST*

The analog inputs are held with the rising edge of the CONVST (conversion start) signal. The setup time of CONVST referred to the next rising edge of CLOCK (system clock) is 10ns (minimum). The conversion automatically starts with the rising CLOCK edge. CONVST should not be issued during a conversion, that is, when BUSY is high.

RD (read data) and CONVST can be shorted to minimize necessary software and wiring. The RD signal is triggered by the ADS7863 on the falling edge of CLOCK. Therefore, the combined signals must be activated with the rising CLOCK edge. The conversion then starts with the subsequent rising CLOCK edge.

#### *CLOCK*

The ADC uses an external clock in the range of 1MHz to 32MHz. 12 clock cycles are needed for a complete conversion; the following clock cycle is used for pre-charging the sample capacitors and a minimum of two clock cycles are required for the sampling. With a minimum of 16 clocks used for the entire process, one clock cycle is left for the required setup and hold times along with some margin for delay caused by layout. The clock input can remain low between conversions (after applying the 16th falling edge to complete a running conversion). It can also remain low after applying the 14th falling edge during a DAC register write access if the device is not required to perform a conversion on CHBx (for example, during an initiation phase after power-up).

The CLOCK duty cycle should be 50%. However, the ADS7863 functions properly with a duty cycle between 30% and 70%.

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### *RESET*

The ADS7863 features an internal power-on-reset (POR) function. When the device is powered up, the POR sets the device in default mode when the AVDD reaches 1.8V. An external software reset can be issued using SDI register bits A[2:0] (see the *Digital* section).

### *$REF_{IN}$*

The reference input is not buffered and is directly connected to the ADC. The converter generates spikes on the reference input voltage because of internal switching. Therefore, an external capacitor to the analog ground (AGND) should be used to stabilize the reference input voltage. This capacitor should be at least 470nF. Ceramic capacitors (X5R type) with values up to 1μF are commonly available as SMD in 0402 size.

### *$REF_{OUT}$*

The ADS7863 includes a low-drift, 2.5V internal reference source. This source feeds a 10-bit string DAC that is controlled via the serial interface. As a result of this architecture, the voltage at the $REF_{OUT}$ pin is programmable in 2.44mV steps and can be adjusted to specific application requirements without the use of additional external components.

However, the DAC output voltage should not be programmed below 0.5V to ensure the correct functionality of the reference output buffer. This buffer is connected between the DAC and the $REF_{OUT}$ pin, and is capable of driving the capacitor at the $REF_{IN}$ pin. A minimum of 470nF is required to keep the reference stable (see the previous discussion of $REF_{IN}$ above). For applications that use an external reference source, the internal reference can be disabled using bit RP in the SDI Register (see the *Digital* section). The settling time of the $REF_{OUT}$ pin is 500μs, maximum with the reference capacitor connected. The default value of the $REF_{OUT}$ pin after power-up is 2.5V.

For operation with a 2.7V analog supply and a 2.5V reference, the internal reference buffer requires a rail-to-rail input and output. Such buffers typically contain two input stages; when the input voltage passes the mid-range area, a transition occurs at the output because of switching between the two input stages. In this voltage range, rail-to-rail amplifiers generally show a very poor power-supply rejection.

As a result of this poor performance, the ADS7863 buffer has a fixed transition at DAC code 509 (0x1FD). At this code, the DAC may show a jump of up to 10mV in its transfer function.


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## DIGITAL

This section addresses the timing and control of the ADS7863 serial interface.

### Serial Data Input (SDI)

The serial data input or SDI pin is coupled to RD and clocked into the ADS7863 on each falling edge of CLOCK. The data word length of the SDI Register is 12 bits. Table 3 shows the register structure. The data must be transferred MSB-first. Table 4 through Table 6 describe specific bits of this register. The default value of this register after power-up is 0x000.

**Table 3. SDI Register Contents**

| SDI REGISTER BIT | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| C1 | C0 | P1 | P0 | DP | N | AN | RP | S4 | A2 | A1 | A0 |

**Table 4. C1 and C0: Channel Selection**

| C1 | C0 | ADC A/B | |
|---|---|---|---|
| | | POSITIVE INPUT | NEGATIVE INPUT |
| 0 | 0 | CHA0+/CHB0+ | CHA0–/CHB0– |
| 0 | 1 | CHA1–/CHB1– | CHA0–/CHB0– |
| 1 | 0 | CHA1+/CHB1+ | CHA0–/CHB0– |
| 1 | 1 | CHA1+/CHB1+ | CHA1–/CHB1– |

**Table 5. P1 and P0: Additional Features Enable**

| P1 | P0 | FUNCTION |
|---|---|---|
| 0 | 0 | Additional features are not changed |
| 0 | 1 | Update additional features |
| 1 | 0 | Reserved for factory test (do not use) |
| 1 | 1 | Additional features are not changed |

**DP:** Deep power-down enable ('1' = device in deep power-down mode)

**N:** Nap power-down enable ('1' = device in Nap power-down mode)

**AN:** AutoNap power-down enable ('1' = device in AutoNap power-down mode)

**RP:** Reference power-down ('1' = reference turned off)

**S4:** Special read mode for Modes II and IV ('1' = special mode enabled)

**Table 6. A2, A1, and A0: DAC Control and Device Reset**

| A2 | A1 | A0 | FUNCTION |
|---|---|---|---|
| 0 | 0 | 0 | No action |
| 0 | 0 | 1 | DAC write with next access |
| 0 | 1 | 0 | No action |
| 0 | 1 | 1 | DAC read with next access |
| 1 | 0 | 0 | No action |
| 1 | 0 | 1 | Device reset |
| 1 | 1 | 0 | No action |
| 1 | 1 | 1 | No action |

All additional features become active with the rising edge of the 12th CLOCK signal after issuing the RD pulse.

The reference DAC is controlled by the 12-bit DAC register that can also be accessed using the SDI pin (see Figure 40 for details). Table 7 shows the content of this register; the default value after power-up is 0x3FF.

**Table 7. DAC Register Contents**

| DAC REGISTER CONTENT | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| X(1) | X | MSB | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |

(1) X = don't care.

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### Serial Data Output (SDOx)

Converted data on the SDOx pins become valid with the third falling CLOCK edge after generating an RD pulse. The following sections explain the different modes of operation in detail.

The digital output code format of the ADS7863 is binary twos complement, as shown in Table 9. Conversion results can be read out multiple times until a new conversion is issued from the CONVST input.

### Timing and Control

**IMPORTANT:**

Consider the Detailed Timing Diagram (Figure 1) and CONVST timing diagram (Figure 2) shown in the Timing Characteristics section. For maximum data throughput, the descriptions and diagrams given in this data sheet assume that the CONVST and RD pins are tied together. Note that they can also be controlled independently.

The operation of the ADS7863 can be configured in four different modes by using the mode pins M0 and M1, as shown in Table 8.

Pin M0 sets either manual or automatic channel selection. In manual mode, the SDI register bits C[1:0] are used to select between channels CHx0 and CHx1; in automatic operation, the SDI register bits C[1:0] are ignored and channel selection is controlled by the device after each conversion. Pin M1 selects between serial data being transmitted simultaneously on both outputs SDOA and SDOB for each channel respectively, or using only the SDOA output for transmitting data from both channels (see Figure 32 through Figure 39 and the associated text for more information).

**Table 8. M0/M1 Truth Table**

| M0 | M1 | CHANNEL SELECTION | SDOx USED |
|---|---|---|---|
| 0 | 0 | Manual (via SDI) | SDOA and SDOB |
| 0 | 1 | Manual (via SDI) | SDOA only |
| 1 | 0 | Automatic | SDOA and SDOB |
| 1 | 1 | Automatic | SDOA only |

Additionally, the SDI pin is used for controlling device functionality; see the *Serial Data Input* section for details.

**Table 9. ADS7863 Output Data Format**

| DESCRIPTION | DIFFERENTIAL INPUT VOLTAGE (CHXX+) – (CHXX–) | INPUT VOLTAGE AT CHXX+ (CHXX– = $V_{REF}$ = 2.5V) | BINARY CODE | HEXADECIMAL CODE |
|---|---|---|---|---|
| Positive full-scale | $V_{REF}$ | 5V | 0111 1111 1111 | 7FF |
| Mid-scale | 0V | 2.5V | 0000 0000 0000 | 000 |
| Mid-scale – 1LSB | $–V_{REF}/4096$ | 2.49878V | 1111 1111 1111 | FFF |
| Negative full-scale | $–V_{REF}$ | 0V | 1000 0000 0000 | 800 |


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## MODE I

With the M0 and M1 pins both set to '0', the ADS7863 enters manual channel control operation and outputs data on both SDOA and SDOB, respectively. The SDI pin switches between the channels. A conversion is initiated by bringing CONVST high.

16 clock cycles are required to perform a single conversion. With the rising edge of CONVST, the ADS7863 switches asynchronously to the external CLOCK from sample to hold mode.

After some delay ($t_{12}$), the BUSY output pin goes high and remains high for the duration of the conversion cycle. On the falling edge of the second CLOCK cycle, the ADS7863 latches in the channel for the next conversion cycle, depending on the status of the SDI Register bits C[1:0]. $\overline{CS}$ must be brought low to enable both serial outputs. Data are valid on the falling edge of every 16 clock cycles per conversion. The first two bits are set to '0'. The subsequent data contain the 12-bit conversion result (the most significant bit is transferred first), followed by two '0's (see Figure 1 and Figure 32).

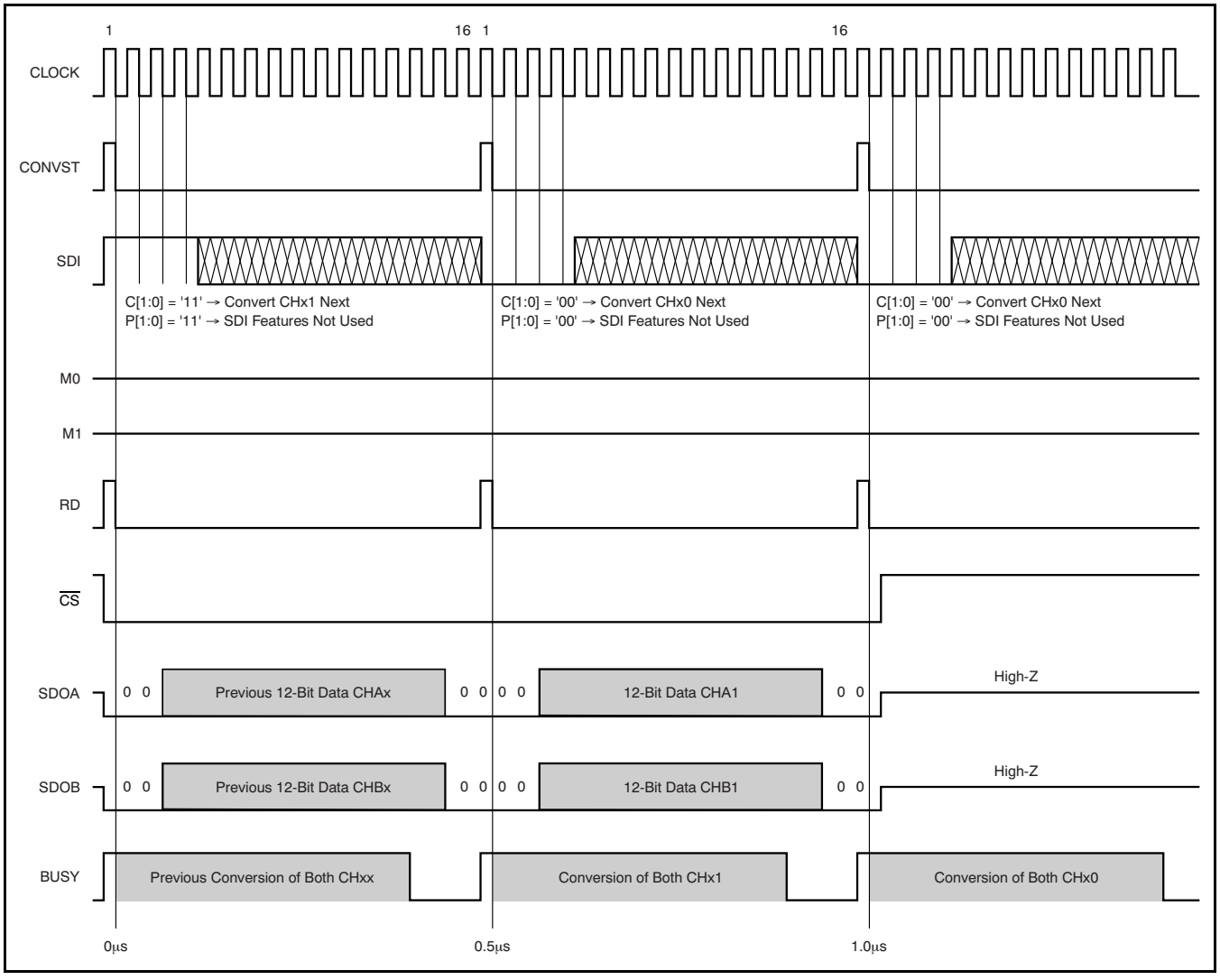



**Figure 32. Mode I Timing Diagram (M0 = 0; M1 = 0)**

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## MODE II

With M0 = '0' and M1 set to '1', the ADS7863 also operates in manual channel control mode and outputs data on the SDOA pin only while SDOB is set to 3-state. All other pins function in the same manner as they do in Mode I.

Because it takes 32 clock cycles to output the results from both ADCs (instead of 16 cycles, if M1 = '0'), the ADS7863 requires 1.0µs to perform a complete conversion/read cycle. If the CONVST signal is issued every 0.5µs (required for the RD signal) as in Mode I, every second pulse is ignored; see Figure 33.

The output data consist of a '0' followed by an ADC indicator ('0' for CHAx or '1' for CHBx), 12 bits of conversion results, and another '00'.

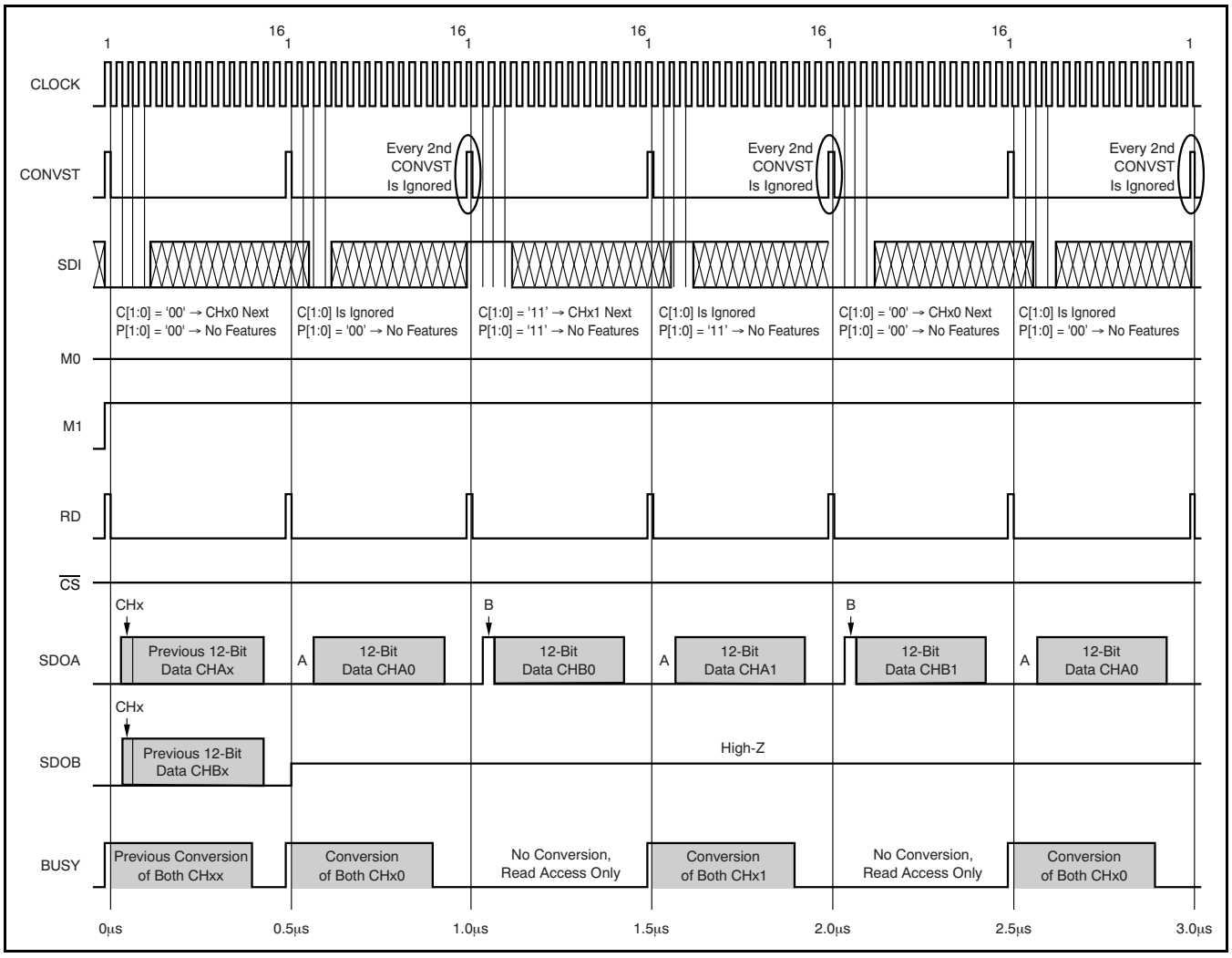



**Figure 33. Mode II Timing Diagram (M0 = 0; M1 = 1)**


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## MODE III

With M0 set to '1' and M1 = '0', the ADS7863 automatically cycles between the differential inputs (ignoring the SDI register bits C[1:0]) while offering the conversion result of CHAx on SDOA and the conversion result of CHBx on SDOB (see Figure 34).

Output data consist of a channel indicator ('0' for CHx0 or '1' for CHx1), followed by a '0', 12 bits of conversion results, and another '00'.

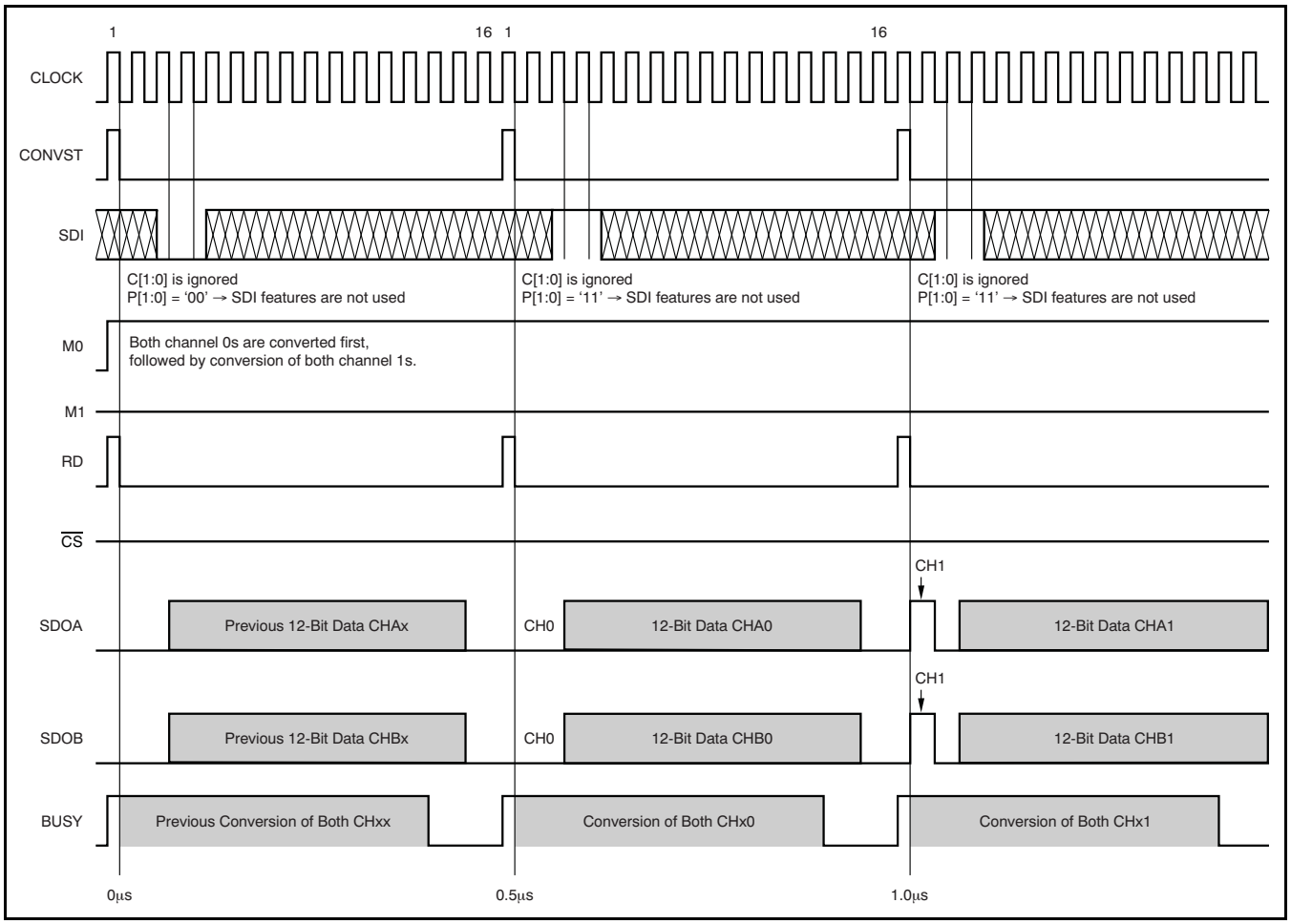



**Figure 34. Mode III Timing Diagram (M0 = 1; M1 = 0)**

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## MODE IV

In the same way as Mode II, Mode IV uses the SDOA output line exclusively to transmit data while the differential channels are switched automatically. Following the first conversion after M1 goes high, the SDOB output 3-states (see Figure 35).

Output data consist of a channel indicator ('0' for CHx0 or '1' for CHx1), followed by the ADC indicator ('0' for CHAx or '1' for CHBx), 12 bits of conversion results, and end with '00'.

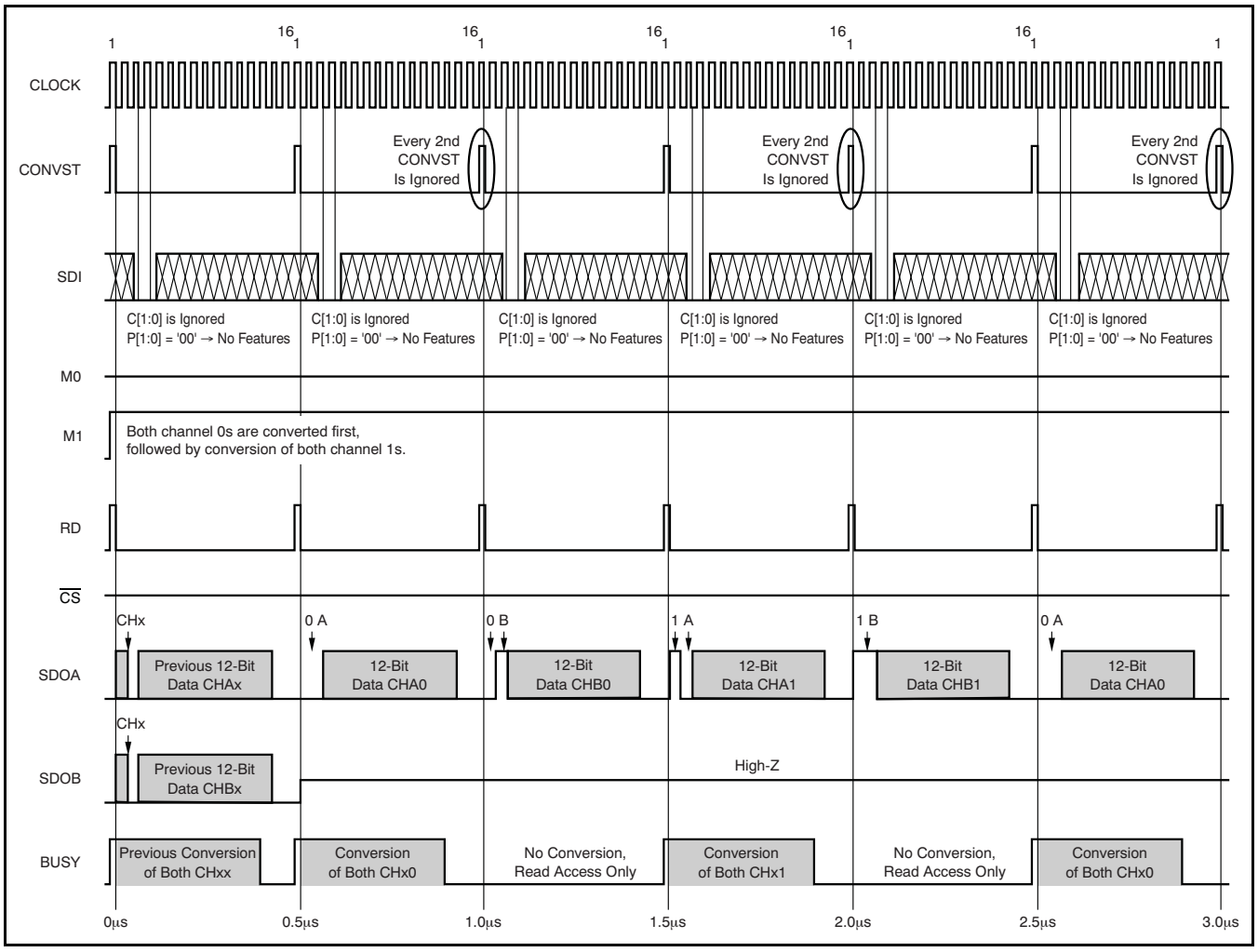



**Figure 35. Mode IV Timing Diagram (M0 = 1 ; M1 = 1)**


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### SPECIAL MODE II (Not ADS7861-Compatible)

For Mode II, a special read mode is available in the ADS7863 where both data results can be read out, triggered by a single RD pulse. To activate this mode, bit S4 in the SDI Register must be set to '1' (see also the Serial Data Input section).

The CONVST and RD pins can remain tied together, but do not need to be issued every 16 CLOCK cycles. Output data are presented on both terminals, SDOA and SDOB. Figure 36 illustrates the special read mode.

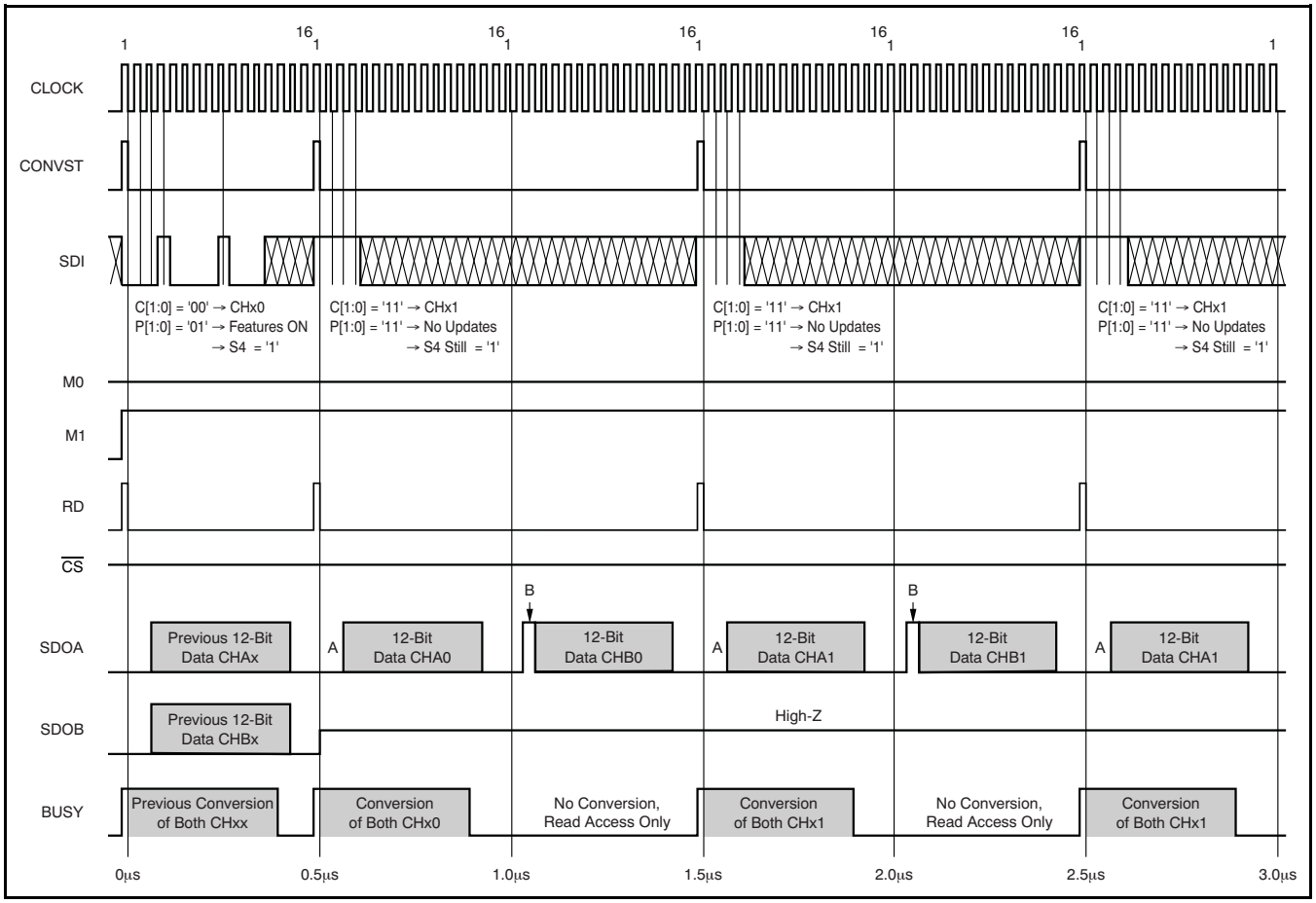



**Figure 36. Special Mode II Timing Diagram (M0 = 0; M1 = 1; S4 = 1)**

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## SPECIAL MODE IV (Not ADS7861-Compatible)

Analogous to Special Mode II, the ADS7863 also offers a special read mode for Mode IV in which both data results of a conversion can be read, triggered by a single RD pulse. In this case as well, bit S4 in the SDI register must be set to '1' while the CONVST and RD pins can still be tied together .

As with Special Mode II, these two pins do not need to be issued every 16 CLOCK cycles. Data are available on the SDOA pin.

This special read mode (shown in Figure 37) is not available in Mode I or Mode III.

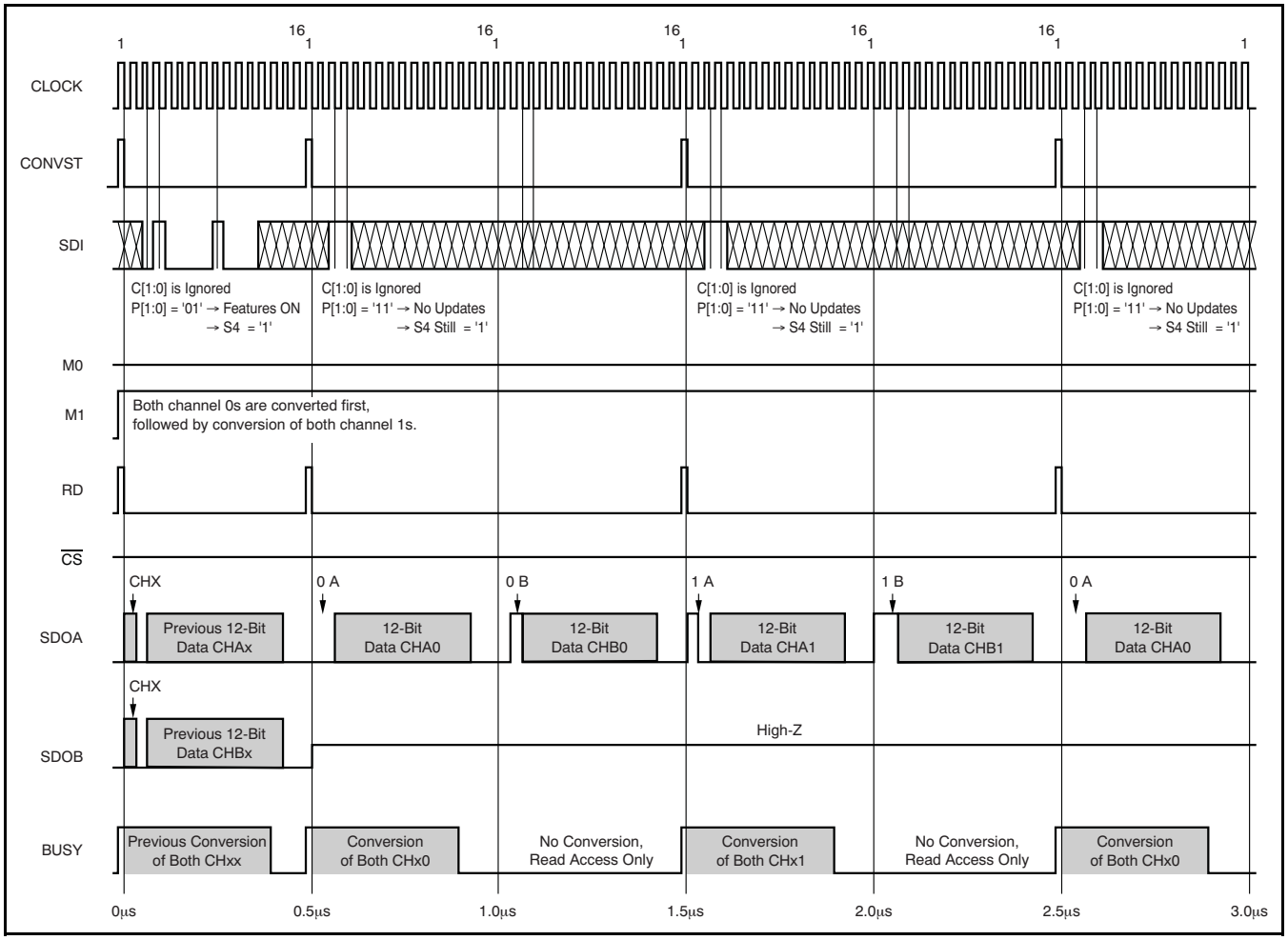



**Figure 37. Special Mode IV Timing Diagram (M0 = 1; M1 = 1; S4 = 1)**


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### PSEUDO-DIFFERENTIAL MODE I (Not ADS7861-Compatible)

In Mode I, the ADS7863 input multiplexers can also operate in a pseudo-differential manner. In this case, SDI bits C[1:0] are used to choose the channels accordingly.

For more details, see the Serial Data Input section. Data are available on both output terminals, SDOA and SDOB.

The input multiplexer cannot be used for pseudo-differential signals in Mode III or Mode IV.

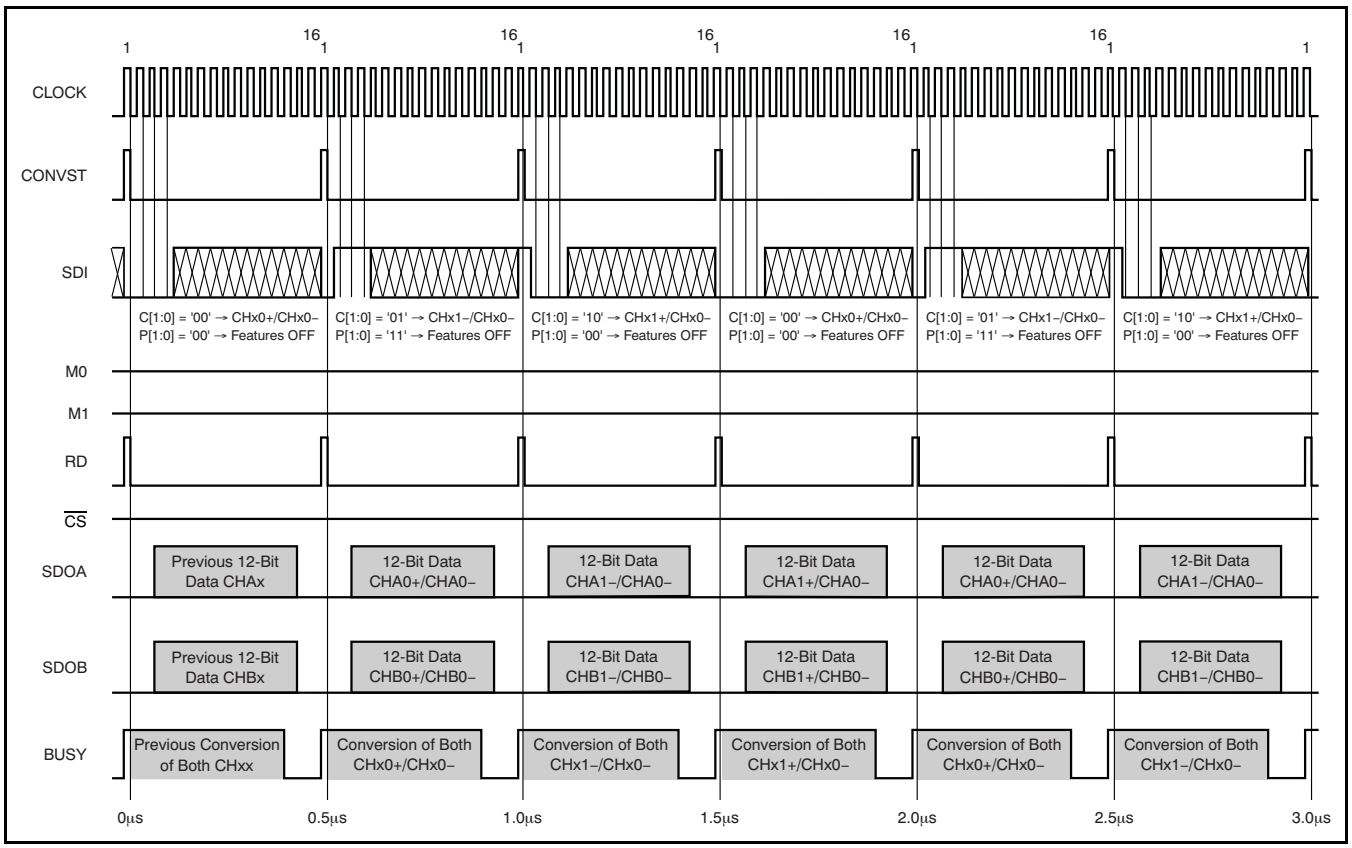



**Figure 38. Pseudo-Differential Mode I (M0 = 0; M1 = 0)**

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## PSEUDO-DIFFERENTIAL MODE II (Not ADS7861-Compatible)

In Mode II, the ADS7863 input multiplexers can also operate in a pseudo-differential configuration. In this case, output data are available on terminal SDOA only, while SDOB is held in 3-state.

Channel switching is performed by setting the C[1:0] bits in the SDI Register accordingly (see also the Serial Data Input section).

The input multiplexer cannot be used for pseudo-differential signals in Mode III or Mode IV.

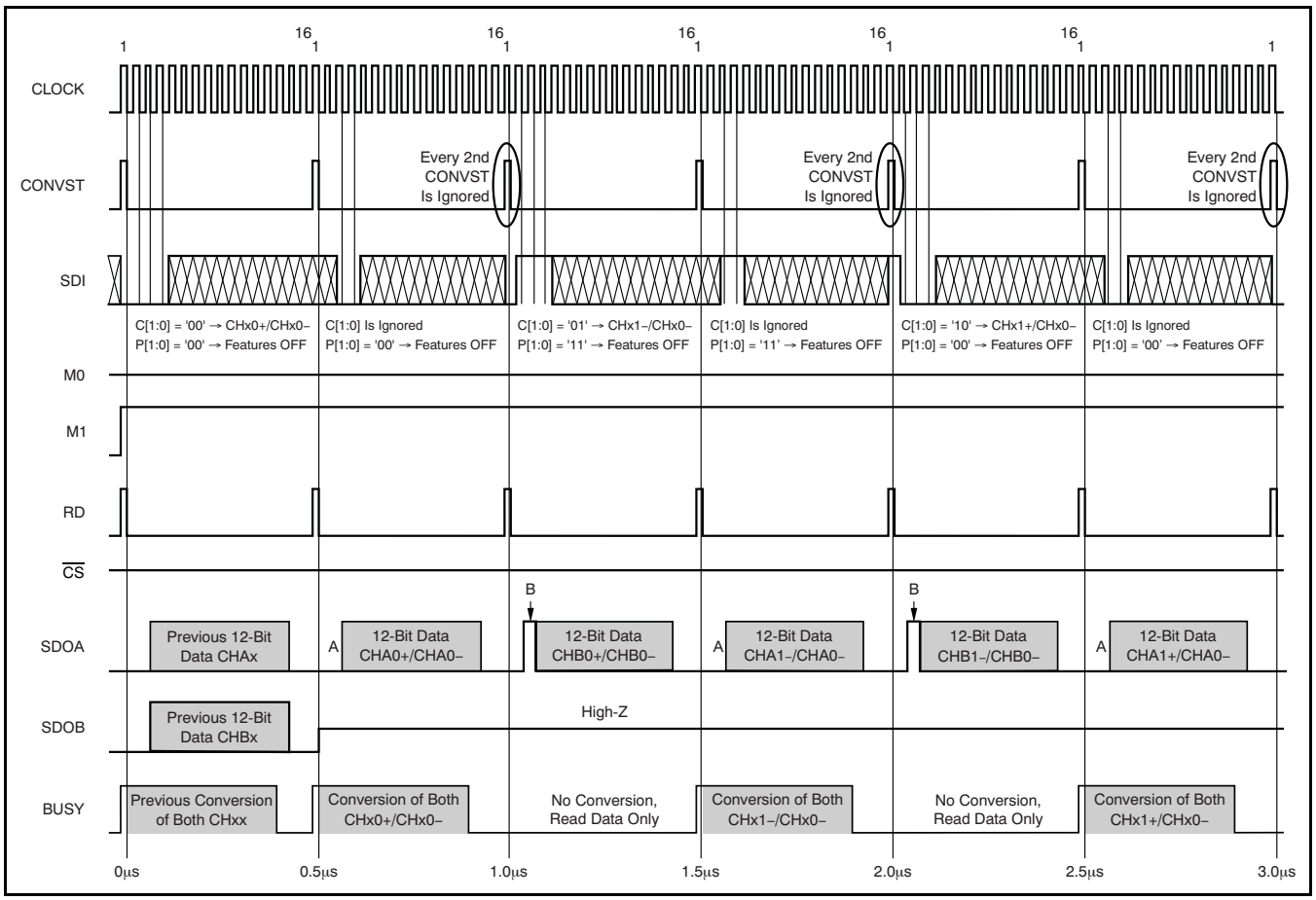



**Figure 39. Pseudo-Differential Mode II (M0 = 0; M1 = 1)**


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### Programming the Reference DAC (Not ADS7861-Compatible)

The internal reference DAC can be set by issuing an RD pulse while providing an SDI word with P[1:0] = '01' and A[2:0] = '001'. Thereafter, a second RD pulse must be generated with an SDI word starting with the first two bits being ignored, followed by the actual 10-bit DAC value (see Figure 40).

To verify the DAC setting, an RD pulse must be generated while providing an SDI word containing P[1:0] = '01' and A[2:0] = '011' to initialize the DAC read access. Triggering the RD line again causes the SDOA output to send '0000' followed by the 10-bit DAC value and another '00'. During the second RD access, data present on SDI are ignored, while in Mode I and Mode III valid conversion data for channel B are present on SDOB; the conversion results of channel A are lost. The default value of the DAC register after power-up is 0x3FF, corresponding to a reference voltage of 2.5V on the $REF_{OUT}$ pin.

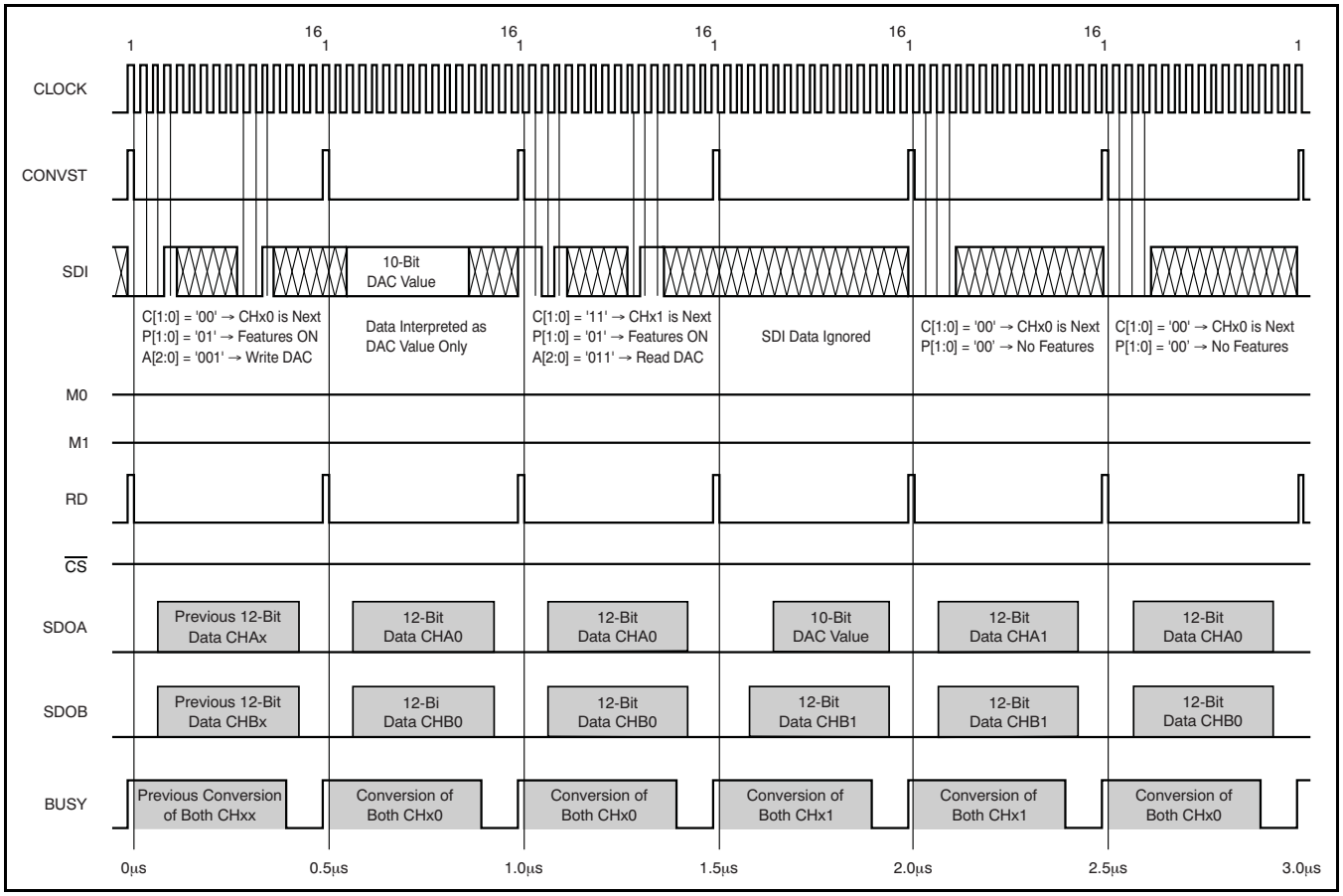



**Figure 40. DAC Write and Read Access Timing Diagram**

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### Power-Down Modes and Reset (Not ADS7861-Compatible)

The ADS7863 has a comprehensive built-in power-down feature. There are three power-down modes: deep power-down, nap power-down, and auto-nap power-down. All three power-down modes are activated with the 12th falling CLOCK edge of the SDI access, during which the related bit asserts (DP = '1', N = '1', or AN = '1'). All modes are deactivated by de-asserting the respective bit in the SDI Register. Contents of the SDI Register are not affected by any of the power-down modes. Any ongoing conversion aborts when deep or nap power-down is initiated. Table 10 lists the differences among the three power-down modes.

In ***deep power-down mode,*** all functional blocks except the digital interface are disabled. The analog block has its bias currents turned off. In this mode, the power dissipation reduces to 1μA within 2μs. The wake-up time from deep power-down mode is 1μs.

In ***nap power-down mode,*** the ADS7863 turns off the biasing of the comparator and the mid-voltage buffer within 200ns. The device goes into nap power-down mode regardless of the conversion state.

The ***auto-nap power-down mode*** is very similar to the nap mode. The only differences are the methods of powering down and waking up the device. The SDI Register bit AN is only used to enable/disable this feature. If the auto-nap mode is enabled, the ADS7863 turns off the biasing automatically after finishing a conversion; thus, the end of conversion actually activates the auto-nap power-down. The device powers down within 200ns in this mode, as well. Triggering a new conversion by applying a CONVST pulse puts the device back into normal operation and automatically starts a new conversion six CLOCK cycles later. Therefore, a complete conversion cycle takes 19 CLOCK cycles; thus, the maximum throughput rate in auto-nap power-down mode is reduced to 1.68MSPS.

To issue a ***device reset***, an RD pulse must be generated along with an SDI word containing A[2:0] = '101'. With the 12th falling edge after generating the RD pulse, the entire device—including the serial interface—is forced into reset. After approximately 500ns, the serial interface becomes active again.

**Table 10. Power-Down Modes**

| POWER-DOWN TYPE | ENABLED BY | ACTIVATED BY | ACTIVATION TIME | RESUMED BY | REACTIVATION TIME | DISABLED BY |
|---|---|---|---|---|---|---|
| Deep | DP = ‘1’ | 13th clock | 2μs | DP = ‘0’ | 1μs | DP = ‘0’ |
| Nap | N = ‘1’ | 13th clock | 200ns | N = ‘0’ | 3 clocks | N = ‘0’ |
| Auto-nap | AN = ‘1’ | Each end of conversion | 200ns | CONVST pulse | 3 clocks | AN = ‘0’ |


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## ADS7861 COMPATIBILITY

The ADS7863IDBQ is pin-compatible with the ADS7861E/EB/EG4. However, there are some differences between the two devices that must be considered when migrating from the ADS7861 to the ADS7863 in an existing design.

### SDI versus A0

One of the differences is that pin 16 (A0), which updates the internal SDI register of the ADS7863, is used in conjunction with M0 to select the input channel on the ADS7861.

If, in an existing design, the ADS7861 is used in two-channel mode (M0 = '0') and the status of the A0 pin is unchanged within the first four clock cycles after issuing a conversion start (rising edge of CONVST), the ADS7863 would act similarly to the ADS7861 and convert either channels CHx0 (if SDI is held low during the entire period) or channels CHx1 (if SDI is held high during the entire period). Figure 33 describes the behavior of the ADS7863 in such a situation.

The ADS7863 can also be used to replace the ADS7861 when run in four-channel mode (M0 = '1'). In this case, the A0 pin is held static (high or low) which is also required in the case of SDI to prevent accidental update of the SDI register.

In both cases described above, the additional features of the ADS7863 (pseudo-differential input mode, programmable reference voltage output, and the different power-down modes) could not be accessed but the hardware and software would remain backward-compatible to the ADS7861.

### $REF_{IN}$

The ADS7863 offers an unbuffered $REF_{IN}$ input with a code-dependent input impedance while featuring a programmable and buffered reference output ($REF_{OUT}$). The ADS7861 offers a high-impedance (buffered) reference input. If an existing ADS7861-based design uses the internal reference of the device and relies on an external resistor divider to adjust the input voltage range of the ADC, migration to ADS7863 requires one of the following conditions:

- a software change to setup the internal reference DAC properly via SDI while removing the external resistors; ***or***
- an additional external buffer between the resistor divider and the required 470nF (minimum) capacitor on the $REF_{IN}$ input.

In the latter case, while the capacitor stabilizes the reference voltage during the entire conversion, the buffer has to re-charge it by providing an average current only; thus the required minimum bandwidth of the buffer can be calculated using Equation 2:

$$f_{-3dB} = \frac{\ln(2) \times 2}{2\pi \times 16 \times T_{CLK}} \quad (2)$$

The buffer must also be capable of driving the 470nF load while maintaining its stability.

### Timing

The only timing requirement that may cause the ADS7863 to malfunction in an existing ADS7861-based design is the CONVST high time ($t_1$) which is specified to be 20ns minimum while the ADS7861 works properly with a pulse as short as 15ns. All the other required minimum setup and hold times are specified to be either the same as or lower than the ADS7863; therefore, there are no conflicts with the ADS7861 requirements.

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## APPLICATION INFORMATION

The absolute minimum configuration of the ADS7863 is shown in Figure 41. In this case, the ADS7863 is used in dual-channel mode only, with the default settings of the device after power up.

The input signal for the amplifiers must fulfill the common-mode voltage requirements of the ADS7863 in this configuration. The actual values of the resistors and capacitors depend on the bandwidth and performance requirements of the application.

Those values can be calculated using Equation 3, with n = 12 being the resolution of the ADS7863.

$$f_{FILTER} = \frac{\ln(2) \times (n + 1)}{2 \times \pi \times 2 \times R \times C} \quad (3)$$

It is recommended to use a capacitor value of at least 20pF.

Keep the acquisition time in mind; the resistor value can be calculated as shown in Equation 4 for each of the series resistors (with n = 12, being the resolution of the ADSS7863).

$$R = \frac{t_{ACQ}}{\ln(2) \times (n + 1) \times 2 \times C} \quad (4)$$

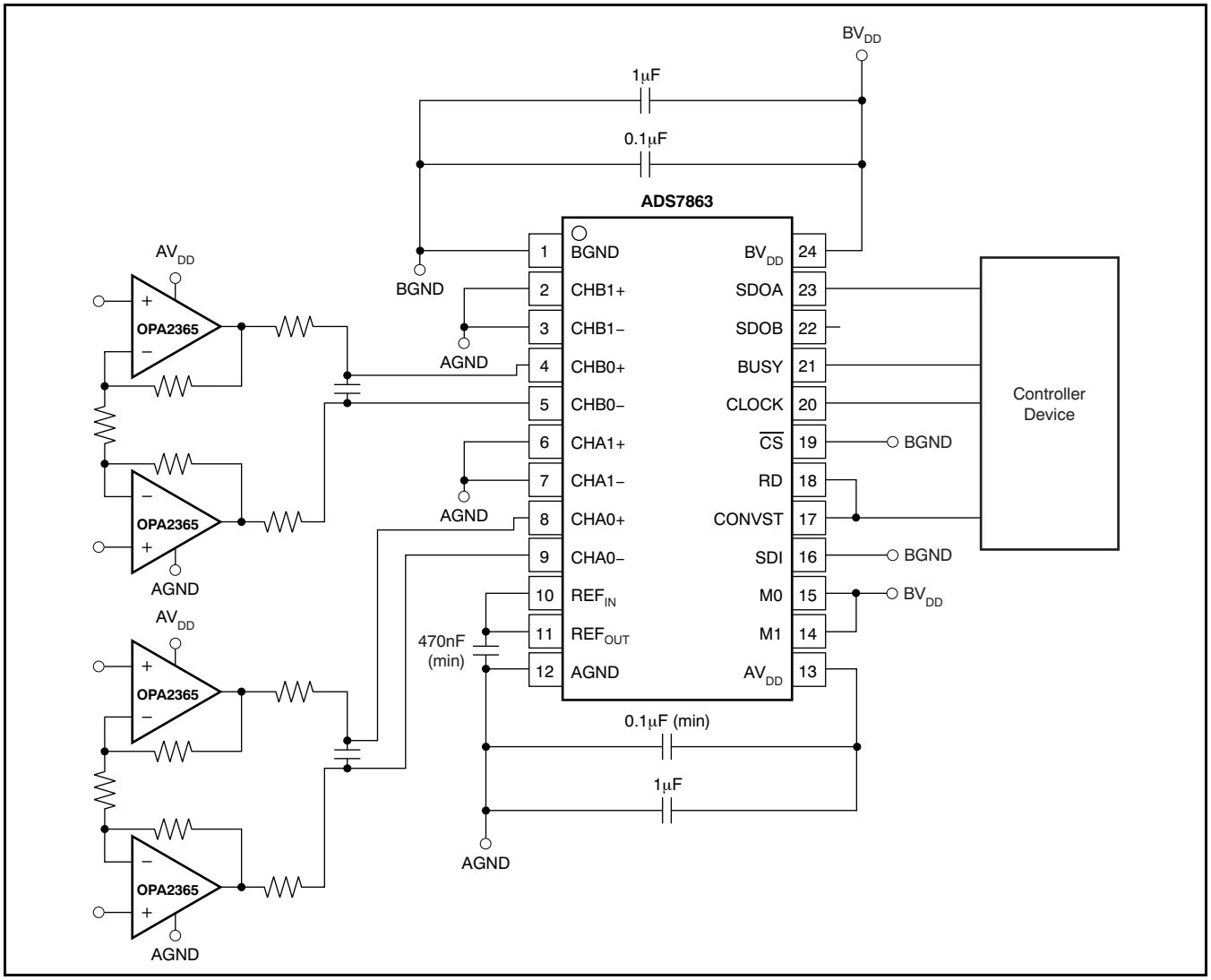



**Figure 41. Minimum ADS7863 Configuration**


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## LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS7863 circuitry. This condition is particularly true if the CLOCK input is approaching the maximum throughput rate. In this case, it is recommended to have a fixed phase relationship between CLOCK and CONVST. The best performance can be achieved when the digital interface is run in SPI mode; thus, the CLOCK signal is switched off after the 16th cycle and remains low when CONVST is issued.

Additionally, the basic SAR architecture is quite sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just before latching the output of the analog comparator. Therefore, when driving any single conversion for an *n*-bit SAR converter, there are *n* windows in which large external transient voltages can affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, or high-power devices. The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. These errors can change if the external event also changes in time with respect to the CLOCK input.

With this possibility in mind, power to the ADS7863 should be clean and well-bypassed. A 0.1μF ceramic bypass capacitor should be placed as close to the device as possible. In addition, a 1μF to 10μF capacitor is recommended. If needed, an even larger capacitor and a 5Ω or 10Ω series resistor may be used to low-pass filter a noisy supply.

If the reference voltage is external and originates from an operational amplifier, be sure that it can drive the reference capacitor without oscillation. The connection between the output of the external reference driver and $REF_{IN}$ should be of low resistance (10Ω max) to minimize any code-dependent voltage drop on this path.

### Grounding

The xGND pins should be connected to a clean ground reference. These connections should be kept as short as possible to minimize the inductance of these paths. It is recommended to use vias connecting the pads directly to the ground plane. In designs without ground planes, the ground trace should be kept as wide as possible. Avoid connections that are too near the grounding point of a microcontroller or digital signal processor.

Depending on the circuit density of the board, placement of the analog and digital components, and the related current loops, a single solid ground plane for the entire printed circuit board (PCB) or a dedicated analog ground area may be used. In an instance of a separated analog ground area, ensure a low-impedance connection between the analog and digital ground of the ADC by placing a bridge underneath (or next to) the ADC. Otherwise, even short undershoots on the digital interface with a value lower than –300mV lead to conduction of ESD diodes, causing current flow through the substrate and degrading the analog performance.

During the PCB layout, care should also be taken to avoid any return currents crossing any sensitive analog areas or signals. No signal must exceed the limit of –300mV with respect to the according ground plane. Figure 42 illustrates the recommended layout of the ground and power-supply connections for both package options.

### Supply

The ADS7863 has two separate supplies: the $BV_{DD}$ pin for the digital interface and the $AV_{DD}$ pin for all remaining circuits.

$BV_{DD}$ can range from 2.7V to 5.5V, allowing the ADS7863 to easily interface with processors and controllers. To limit the injection of noise energy from external digital circuitry, $BV_{DD}$ should be filtered properly. Bypass capacitors of 0.1μF and 10μF should be placed between the $BV_{DD}$ pin and the ground plane.

$AV_{DD}$ supplies the internal analog circuitry. For optimum performance, a linear regulator (for example, the UA7805 family) is recommended to generate the analog supply voltage in the range of 2.7V to 5.5V for the ADS7863 and the necessary analog front-end circuitry.

Bypass capacitors should be connected to the ground plane such that the current is allowed to flow through the pad of the capacitor (that is, the vias should be placed on the opposite side of the connection between the capacitor and the power-supply pin of the ADC).

### Digital Interface

To further optimize device performance, a resistor of 10Ω to 100Ω can be used on each digital pin of the ADS7863. In this way, the slew rate of the input and output signals is reduced, limiting the noise injection from the digital interface.

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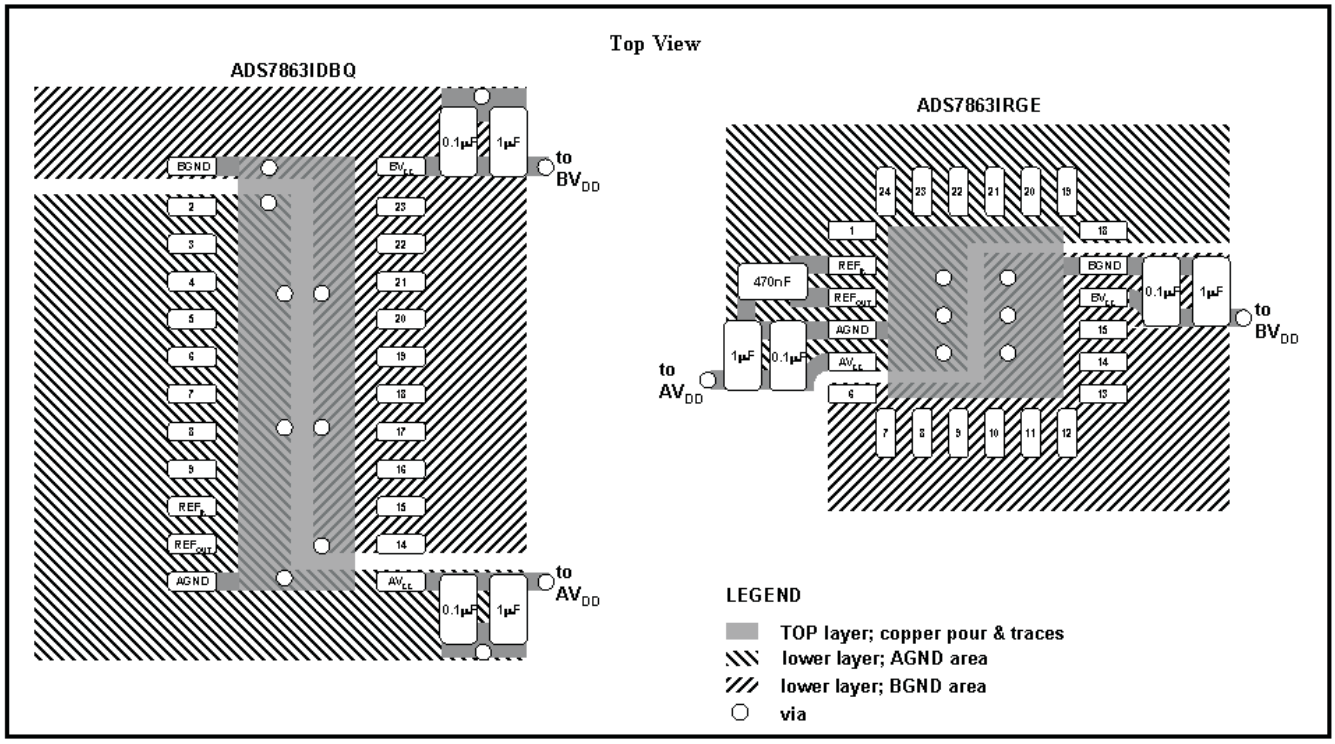



**Figure 42. Optimized Layout Recommendation**


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## REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision D (April 2010) to Revision E** **Page**

- Changed DC Accuracy, $G_{ERR}$ maximum specification in ELectrical Characteristics table ..... 4

**Changes from Revision C (April 2009) to Revision D** **Page**

- Deleted footnote 2 from Electrical Characteristics ..... 4
- Replaced Figure 1 ..... 7
- Changed $t_9$ to $t_{12}$ specifications in the *Timing Requirements* table ..... 8
- Deleted $t_{13}$ specification from the *Timing Requirements* table ..... 8
- Updated *RESET* section of *Applications Information* ..... 16

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ADS7863IDBQ | ACTIVE | SSOP | DBQ | 24 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | ADS7863I A | Samples |
| ADS7863IDBQG4 | ACTIVE | SSOP | DBQ | 24 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | ADS7863I A | Samples |
| ADS7863IDBQR | ACTIVE | SSOP | DBQ | 24 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | ADS7863I A | Samples |
| ADS7863IDBQRG4 | ACTIVE | SSOP | DBQ | 24 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | ADS7863I A | Samples |
| ADS7863IRGER | ACTIVE | VQFN | RGE | 24 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | ADS 7863I A | Samples |
| ADS7863IRGERG4 | ACTIVE | VQFN | RGE | 24 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | ADS 7863I A | Samples |
| ADS7863IRGET | ACTIVE | VQFN | RGE | 24 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | ADS 7863I A | Samples |
| ADS7863IRGETG4 | ACTIVE | VQFN | RGE | 24 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | ADS 7863I A | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

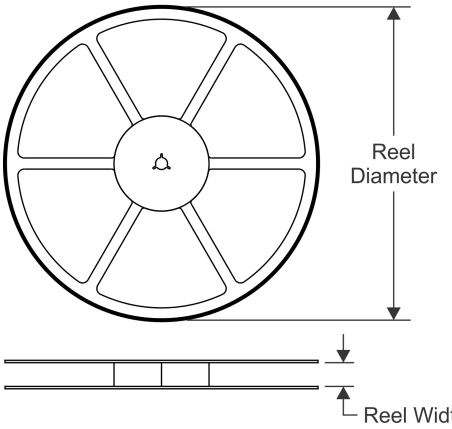
**(4)** Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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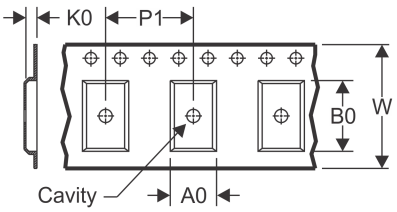
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

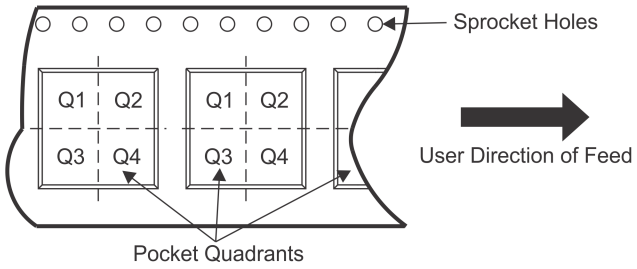



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

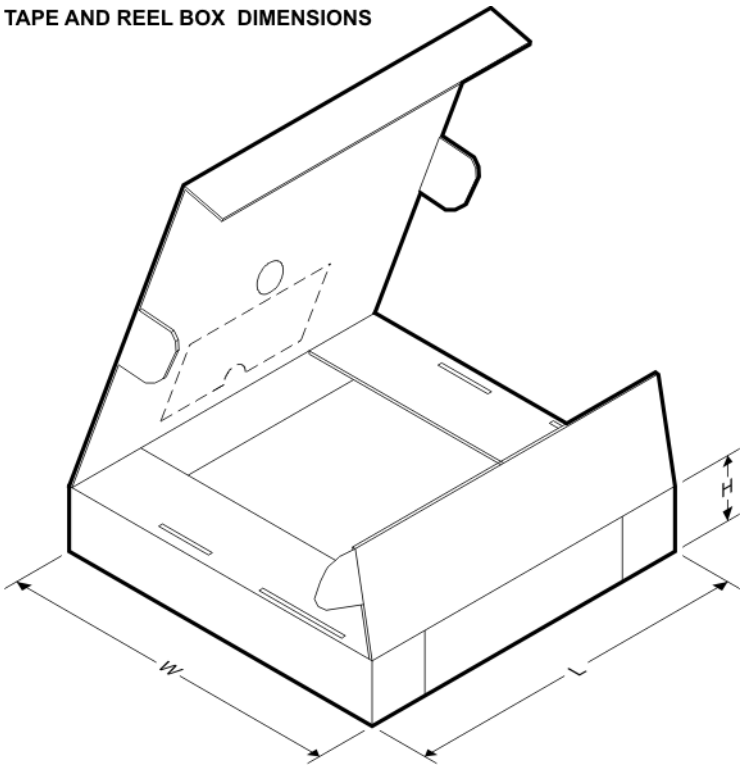
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADS7863IDBQR | SSOP | DBQ | 24 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| ADS7863IRGER | VQFN | RGE | 24 | 3000 | 330.0 | 12.4 | 4.3 | 4.3 | 1.5 | 8.0 | 12.0 | Q2 |
| ADS7863IRGET | VQFN | RGE | 24 | 250 | 180.0 | 12.4 | 4.3 | 4.3 | 1.5 | 8.0 | 12.0 | Q2 |

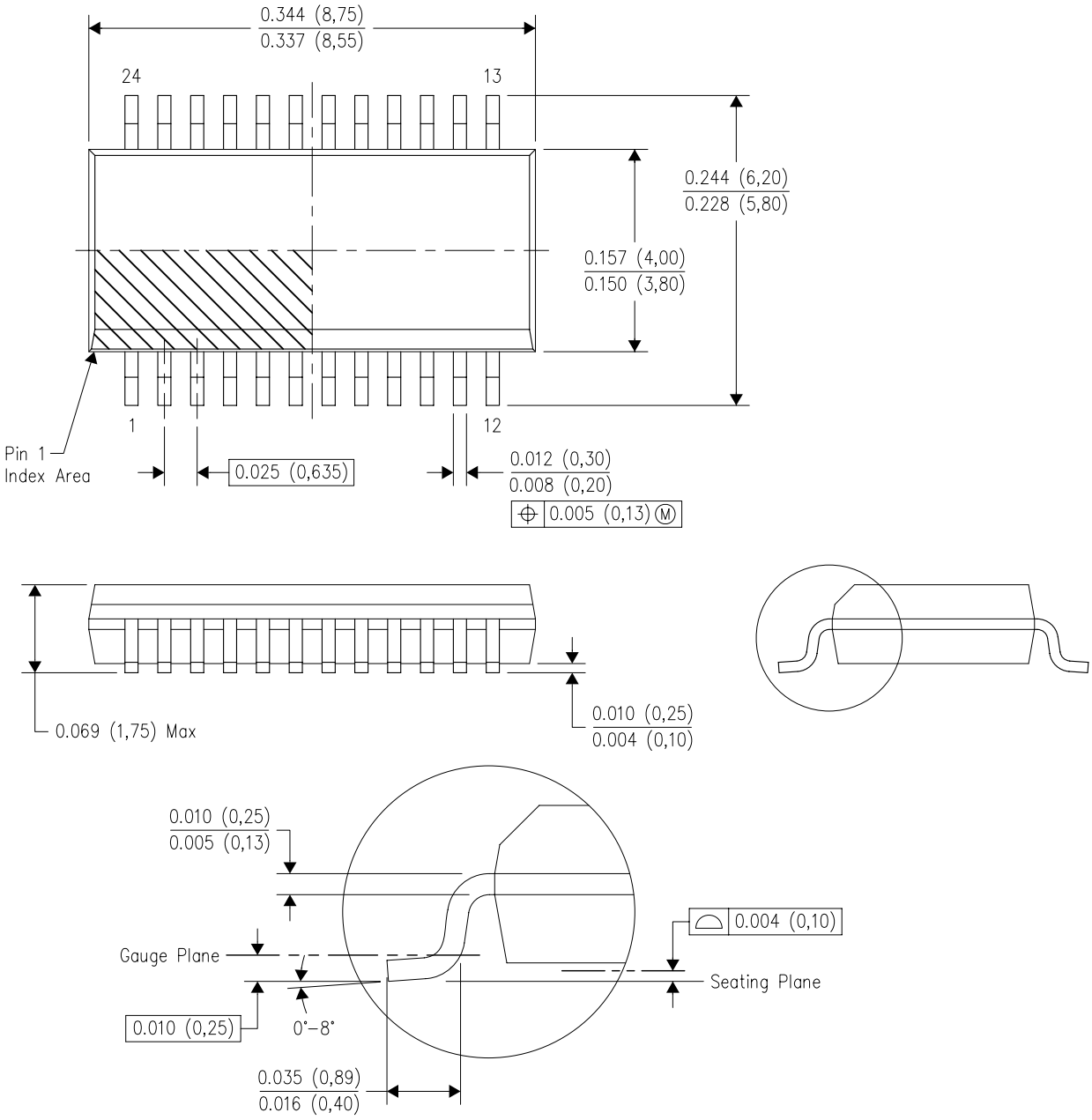
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

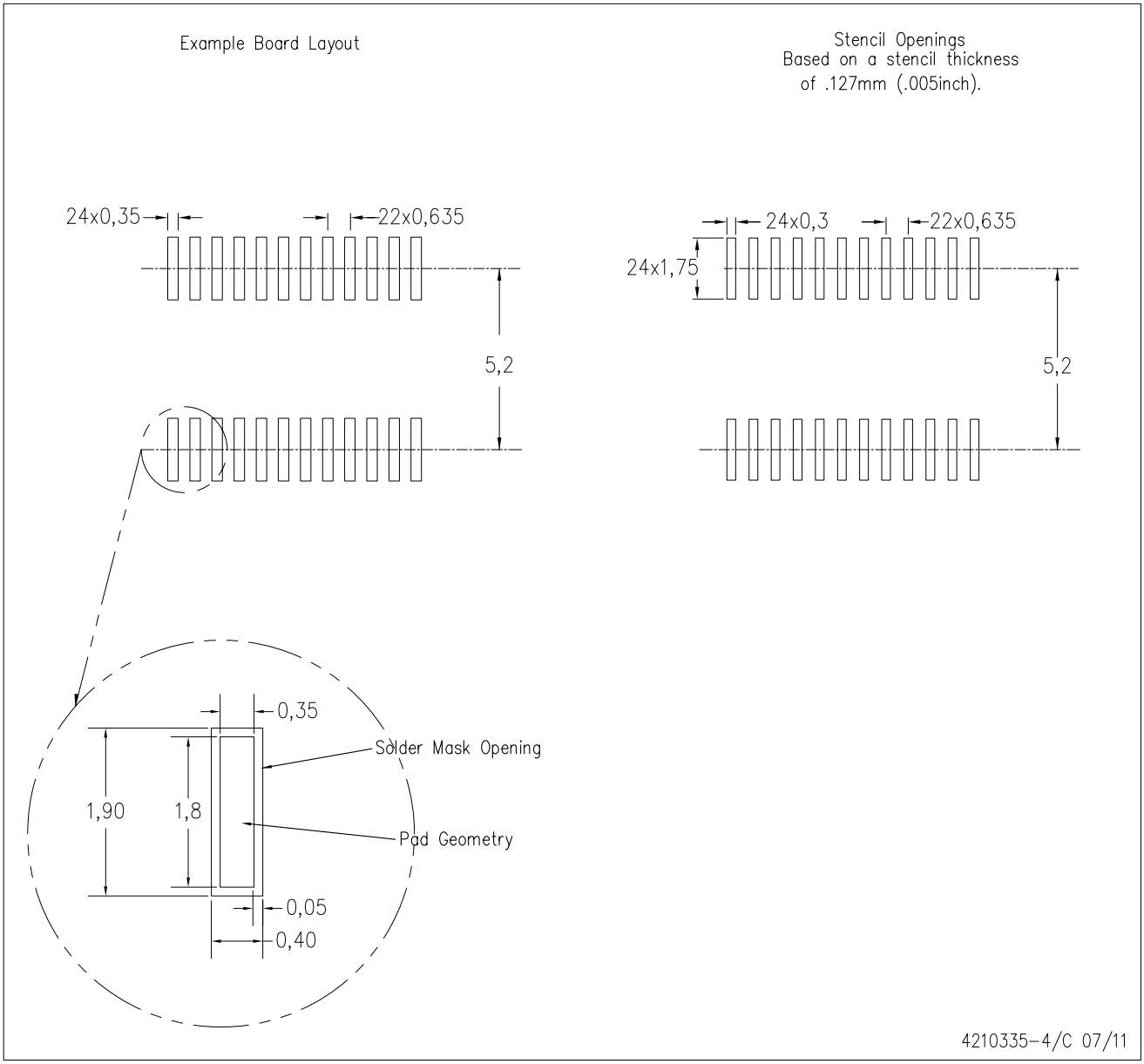
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| ADS7863IDBQR | SSOP | DBQ | 24 | 2500 | 367.0 | 367.0 | 38.0 |
| ADS7863IRGER | VQFN | RGE | 24 | 3000 | 338.1 | 338.1 | 20.6 |
| ADS7863IRGET | VQFN | RGE | 24 | 250 | 210.0 | 185.0 | 35.0 |

DBQ (R–PDSO–G24) PLASTIC SMALL–OUTLINE PACKAGE



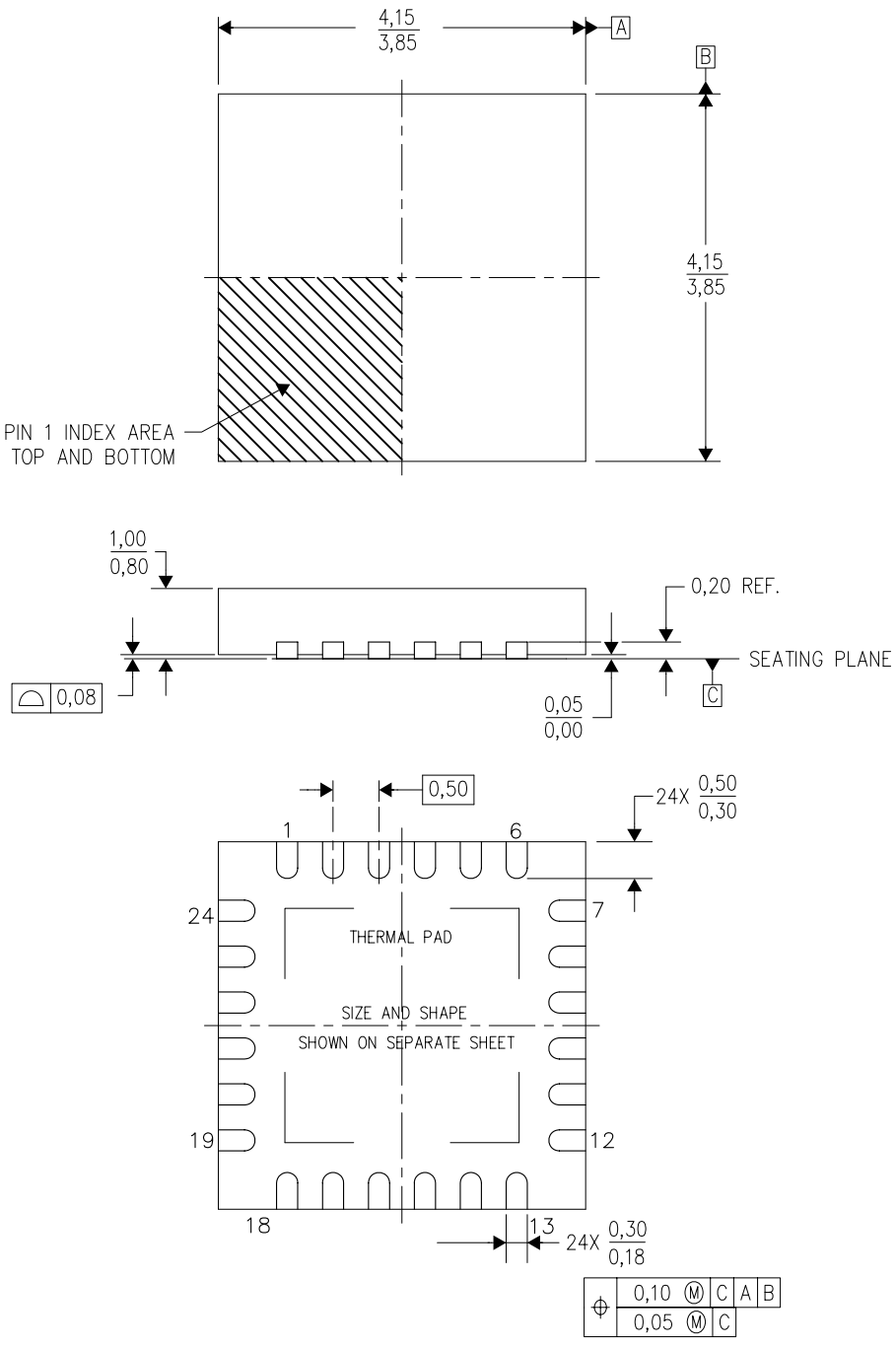

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AE.

# DBQ (R–PDSO–G24) PLASTIC SMALL OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

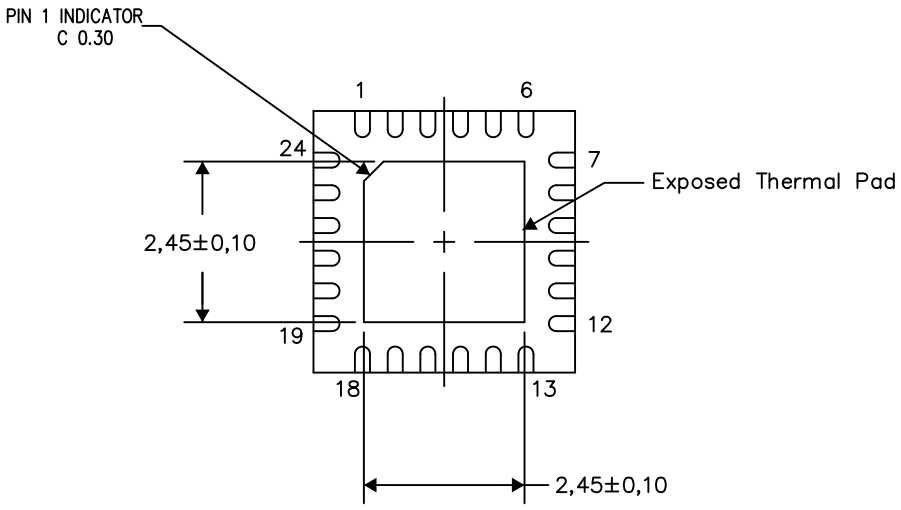
RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



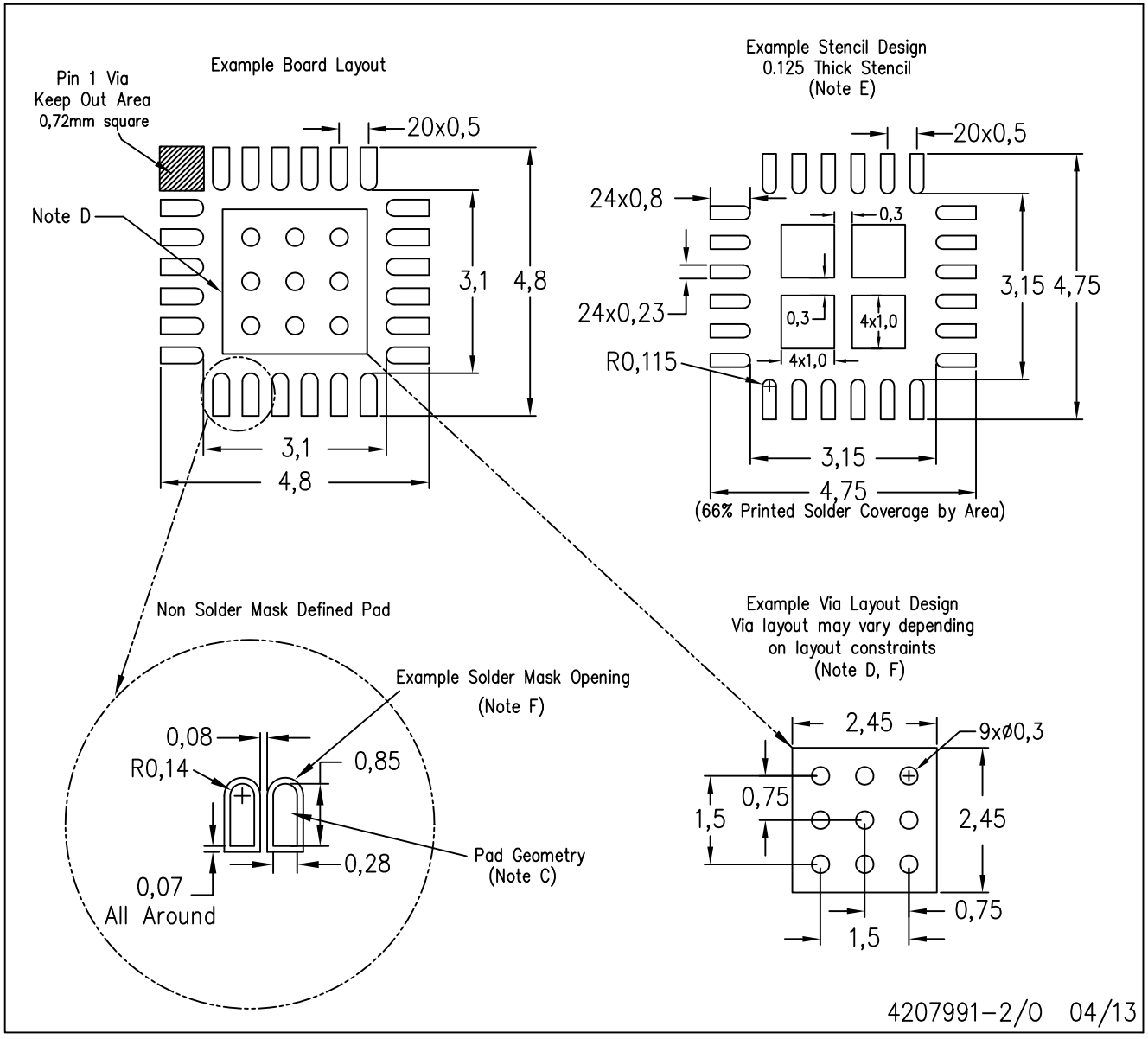

Bottom View

Exposed Thermal Pad Dimensions

4206344–3/AC 03/13

NOTES: A. All linear dimensions are in millimeters

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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