# NTGD4167C

# Power MOSFET
## Complementary, 30 V, +2.9/−2.2 A, TSOP−6 Dual

### Features
- Complementary N−Channel and P−Channel MOSFET
- Small Size (3 x 3 mm) Dual TSOP−6 Package
- Leading Edge Trench Technology for Low On Resistance
- Reduced Gate Charge to Improve Switching Response
- Independently Connected Devices to Provide Design Flexibility
- This is a Pb−Free Device

### Applications
- DC−DC Conversion Circuits
- Load/Power Switching with Level Shift

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Parameter | | | Symbol | Value | Unit |
|---|---|---|---|---|---|
| Drain−to−Source Voltage | | | $V_{DSS}$ | 30 | V |
| Gate−to−Source Voltage (N−Ch & P−Ch) | | | $V_{GS}$ | ±12 | V |
| **N−Channel** Continuous Drain Current (Note 1) | Steady State | $T_A$ = 25°C | $I_D$ | 2.6 | A |
| | | $T_A$ = 85°C | | 1.9 | |
| | t ≤ 5 s | $T_A$ = 25°C | | 2.9 | |
| **P−Channel** Continuous Drain Current (Note 1) | Steady State | $T_A$ = 25°C | $I_D$ | −1.9 | A |
| | | $T_A$ = 85°C | | −1.4 | |
| | t ≤ 5 s | $T_A$ = 25°C | | −2.2 | |
| Power Dissipation (Note 1) | Steady State | $T_A$ = 25°C | $P_D$ | 0.9 | W |
| | t ≤ 5 s | | | 1.1 | |
| Pulsed Drain Current | N−Ch | $t_p$ = 10 μs | $I_{DM}$ | 8.6 | A |
| | P−Ch | | | −6.3 | |
| Operating Junction and Storage Temperature | | | $T_J$, $T_{STG}$ | −55 to 150 | °C |
| Source Current (Body Diode) | | | $I_S$ | ±0.9 | A |
| Lead Temperature for Soldering Purposes (1/8″ from case for 10 s) | | | $T_L$ | 260 | °C |

**THERMAL RESISTANCE RATINGS**

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Junction−to−Ambient − Steady State (Note 1) | $R_{\theta JA}$ | 140 | °C/W |
| Junction−to−Ambient − t ≤ 5 s (Note 1) | $R_{\theta JA}$ | 110 | °C/W |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).

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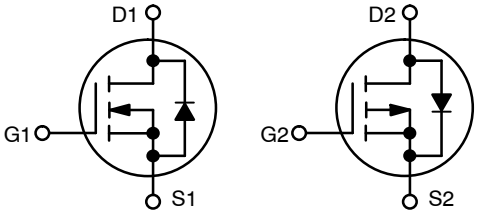
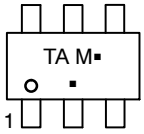
| $V_{(BR)DSS}$ | $R_{DS(on)}$ MAX | $I_D$ MAX (Note 1) |
|---|---|---|
| N−Ch 30 V | 90 mΩ @ 4.5 V | 2.6 A |
| | 125 mΩ @ 2.5 V | 2.2 A |
| P−Ch −30 V | 170 mΩ @ −4.5 V | −1.9 A |
| | 300 mΩ @ −2.5 V | −1.0 A |




**N−CHANNEL MOSFET** **P−CHANNEL MOSFET**


**TSOP−6**
**CASE 318G**
**STYLE 13**

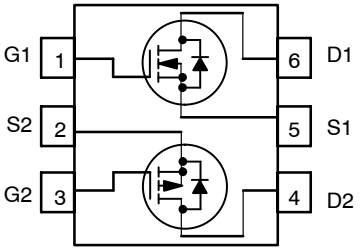
**MARKING DIAGRAM**




TA = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

**PIN CONNECTION**




(Top View)

**ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Parameter | Symbol | N/P | Test Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | | |
| Drain−to−Source Breakdown Voltage | $V_{(BR)DSS}$ | N | $V_{GS}$ = 0 V | $I_D$ = 250 μA | 30 | | | V |
| | | P | | $I_D$ = −250 μA | −30 | | | |
| Drain−to−Source Breakdown Voltage Temperature Coefficient | $V_{(BR)DSS}/T_J$ | N | | | | 21.4 | | mV/°C |
| | | P | | | | 22.2 | | |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | N | $V_{GS}$ = 0 V, $V_{DS}$ = 24 V | $T_J$ = 25 °C | | | 1.0 | μA |
| | | P | $V_{GS}$ = 0 V, $V_{DS}$ = −24 V | | | | −1.0 | |
| | | N | $V_{GS}$ = 0 V, $V_{DS}$ = 24 V | $T_J$ = 85 °C | | | 10 | |
| | | P | $V_{GS}$ = 0 V, $V_{DS}$ = −24 V | | | | −10 | |
| Gate−to−Source Leakage Current | $I_{GSS}$ | N | $V_{DS}$ = 0 V, $V_{GS}$ = ±12 V | | | | ±100 | nA |
| | | P | $V_{DS}$ = 0 V, $V_{GS}$ = ±12 V | | | | ±100 | |
| **ON CHARACTERISTICS** (Note 2) | | | | | | | | |
| Gate Threshold Voltage | $V_{GS(TH)}$ | N | $V_{GS}$ = $V_{DS}$ | $I_D$ = 250 μA | 0.5 | 0.9 | 1.5 | V |
| | | P | | $I_D$ = −250 μA | −0.5 | −1.1 | −1.5 | |
| Drain−to−Source On Resistance | $R_{DS(on)}$ | N | $V_{GS}$ = 4.5 V , $I_D$ = 2.6 A | | | 52 | 90 | mΩ |
| | | | $V_{GS}$ = 2.5 V , $I_D$ = 2.2 A | | | 67 | 125 | |
| | | P | $V_{GS}$ = −4.5 V , $I_D$ = −1.9 A | | | 130 | 170 | |
| | | | $V_{GS}$ = −2.5 V, $I_D$ = −1.0 A | | | 202 | 300 | |
| Forward Transconductance | $g_{FS}$ | N | $V_{DS}$ = 15 V, $I_D$ = 2.6 A | | | 2.6 | | S |
| | | P | $V_{DS}$ = −15 V , $I_D$ = −1.9 A | | | 2.6 | | |
| **CHARGES AND CAPACITANCES** | | | | | | | | |
| Input Capacitance | $C_{ISS}$ | N | f = 1 MHz, $V_{GS}$ = 0 V | $V_{DS}$ = 15 V | | 295 | | pF |
| Output Capacitance | $C_{OSS}$ | | | | | 48 | | |
| Reverse Transfer Capacitance | $C_{RSS}$ | | | | | 27 | | |
| Input Capacitance | $C_{ISS}$ | P | | $V_{DS}$ = −15 V | | 419 | | |
| Output Capacitance | $C_{OSS}$ | | | | | 51 | | |
| Reverse Transfer Capacitance | $C_{RSS}$ | | | | | 26 | | |
| Total Gate Charge | $Q_{G(TOT)}$ | N | $V_{GS}$ = 4.5 V, $V_{DS}$ = 15 V, $I_D$ = 2.0 A | | | 3.7 | 5.5 | nC |
| Threshold Gate Charge | $Q_{G(TH)}$ | | | | | 0.6 | | |
| Gate−to−Source Gate Charge | $Q_{GS}$ | | | | | 0.9 | | |
| Gate−to−Drain “Miller” Charge | $Q_{GD}$ | | | | | 0.8 | | |
| Total Gate Charge | $Q_{G(TOT)}$ | P | $V_{GS}$ = −4.5 V, $V_{DS}$ = −15 V, $I_D$ = −2.0 A | | | 3.9 | 6.0 | |
| Threshold Gate Charge | $Q_{G(TH)}$ | | | | | 0.6 | | |
| Gate−to−Source Gate Charge | $Q_{GS}$ | | | | | 1.0 | | |
| Gate−to−Drain “Miller” Charge | $Q_{GD}$ | | | | | 1.0 | | |
| **SWITCHING CHARACTERISTICS** (Note 3) | | | | | | | | |
| Turn−On Delay Time | $t_{d(ON)}$ | N | $V_{GS}$ = 4.5 V, $V_{DD}$ = 15 V, $I_D$ = 1.0 A, $R_G$ = 6.0 Ω | | | 7.0 | | ns |
| Rise Time | $t_r$ | | | | | 4.0 | | |
| Turn−Off Delay Time | $t_{d(OFF)}$ | | | | | 14 | | |
| Fall Time | $t_f$ | | | | | 2.0 | | |
| Turn−On Delay Time | $t_{d(ON)}$ | P | $V_{GS}$ = −4.5 V, $V_{DD}$ = −15 V, $I_D$ = −1.0 A, $R_G$ = 6.0 Ω | | | 8.0 | | |
| Rise Time | $t_r$ | | | | | 8.0 | | |
| Turn−Off Delay Time | $t_{d(OFF)}$ | | | | | 22 | | |
| Fall Time | $t_f$ | | | | | 8.0 | | |

2. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

3. Switching characteristics are independent of operating junction temperatures.

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Parameter | Symbol | N/P | Test Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| **DRAIN−SOURCE DIODE CHARACTERISTICS** | | | | | | | | |
| Forward Diode Voltage | $V_{SD}$ | N | $V_{GS}$ = 0 V, $T_J$ = 25 °C | $I_S$ = 0.9 A | | 0.7 | 1.2 | V |
| | | P | | $I_S$ = −0.9 A | | −0.8 | −1.2 | |
| Reverse Recovery Time | $t_{RR}$ | N | $V_{GS}$ = 0 V, $dI_S / dt$ = 100 A/μs, $I_S$ = 0.9 A | | | 8.0 | | ns |
| Charge Time | $t_a$ | | | | | 5.0 | | |
| Discharge Time | $t_b$ | | | | | 3.0 | | |
| Reverse Recovery Charge | $Q_{RR}$ | | | | | 3.0 | | nC |
| Reverse Recovery Time | $t_{RR}$ | P | $V_{GS}$ = 0 V, $dI_S / dt$ = 100 A/μs, $I_S$ = −0.9 A | | | 12 | | ns |
| Charge Time | $t_a$ | | | | | 10 | | |
| Discharge Time | $t_b$ | | | | | 2.0 | | |
| Reverse Recovery Charge | $Q_{RR}$ | | | | | 7.0 | | nC |

## N−CHANNEL TYPICAL CHARACTERISTICS

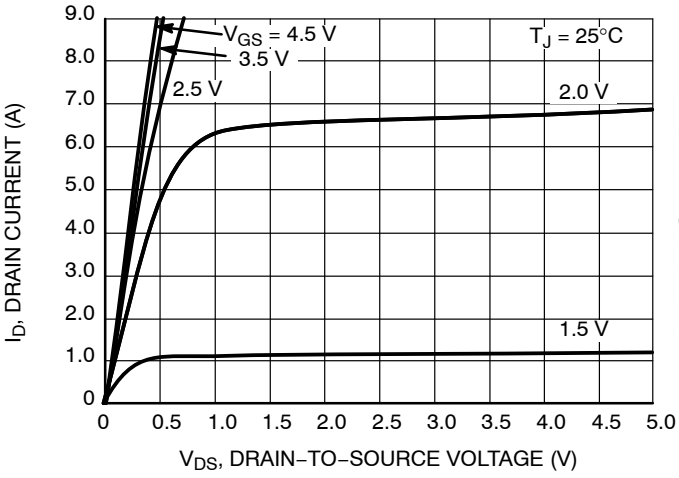



**Figure 1. On−Region Characteristics**

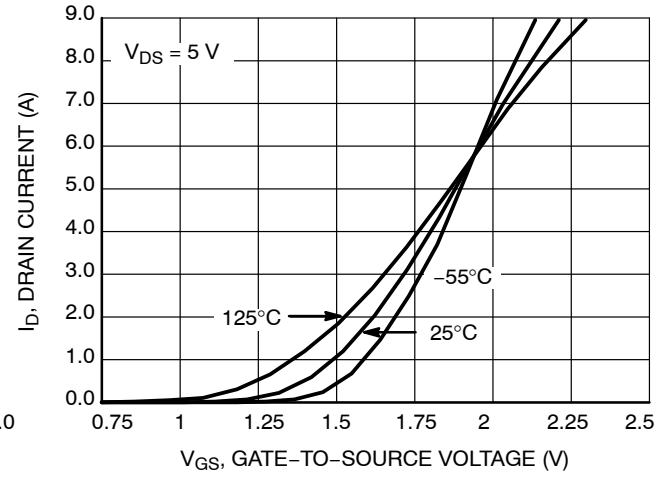



**Figure 2. Transfer Characteristics**

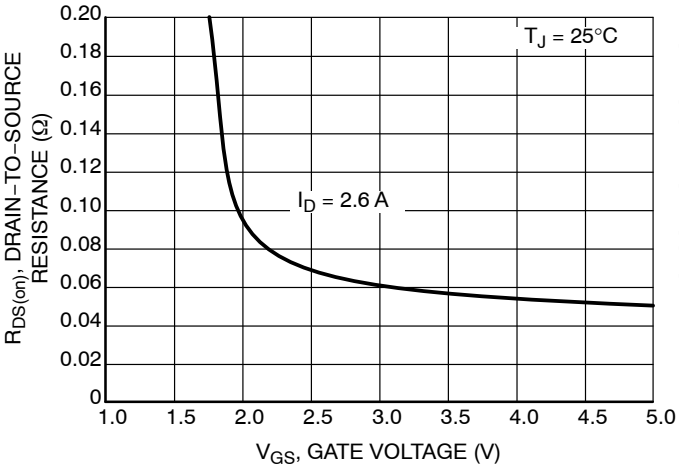



**Figure 3. On−Region vs. Gate−To−Source Voltage**

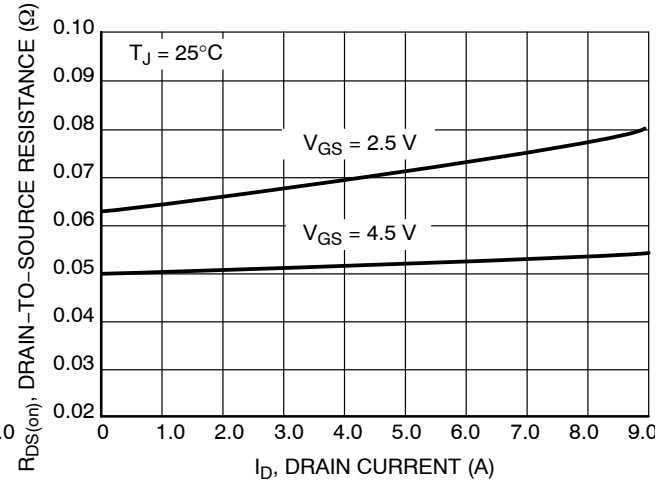



**Figure 4. On−Resistance vs. Drain Current and Temperature**

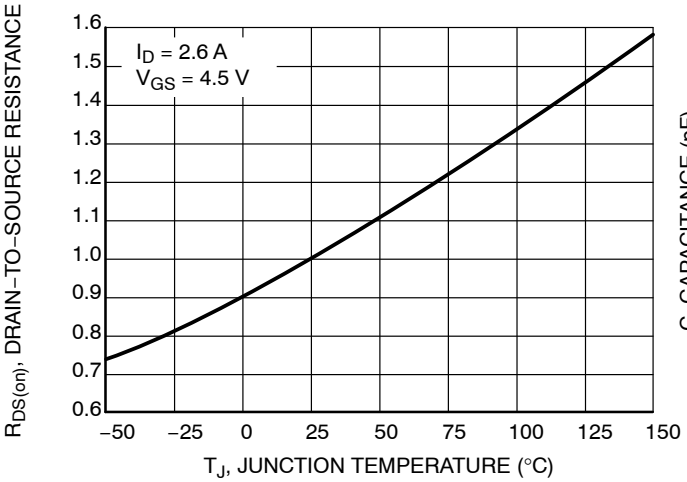



**Figure 5. On−Resistance Variation with Temperature**

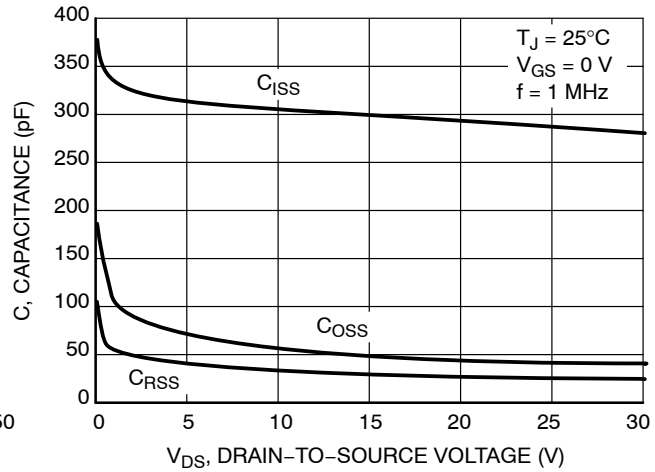



**Figure 6. Capacitance Variation**

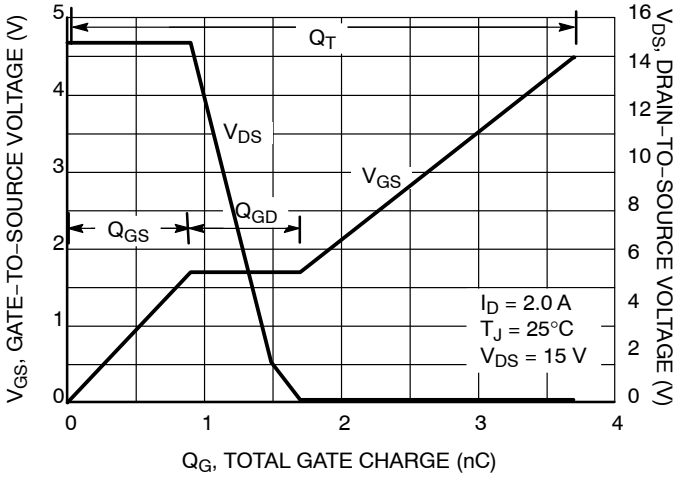



**Figure 7. Gate−to−Source and Drain−to−Source Voltage versus Total Charge**

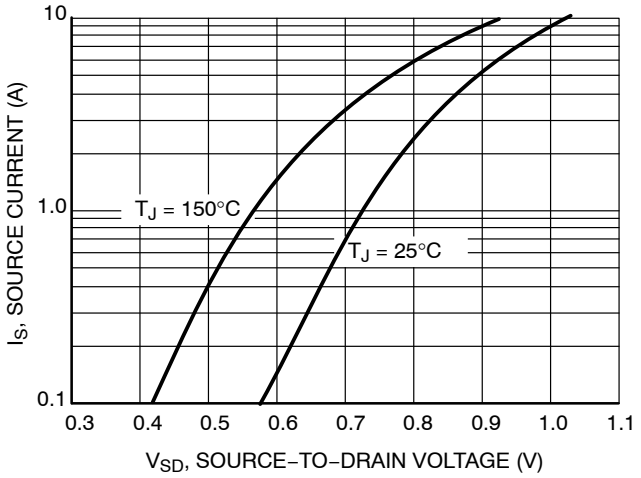



**Figure 8. Diode Forward Voltage versus Current**

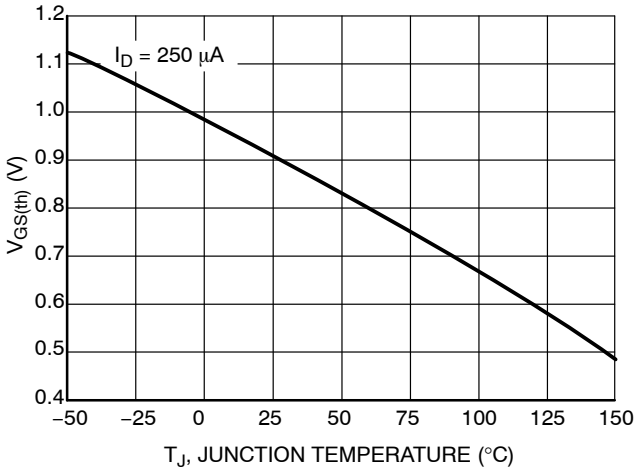



**Figure 9. Threshold Voltage**

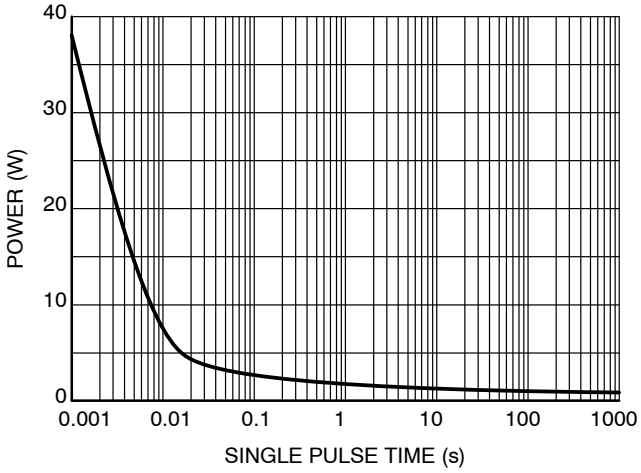



**Figure 10. Single Pulse Maximum Power Dissipation**

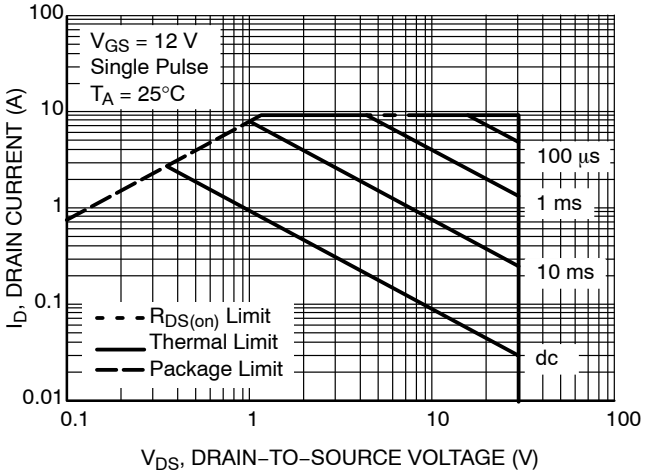



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

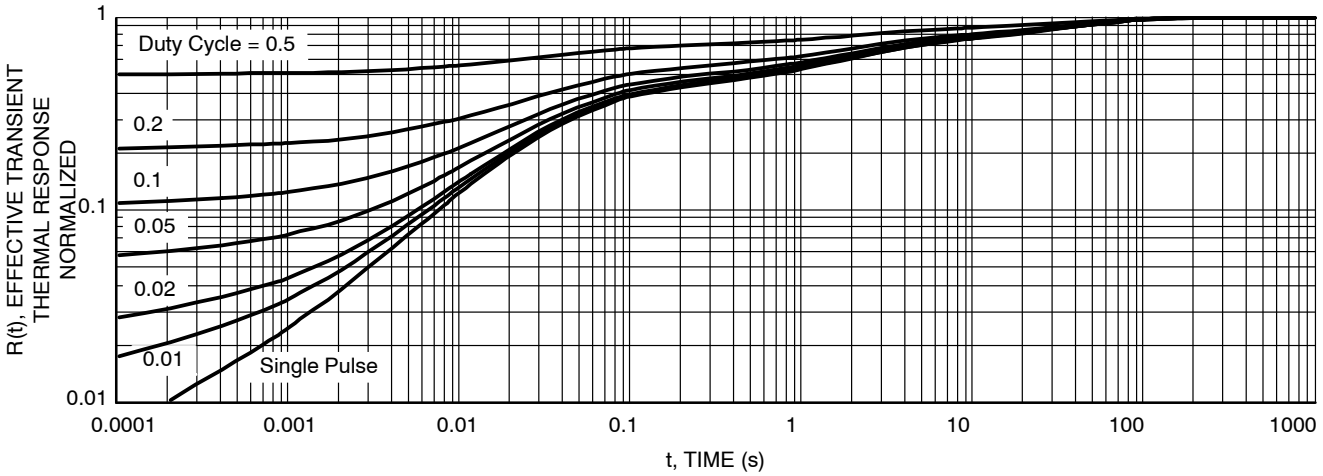



**Figure 12. FET Thermal Response**

## P−CHANNEL TYPICAL CHARACTERISTICS

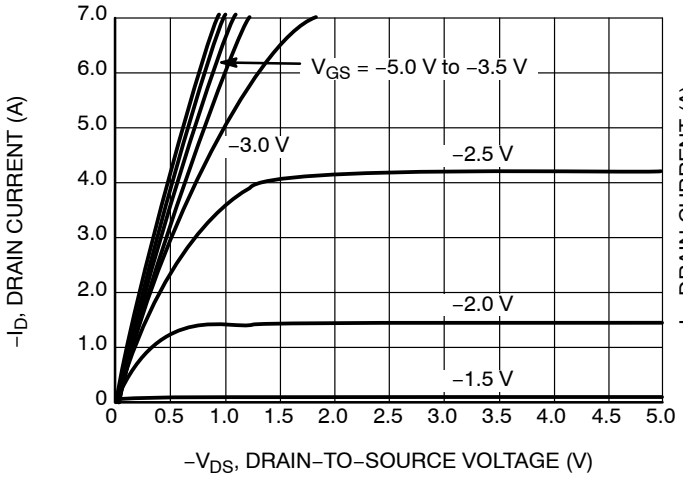



**Figure 13. On−Region Characteristics**

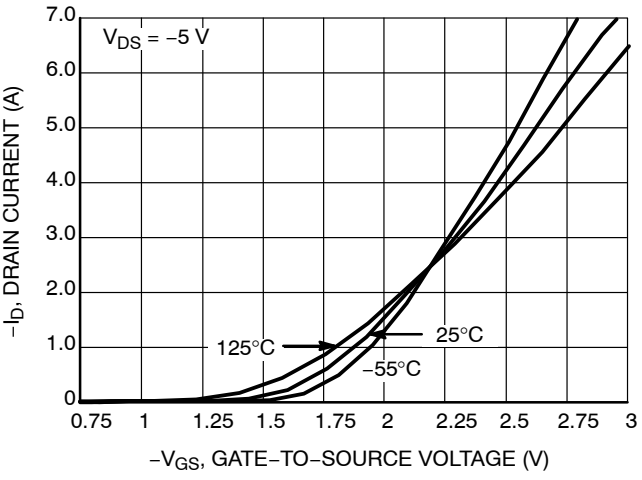



**Figure 14. Transfer Characteristics**

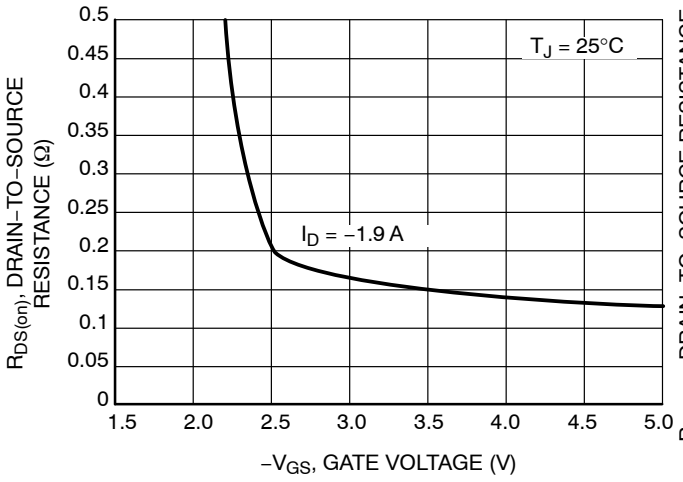



**Figure 15. On−Region vs. Gate−To−Source Voltage**

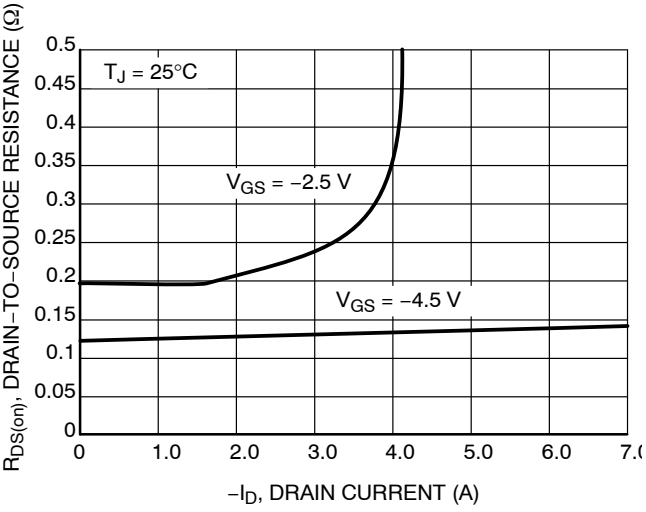



**Figure 16. On−Resistance vs. Drain Current and Temperature**

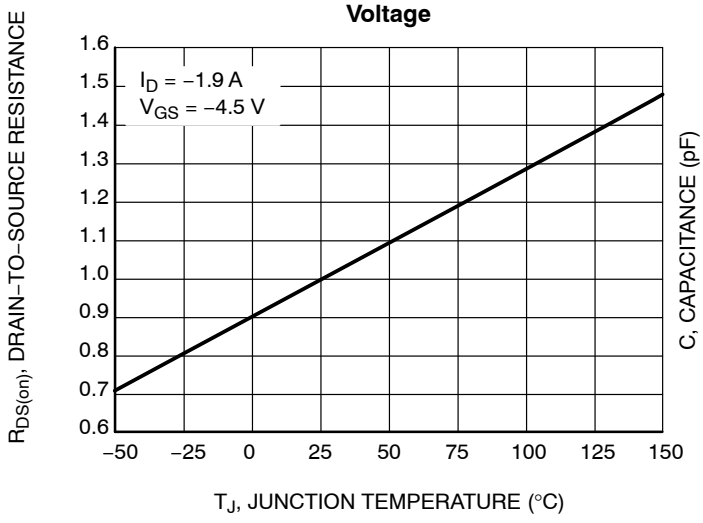



**Figure 17. On−Resistance Variation with Temperature**

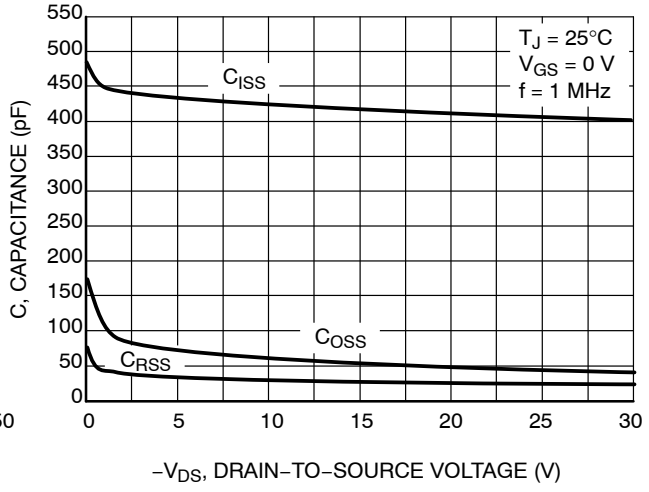



**Figure 18. Capacitance Variation**

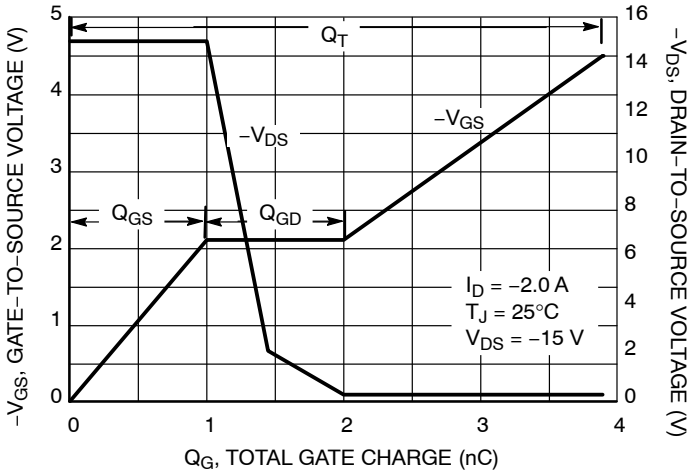



**Figure 19. Gate−to−Source and Drain−to−Source Voltage versus Total Charge**

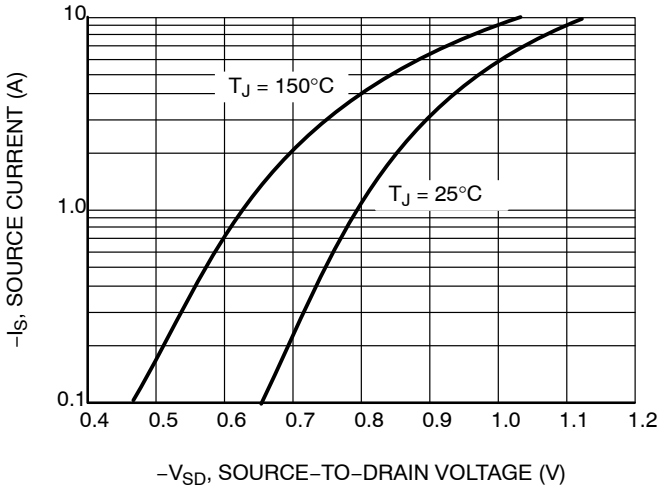



**Figure 20. Diode Forward Voltage versus Current**

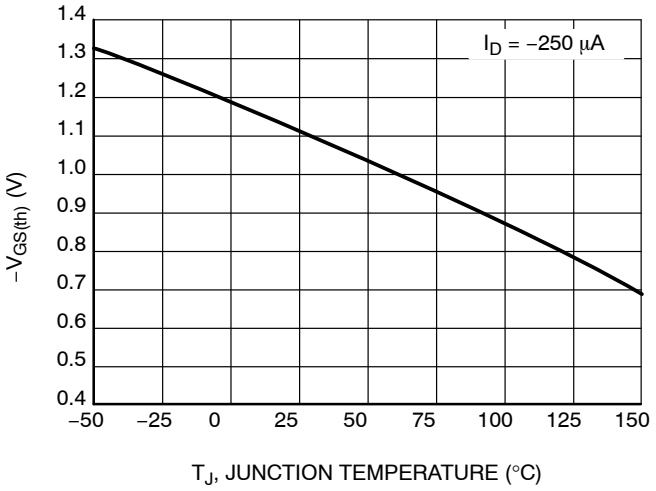



**Figure 21. Threshold Voltage**

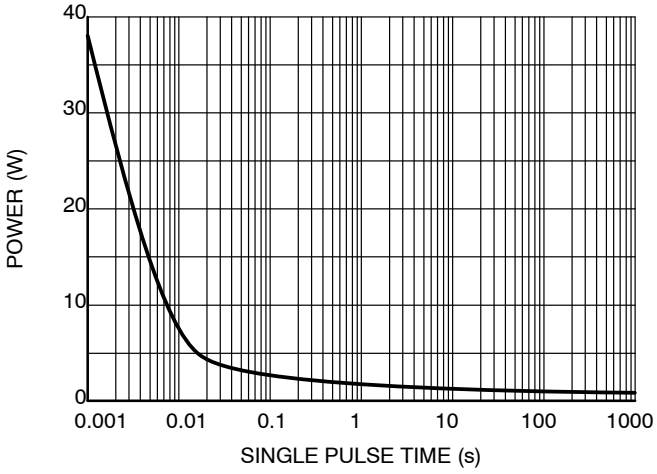



**Figure 22. Single Pulse Maximum Power Dissipation**

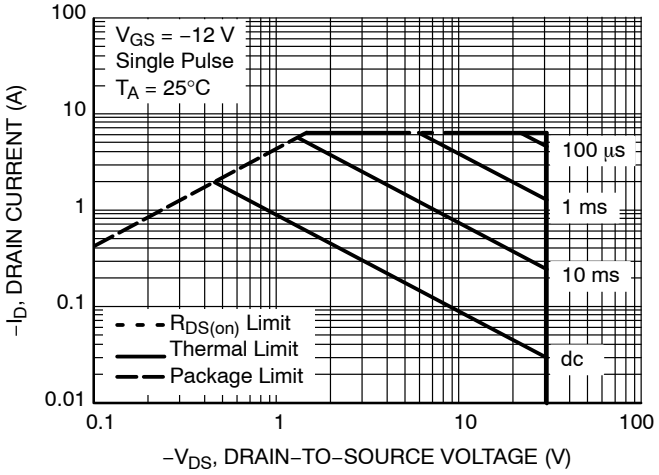



**Figure 23. Maximum Rated Forward Biased Safe Operating Area**

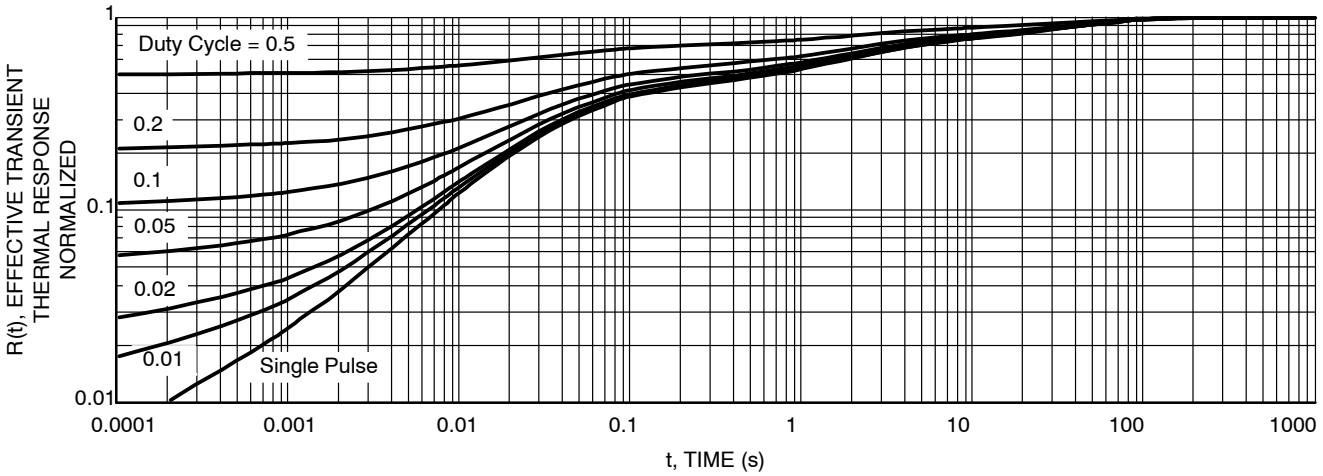



**Figure 24. FET Thermal Response**

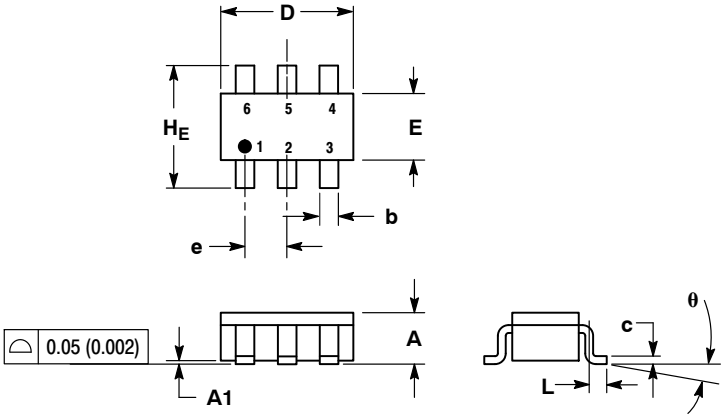
**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| NTGD4167CT1G | TSOP6<br>(Pb−Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## PACKAGE DIMENSIONS

**TSOP−6**
CASE 318G−02
ISSUE T

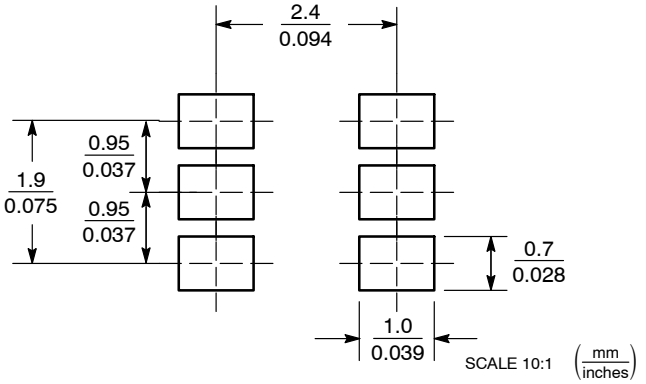



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

| | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| DIM | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.90 | 1.00 | 1.10 | 0.035 | 0.039 | 0.043 |
| A1 | 0.01 | 0.06 | 0.10 | 0.001 | 0.002 | 0.004 |
| b | 0.25 | 0.38 | 0.50 | 0.010 | 0.014 | 0.020 |
| c | 0.10 | 0.18 | 0.26 | 0.004 | 0.007 | 0.010 |
| D | 2.90 | 3.00 | 3.10 | 0.114 | 0.118 | 0.122 |
| E | 1.30 | 1.50 | 1.70 | 0.051 | 0.059 | 0.067 |
| e | 0.85 | 0.95 | 1.05 | 0.034 | 0.037 | 0.041 |
| L | 0.20 | 0.40 | 0.60 | 0.008 | 0.016 | 0.024 |
| $H_E$ | 2.50 | 2.75 | 3.00 | 0.099 | 0.108 | 0.118 |
| θ | 0° | – | 10° | 0° | – | 10° |

STYLE 13:
PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1

## SOLDERING FOOTPRINT*




*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



**PUBLICATION ORDERING INFORMATION**

**LITERATURE FULFILLMENT**:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
**Phone**: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
**Fax**: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
**Email**: orderlit@onsemi.com

**N. American Technical Support**: 800−282−9855 Toll Free USA/Canada
**Europe, Middle East and Africa Technical Support:**
Phone: 421 33 790 2910
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