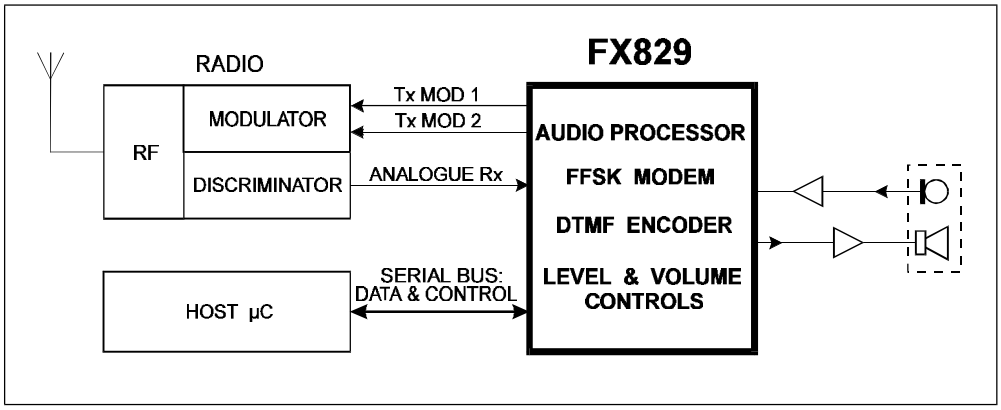
CML Semiconductor Products

Baseband Signal Processor FX829

D/829/4 September 1997
Provisional Issue

1.0 Features

- **Rx Audio Processing**
- **Tx Audio Processing**
- **1200/2400 Baud Modem**
- **DTMF Encoder**
- **Multi-standard Modem Formats**
- **ETS/MPT/PAA Standards Compatible**
- **Low Voltage Operation**
- **24-pin Small Form Package**



1.1 Brief Description

The FX829 is a low voltage CMOS integrated circuit, designed to provide the baseband audio and system signal-processing functions required for PAMR or PMR trunked radio applications. It operates in half-duplex mode under serial-bus control of the host µC.

The FX829 incorporates a dual-rate 1200/2400bps FFSK modem, with a software-flexible choice of synchronisation codewords, data run-length and CRC checking to suit a wide range of applications. These features allow very flexible handling of non-prescribed data on traffic channels in addition to the network signalling sent on control channels. A 16 character DTMF encoder is available in the transmit mode. The two-point modulation output has software programmable level-adjustment.

The audio processing stages include transmit and receive filtering, to the standards specified for 12.5kHz and 25kHz PAMR/PMR channel operation, plus transmit deviation limiting and a programmable Rx volume control. Power saving is automatic when audio functions are deselected.

The FX829 is designed for use in radios compatible with MPT1327, PAA1382 and ETS 300 086 trunking standards. Its features and flexibility ensure that it is equally suitable for use with modified or proprietary standards.

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1.2 Block Diagram

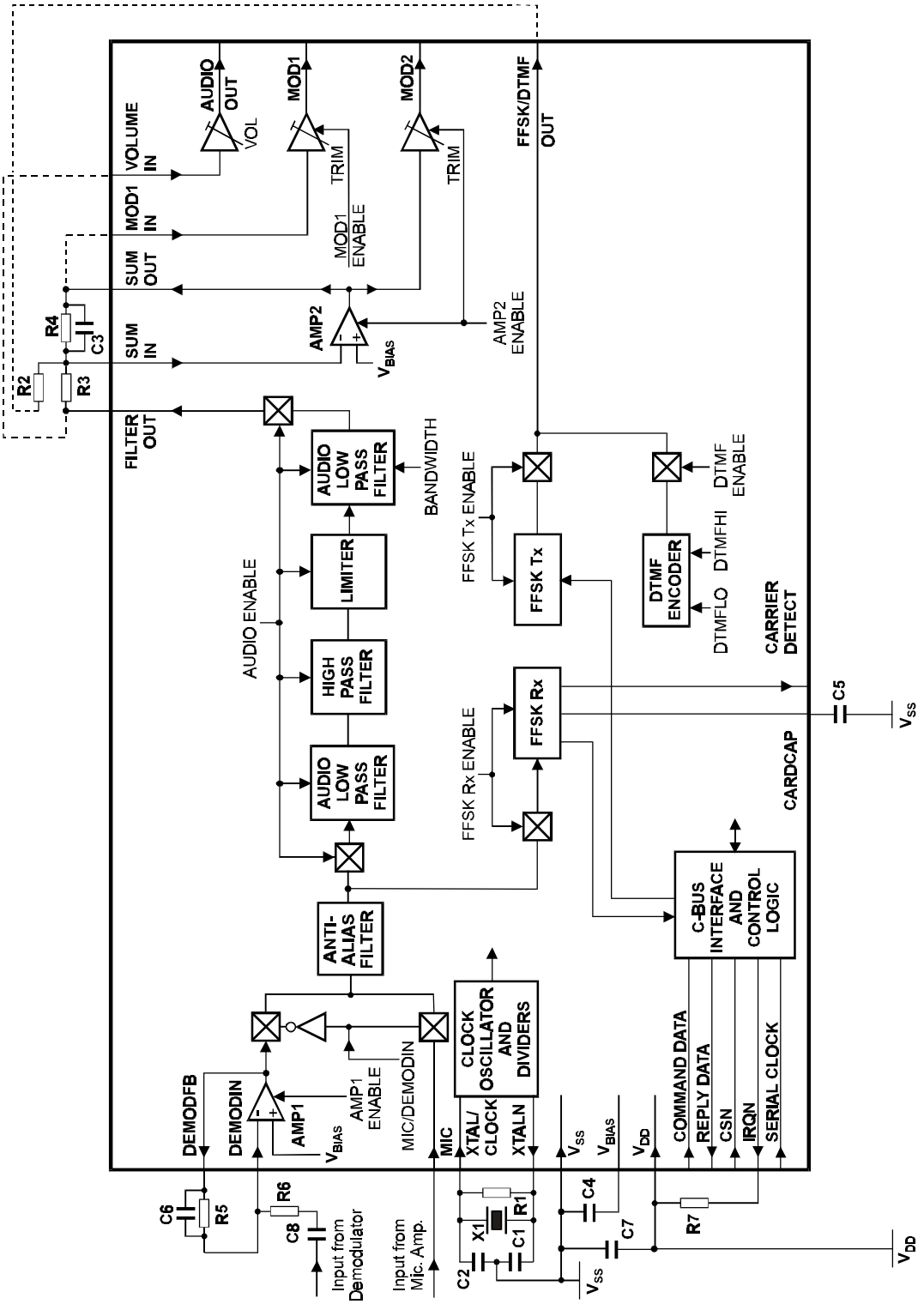


Figure 1 Block Diagram

1.3 Signal List

Package D2/D5	Signal		Description
Pin No.	**Name**	**Type**	
1	XTALN	O/P	The inverted output of the on-chip oscillator.
2	XTAL/CLOCK	I/P	The input to the on-chip oscillator, for external Xtal circuit or clock.
3	SERIAL CLOCK	I/P	The "C-BUS" serial clock input. This clock, produced by the µController, is used for transfer timing of commands and data to and from the device. See "C-BUS" Timing Diagram.
4	COMMAND DATA	I/P	The "C-BUS" serial data input from the µController. Data is loaded into this device in 8-bit bytes, MSB (B7) first, and LSB (B0) last, synchronised to the SERIAL CLOCK. See "C-BUS" Timing Diagram.
5	REPLY DATA	O/P	The "C-BUS" serial data output to the µController. The transmission of REPLY DATA bytes is synchronised to the SERIAL CLOCK under the control of the CSN input. This 3-state output is held at high impedance when not sending data to the µController. See "C-BUS" Timing Diagram.
6	CSN	I/P	The "C-BUS" data loading control function: this input is provided by the µController. Data transfer sequences are initiated, completed or aborted by the CSN signal. See "C-BUS" Timing Diagram.
7	IRQN	O/P	This output indicates an interrupt condition to the µController by going to a logic "0". This is a "wire-ORable" output, enabling the connection of up to 8 peripherals to 1 interrupt port on the µController. This pin has a low impedance pulldown to logic "0" when active and a high-impedance when inactive. An external pullup resistor is required. The conditions that cause interrupts are indicated in the STATUS register and are effective if not masked out by a corresponding bit in the CONTROL register.
8	CARRIER DETECT	O/P	The carrier detect output for the FFSK Rx.

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1.3 Signal List (continued)

Package D2/D5	Signal		Description
Pin No.	**Name**	**Type**	
9	CARDCAP	O/P	The carrier detect integrating capacitor.
10	V_{BIAS}	O/P	A bias line for the internal circuitry, held at ½ V_{DD}. This pin must be decoupled by a capacitor mounted close to the device pins.
11	MIC	I/P	The ac coupled Tx audio input (external amplification is required for use as a microphone input).
12	V_{SS}	Power	The negative supply rail (ground).
13	DEMODIN	I/P	The ac coupled inverting input to the Rx input amplifier (AMP1).
14	DEMODFB	O/P	The output of the Rx input amplifier (AMP1) and the input to the audio filter/limiter section.
15	FILTER OUT	O/P	Output of the audio filter/limiter section. In powersave mode this output is connected to V_{BIAS} via a 500kΩ resistor.
16	FFSK/DTMFOUT	O/P	The 1200 or 2400 baud FFSK Tx output and the DTMF encoder output. When enabled but not transmitting FFSK or DTMF signals, or when in powersave mode, this output is connected to V_{BIAS} via a 500kΩ resistor. On power-up, this output can be any level: a General Reset command is required to ensure that this output attains V_{BIAS} initially.
17	SUM IN	I/P	Input to the audio summing amplifier (AMP2).
18	SUM OUT	O/P	Output of the audio summing amplifier (AMP2).
19	MOD1 IN	I/P	Input to MOD1 audio gain control.
20	VOL IN	I/P	Input to the audio volume control.
21	AUDIO OUT	O/P	Output of the audio volume control.
22	MOD1	O/P	Output of MOD1 audio gain control.

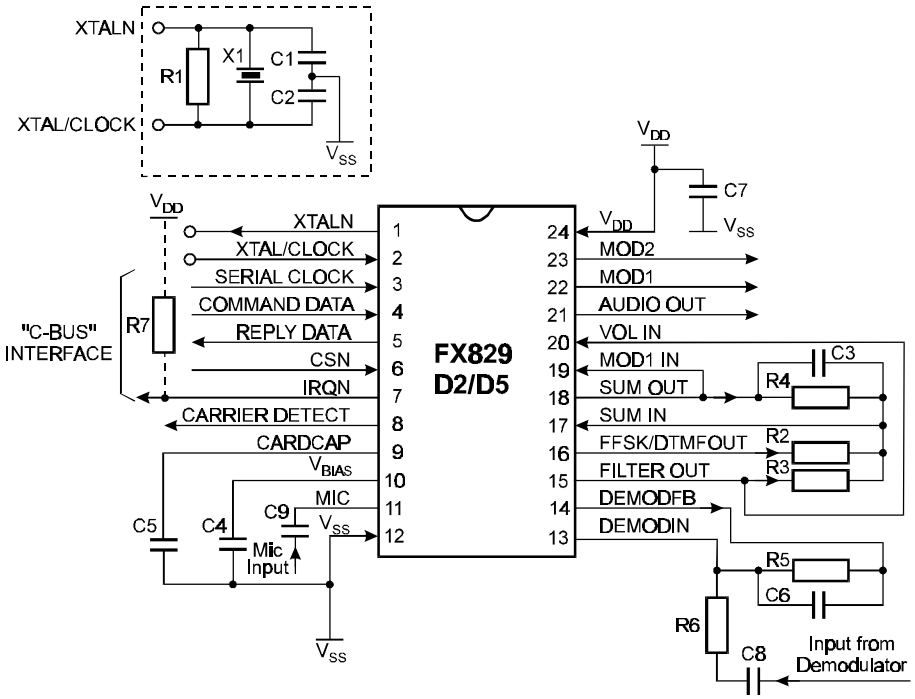
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1.3 Signal List (continued)

Package D2/D5	Signal		Description
Pin No.	**Name**	**Type**	
23	MOD2	O/P	Output of MOD2 audio gain control.
24	V_{DD}	Power	The positive supply rail. Levels and voltages are dependent upon this supply. This pin should be decoupled to V_{SS} by a capacitor.

Notes: I/P = Input
O/P = Output

1.4 External Components



C1	22pF	±20%	R1	1MΩ	±5%	X1	4.032MHz	±100ppm
C2	22pF	±20%	R2	Note 1	±10%			
C3	68pF	±20%	R3	Note 1	±10%			
C4	0.1µF	±20%	R4	100kΩ	±10%			
C5	0.1µF	±10%	R5	100kΩ	±10%			
C6	100pF	±20%	R6	Note 2	±10%			
C7	0.1µF	±20%	R7	22kΩ	±10%			
C8	Note 2	±20%						
C9	5.6nF	±20%						

Notes: 1. R2, R3, R4 and C3 form the gain components for the Summing Amplifier (AMP2). R2 and R3 should be chosen as required from the system specification, using the following formulae:

$$\text{Audio Gain} = -\frac{R4}{R3}$$

$$\text{DTMF Gain} = -\frac{R4}{R2}$$

2. R5, R6, C6 and C8 form the gain components for the Rx Input Amplifier (AMP1). R6 should be chosen as required by the signal level, using the following formula:

$$\text{Gain} = -\frac{R5}{R6}$$

C8 x R6 should be chosen so as not to compromise the low frequency performance of this product.

Figure 2 Recommended External Components

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1.5 General Description

The FX829 consists of five main sections: the audio filter section, the programmable attenuators, the DTMF encoder, the FFSK transmitter and the FFSK receiver. All these sections are controlled via a serial ("C-BUS") interface. The four sections are described below.

Audio Filtering
This consists of an input amplifier and a common audio filter section, which may be switched between Rx and Tx. The filter section comprises an anti-alias filter followed by low-pass and high-pass filtering with an amplitude limiter to set the maximum deviation. Three variable attenuation blocks may be used to set the volume (in Rx) or the modulation level (in Tx). Pre- and de-emphasis can be added externally using resistors and capacitors around AMP1, AMP2 and the microphone amplifiers, see Figure 7. The anti-alias filter is designed to reduce aliasing effects above 50kHz which is approximately half the internal filter's sample rate.

The filtering is designed to meet the ETS 300 086 specification.

Various powersave modes are incorporated.

MOD1 and MOD2 Attenuators
The MOD1 input can be connected directly to SUM OUT, so that the MOD1 and MOD2 outputs can then be used for two point modulation. Alternatively, the MOD1 attenuator can be used for auxiliary gain adjustment, in which case the input signal must be ac coupled with a suitable capacitor.

DTMF Encoder
This generates the standard DTMF tones according to the CONTROL 2 Register settings. It also has a powersave mode.

FFSK Tx
The Tx function of the FFSK modem operates continuously in a free format mode, which means that the preamble and frame sync have to be programmed like normal data bytes. However, a 2-byte checksum may be generated automatically by simply marking the beginning and end of the data to be used. Any number of whole bytes may be used to generate the checksum.

After the last byte has been transmitted one additional "hang bit" is automatically added to the end. All Tx operations are programmed from the "C-BUS" via an 8-bit buffer. The Tx part of the FFSK modem has a powersave mode.

The modulation output is one cycle of 1200Hz for a "1" and one and a half cycles of 1800Hz for a "0" at 1200 baud, or one half cycle of 1200Hz for a "1" and one cycle of 2400Hz for a "0" at 2400 baud.

FFSK Rx
In Rx, the modem automatically achieves bit sync and then recognises the previously selected SYNC and/or SYNT word of the MPT1327, ETS 300 230 or PAA1382 specifications. At the same time as the above, it can also recognise a user programmed 16-bit RX SYNC WORD.

On reception of the SYNC, SYNT or RX SYNC WORD, the device will automatically (or manually at any time) start checking the data and checksum. It provides a 1-bit correct/incorrect result every byte, so that any number of bytes can be checked.

The Rx part of the FFSK modem operates at 1200 or 2400 baud and has a powersave mode. Both FFSK Rx and Tx work in half duplex mode.

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1.5.1 Software Description

Address/Commands
Instructions and data are transferred, via "C-BUS", in accordance with the timing information given in Figure 11.

Instruction and data transactions to and from the FX829 consist of an Address/Command (A/C) byte followed by either:

(i) a further instruction or data (1 or 2 bytes) or
(ii) a status or Rx data reply (1 byte)

8-bit Write Only Registers

HEX ADDRESS/ COMMAND	REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
$01	RESET	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
$10	CONTROL 1	AMP1	AMP2	AUDIO	FFSKRX	FFSKTX	UK/F	MIC	B/W
$11	CONTROL 2	CHKSUM	DTMFEN	DTMFHI	DTMFLO	DTMF3	DTMF2	DTMF1	DTMF0
$13	AUDIO ATTENUATION	0	0	0	<---------- GAIN ----------> BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$40	CONTROL 3/ IRQ ENABLE	0	1200/2400	TXIDLEM	RXDATAM	TXDATAM	RX SYNC WORD PRIME	SYNT PRIME	SYNC PRIME
$43	TXDATA	<---------- TXDATA ----------> BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

16-bit Write Only Registers

HEX ADDRESS/ COMMAND	REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
$12	MOD LEVELS (1)	0	0	MOD 1 ENABLE	<---------- MOD 1 ----------> BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	(2)	0	0	0	<---------- MOD 2 ----------> BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$44	RX SYNC WORD (1)	<---------- RX SYNC WORD ---------- BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
	(2)	<---------- RX SYNC WORD ---------- BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

Write Only Register Description

RESET Register (Hex address $01)
The reset command has no data attached to it. It sets the device registers into the specific states as listed below:

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REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 D0)
CONTROL 1	0	0	0	0	0	0	0	0
CONTROL 2	0	0	0	0	0	0	0	0
CONTROL 3/IRQ ENABLE	0	0	0	0	0	0	0	0
AUDIO ATTENUATION	0	0	0	0	0	0	0	0
TXDATA	X	X	X	X	X	X	X	X
MOD LEVELS (1)	0	0	0	0	0	0	0	0
MOD LEVELS (2)	0	0	0	0	0	0	0	0
RX SYNC WORD (1)	X	X	X	X	X	X	X	X
RX SYNC WORD (2)	X	X	X	X	X	X	X	X
STATUS	0	0	0	0	0	0	0	0
RXDATA	X	X	X	X	X	X	X	X

X = undefined

CONTROL1 Register (Hex address $10)
This register is used to control the functions of the device as described below:

AMP1 (Bit 7)
When this bit is "1", AMP1 is enabled.
When this bit is "0", AMP1 is disabled (i.e. powersaved).

AMP2 (Bit 6)
When this bit is "1", both AMP2 and MOD2 are enabled.
When this bit is "0", both AMP2 and MOD2 are disabled (i.e. powersaved) and the MOD2 output is pulled to V_{BIAS} via a 1MΩ resistor.

AUDIO (Bit 5)
When this bit is "1", the audio filter/limiter section is enabled.
When this bit is "0", the audio filter/limiter section is disabled (i.e. powersaved).

FFSKRX (Bit 4)
When this bit is "1", the FFSK Rx is enabled.
When this bit is "0", the FFSK Rx is disabled (i.e. powersaved).

Note:
1. The FFSK Rx and Tx cannot both be enabled at the same time. If both FFSKRX and FFSKTX are "1", then they will both be disabled (i.e. powersaved).

FFSKTX (Bit 3)
When this bit is "1", the FFSK Tx is enabled.
When this bit is "0", the FFSK Tx is disabled (i.e. powersaved).

Note:
1. The FFSK Tx and Rx cannot both be enabled at the same time. If both FFSKTX and FFSKRX are "1", then they will both be disabled (i.e. powersaved).
2. The DTMF Encoder and FFSK Tx cannot both be enabled at the same time. If both DTMFEN and FFSKTX are "1", then they will both be disabled.

UK/F (Bit 2)
When this bit is "1", the SYNC/SYNT is set to the PAA standard of "1011010000110011" (SYNC)
When this bit is "0", the SYNC/SYNT is set to the MPT standard of "1100010011010111" (SYNC)

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MIC (Bit 1)
When this bit is "1", the MIC input is enabled and the AMP1 (DEMODIN) input is disabled.
When this bit is "0", the AMP1 (DEMODIN) input is enabled and the MIC input is disabled.

B/W (Bit 0)
When this bit is "1", the bandwidth of the audio path is set wide for 20kHz/25kHz RF channel spacing.
When this bit is "0", the bandwidth of the audio path is set narrow for 12.5kHz RF channel spacing.

CONTROL 2 Register (Hex address $11)
This register is used to control the functions of the device as described below:

CHKSUM (Bit 7)
In the Tx mode, when this bit is "1", the checksum generator is enabled. All complete bytes that are transmitted after this time are used in the checksum calculation.
When this bit goes from "1" to "0", the checksum generator will complete its calculations on the current byte and the result will be sent as the next two bytes of transmitted data.

In the Rx mode, the "0" to "1" transition of the CHKSUM bit is used at the start of the next byte received at DEMODIN to manually reset the Rx checksum calculation, see Figure 4. The calculation can also be reset automatically by a SYNC, SYNT, or RX SYNC WORD detection - see CONTROL 3 / IRQ ENABLE Register. In this case, the Rx checksum calculation starts with the first data byte after the 2-byte sync word has been detected. The CHKSUM bit can be reset to "0" at any time. The result of the checksum is made available in the STATUS Register after the reception of every complete byte (See RXSUMF bit of the STATUS Register).

Note that the device is designed to work with any message length, and as a consequence it is not aware of the position of the checksum within the incoming data message. It thus performs a checksum assessment after every received byte. The controlling software should use its knowledge of the system message length in order to determine which RXSUMF reading is valid, i.e. after the second of the two checksum bytes has been received.

The timing of data bytes relative to the checksum bit is shown in Figures 3 and 4.

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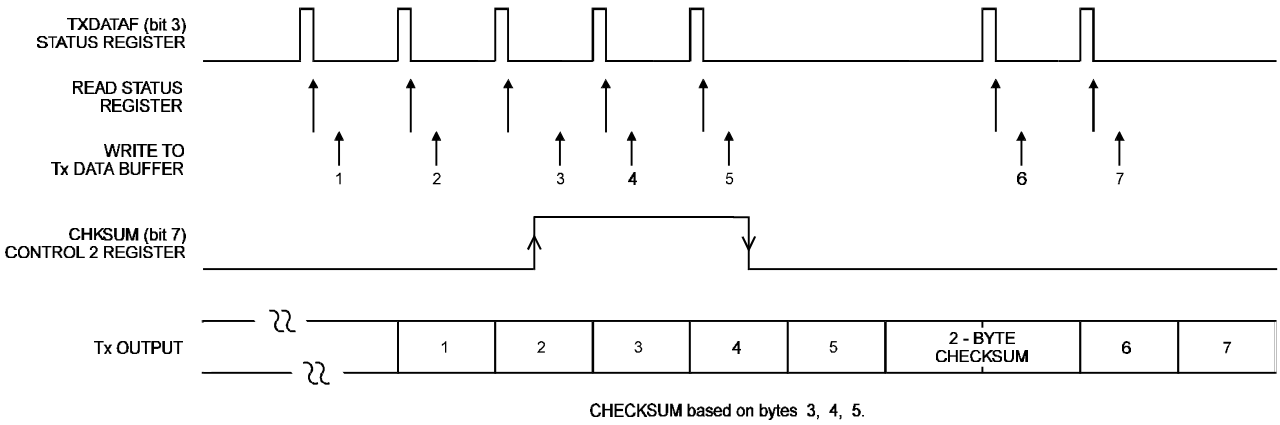


Figure 3 Checksum Generation in Tx Mode

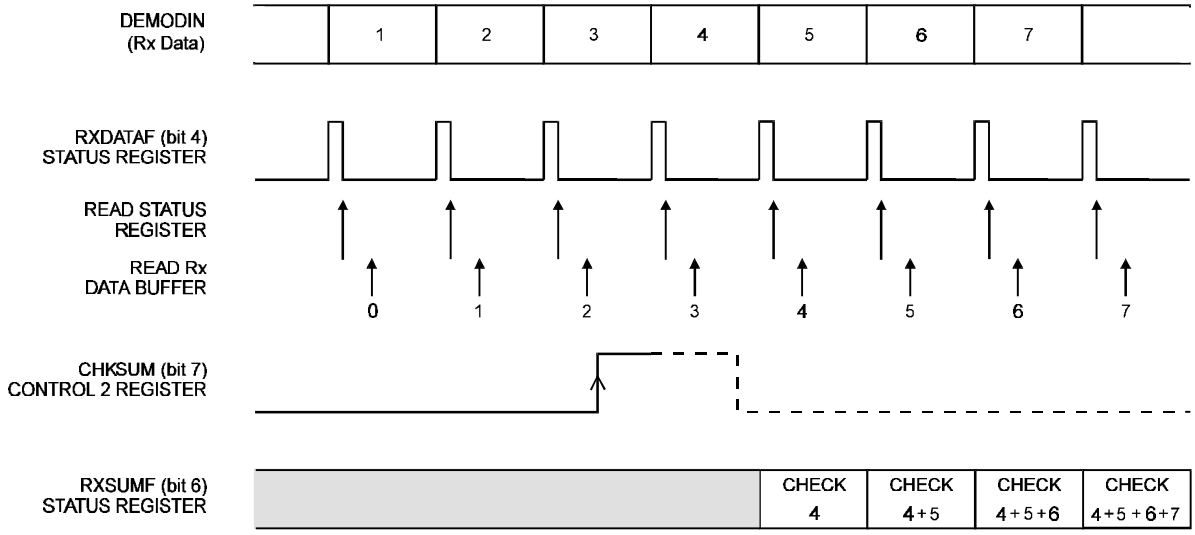


Figure 4 Checksum Calculation in Rx Mode

DTMFEN (Bit 6)

When this bit is "1", the DTMF output is enabled.
When this bit is "0", the DTMF output is disabled. As the powersave of the DTMF is performed in the DTMFHI and DTMFLO registers, this bit allows a fast start up time for the tones.

Note:
1. The DTMF Encoder and FFSK Tx cannot both be enabled at the same time. If both DTMFEN and FFSKTX are "1", then they will both be disabled.

DTMFHI (Bit 5)

When this bit is "1", the DTMF high frequency tone generator is enabled. It will not appear on the output pin unless or until the DTMFEN is "1".
When this bit is "0", the DTMF high frequency tone generator is disabled (i.e. powersaved).

DTMFLO (Bit 4)

When this bit is "1", the DTMF low frequency tone generator is enabled. It will not appear on the output pin unless or until the DTMFEN is "1".
When this bit is "0", the DTMF low frequency tone generator is disabled (i.e. powersaved).

DTMF3, DTMF2, DTMF1, DTMF0 (Bit 3, Bit 2, Bit 1, Bit 0)

These four bits define the DTMF tones according to the table below:

Bit 3	Bit 2	Bit 1	Bit 0	DTMF Tones	DTMF 'Digit'
0	0	0	0	1209Hz + 697Hz	1
0	0	0	1	1209Hz + 770Hz	4
0	0	1	0	1209Hz + 852Hz	7
0	0	1	1	1209Hz + 941Hz	*
0	1	0	0	1337Hz + 697Hz	2
0	1	0	1	1337Hz + 770Hz	5
0	1	1	0	1337Hz + 852Hz	8
0	1	1	1	1337Hz + 941Hz	0
1	0	0	0	1478Hz + 697Hz	3
1	0	0	1	1478Hz + 770Hz	6
1	0	1	0	1478Hz + 852Hz	9
1	0	1	1	1478Hz + 941Hz	#
1	1	0	0	1634Hz + 697Hz	A
1	1	0	1	1634Hz + 770Hz	B
1	1	1	0	1634Hz + 852Hz	C
1	1	1	1	1634Hz + 941Hz	D

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AUDIO ATTENUATION Register (Hex Address $13)
The five least significant bits in this register are used to set the attenuation of the audio volume control according to the table below:

4	3	2	1	0	Audio Attenuation
0	0	0	0	0	Off
0	0	0	0	1	48.0dB
0	0	0	1	0	46.4dB
0	0	0	1	1	44.8dB
0	0	1	0	0	43.2dB
0	0	1	0	1	41.6dB
0	0	1	1	0	40.0dB
0	0	1	1	1	38.4dB
0	1	0	0	0	36.8dB
0	1	0	0	1	35.2dB
0	1	0	1	0	33.6dB
0	1	0	1	1	32.0dB
0	1	1	0	0	30.4dB
0	1	1	0	1	28.8dB
0	1	1	1	0	27.2dB
0	1	1	1	1	25.6dB
1	0	0	0	0	24.0dB
1	0	0	0	1	22.4dB
1	0	0	1	0	20.8dB
1	0	0	1	1	19.2dB
1	0	1	0	0	17.6dB
1	0	1	0	1	16.0dB
1	0	1	1	0	14.4dB
1	0	1	1	1	12.8dB
1	1	0	0	0	11.2dB
1	1	0	0	1	9.6dB
1	1	0	1	0	8.0dB
1	1	0	1	1	6.4dB
1	1	1	0	0	4.8dB
1	1	1	0	1	3.2dB
1	1	1	1	0	1.6dB
1	1	1	1	1	0dB

Bits 5, 6 and 7 should always be set to "0".

CONTROL 3 / IRQ ENABLE Register (Hex address $40**)**
This register is a mixture of control bits and interrupt mask bits, as detailed below:

Bit 7 Not used, set to zero.

1200/2400 (Bit 6) When this bit is "1", the FFSK Rx and Tx are set to operate at 1200 baud. When this bit it "0", the FFSK Rx and Tx are set to operate at 2400 baud.

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TXIDLEM (Bit 5) When this bit is "1", the TXIDLE interrupt will be gated out to the IRQN pin. When this bit is "0", the TXIDLE interrupt will be inhibited. This bit has no effect on the contents of the STATUS register.

RXDATAM (Bit 4) When this bit is "1", the RXDATA interrupt will be gated out to the IRQN pin. When this bit is "0", the RXDATA interrupt will be inhibited. This bit has no effect on the contents of the STATUS register.

TXDATAM (Bit 3) When this bit is "1", the TXDATA interrupt will be gated out to the IRQN pin. When this bit is "0", the TXDATA interrupt will be inhibited. This bit has no effect on the contents of the STATUS register.

RX SYNC WORD PRIME (Bit 2) When this bit is set to "1", it enables the RX SYNC WORD detection. It is cleared/disabled when a SYNC, SYNT, or RX SYNC WORD is detected. It may also be cleared/disabled by writing "0" directly to this bit.

SYNT PRIME (Bit 1) When this bit is set to "1", it enables the SYNT detection. It is cleared/disabled when a SYNC, SYNT, or RX SYNC WORD is detected. It may also be cleared/disabled by writing "0" directly to this bit.

SYNC PRIME (Bit 0) When this bit is set to "1", it enables the SYNC detection. It is cleared/disabled when a SYNC, SYNT, or RX SYNC WORD is detected. It may also be cleared/disabled by writing "0" directly to this bit.

TXDATA Register (Hex Address $43)

This is the Tx data output register. It is double buffered, thus giving the user up to 8 bit periods to load in the next 8 bits. FFSK data is transmitted immediately it is loaded if the transmitter is idle. Data is transmitted in 8-bit bytes, bit 7 (MSB) will be transmitted first.

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MOD LEVELS Register (Hex address $12)
The six least significant bits of the first byte in this register are used to set the attenuation of the Modulator 1 amplifier and the five least significant bits of the second byte in this register are used to set the attenuation of the Modulator 2 amplifier, according to the tables below:

5	4	3	2	1	0	Mod. 1 Attenuation
0	X	X	X	X	X	Disabled (V_{BIAS})
1	0	0	0	0	0	>40dB
1	0	0	0	0	1	12.0dB
1	0	0	0	1	0	11.6dB
1	0	0	0	1	1	11.2dB
1	0	0	1	0	0	10.8dB
1	0	0	1	0	1	10.4dB
1	0	0	1	1	0	10.0dB
1	0	0	1	1	1	9.6dB
1	0	1	0	0	0	9.2dB
1	0	1	0	0	1	8.8dB
1	0	1	0	1	0	8.4dB
1	0	1	0	1	1	8.0dB
1	0	1	1	0	0	7.6dB
1	0	1	1	0	1	7.2dB
1	0	1	1	1	0	6.8dB
1	0	1	1	1	1	6.4dB
1	1	0	0	0	0	6.0dB
1	1	0	0	0	1	5.6dB
1	1	0	0	1	0	5.2dB
1	1	0	0	1	1	4.8dB
1	1	0	1	0	0	4.4dB
1	1	0	1	0	1	4.0dB
1	1	0	1	1	0	3.6dB
1	1	0	1	1	1	3.2dB
1	1	1	0	0	0	2.8dB
1	1	1	0	0	1	2.4dB
1	1	1	0	1	0	2.0dB
1	1	1	0	1	1	1.6dB
1	1	1	1	0	0	1.2dB
1	1	1	1	0	1	0.8dB
1	1	1	1	1	0	0.4dB
1	1	1	1	1	1	0dB

4	3	2	1	0	Mod. 2 Attenuation
0	0	0	0	0	>40dB
0	0	0	0	1	6.0dB
0	0	0	1	0	5.8dB
0	0	0	1	1	5.6dB
0	0	1	0	0	5.4dB
0	0	1	0	1	5.2dB
0	0	1	1	0	5.0dB
0	0	1	1	1	4.8dB
0	1	0	0	0	4.6dB
0	1	0	0	1	4.4dB
0	1	0	1	0	4.2dB
0	1	0	1	1	4.0dB
0	1	1	0	0	3.8dB
0	1	1	0	1	3.6dB
0	1	1	1	0	3.4dB
0	1	1	1	1	3.2dB
1	0	0	0	0	3.0dB
1	0	0	0	1	2.8dB
1	0	0	1	0	2.6dB
1	0	0	1	1	2.4dB
1	0	1	0	0	2.2dB
1	0	1	0	1	2.0dB
1	0	1	1	0	1.8dB
1	0	1	1	1	1.6dB
1	1	0	0	0	1.4dB
1	1	0	0	1	1.2dB
1	1	0	1	0	1.0dB
1	1	0	1	1	0.8dB
1	1	1	0	0	0.6dB
1	1	1	0	1	0.4dB
1	1	1	1	0	0.2dB
1	1	1	1	1	0dB

X = don't care

MOD1 ENABLE (Bit 5, first byte) When this bit is "1" the MOD1 attenuator is enabled. When this bit is "0" the MOD1 attenuator is disabled (i.e. powersaved).

Bits 6 and 7 in the first byte and bits 5, 6 and 7 in the second byte should always be set to "0". MOD LEVELS (1) register is loaded first.

Note: The MOD2 attenuator is enabled by the AMP2 ENABLE signal (bit 6 of CONTROL1 register).

RX SYNC WORD Register (Hex $44)
This is a two byte register that defines the 16-bit programmable synchronisation word. This word is compared with the incoming Rx data and, if a match is found, it is indicated in the STATUS register and an interrupt is generated. Bit 15, the MSB of the first byte, is loaded first.

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8-bit Read Only Registers

HEX ADDRESS/ COMMAND	REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
$41	STATUS	0	RXSUMF	TXIDLEF	RXDATAF	TXDATAF	RX SYNC WORDF	SYNTF	SYNCF
$42	RXDATA	<---------- RXDATA ---------->							
		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

Read Only Register Description

STATUS Register (Hex address $41**)**
This register is used to indicate the status of the device as described below:

Bit 7 Not used, always set to zero.

RXSUMF (Bit 6) When this bit is "1", the Rx checksum is correct.
When this bit is "0", the Rx checksum is incorrect.
This bit is updated and latched in after reception of every eight bits (see CHKSUM bit of the CONTROL2 register).

TXIDLEF (Bit 5) When all the Tx data and any checksum and one "hang-bit" have been transmitted, this bit will be set to "1" to indicate that the transmitter is idle. This bit is reset to "0" immediately after reading the STATUS register. When this bit is set to "1", an interrupt may be generated depending on the state of the TXIDLEM bit in the CONTROL 3 / IRQ ENABLE register.

RXDATAF (Bit 4) When a full byte of data is received and is available in the RXDATA register, this bit will be set to "1". This bit is reset to "0" immediately after reading the STATUS register. When this bit is set to "1" an interrupt may be generated depending on the state of the RXDATAM bit in the CONTROL 3 / IRQ ENABLE register.

TXDATAF (Bit 3) When the Tx data buffer is empty this bit will be set to "1".
This bit is reset to "0" immediately after reading the STATUS register. When this bit is set to "1", an interrupt may be generated depending on the state of the TXDATAM bit in the CONTROL 3 / IRQ ENABLE register.

RX SYNC WORDF (Bit 2) This bit is only defined when RX SYNC WORD PRIME is enabled.
When the data sequence specified in the RX SYNC WORD register has been successfully matched to the Rx incoming data, this bit will be set to "1".
This bit is reset to "0" immediately after reading the STATUS register. When this bit is set to "1", an interrupt will be generated, the checksum generator and byte counter will be reset and SYNC PRIME, SYNT PRIME and RX SYNC WORD PRIME will be reset.

SYNTF (Bit 1) This bit is only defined when SYNT PRIME is enabled.
When the data sequence specified by SYNT has been successfully matched to the Rx incoming data, this bit will be set to "1".
This bit is reset to "0" immediately after reading the STATUS register. When this bit is set to "1", an interrupt will be generated, the checksum generator and byte counter will be reset and SYNC PRIME, SYNT PRIME and RX SYNC WORD PRIME will be reset.

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SYNCF (Bit 0) This bit is only defined when SYNC PRIME is enabled.
When the data sequence specified by SYNC has been successfully matched to the Rx incoming data, this bit will be set to "1".
This bit is reset to "0" immediately after reading the STATUS register. When this bit is set to "1", an interrupt will be generated, the checksum generator and byte counter will be reset and SYNC PRIME, SYNT PRIME and RX SYNC WORD PRIME will be reset.

RXDATA Register (Hex address $42)
This register contains the last byte of data received. It is updated every 8 bits at the same time as the RXSUMF bit in the STATUS register is updated.

The RXDATA register is double buffered, thus giving the user up to 8 bit periods to read the data before it is overwritten by the next byte.

1.5.2 FFSK Checksum Generation and Checking

Generation
The checksum generator takes the m x 8 bits from the m bytes of information, sequentially loaded into the TXDATA register and divides them modulo-2, by the generating polynomial:

$$X^{15} + X^{14} + X^{13} + X^{11} + X^4 + X^2 + 1$$

It then takes the 15-bit remainder from the polynomial divider, inverts the last bit and appends an EVEN parity bit generated from the initial m x 8 bits and the 15-bit remainder (with the last bit inverted).

This 16-bit word is used as the "CHECKSUM". See Figure 5.

(m = the number of bytes in the information to be sent)

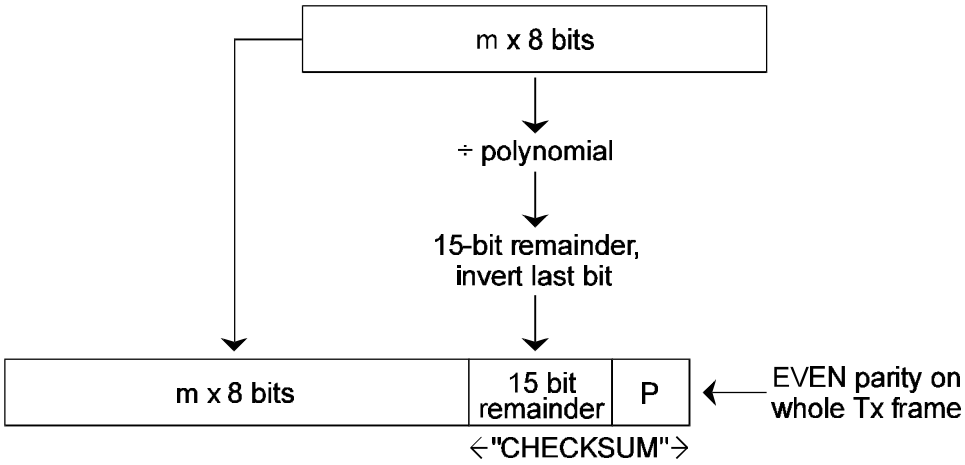


Figure 5 Checksum Generation

Checking
The checksum checker performs two tasks:

It takes the first n-1 bits of a received (n = 8m + 16 bits) message, inverts bit n-1, and divides them modulo-2, by the generating polynomial:

$$X^{15} + X^{14} + X^{13} + X^{11} + X^4 + X^2 + 1$$

The 15 bits remaining in the polynomial divider are checked for all zero.

Secondly, it generates an EVEN parity bit from the first n-1 bits of a received message and compares this bit with the received parity bit (bit n). See Figure 6.

If the 15 bits in the polynomial divider are all zero, and the two parity bits are equal, then the RXSUMF bit (STATUS register bit 6) is set. This is updated and latched every 8 bits, starting at the bit immediately after the initialisation of the bit counter. This initialisation takes place on detection of frame synchronisation, i.e. the matching of received data to the SYNC, SYNT or RX SYNC WORD.

Note that the checksum is calculated on the received data before it is double buffered (see Figure 4).

n = the number of bits in the received message
m = the number of bytes of transmitted data, excluding checksum

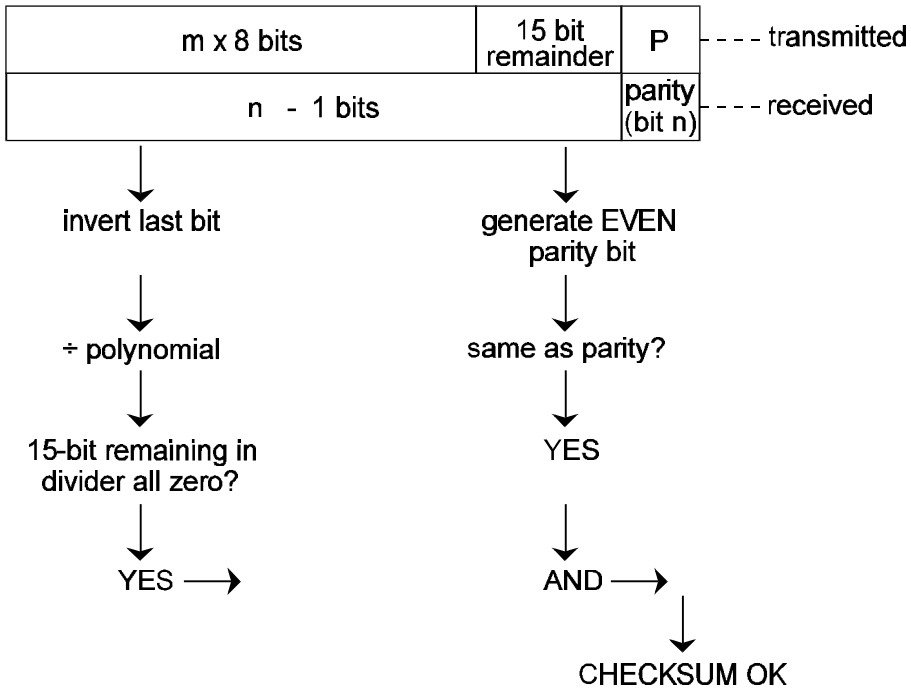


Figure 6 Checksum Checking

1.6 Application Notes

The following block diagrams show the possible arrangements for the pre- and de-emphasis required by PAA1382 and MPT1327 specifications.

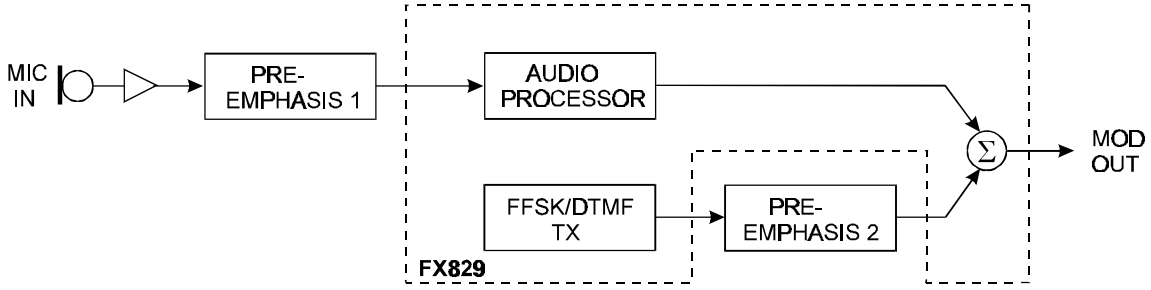


Figure 7a Transmitter Pre-emphasis
(showing both pre-emphasis positions, as required by the PAA1382 specification. Remove pre-emphasis 2 for the MPT1327 specification requirement)

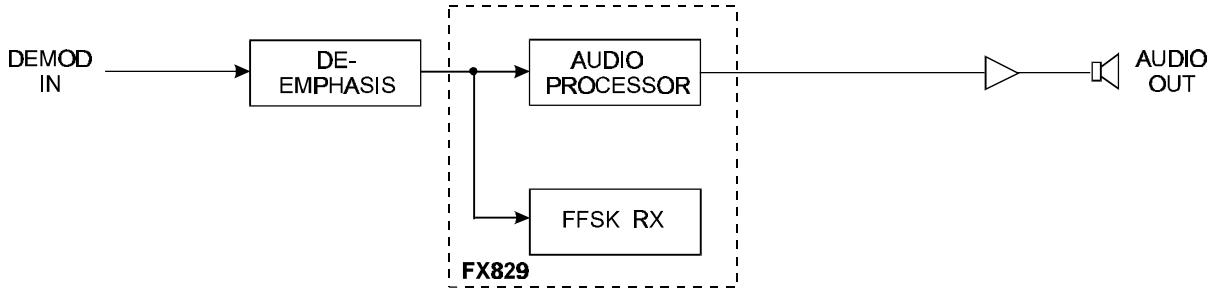


Figure 7b PAA1382 Receiver De-emphasis
(showing position of de-emphasis in all paths, as required by the PAA1382 specification)

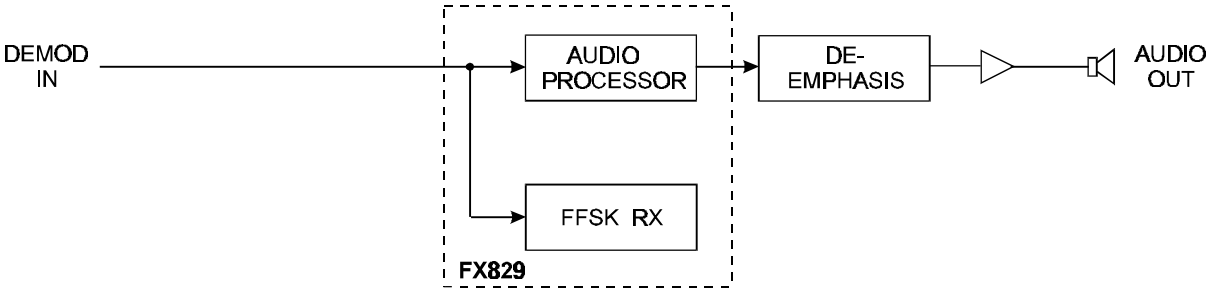


Figure 7c MPT1327 Receiver De-emphasis
(showing position of de-emphasis in audio path only, as required by the MPT1327 specification)

The FX829 should be programmed in the following manner:

1. Perform a General Reset when first applying power to the FX829.

2. Program the FX829 configuration whilst in powersave.

   e.g. UK/F, MIC, B/W, 1200/2400, DTMF0-3,
   DTMFHI, DTMFLO, TXIDLEM, RXDATAM, TXDATAM,
   RX SYNC WORD PRIME, SYNT PRIME, SYNC PRIME,
   MOD1, MOD2, RX SYNC WORD and AUDIO ATTENUATOR.

3. Take the appropriate parts of the FX829 out of powersave by enabling:

   AMP1, AMP2, MOD1, MOD2, AUDIO and (DTMFEN or FFSKTX or FFSKRX).

4. In DTMF Tx mode, a DTMF tone will be generated for the duration that DTMFEN is set to “1”.

5. In FFSK Rx mode, wait for an interrupt (IRQN = “0”) or poll the STATUS register. Remember that all status flags are reset after reading the STATUS register.

   (a) If RXSYNCWORDF, SYNTF or SYNCF become set to “1”, the corresponding synchronisation word has been detected. This indicates the start of valid Rx data. The checksum calculation will be automatically reset. Note that the timing of RXDATAF will be re-aligned by the generation of a SYNC, SYNT or RX SYNC WORD interrupt.

   (b) When RXDATAF subsequently becomes set to “1”, read the Rx data from the RXDATA register. (Note that RXDATAF will be set every 8 bits regardless of whether valid Rx data is being received or not. Sync and checksum patterns should be considered for validating the data).

   (c) If RXSUMF becomes set to “1”, then all of the Rx data sent (starting after the synchronisation word and terminating with a checksum) will have been correctly received. Note that it is necessary to know in advance what message length is expected, in order to determine at which point RXSUMF is valid (i.e. after the interrupt for the second checksum data byte being received has occurred). The RXSUMF bit is invalid at all other times. When RXSUMF becomes set to “1”, the last two bytes of Rx data received will represent the two-byte checksum transmitted. The first checksum byte will already have been read from the RXDATA register, the last byte is available to be read, as the RXDATAF bit will also have been set to “1”.

6. In FFSK Tx mode, wait for an interrupt (IRQN = “0”) or poll the STATUS register. Remember that all status flags are reset after reading the STATUS register.

   (a) Do not send Tx data until the TXDATAF bit has been set to “1”. When the TXDATAF bit is next set to “1”, write the first byte of Tx data to the TXDATA register. If the transmit buffer is empty, this data will be transmitted immediately, causing the TXDATAF bit to be set to “1” approximately one FFSK bit-period after the TXDATA register has been loaded with data. (Any TXIDLEF bit set upon entering FFSK Tx mode should be ignored).

   (b) The next byte of Tx data should be written to the TXDATA register as soon as the TXDATAF bit has been set to “1”. Once this has been done, the TXDATAF bit will again be set to “1” eight FFSK bit-periods after the TXDATA register was loaded with the second byte of data.

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(c) Subsequent bytes of Tx data should be written to the TXDATA register as soon as the TXDATAF bit has been set to"1". After the last byte of Tx data has been loaded, the TXDATAF bit will be set after both 8 and 16 FFSK bit-periods followed by the TXIDLEF bit which will be set approximately one FFSK bit-period later, to indicate that the final bit has been transmitted.

(d) The TXDATAF bit will continue to be set every 8 FFSK bit-periods, regardless of whether Tx data is written to the TXDATA register or not, providing the transmitter is enabled (FFSK Tx mode = FFSKTX bit set to "1"). Note that whilst the 2-byte checksum is being generated and transmitted, the TXDATAF bit will not be set for approximately 24 FFSK bit-periods.

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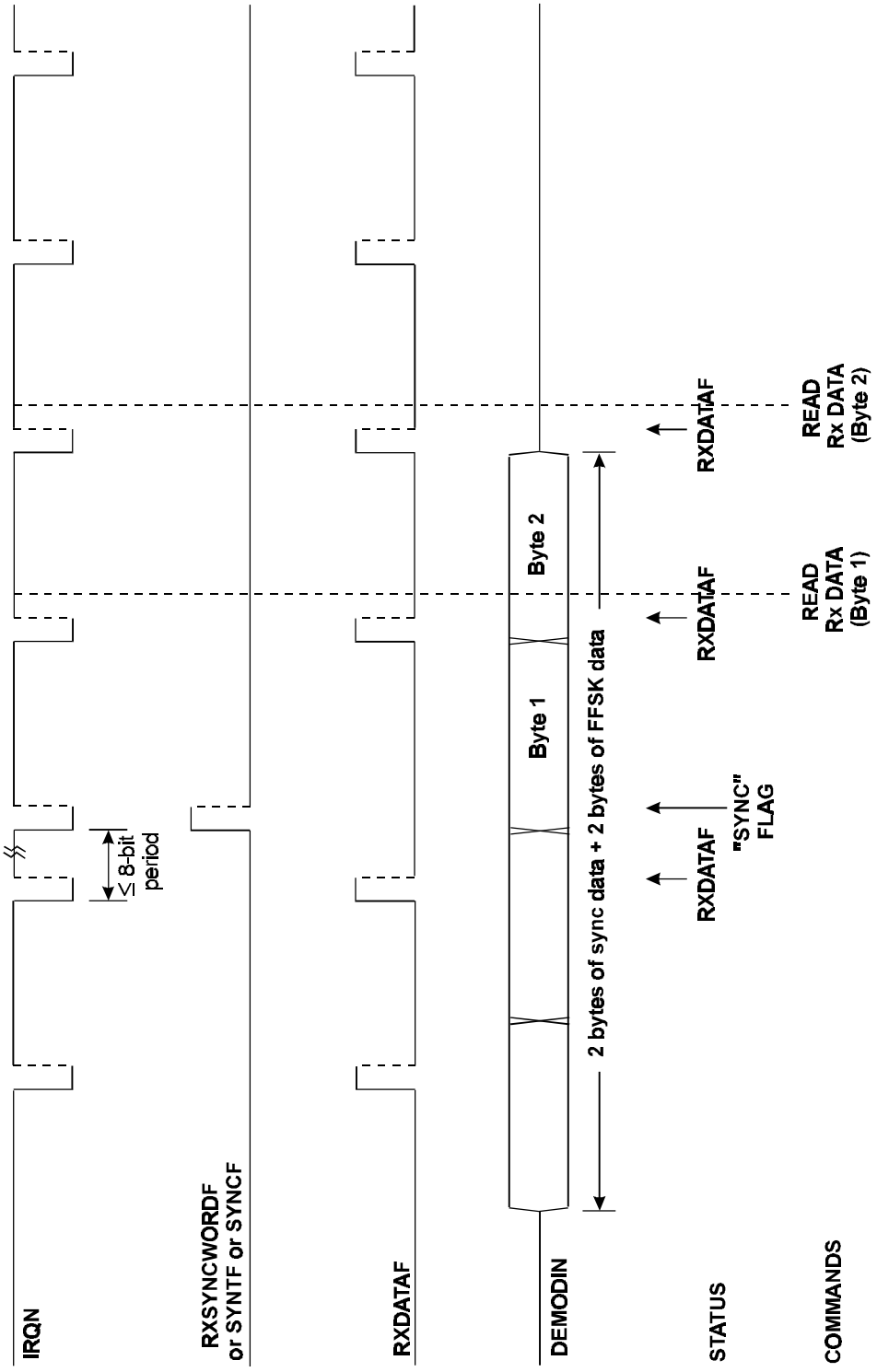


Figure 8 Reception of 2 Bytes of Data

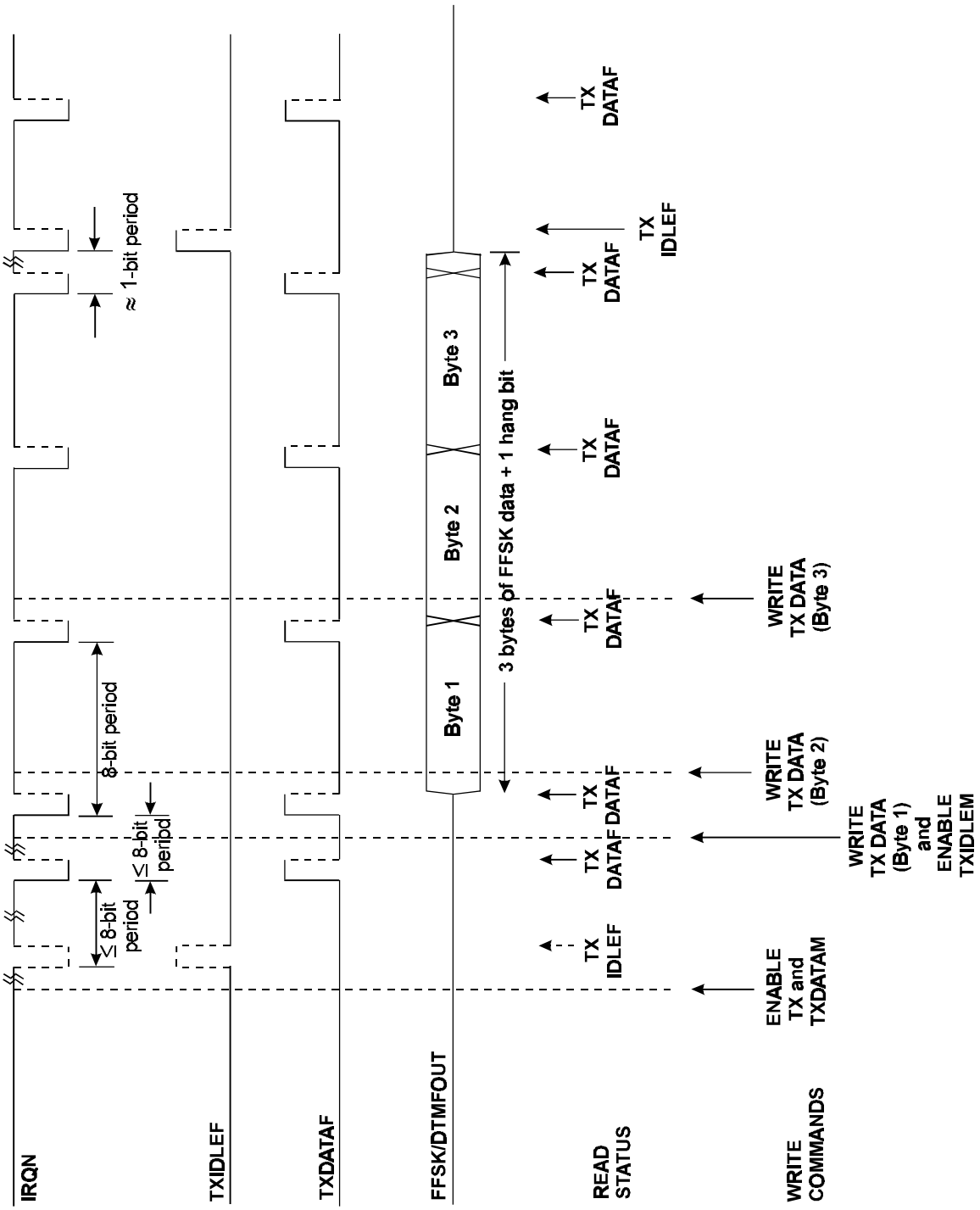


Figure 9 Transmission of 3 Bytes of Data

1.7 Performance Specification

1.7.1 Electrical Performance

Absolute Maximum Ratings
Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current into or out of V_{DD} and V_{SS} pins	-30	+30	mA
Current into or out of any other pin	-20	+20	mA

D2 Package	**Min.**	**Max.**	**Units**
Total Allowable Power Dissipation at Tamb = 25°C		800	mW
... Derating		13	mW/°C
Storage Temperature	-40	+85	°C
Operating Temperature	-40	+85	°C

D5 Package	**Min.**	**Max.**	**Units**
Total Allowable Power Dissipation at Tamb = 25°C		550	mW
... Derating		9	mW/°C
Storage Temperature	-40	+85	°C
Operating Temperature	-40	+85	°C

Operating Limits
Correct operation of the device outside these limits is not implied.

	Notes	**Min.**	**Max.**	**Units**
Supply (V_{DD} - V_{SS})		3.0	5.5	V
Operating Temperature		-40	+85	°C
Xtal Frequency		4.0315968	4.0324032	MHz

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Operating Characteristics

For the following conditions unless otherwise specified:

Xtal Frequency = 4.032MHz, Bit Rate = 1.2k bits/sec, Noise Bandwidth = Bit Rate,
Audio Level 0dB ref = 308mVrms at 1kHz
V_{DD} = 3.3V to 5.0V, Tamb = -40°C to +85°C.

		Notes	Min.	Typ.	Max.	Units
DC Parameters						
I_{DD} (Powersaved)	(V_{DD} = 5.0V)	2	-	0.6	1.5	mA
I_{DD} (Tx or Rx Voice)	(V_{DD} = 5.0V)	2	-	5.0	8.0	mA
I_{DD} (Powersaved)	(V_{DD} = 3.3V)	2	-	0.3	1.0	mA
I_{DD} (Tx or Rx Voice)	(V_{DD} = 3.3V)	2	-	2.7	4.0	mA
"C-BUS" Interface						
Input Logic "1"			70%	-	-	V_{DD}
Input Logic "0"			-	-	30%	V_{DD}
Input Leakage Current (logic "1" or "0")			-1.0	-	1.0	µA
Input Capacitance			-	-	7.5	pF
Output Logic "1" (I_{OH} = 120µA)			90%			V_{DD}
Output Logic "0" (I_{OL} = 360µA)					10%	V_{DD}
"Off" State Leakage Current (Vout = V_{DD})		9	-	-	10	µA
AC Parameters						
Input Sensitivity (for 0dB output)						
Tx Audio Input (MIC)		8	-	308	-	mVrms
Rx Audio Input (DEMODFB)		8	-	308	-	mVrms
Output Drive Level						
For 60% Deviation		1, 6, 8	291	308	326	mVrms
For 100% Deviation		1, 6, 7, 8	-	1440	-	mVpk-pk
Audio Filters						
Gain at 1kHz		5	-	0	-	dB
Passband Ripple		5	-2.0	-	0.5	dB
SINAD		5, 14	-	59	-	dBp
Signal Path Noise		5	-	-55	-	dB
Narrrow Audio Bandwidth Setting						
Passband Frequencies		5	300	-	2550	Hz
Stopband Attenuation:	(f = 100Hz)	5	-	3.0	-	dB
	(f = 3400Hz)	5	-	5.5	-	dB
	(f = 6000Hz)	5	10.5	24	-	dB
	(f = 12500Hz)	5	25	49	-	dB
Wide Audio Bandwidth Setting						
Passband Frequencies		5	300	-	3000	Hz
Stopband Attenuation:	(f = 100Hz)	5	-	3.0	-	dB
	(f = 3400Hz)	5	-	3.0	-	dB
	(f = 6000Hz)	5	10.5	19	-	dB
	(f = 25000Hz)	5	39.5	68	-	dB

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		Notes	Min.	Typ.	Max.	Units
Amp 1 and Amp 2						
Open Loop Gain	(I/P = 1mV at 100Hz)		-	70	-	dB
Unity Gain Bandwidth			-	5.0	-	MHz
Input Impedance	(at 100Hz)		10	-	-	MΩ
Output Impedance	(Open Loop)		-	6.0	-	kΩ
	(Closed Loop)		-	600	-	Ω
Distortion (DTMF)			-	2	5	%
FFSK/DTMF TX OUT						
Tx O/P impedance (not powersaved)		3		1.0	2.5	kΩ
Tx O/P impedance (powersaved)		3	300	500	-	kΩ
Signal Level (FFSK)		1	-1	0	+1	dB
Signal Level (DTMF High Tone)		1	-	+2.0	-	dB
Signal Level (DTMF Low Tone)		1	-	0	-	dB
Distortion (DTMF)			-	2	5	%
FFSK TX OUT						
Isochronous Distortion:						
(1200Hz - 1800Hz)				25	40	µs
(1800Hz - 1200Hz)				25	40	µs
(1200Hz - 2400Hz)				20	30	µs
(2400Hz - 1200Hz)				20	30	µs
Third Harmonic Distortion				2	3	%
Deviation Limiter						
Threshold		1	-	1300	-	mVpk-pk
Gain			-0.5	-	0.5	dB
Transmitter Modulator Drives						
Input Impedance						
(MOD1 IN, VOLUME IN)	(at 100Hz)		-	15.0	-	kΩ
Mod.1 Attenuator						
Nominal Adjustment Range			0		12.0	dB
Attenuation Accuracy			-1.0	-	1.0	dB
Step Size			0.2	0.4	0.6	dB
Output Impedance		3	-	600	-	Ω
Mod.2 Attenuator						
Nominal Adjustment Range			0		6.0	dB
Attenuation Accuracy			-0.6	-	0.6	dB
Step Size			0.1	0.2	0.3	dB
Output Impedance		3	-	600	-	Ω
Audio Output Attenuator						
Nominal Adjustment Range			0		48.0	dB
Attenuation Accuracy			-1.5	-	1.5	dB
Step Size			-	1.6	-	dB
Output Impedance		3	-	600	-	Ω

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	Notes	Min.	Typ.	Max.	Units
FFSK Receiver					
Signal Input Dynamic Range (SNR = 50dB)	10, 11	100	230	1000	mVrms
Bit Error Rate					
(SNR = 12dB at 1200 Baud)	11	-	2.5	-	10^{-4}
(SNR = 12dB at 2400 Baud)	11	-	1.5	-	10^{-3}
(SNR = 20dB at 1200/2400 Baud)	11	-	1.0	-	10^{-8}
Receiver Synchronisation (SNR = 12dB)	12				
Probability of Bit 16 being correct			0.995		
Carrier Detect					
Sensitivity	12, 13	-	-	150	mVrms
Probability of Carrier Detection					
- After Bit 16 (SNR = 12dB)			0.995		
- With 230mVrms Noise (No Signal)			0.05		
Miscellaneous Impedances					
FILTER OUT		-	600	-	Ω
Tx Audio Input (MIC) (at 100Hz)		10	-	-	MΩ
Xtal/Clock Input					
'High' pulse width	4	40			ns
'Low' pulse width	4	40			ns
Input Impedance (at 100Hz)		10			MΩ
Gain (I/P = 1mVrms at 100Hz)		20			dB

Notes:

1. At V_{DD} = 5.0V only. Signal levels are proportional to V_{DD}.
2. Not including any current drawn from the modem pins by external circuitry.
   Powersaved = all functions disabled.
   Tx or Rx = device configured into any half-duplex operating mode.
   Currents measured at Tamb = 25°C only.
3. Small signal impedance, at V_{DD} = 5.0V and Tamb = 25°C. A minimum load resistance of 6kΩ is suggested.
4. Timing for an external input to the XTAL/CLOCK pin.
5. Between MIC or AMP1 inputs to Modulator and Audio outputs, see Figures 10a and 10b.
6. It is recommended that these output levels are used to produce 60% or 100% deviation in the transmitter.
7. With the Tx Audio input level 20dB above the level required to produce 0dB at the Output Drives.
8. With output gains set to 0dB.
9. IRQN pin.
10. See Figure 13 (variation of BER with Input Signal Level).
11. SNR = Signal to Noise Ratio in the Bit Rate Bandwidth.
12. For a "10101010101 ...01" pattern.
13. Measured with a 150mVrms input signal (no noise).
14. dBp represents a psophometrically weighted measurement.

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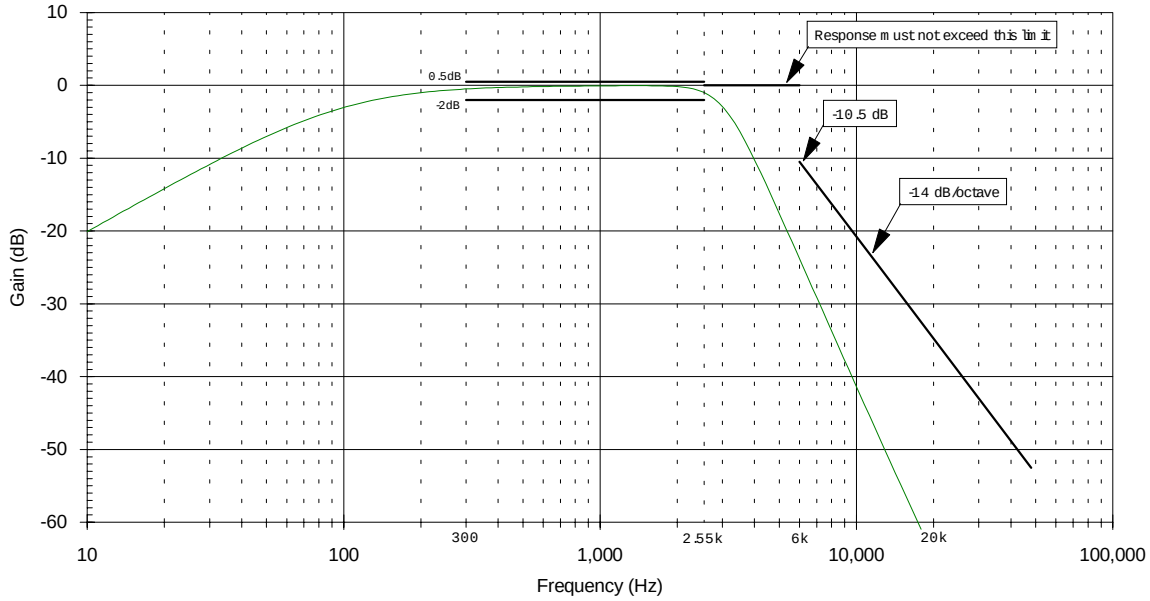


Figure 10a Overall Audio Frequency Response for 12.5kHz Channel Separation

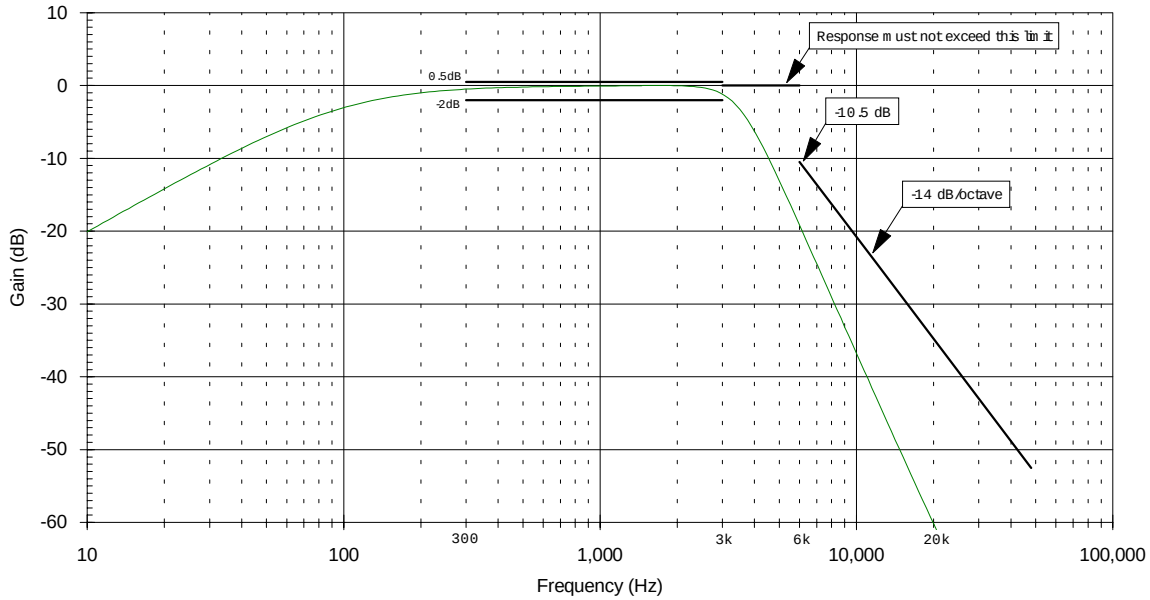


Figure 10b Overall Audio Frequency Response for 20kHz/25kHz Channel Separation

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1.7.1 **Electrical Performance** (continued)

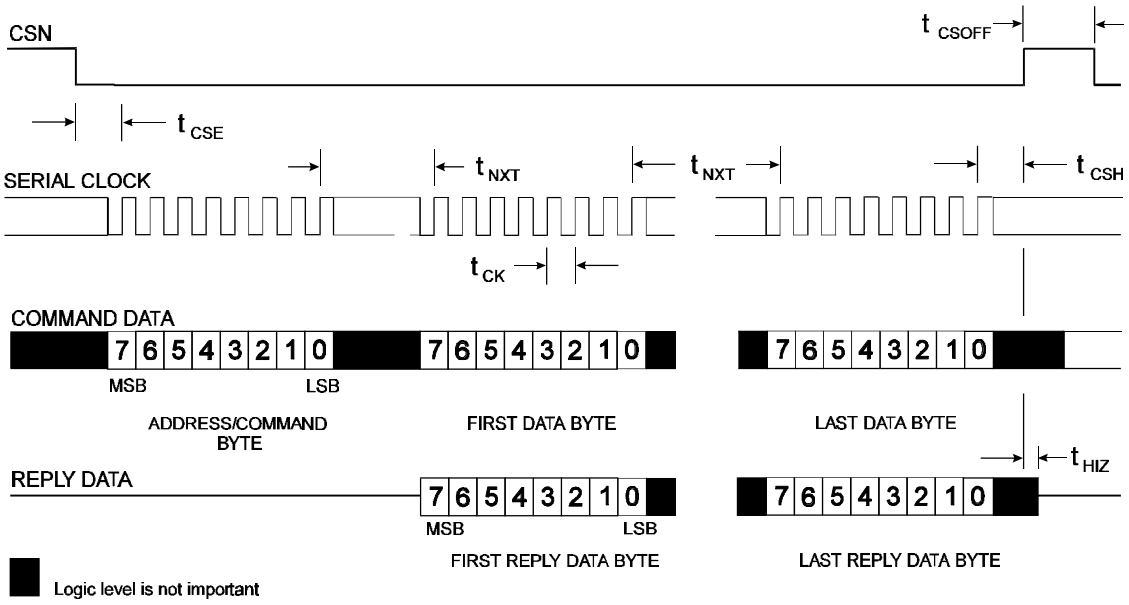


Figure 11 "C-BUS" Timing

For the following conditions unless otherwise specified:

Xtal Frequency = 4.032MHz, V_{DD} = 3.3V to 5.0V, Tamb = -40°C to +85°C.

	Parameter	Notes	Min.	Typ.	Max.	Units
t_{CSE}	"CS-Enable to Clock-High"		2.0		-	µs
t_{CSH}	Last "Clock-High to CS-High"		4.0		-	µs
t_{HIZ}	"CS-High to Reply Output 3-state"		-		2.0	µs
t_{CSOFF}	"CS-High" Time between transactions		2.0		-	µs
t_{NXT}	"Inter-Byte" Time		4.0		-	µs
t_{CK}	"Clock-Cycle" time		2.0		-	µs

Notes:
1. Depending on the command, 1 or 2 bytes of COMMAND DATA are transmitted to the peripheral MSB (bit 7) first, LSB (bit 0) last. REPLY DATA is read from the peripheral MSB (bit 7) first, LSB (bit 0) last.
2. Data is clocked into and out of the peripheral on the rising SERIAL CLOCK edge.
3. Loaded commands are acted upon at the end of each command.
4. To allow for differing µController serial interface formats "C-BUS" compatible ICs are able to work with either polarity SERIAL CLOCK pulses.

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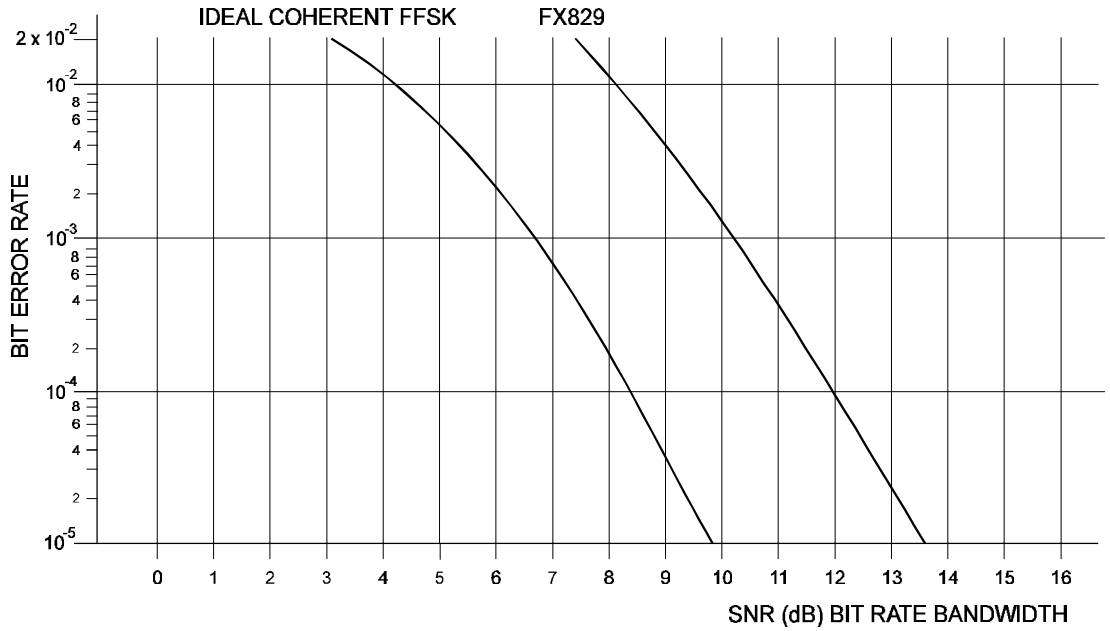


Figure 12 Bit Error Rate Graph

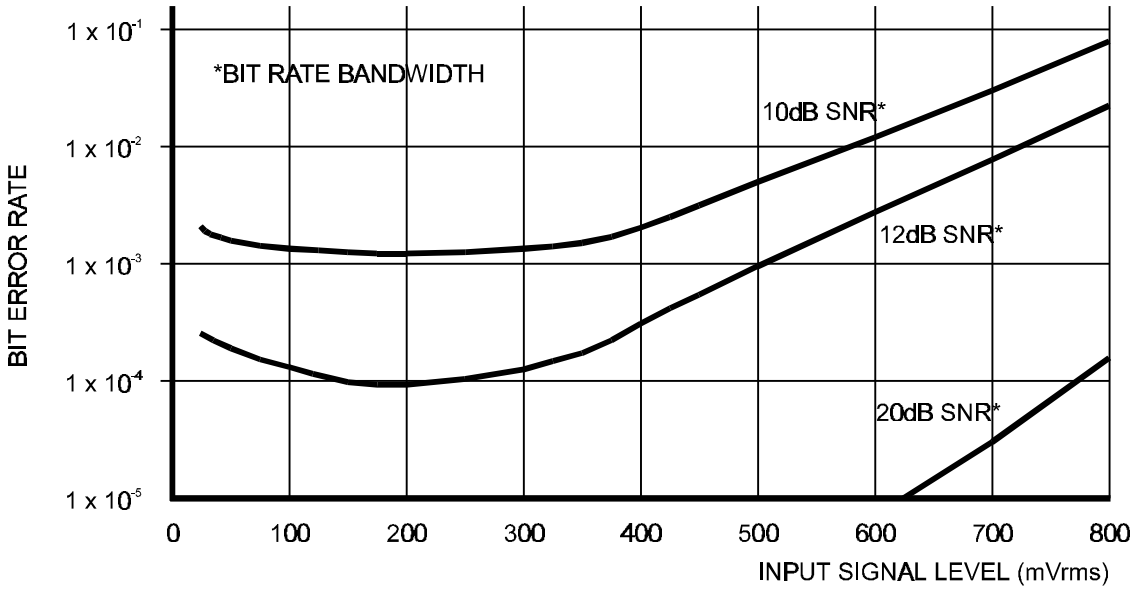
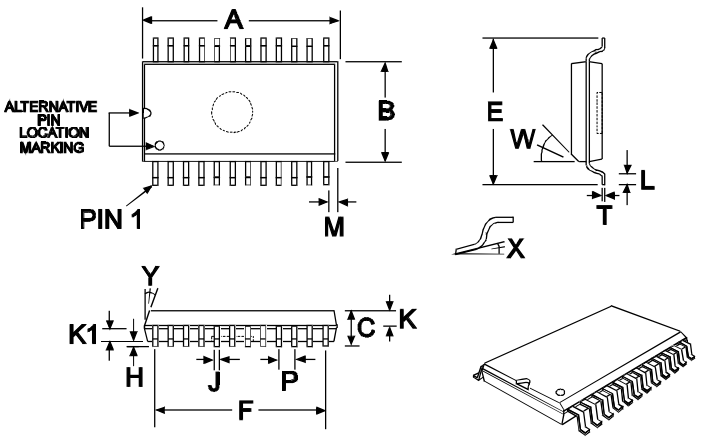


Figure 13 Typical Variation of Bit Error Rate with Input Signal Level

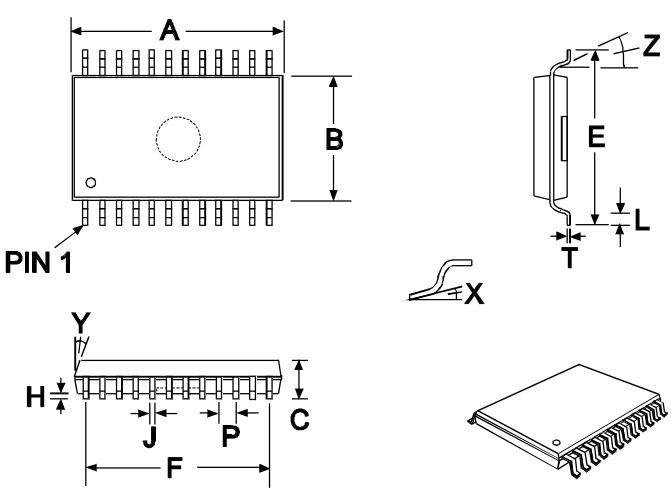
1.7.2 Packaging



DIM.	MIN.	TYP.	MAX.
A	0.597 (15.16)		0.613 (15.57)
B	0.291 (7.39)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.394 (10.01)		0.419 (10.64)
F		0.566 (14.37)	
H	0.004 (0.10)		0.012 (0.30)
J	0.014 (0.36)		0.018 (0.46)
K	0.036 (0.91)		0.046 (1.17)
K1	0.036 (0.91)		0.046 (1.17)
L	0.016 (0.41)		0.050 (1.27)
M	0.021 (0.53)		0.031 (0.79)
P		0.050 (1.27)	
T	0.009 (0.23)		0.012 (0.30)
W		45°	
X	0°		8°
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles in degrees

Figure 14 D2 Mechanical Outline: *Order as part no. FX829D2*

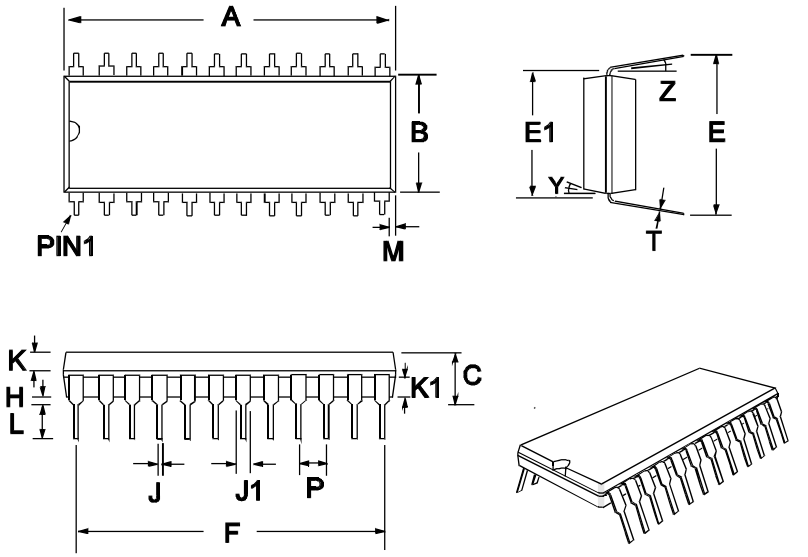


DIM.	MIN.	TYP.	MAX.
A	0.318 (8.07)		0.328 (8.33)
B	0.205 (5.20)		0.212 (5.38)
C	0.068 (1.73)		0.078 (1.99)
E	0.301 (7.65)		0.311 (7.90)
F		0.286 (7.15)	
H	0.002 (0.05)		0.008 (0.21)
J	0.010 (0.25)		0.015 (0.38)
L	0.022 (0.55)		0.037 (0.95)
P		0.026 (0.65)	
T	0.005 (0.13)		0.009 (0.22)
X	0°		8°
Y	7°		9°
Z	4°		10°

NOTE : All dimensions in inches (mm.)
Angles in degrees

Figure 15 D5 Mechanical Outline: *Order as part no. FX829D5*

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DIM.	MIN.	TYP.	MAX.
A	1.200 (30.48)		1.270 (32.26)
B	0.500 (12.70)		0.552 (14.02)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
F		1.10 (27.94)	
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.68)		0.074 (1.88)
K1	0.060 (1.52)		0.074 (1.88)
L	0.121 (3.07)		0.150 (3.81)
M		0.180 (4.58)	
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	
Z		4°	

NOTE : All dimensions in inches (mm.)
Angles in degrees

Figure 16 P4 Mechanical Outline: *Order as part no. FX829P4*

Handling precautions: This product includes input protection, however, precautions should be taken to prevent device damage from electro-static discharge. CML does not assume any responsibility for the use of any circuitry described. No IPR or circuit patent licences are implied. CML reserves the right at any time without notice to change the said circuitry and this product specification. CML has a policy of testing every product shipped using calibrated test equipment to ensure compliance with this product specification. Specific testing of all circuit parameters is not necessarily performed.

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CML Microcircuits

COMMUNICATION SEMICONDUCTORS

CML Product Data

In the process of creating a more global image, the three standard product semiconductor companies of CML Microsystems Plc *(Consumer Microcircuits Limited (UK), MX-COM, Inc (USA) and CML Microcircuits (Singapore) Pte Ltd)* have undergone name changes and, whilst maintaining their separate new names *(CML Microcircuits (UK) Ltd, CML Microcircuits (USA) Inc and CML Microcircuits (Singapore) Pte Ltd*), now operate under the single title **CML Microcircuits**.
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Until the latter part of 1996, the differentiator between products manufactured and sold from MXCOM, Inc. and Consumer Microcircuits Limited were denoted by the prefixes MX and FX respectively. These products use the same silicon etc. and today still carry the same prefixes. In the latter part of 1996, both companies adopted the common prefix: CMX.

This notification is relevant product information to which it is attached.

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