SCG2000iG Synchronous Clock Generators

PLL

2111 Comprehensive Drive
Aurora, Illinois 60505
Phone: 630-851-4722
Fax: 630-851-5040
www.conwin.com

Application

The Connor-Winfield SCG2000iG provides high precision phase lock loop frequency translation for telecommunication applications that require a temperature range of -40°C to 85°C.

SCG2000iG is well suited for use in line cards, service termination cards and similar functions to provide reliable reference, phase locked, synchronization and low phase gain for TDM, PDH, SONET and SDH network equipment. The SCG2000iG provides a jitter filtered, wander following, output signal synchronized to a superior Stratum or peer input reference signal. This product is also compliant with all required ROHS specifications.

Features

- **Industrial Temperature Range**
- **3.3V High Precision PLL**
- **Tri-State Capability**
- **Active Alarms**
- **Guaranteed Free Run (20ppm for 19.44MHz output, 25ppm for 65.536MHz and 30ppm for 125.0 MHz)**
- **1 Sec. Acquisition Time**
- **ROHS Compliant**

RoHS COMPLIANT

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General Description

The SCG2000iG provides high precision phase lock loop frequency translation for telecommunication applications. The SCG2000iG generates a CMOS output from an intrinsically low jitter, voltage controlled crystal oscillator. while providing a jitter attenuated, internal reference that is connected to a Reference Output pin.

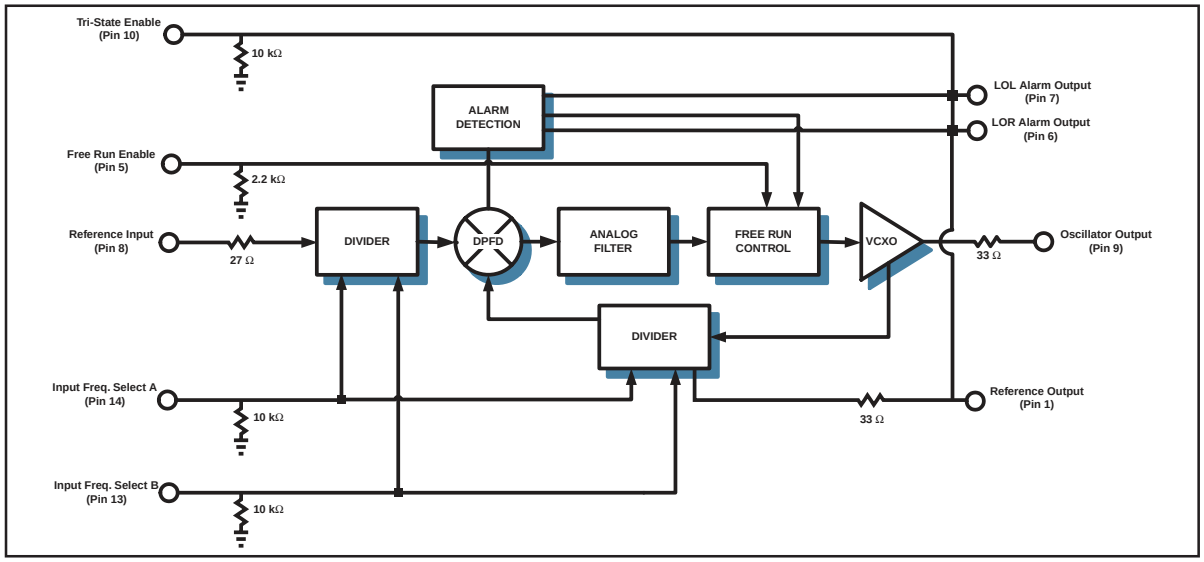
SCG2000iG is well suited for use in line cards, service termination cards and similar functions to provide reliable reference, phase locked, synchronization for TDM, PDH, SONET and SDH network equipment . The SCG2000iG provides a low phase gain (<0.2dB), jitter filtered, wander following output signal synchronized to a superior Stratum or peer input reference signal.

The SCG2000iG include the following features: Free Run, Tri-state and alarm outputs for Loss-of-Reference, (LOR), Loss-of-Lock, (LOL). During the LOR alarm, the SCG2000iG will also enter a Free Run state which will guarantee a 20 ppm accurate output with the 19.44 MHz model, 25ppm accurate with the 65.536 MHz and 30 ppm accurate output with the 125.0 MHz model. Additionally the Free Run mode may be entered manually by asserting a high signal to the Free Run Enable pin. The outputs, except the oscillator output, may be put into the tri-state high impedance condition for external testing purposes by asserting a high signal to the Tri-State Enable pin.

The SCG2000iG operates at 3.3 Volts and typically draws less than 100 mA. All models have an acquisition time of approximately 1.0 second and can be used in applications that require temperature rating of -40° to 85° C. All models have a 33Ω resistor in series with the oscillator output. The SCG2000iG maximum package dimensions are .78" x .83" x .35" on a six layer FR4 board with surface mount pins. Parts are assembled using high temperature solder to withstand surface mount reflow process.

Functional Block Diagram

Figure 1



Model Comparison Table

Table 1

Model	Input Ref Freq	Max Duty Cycle	Reference Output (Pin #1)	Oscillator Output (Pin #9)	Notes
SCG2000G	8-64 kHz	40/60	= Input Ref Freq.	1.544 MHz to 125.0 MHz	Basic Model
SCG2000iG	8-64 kHz	45/55	= Input Ref Freq.	19.44 MHZ, 65.536 MHz, 125.0 MHz	**Industrial Temp. Range**
SCG2010G	**19.44 MHz**	40/60	**8 kHz**	**19.44 MHz**	
SCG2020G	**19.44 MHz**	40/60	**19.44 MHz**	**77.76 MHz**	
SCG2030G	8-64 kHz	**45/55**	= Input Ref Freq.	1.544 MHz to 125.0 MHz	Tight Duty Cycle
SCG2050G	8-64 kHz	40/60	**19.44 MHz**	**77.76 MHz**	
SCG2070G	**19.44 MHz**	40/60	**51.84 MHz, 77.76 MHz**	**51.84 MHz, 77.76 MHz**	Ref Output = Osc Output

*Features which differentiate a model from the base model (SCG2000G) are highlighted in boldface color and in the notes column.

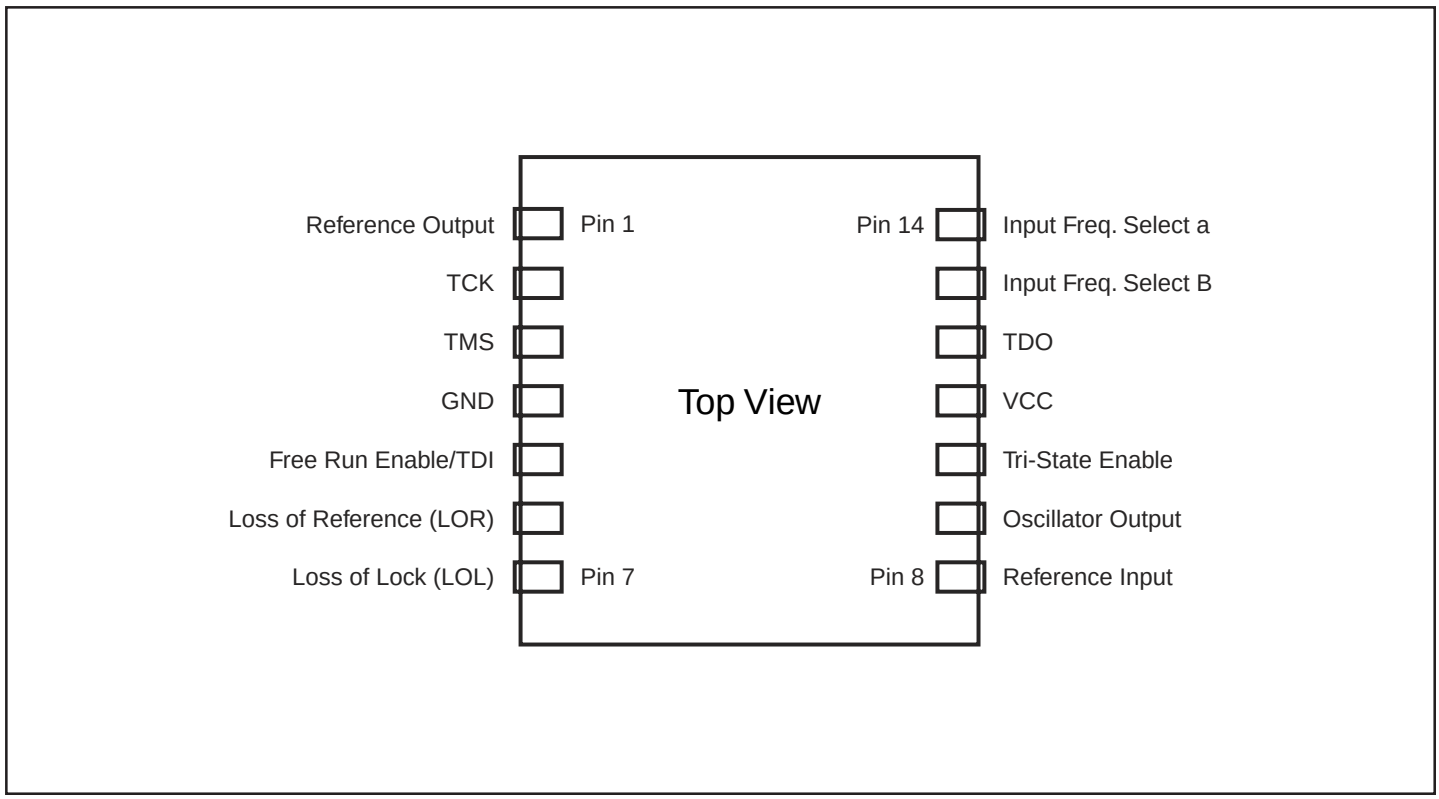
Pin Description

Table 2

Pin #	Connection	Description
1	Reference Output	Output frequency is dependent on SCG model
2	TCK	JTAG pin that is used only by Connor-Winfield for programming. Do not connect
3	TMS	JTAG pin that is used only by Connor-Winfield for programming. Do not connect
4	Ground	Ground
5	Free Run Enable/TDI	Free Run enable pin. 1 = Free Run. Input is pulled to GND
6	Loss of Reference (LOR)	Alarm indicator. 1 = The reference has been lost.
7	Loss of Lock (LOL)	Alarm indicator. 1 = Phase lock has been lost
8	Reference Input	Input reference frequency
9	Oscillator Output	Output frequency is dependent on SCG model
10	Tri-State enable	Tri State control for all outputs except Oscillator Output. 1 = Hi-Z, 0 = normal. Input is pulled to GND.
11	Vcc	3.3V Supply Voltage.
12	TDO	JTAG pin that is used only by Connor-Winfield for programming. Do not connect
13	Input Freq. Select B	Control pin B used to select input frequency. Input is pulled to GND.
14	Input Freq. Select A	Control pin A used to select input frequency. Input is pulled to GND.

Pin Out Diagram

Figure 2



Absolute Maximum Rating

Table 3

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
Vcc	Power Supply Voltage	-0.5		4	Volts	
V1	Input Voltage	-0.5		5.5	Volts	
Ts	Storage Temperature	-65		150	deg. C	

Specifications

Table 4

Parameter	Specifications	Notes
Voltage	3.3V ±5%	1.0
Current	<100 mA Typical	
Temperature Range	-40° to 85°C	
Input Jitter Tolerance *(Input Jitter Frequencies ≥ 10 Hz)*	≥31.25us Typical	
Jitter Bandwidth	<15 Hz (8 Hz Typical)	
Typical Acquisition Time Data (SCG2000iG-019.44M & SCG2000iG-125.00M)		
Acquisition from a cold power-up: Phase lock within 1 UI: Phase lock settled: Alarm time: Acquisition from Free Run: Phase lock within 1 UI: Phase lock settled: Alarm time: Frequency lock with a 20PPM reference frequency step: Typically <1 sec.	 ~ 35 sec. ~ 160 sec. < 1 sec. ~ 35 sec. ~ 160 sec, Typically no alarm	
Typical Acquisition Time Data (SCG2000iG-65.536M)		
Acquisition from a cold power-up: Phase lock within 1 UI: Phase lock settled: Alarm time: Acquisition from Free Run: Phase lock within 1 UI: Phase lock settled: Alarm time: Frequency lock with a 20PPM reference frequency step: Typically <0.5 sec.	 ~ 4 sec. ~ 60 sec. < 1 sec. ~ 4 sec. ~ 60 sec. Typically no alarm	
Output Duty Cycle	45/55% Min/Max @ 50% Level	
Capture/Pull-in Range (SCG2000iG-019.44M & SCG2000iG-125.00M)	±32 ppm Minimum	
Capture/Pull-in Range (SCG2000iG-65.536M)	±50 ppm Minimum	
Output Rise and Fall Time (SCG2000iG-019.44M & SCG2000iG-125.00M)	3 ns @ 20% to 80% output level	
Output Rise and Fall Time (SCG2000iG-65.536M)	1ns Typ. (1.5ns Max.) @ 20% to 80% output level	
Output Load (SCG2000iG-019.44M & SCG2000iG-125.00M)	30 pF	
Output Load (SCG2000iG-65.536M)	7.5 pF Max.	

Specifications (Continued)

Alarms	LOR, LOL Status on seperate outputs	
Free Run Accuracy	±20 ppm (19.44 MHz output) ±25 ppm (65.536 MHz output) ±30 ppm (125.0 MHz output)	
Package	Fr4 SM 0.78" x .83" x 0.35" (maximum)	
TDEV	60 ps Typical @60s	
MTIE	750 ps Typical @60s	
Reference Output/Oscillator Output Offset	≤ 8 ns	
Static Offset	± 35 ns Maximum	2.0
Dynamic Offset (25°C - 85°C) (-40°C - 85°C)	± 18 ns Maximum ± 33 ns Maximum	

NOTES: 1.0: Requires external regulation
2.0: Offset between Reference Input and Reference Output @ room temp.

Input And Output Characteristics

Table 5

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
V_{IH}	High Level Input Voltage	2		5.5	V	
V_{IL}	Low Level Input Voltage	0		0.8	V	
T_{IO}	I/O to Output Valid			10	nS	
C_O	Output Capacitance			10	pF	
V_{HO}	High Level Output Voltage I_{oH} = -4mA	2.4				Vcc Min.
V_{IO}	Low Level Output Voltage I_{oL} = 8mA			0.4		Vcc Max.
T_{IR}	Input Reference Signal Pulse Width	30			nS	

Output Jitter Specifications

Table 6

	Jitter BW 10 Hz - 20 MHz		SONET Jitter BW 12 KHz - 20 MHz	
Frequency (MHz)	pS (RMS)	m UI	pS (RMS)	m UI
19.44	10 Typ.	0.194 Typ.	1 Max., 0.5 Typ.	0.019 Max.
65.536	10 Typ.	0.655 Typ.	1 Max., 0.5 Typ.	0.066 Max.
125.0	10 Typ.	1.250 Typ.	1 Max., 0.5 Typ.	0.125 Max.

Output Programming

Table 7

Tristate	Free Run	Output
0	0	Locked to reference selected (default)
1	X	Hi-Z Tristate condition
0	1	Free run

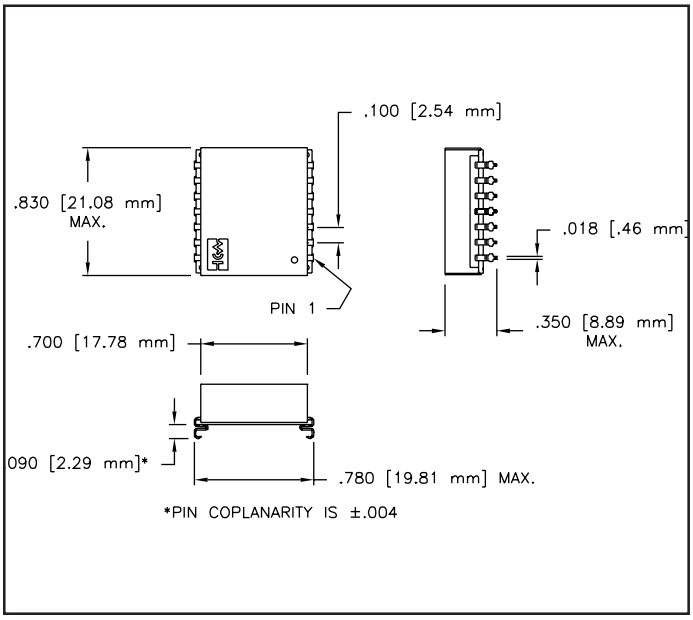
Alarm Status

Table 8

LOL Output	LOR Output	Alarm Output
0	0	No alarm
1	0	Loss-of-Lock
X	1	Loss-of-Reference

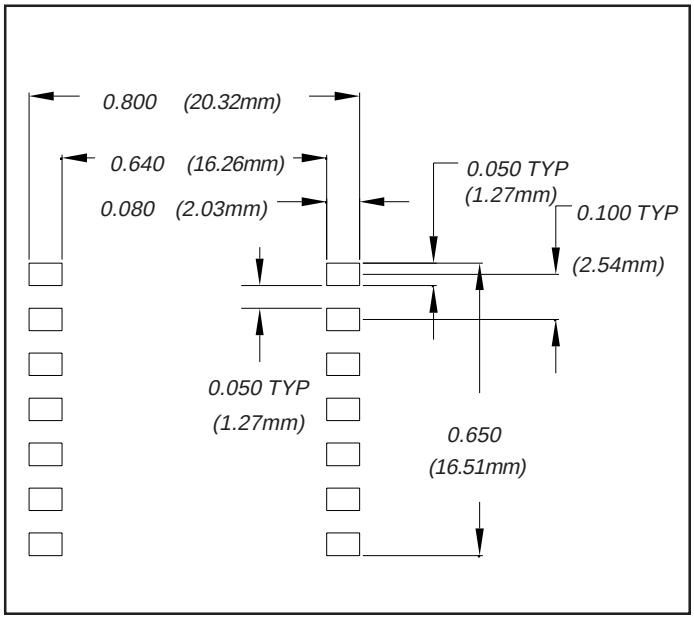
Maximum Package Dimensions

Figure 3



Recommended Footprint Dimensions

Figure 4



Input Reference Selection

Table 9

Input Sel A (Pin #14)	Input Sel B (Pin #13)	Reference Frequency (Pin #8)
0	0	8 kHz (default)
1	0	16 kHz
0	1	32 kHz
1	1	64 kHz

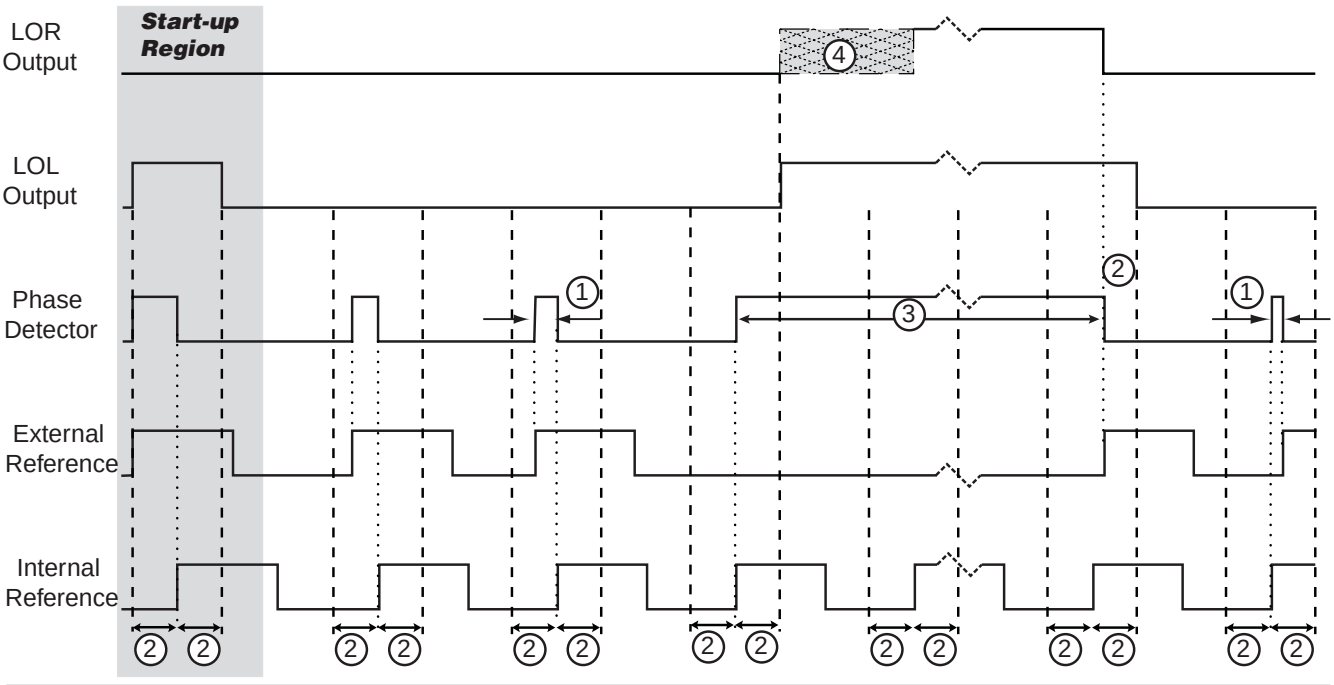
Reference and Output Availability

Table 10

Input Reference (Pin #8)	Oscillator Output (Pin #9)	Reference Output (Pin #1)
8 kHz 16 kHz	19.44 MHz	8 kHz 16 kHz
8 kHz 16 kHz 32 kHz 64 kHz	65.536 MHz	8 kHz 16 kHz 32 kHz 64 kHz
8 kHz	125.0 MHz	8 kHz

Alarm Timing Diagram

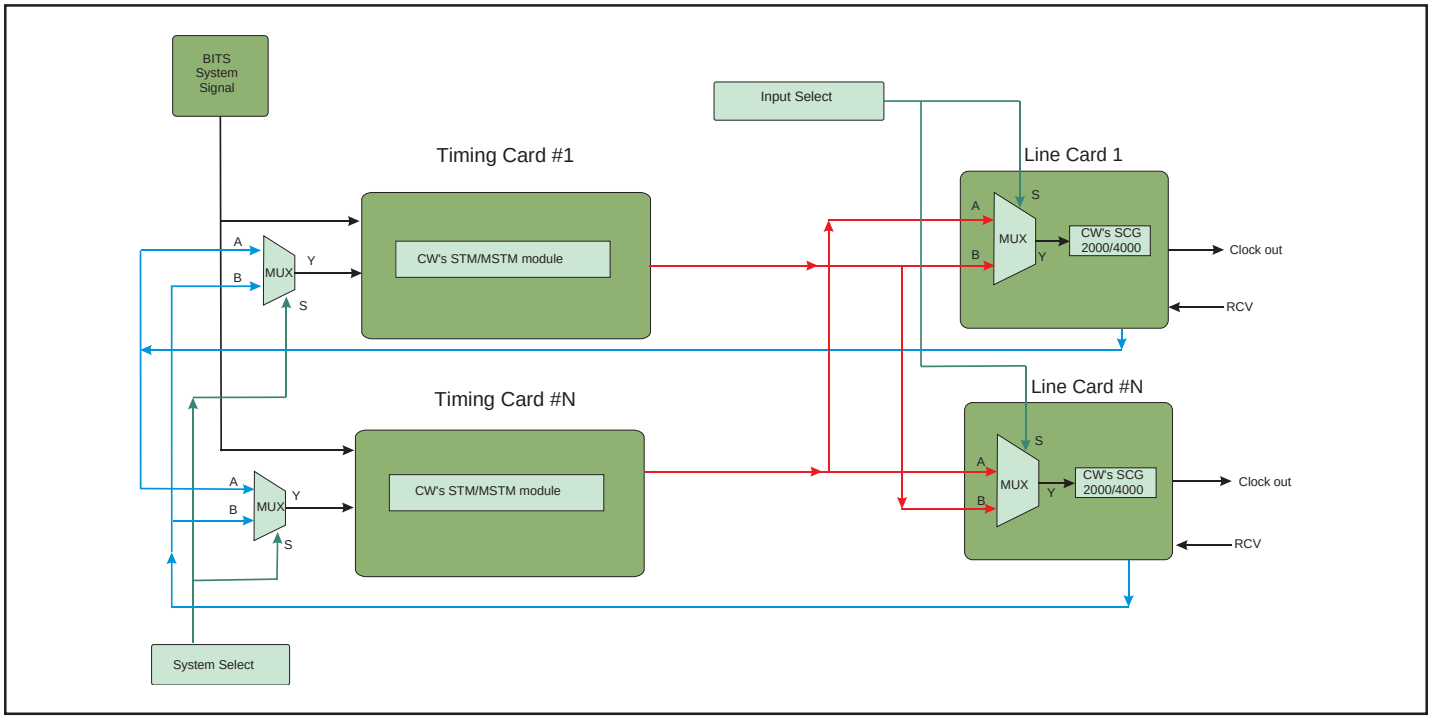
Figure 5



	Reference Input Units
1	< 31.25 µsec
2	31.25 µsec
3	> 31.25 µsec
4	125 µsec wide range
5	Minimum pulse width = 62.5 µsec
Start-up Region	During Start-up, The LOL Alarm will pulse during the first second of operation

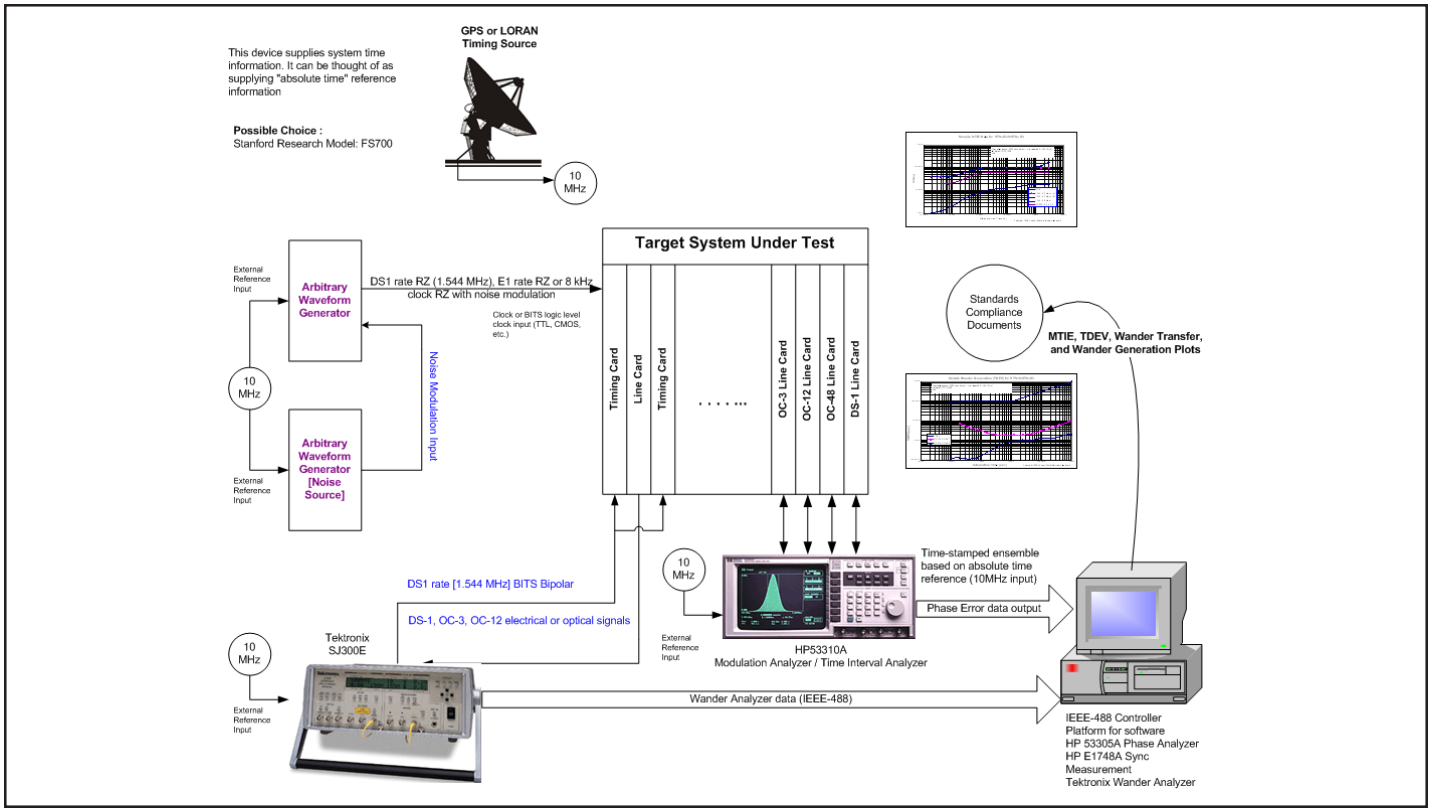
Typical Application

Figure 6



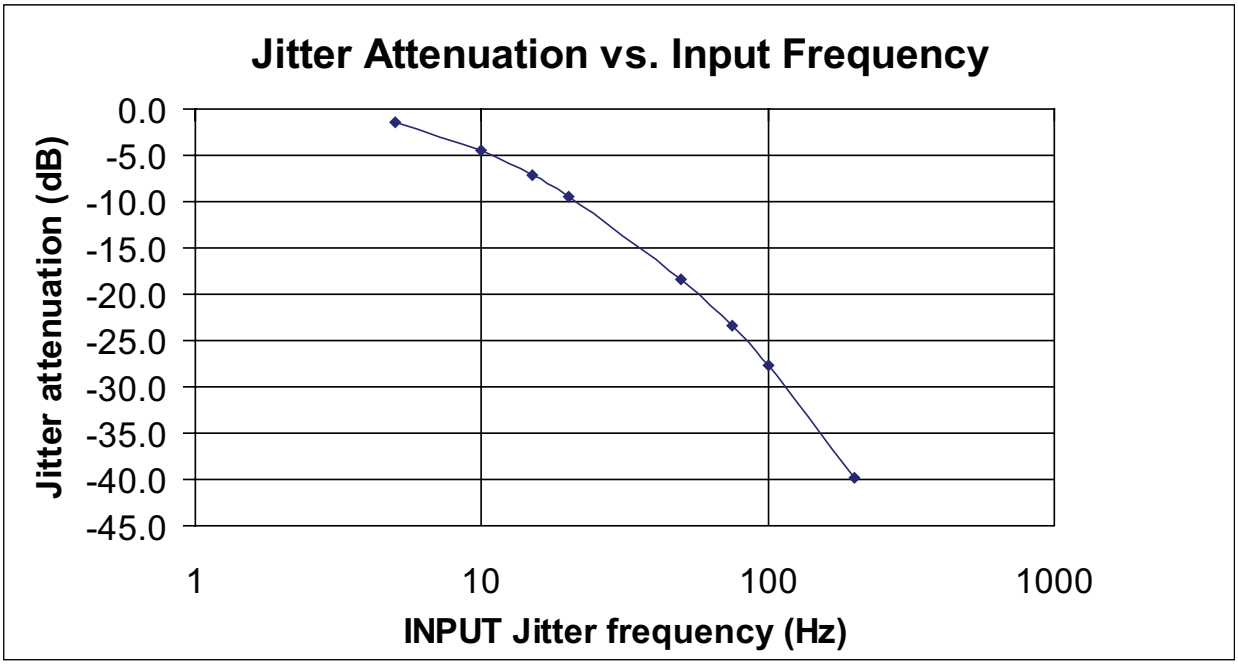
Typical System Test Setup

Figure 7



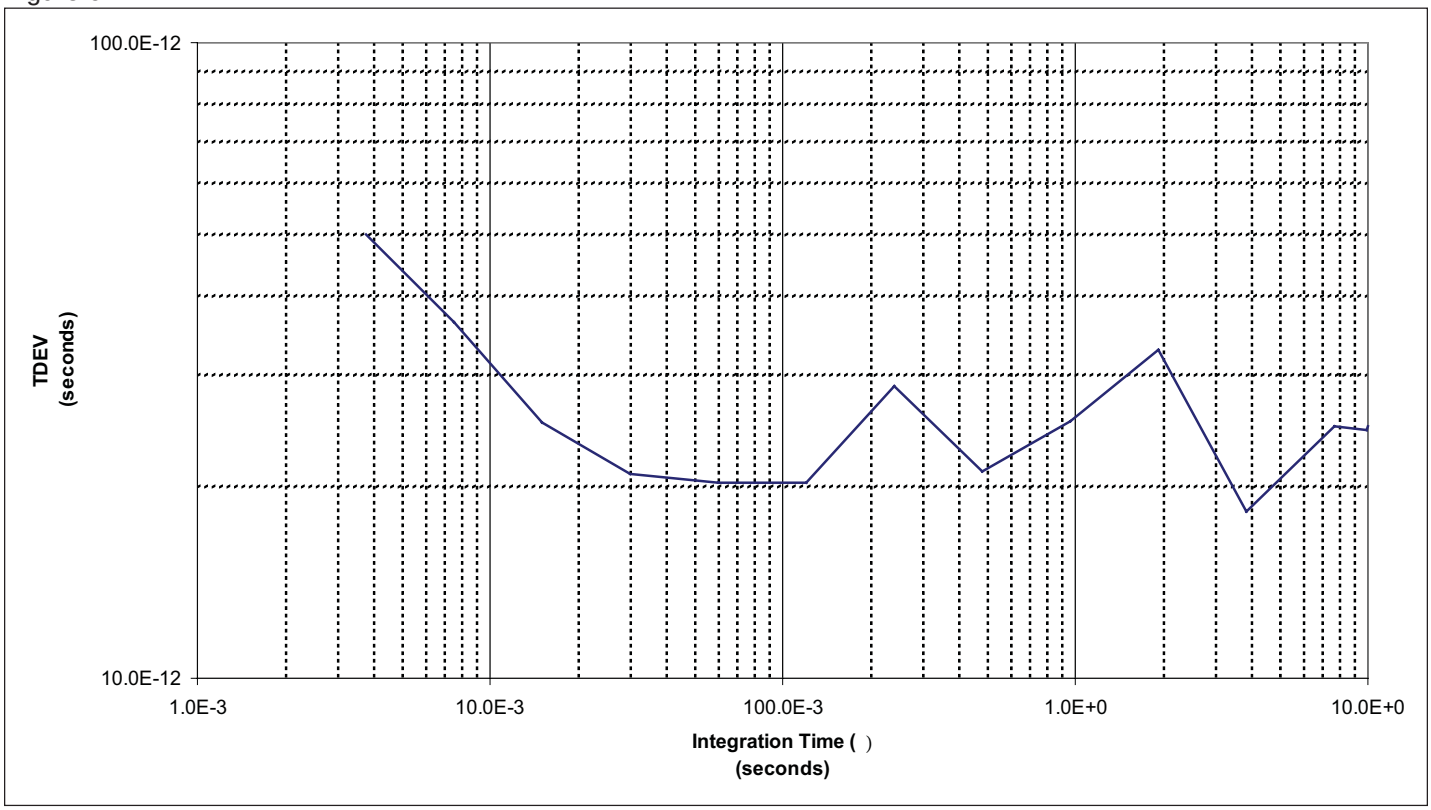
SCG2000iG Typical Jitter Attenuation

Figure 8



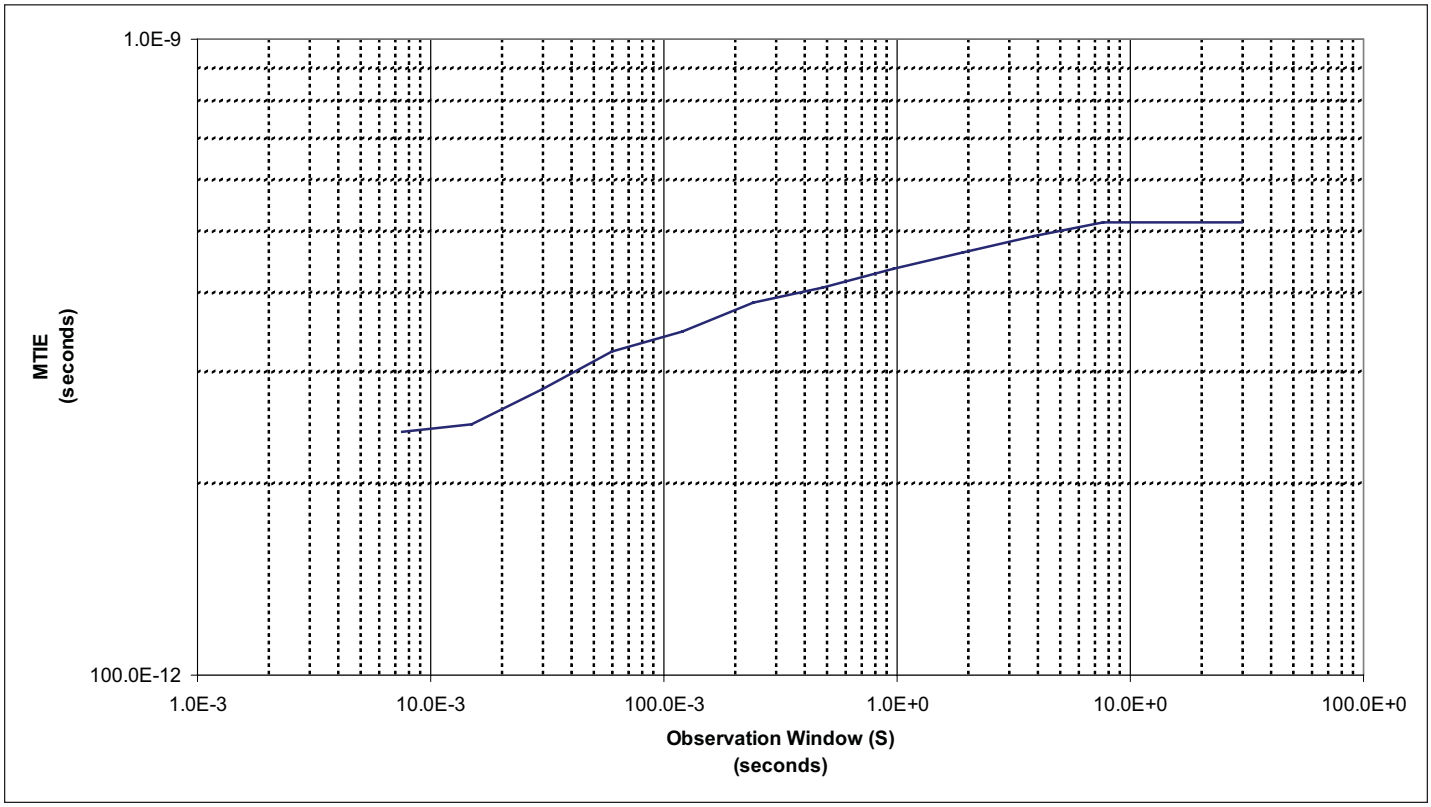
SCG2000iG Typical TDEV

Figure 9



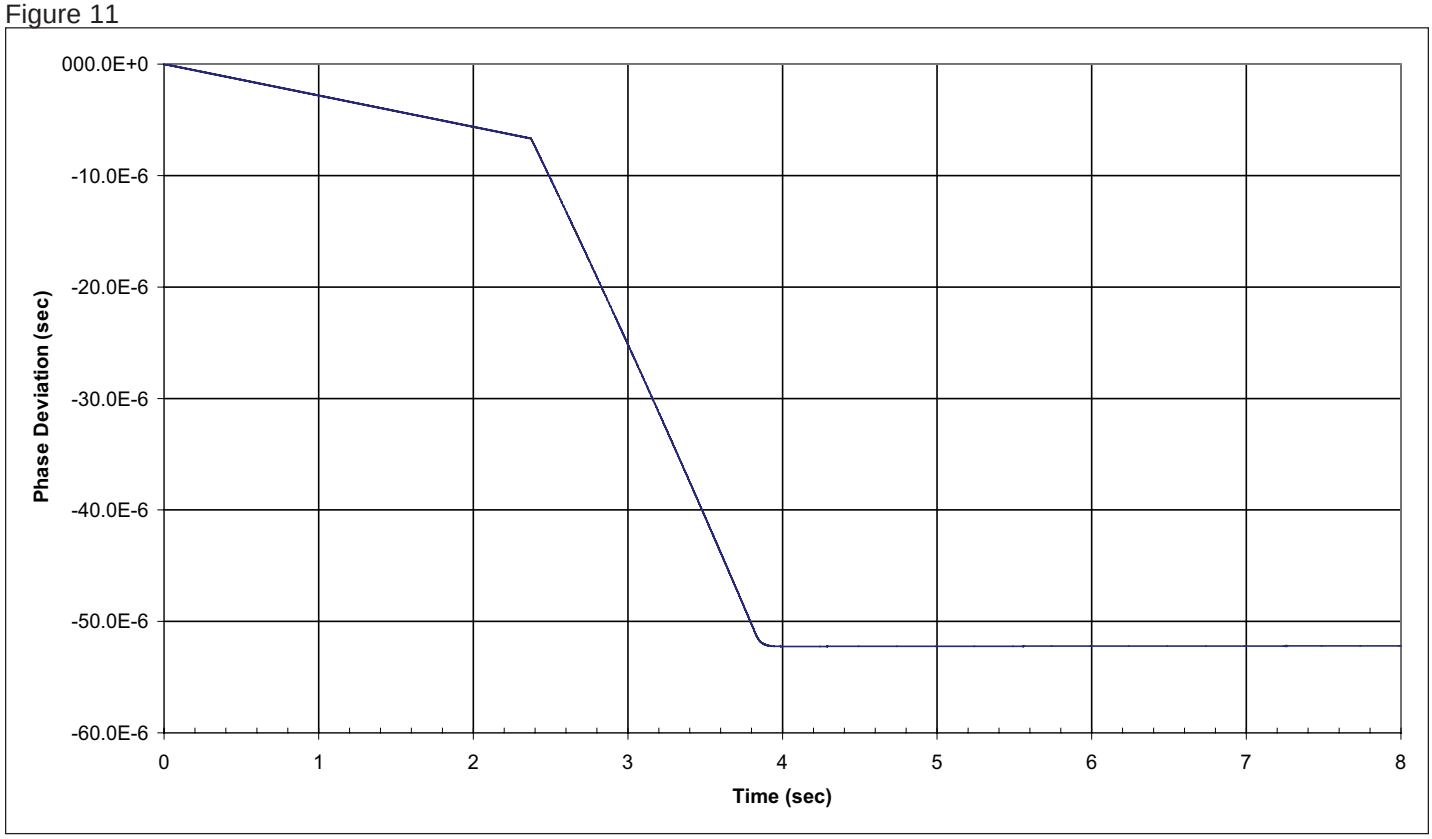
SCG2000iG Typical MTIE

Figure 10



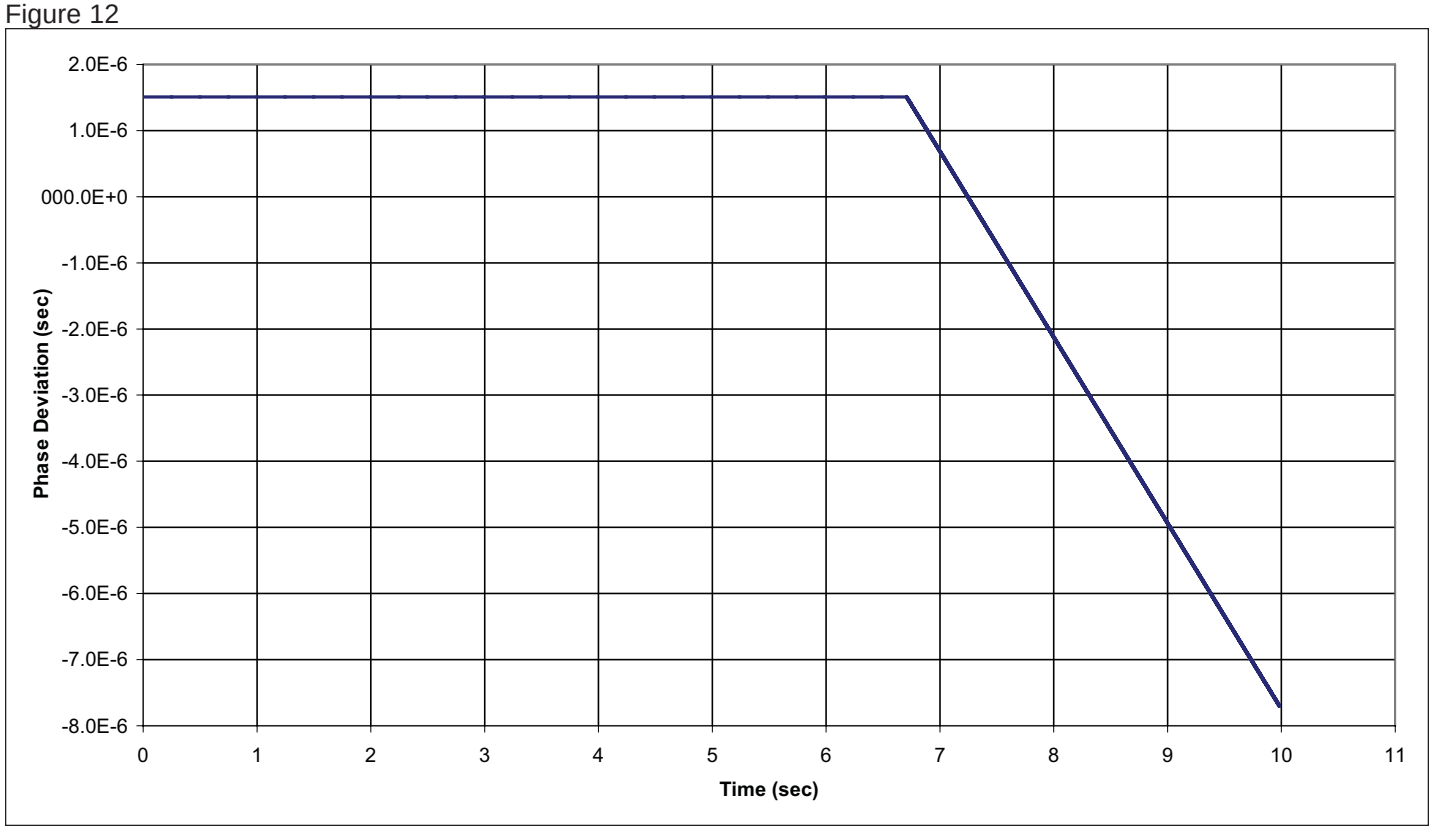
SCG2000iG Typical Switch from Free Run to a new Reference

Figure 11



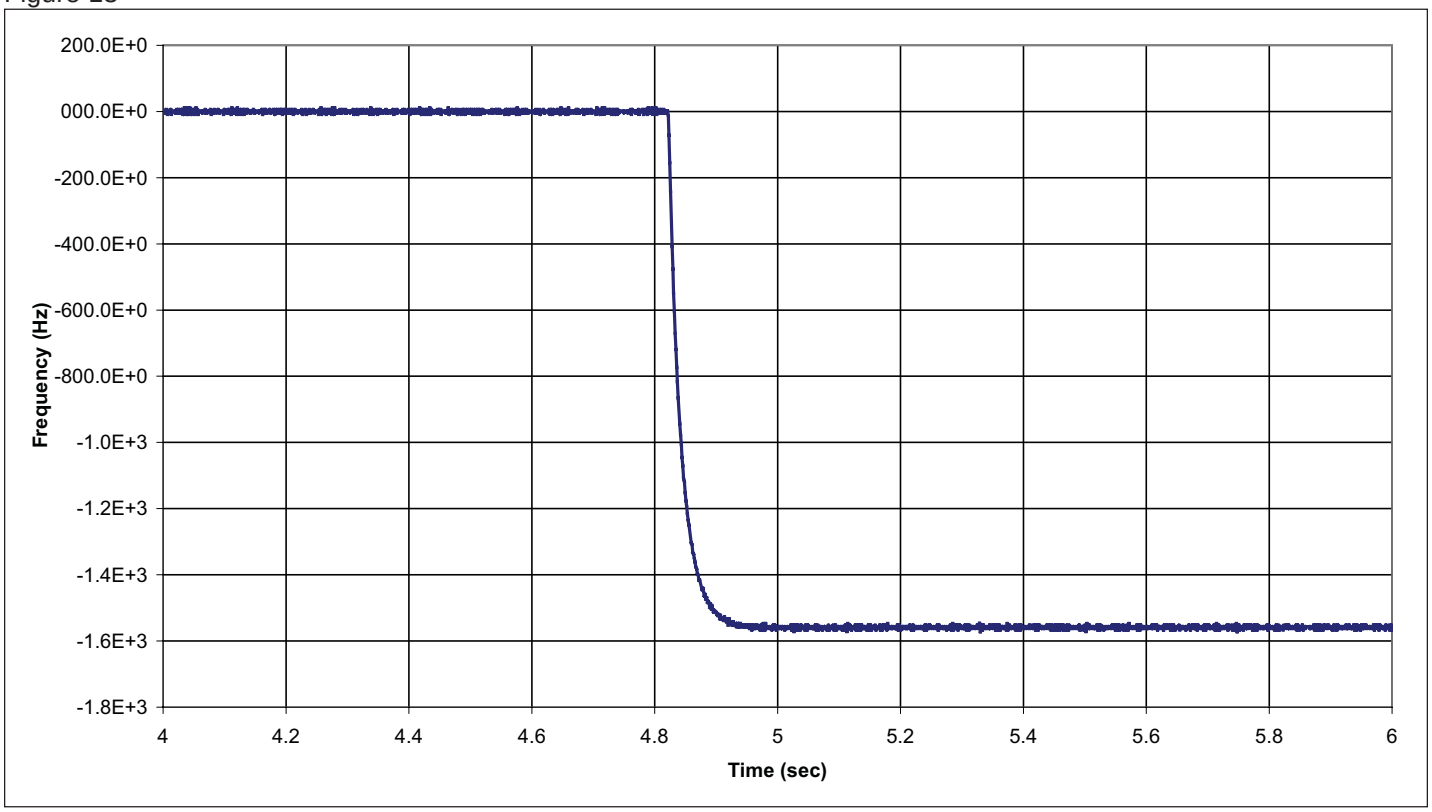
SCG2000iG Typical Switch from a Reference to Free Run

Figure 12



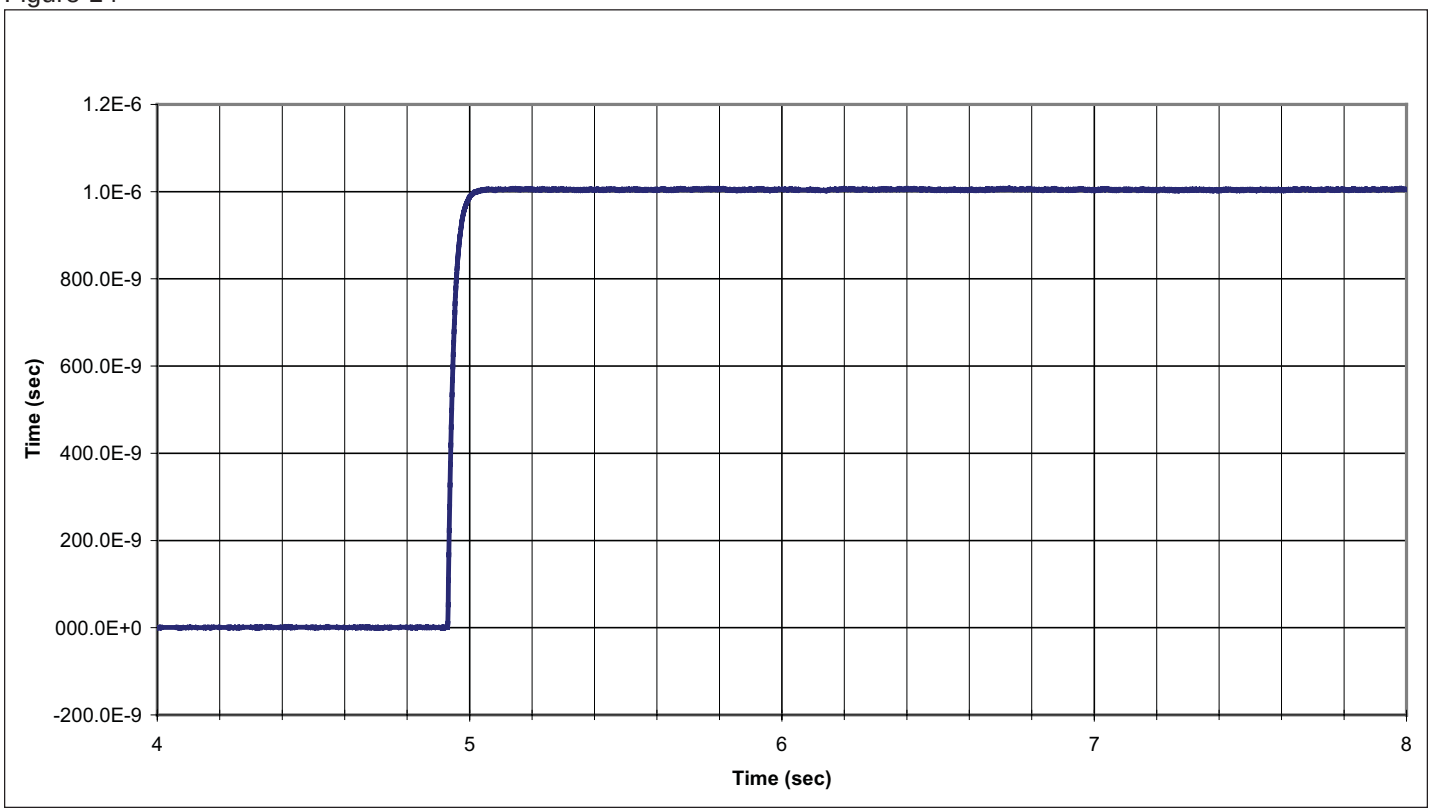
SCG2000iG Typical Step Response due to a -20ppm Freq. Step

Figure 13



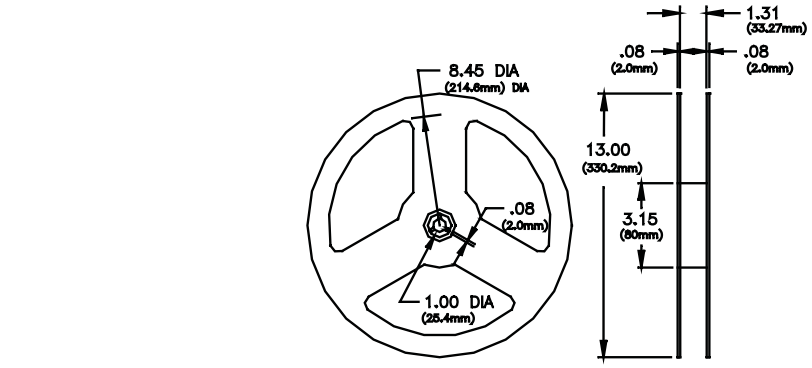
SCG2000iG Typical 1µs Phase Transient Response

Figure 14

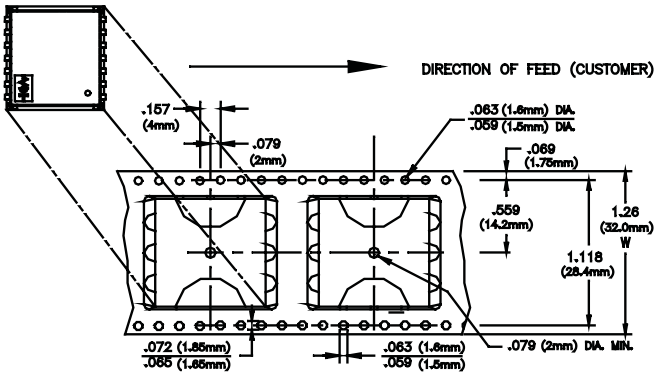


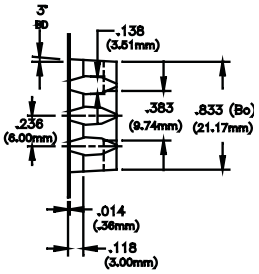
Tape and Reel Dimensions

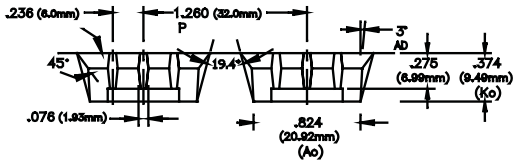
Figure 15



250 PCS/REEL MAXIMUM







POCKET SIZE	
(Ao)	20.92mm (.824")
(Bo)	21.17mm (.833")
(Ko)	9.49mm (.374")
(Ki)	6.99mm (.275")

32mm (1.26") WIDTH
32mm (1.26") PITCH

Ordering Information

SCG{XXXX}-{FFF.FFF}{M}

XXXX equals a specific model (2000iG)
FFF.FFF equals the Oscillator Output frequency (001.544, 002.048, 016.384, 019.44, 020.48, 037.056, 044.736, 049.152, 051.84, 065.536, 077.76, 125.00)
M equals MHZ and is added to all part numbers

Example: To order an SCG2000iG with an Oscillator Output of 19.44 MHz,
Order part number SCG2000iG-019.44M

Please contact Connor-Winfield for other frequencies that may be available.

CONNOR WINFIELD

2111 Comprehensive Drive
Aurora, Illinois 60505
Phone: 630-851-4722
Fax: 630-851-5040
www.conwin.com

Revision	Revision Date	Note
00	7/12/06	Preliminary Release