NB4L6254

2.5V / 3.3V Differential LVPECL 2x2 Clock Switch and Low Skew Fanout Buffer

ON Semiconductor®

http://onsemi.com

Description

The NB4L6254 is a differential 2x2 clock switch and drives precisely aligned clock signals through its LVPECL fanout buffers. It employs a fully differential architecture with bipolar technology, offers superior digital signal characteristics, has very low clock output skew and supports clock frequencies from DC up to 3.0 GHz.

The NB4L6254 is designed for the most demanding, skew critical differential clock distribution systems. Typical applications for the NB4L6254 are clock distribution, switching and data loopback systems of high−performance computer, networking and telecommunication systems, as well as on−board clocking of OC−3, OC−12 and OC−48 communication systems. In addition, the NB4L6254 can be configured as a single 1:6 or dual 1:3 LVPECL fanout buffer.

The NB4L6254 can be operated from a single 3.3 V or 2.5 V power supply.

Features

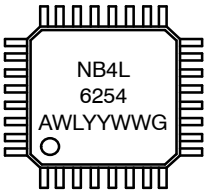
- Maximum Clock Input Frequency, 3 GHz
- Maximum Input Data Rate, 3 Gb/s
- Differential LVPECL Inputs and Outputs
- Low Output Skew: 50 ps Maximum Output−to−Output Skew
- Synchronous Output Enable Eliminating Output Runt Pulse Generation and Metastability
- Operating Range: Single 3.3 V or 2.5 V Supply V_{CC} = 2.375 V to 3.465 V
- LVCMOS Compatible Control Inputs
- Packaged in LQFP−32
- Fully Differential Architecture
- −40°C to 85°C Ambient Operating Temperature
- These are Pb−Free Devices*

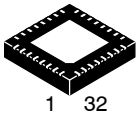
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MARKING DIAGRAMS*

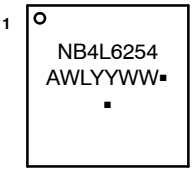


LQFP−32
FA SUFFIX
CASE 873A





QFN32
MN SUFFIX
CASE 488AM



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G or ▪ = Pb−Free Package
(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

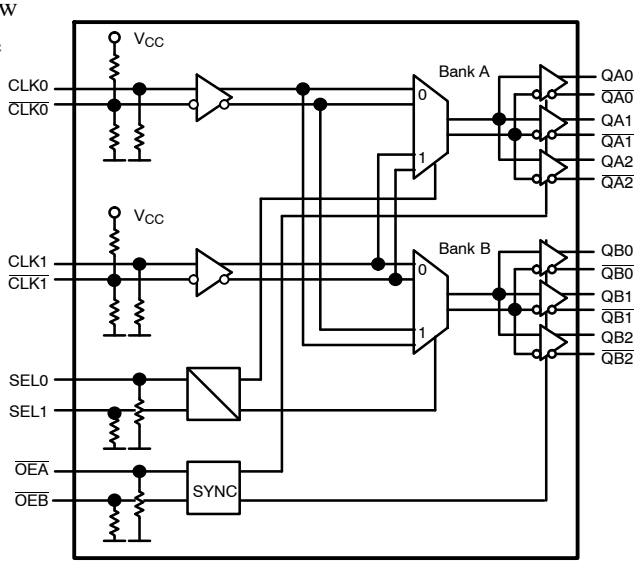


Figure 1. Functional Block Diagram

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

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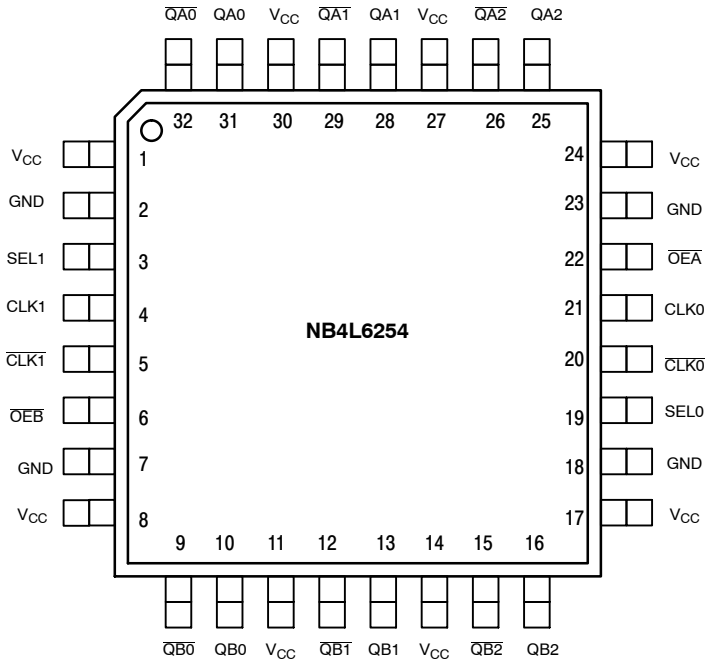


Figure 2. 32−Lead LQFP Pinout (Top View)

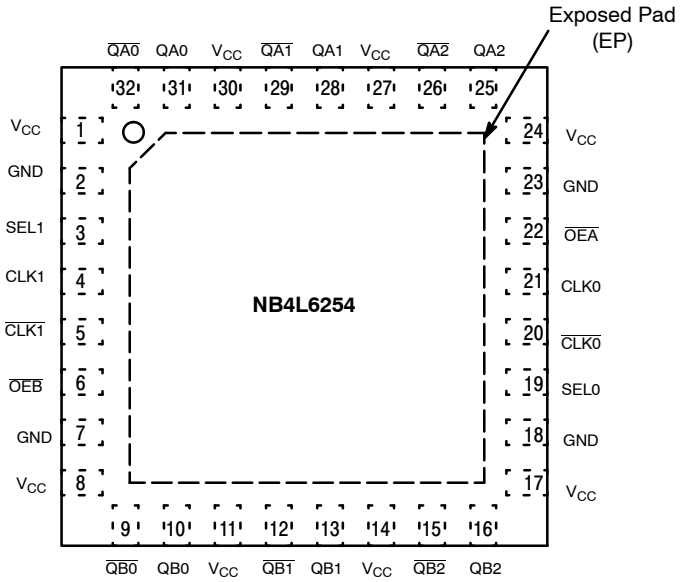


Figure 3. 32−Lead QFN Pinout (Top View)

Table 1. PIN DESCRIPTION

Pin Name	I/O	Description
CLK0, $\overline{CLK0}$	LVPECL Input	Differential reference clock signal input 0.
CLK1, $\overline{CLK1}$	LVPECL Input	Differential reference clock signal input 1.
OEAb, $\overline{OEB}$	LVCMOS Input	Output Enable
SEL0, SEL1	LVCMOS Input	Clock Switch Select
QA[0−2], $\overline{QA[0-2]}$ QB[0−2], $\overline{QB[0-2]}$	LVPECL Output	Differential LVPECL Clock Outputs, (banks A and B) Typically terminated with 50 Ω resistor to V_{CC} − 2.0 V.
GND	Power Supply	Negative Supply Voltage
V_{CC}	Power Supply	Positive supply voltage. All V_{CC} pins must be connected to the positive power supply for correct DC and AC operation.
EP		The exposed pad (EP) on the QFN−32 package bottom is thermally connected to the die for improved heat transfer out of the package. THe exposed pad must be attached to a heat−sinking conduit. The pad is electrically connected to GND.

Table 2. FUNCTION TABLE

Control	Default	0	1
$\overline{OEA}$	0	QA[0−2], $\overline{QA[0-2]}$ are active. Deassertion of $\overline{OEA}$ can be asynchronous to the reference clock without generation of output runt pulses	QA[0−2] = L, $\overline{QA[0-2]}$ = H (outputs disabled). Assertion of $\overline{OE}$ can be asynchronous to the reference clock without generation of output runt pulses
$\overline{OEB}$	0	QB[0−2], $\overline{QB[0-2]}$ are active. Deassertion of $\overline{OEB}$ can be asynchronous to the reference clock without generation of output runt pulses	QB[0−2] = L, $\overline{QB[0-2]}$ = H (outputs disabled). Assertion of $\overline{OE}$ can be asynchronous to the reference clock without generation of output runt pulses
SEL0, SEL1	00	Refer to Table 3	Refer to Table 3

Table 3. CLOCK SELECT CONTROL

SEL0	SEL1	CLK0 Routed To	CLK1 Routed to	Application Mode
0	0	QA[0:2] and QB[0:2]	–	1:6 Fanout of CLK0
0	1	–	QA[0:2] and QB[0:2]	1:6 Fanout of CLK1
1	0	QA[0:2]	QB[0:2]	Dual 1:3 Buffer
1	1	QB[0:2]	QA[0:2]	Dual 1:3 Buffer (Crossed)

Table 4. ATTRIBUTES

Characteristics		Value
Internal Input Pullup Resistor		37.5 kΩ
Internal Input Pulldown Resistor		75 kΩ
ESD Protection	Human Body Model Machine Model	> 2000 V > 200 V
Latchup Immunity		>200 mA
Cin, inputs		4.0 pF (TYP)
Moisture Sensitivity (Note 1)	LQFP−32 QFN32	Level 2 Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		336
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

Table 5. MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition	Condition	Rating	Unit
V_{CC}	Positive Power Supply			$-0.3 \le V_{CC} \le 3.6$	V
V_{IN}	DC Input Voltage			$-0.3 \le V_{IN} \le V_{CC} + 0.3$	V
V_{OUT}	DC Output Voltage			$-0.3 \le V_{OUT} \le V_{CC} + 0.3$	V
I_{IN}	DC Input Current			±20	mA
I_{out}	LVPECL DC Output Current	Continuous Surge		±50 100	mA mA
T_A	Operating Temperature Range	LQFP−32		−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient) (Note 3)	0 lfpm 500 lfpm	LQFP−32 LQFP−32	80 55	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	2S2P (Note 3)	LQFP−32	12 to 17	°C/W
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	QFN−32 QFN−32	31 27	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	2S2P	QFN−32	12	°C/W
T_{sol}	Wave Solder Pb−Free			265	°C
V_{TT}	Output Termination Voltage			V_{CC} − 2.0, TYP	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. Maximum Ratings are those values beyond which device damage may occur.
3. JEDEC standard multilayer board − 2S2P (2 signal, 2 power); MIL−SPEC 883E Method 1012.1.

Table 6. DC CHARACTERISTICS V_{CC} = 2.375 V to 3.465 V, GND = 0 V, T_A = −40°C to +85°C

Symbol	Characteristic	Min	Typ	Max	Unit
POWER SUPPLY CURRENT					
I_{GND}	Power Supply Current (Outputs Open)		60	85	mA
LVPECL CLOCK OUTPUTS					
V_{OH}	LVPECL Output HIGH Voltage (Notes 4, 5) V_{CC} = 3.3 V V_{CC} = 2.5 V	V_{CC} − 1145 2155 1355	V_{CC} − 1020 2280 1480	V_{CC} − 895 2405 1605	mV
V_{OL}	LVPECL Output LOW Voltage (Notes 4, 5) V_{CC} = 3.3 V V_{CC} = 2.5 V	V_{CC} − 1945 1355 555	V_{CC} − 1770 1530 730	V_{CC} − 1600 1700 900	mV
CLOCK INPUTS					
V_{PP}	Dynamic Differential Input Voltage (Clock Inputs)	0.1		1.3	V
V_{CMR}	Differential Cross−point Voltage (Clock Inputs)	1.0		V_{CC} − 0.3	V
LVCMOS CONTROL INPUTS					
V_{IH}	Output HIGH Voltage (LVTTL/LVCMOS)	2.0			V
V_{IL}	Output LOW Voltage (LVTTL/LVCMOS)			0.8	V
I_{IH}	Input Current V_{IN} = V_{CC} or V_{IN} = GND	−100		+100	μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. LVPECL Outputs loaded with 50 Ω termination resistors to V_{TT} = V_{CC} − 2.0 V for proper operation.
5. LVPECL Output parameters vary 1:1 with V_{CC}.

Table 7. AC CHARACTERISTICS V_{CC} = 2.375 V to 3.465 V, GND = 0 V, T_A = −40°C to +85°C (Note 6)

Symbol	Characteristic	Min	Typ	Max	Unit
V_{INPP}	Differential Input Voltage (Peak−to−Peak)	0.3		1.3	V
V_{CMR}	Differential Input Cross−Point Voltage (Clock Inputs)	1.2		V_{CC} − 0.3	V
f_{IN}	Clock Input Frequency	0		3.0	GHz
V_{OUTPP}	Differential Output Output Voltage Amplitude (Peak−to−Peak) (Note 7) f_O < 1.1 GHz f_O < 2.5 GHz f_O < 3.0 GHz	 0.45 0.35 0.2	 0.70 0.55 0.35		V
f_{CLKOUT}	Output Clock Frequency Range	0		3.0	GHz
t_{pd}	Propagation Delay CLKx to Qx (Differential Configuration)	360	485	610	ps
t_{skew}	Within Device Output−to−Output Skew (Differential Configuration) Device−to−Device Skew Output Pulse Skew (Duty Cycle Skew) (Note 8)		25 30 10	50 250 60	ps
DCO	Output CLOCK Duty Cycle (DC Ref = 50%) t_{REF} <100 MHz (Note 9) t_{REF} < 800 MHz	49.4 45.2		50.6 54.8	%
t_{JIT}	CLOCK Random Jitter (RMS) (SEL0 ≠ SEL1) (Note 10)		0.3	0.8	ps
t_r, t_f	Output Rise/Fall Times (Note 11) CLKx / $\overline{CLKx}$	50	130	300	ps
t_{PDL}	Output Disable Time, T = CLK period	2.5 T + t_{PD}		3.5 T + t_{PD}	ns
tPLD	Output Enable Time, T = CLK period	3 T + t_{PD}		4 T + t_{PD}	ns

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

6. LVPECL Outputs loaded with 50 Ω to V_{CC} − 2.0V.
7. V_{OUTPP} MIN = 0.1 V @ +85°C, f_O < 3.0 GHz.
8. Output Pulse Skew is the absolute difference of the propagation delay times: $|t_{PLH} - t_{PHL}|$
9. $DCO_{MIN/MAX}$ = 43.2%/59.2% @ +85°C.
10. t_{JITMAX} = 1.6 ps @ 85°C, 3.0 V
11. Measured 20% to 80%

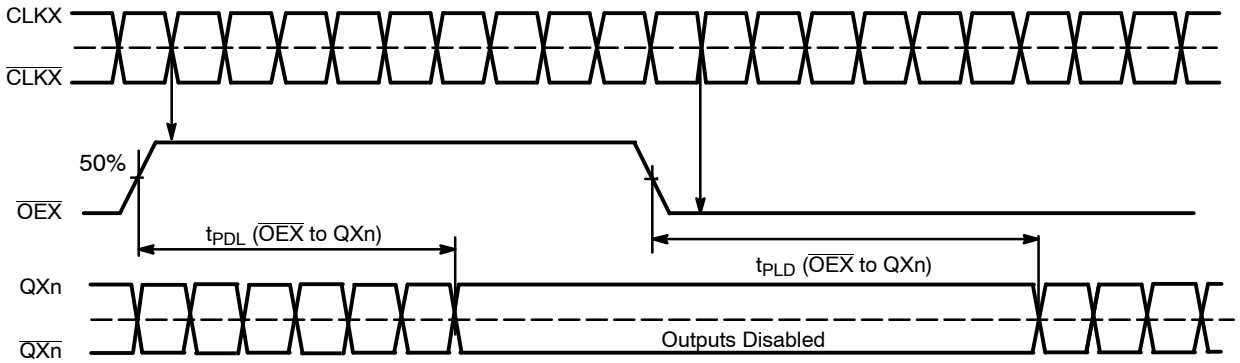


Figure 4. Output Disable / Enable Timing

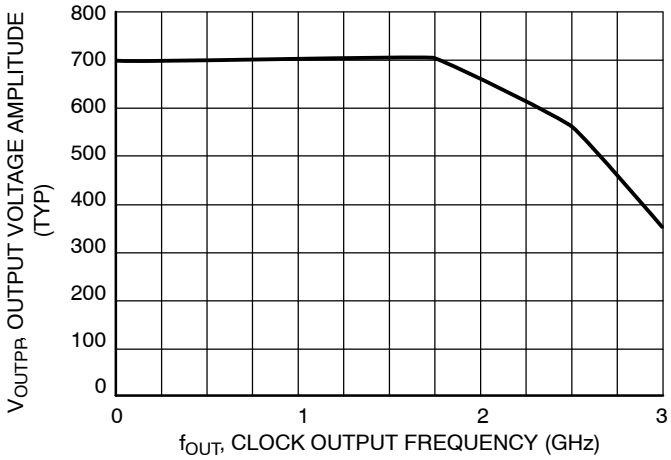


Figure 5. Output Voltage Amplitude (V_{OUTPP}) versus Clock Output Frequency at Ambient Temperature (Typical)

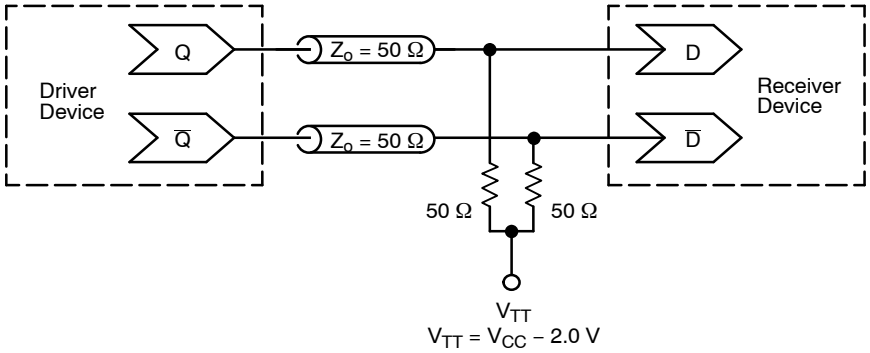


Figure 6. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D – Termination of ECL Logic Devices.)

Example Configurations

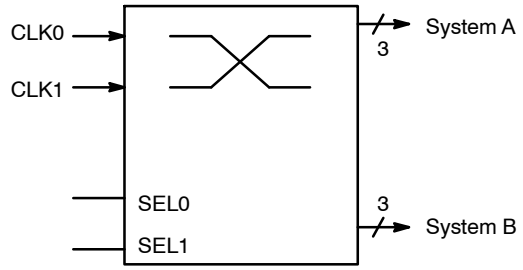


Figure 7. 2 x 2 Clock Switch

SEL0	SEL1	Switch Configuration
0	0	CLK0 Clocks System A and System B
0	1	CLK1 Clocks System A and System B
1	0	CLK0 Clocks System A and CLK1 Clocks System B
1	1	CLK1 Clocks System B and CLK1 Clocks System A

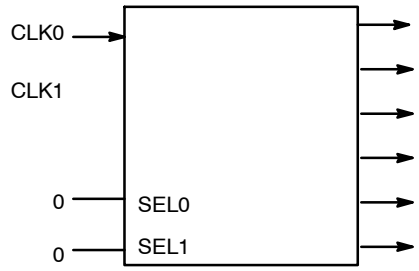


Figure 8. 1:6 Clock Fanout Buffer

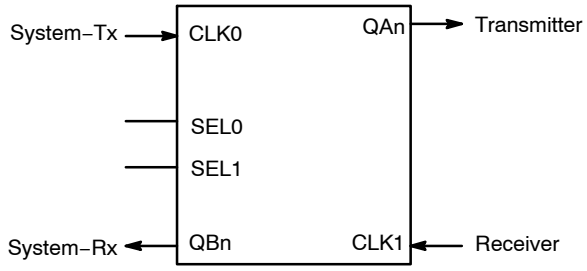


Figure 9. Loopback Device

SEL0	SEL1	Switch Configuration
0	0	System Loopback
0	1	Line Loopback
1	0	Transmit/Receive Operation
1	1	System and Line Loopback

APPLICATIONS INFORMATION

Maintaining Lowest Device Skew

The NB4L6254 guarantees low output−output bank skew at 50 ps and a part−to−part skew of 250 ps. To ensure low skew clock signals in the application, both outputs of any differential output pair need to be terminated identically, even if only one output is used. When fewer than all nine output pairs are used, identical termination of all output pairs within the output bank is recommended. If an entire output bank is not used, it is recommended to leave all of these outputs open and unterminated. This will reduce the device power consumption while maintaining minimum output skew.

Power Supply Bypassing

The NB4L6254 is a mixed analog/digital product. The differential architecture of the NB4L6254 supports low noise signal operation at high frequencies. In order to maintain its superior signal quality all V_{CC} pins should be bypassed by high−frequency ceramic capacitors connected to GND. If the spectral frequencies of the internally generated switching noise on the supply pins cross the series resonant port of an individual bypass capacitor, its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the noise bandwidth.

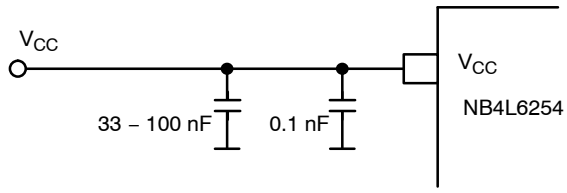


Figure 10. V_{CC} Power Supply Bypass

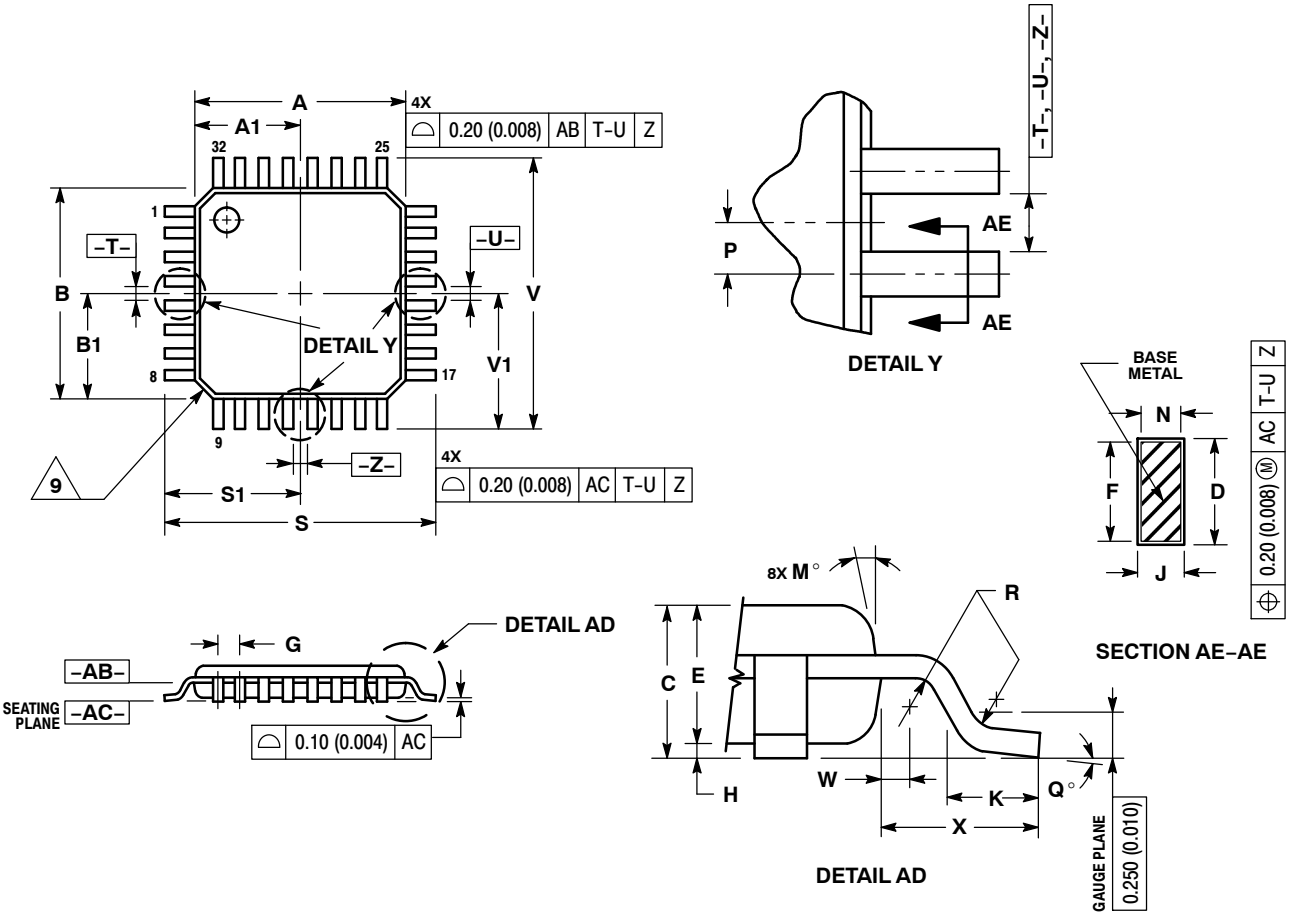
ORDERING INFORMATION

Device	Package	Shipping†
NB4L6254FAG	LQFP−32 (Pb−Free)	250 Units / Tray
NB4L6254FAR2G	LQFP−32 (Pb−Free)	2000 / Tape & Reel
NB4L6254MNG	QFN32 (Pb−Free)	74 Units / Rail
NB4L6254MNR4G	QFN32 (Pb−Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

32 LEAD LQFP
CASE 873A–02
ISSUE C

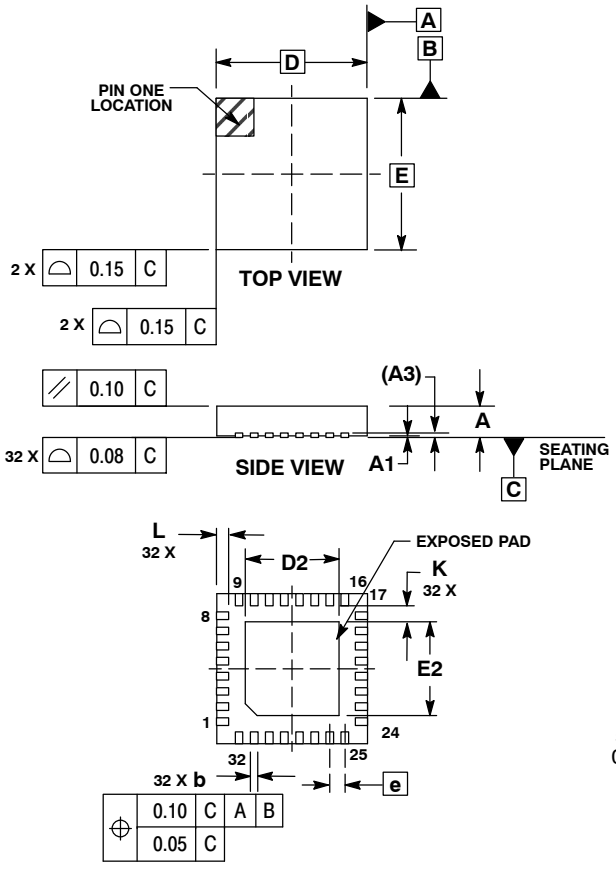


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.450	0.750	0.018	0.030
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

PACKAGE DIMENSIONS

QFN32 5*5*1 0.5 P
CASE 488AM−01
ISSUE O

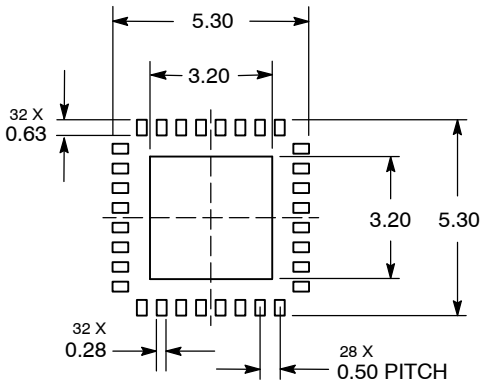


BOTTOM VIEW

NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.800	0.900	1.000
A1	0.000	0.025	0.050
A3		0.200 REF	
b	0.180	0.250	0.300
D		5.00 BSC	
D2	2.950	3.100	3.250
E		5.00 BSC	
E2	2.950	3.100	3.250
e		0.500 BSC	
K	0.200	---	---
L	0.300	0.400	0.500

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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