

TDL2A

Issue 3, 02 August 2012

UHF Multi Channel Transparent Data Link

The TDL2A is a 9600baud half-duplex multi channel OEM radio modem in BiM2 footprint, operating on European 433MHz ISM band. TDL2A acts as a transparent serial cable to attached host. TDL2A is an intermediate level OEM radio modem which is in between a raw FM radio module like BiM2 and a sophisticated OEM radio modem like SPM2. It takes care of preamble, synchronisation, bit balancing and error checking along with automatic noise squelching.



Figure 1: TDL2A-433-9 radio modem

The TDL2A provides a half duplex link. Provided no two devices attempt to transmit simultaneously no further restrictions on data transmission need be made, as all transmit timing, valid data identification and datastream buffering is conducted by the unit. Synchronisation and framing words in the packet prevent the receiver outputting garbage in the absence of wanted RF signal or presence of interference. For multiple radio systems (polled networks) a TDL2A can be set to 1 of 8 unique addresses. As well as having unique addresses, the TDL2A allows operation on one of 5 pre-set frequencies in the 433MHz band. These frequencies are non-overlapping and simultaneous operation of TDL2As in the same area on different channels will be possible.

Features

- Conforms to EN 300 220-3 and EN 301 489-3
- High quality, stable crystal reference; Low noise synthesiser / VCO
- SAW front-end filter
- Multi-stage ceramic IF filtering
- Single conversion superhet
- Serial modem baud rate at 9600bps (half-duplex)
- Carries ASCII and RTU MODBUS messages
- Addressable point-to-point
- 5 serial select wideband channels
- Available as TDL2T transmitter and TDL2R receiver for one way communication

Applications

- PDAs, organisers & laptops
- Handheld / portable terminals
- EPOS equipment, barcode scanners
- In-building environmental monitoring and control
- Remote data acquisition system, data logging
- Fleet management, vehicle data acquisition

Technical Summary

- Operating frequency: 433.925MHz (default)
- Modulation: 16kbps bi-phase FSK
- Supply: 5V at 28mA transmit, 22mA receive/idle
- Transmit power: +10dBm (10mW)
- Receiver sensitivity: -107dBm (for 1% BER)
- 32 byte data buffer
- Adjacent channel rejection: 65db @ ± 320 kHz
- Receiver Blocking: 84dB

Evaluation platforms: TDL2A Evaluation Kit

The diagram illustrates the internal architecture of the TDL2A 433-9, a dual-band (433 MHz and 20.48 MHz) receiver and transmitter. The central component is the CPU, which manages the system's operation.

Power and Control: The circuit is powered by a +5V IN supply, regulated to 4.0V by a VOLTAGE REG. A GND connection is also shown. The CPU is connected to a TEST pin, DATA IN, DATA OUT, and RX BUSY signals.

Receiver Path (Left Side): RF IN (433 MHz) enters through an RF SWITCH and an LC MATCH network. It passes through an LC LPF and a PA (Power Amplifier) before reaching a BUFFER. The signal then goes through a SAW BPF (Surface Acoustic Wave Band Pass Filter) and an LNA (Low Noise Amplifier). The output of the LNA is mixed with a 433 MHz reference signal in a mixer (represented by a circle with an 'X'). The resulting signal passes through another LC MATCH network and an LC LPF before entering the TK14570 (a variable frequency divider/multiplier). The output of the TK14570 is mixed with a 20.48 MHz reference signal in another mixer (represented by a circle with an 'X'). The output of this mixer passes through a 10.7 MHz BPF and a Ceramic Discriminator to produce the RX Data signal.

Transmitter Path (Right Side): The TX Mod signal is fed into the AF LPF (RC) and the AF LPF (RC). The output of the AF LPF (RC) is mixed with a 20.48 MHz reference signal in a mixer (represented by a circle with an 'X'). The output of this mixer passes through a 10.7 MHz BPF and a Ceramic Discriminator to produce the TX Data signal.

Synthesizer (Center): The SYNTHESIZER block contains a VCO (Voltage Controlled Oscillator) and a Phase Detector. The VCO is connected to a 433 / 433 MHz reference signal. The Phase Detector is connected to a 20.48 MHz reference signal. The SYNTHESIZER also includes a Chargepump, a Divider (N), and a Divider (R). The output of the SYNTHESIZER is connected to the CPU via a CONTROL signal.

Other Components: A UVC0 (Ultra-Violet Counter) is connected to the CPU and the SYNTHESIZER. A BUFFER is connected to the output of the TX Mod signal.

Figure 2: TDL2A block diagram

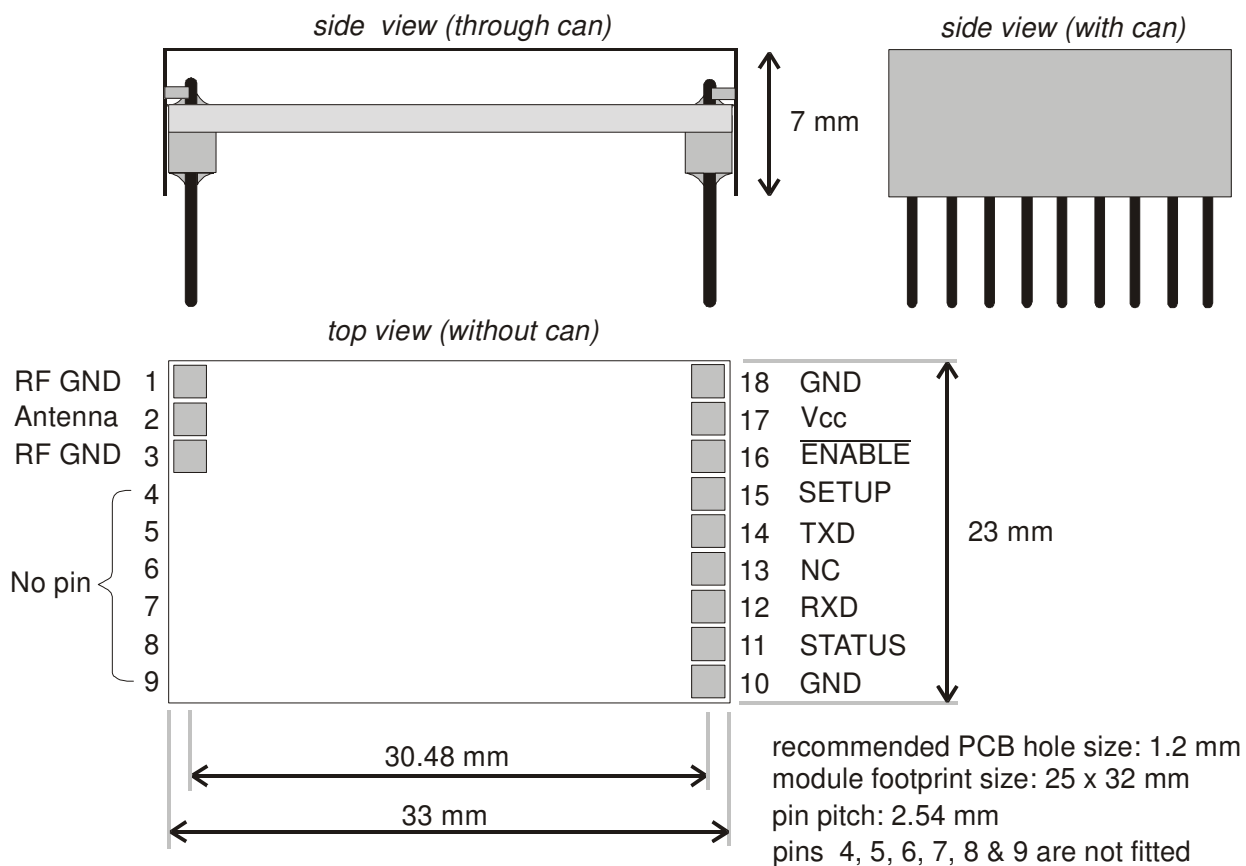


Figure 3: TDL2A footprint (top view)

Pin description

Pin	Name	Function
18	GND	Ground
17	Vcc	5V (regulated power supply)
16	ENABLE	Enable or DTR (5V CMOS logic level input)
15	SETUP	Test/Setup mode selection
14	TXD	Transmit Data (Inverted RS232 at 5V CMOS logic level)
13	NC	No Pin
12	RXD	Receive Data (Inverted RS232 at 5V CMOS logic level)
11	STATUS	Busy or CTS (5V CMOS logic level output)
10	GND	Ground

RF GND *pin 1 & 3*

RF Ground pin, internally connected to the module screen and pin 8, 9, 10 and 18 (0V). This pin should be connected to the RF return path (e.g. co-axial cable braid, main PCB ground plane, etc).

RF *pin 2*

50Ω RF input/output from the antenna, it is DC isolated internally. (see antenna section for details).

GND *pin 8, 9, 10 and 18*

Supply ground connection to ground plane and can.

VCC *pin 17*

5V voltage regulator should be used to have a clean 5V supply to the module. A 4V regulator is used inside for radio circuitry.

ENABLE *pin 16*

Active low Enable pin. It has a 47kΩ pull-ups to Vcc. It should be pulled Low to enable the module. This can also be connected to DTR pin (only if it is asserted by the host) of an RS232 serial port via a MAX232 or equivalent RS232-CMOS level converter.

SETUP *in 15*

Active low input to enter configuration or diagnostic test mode. It has a 47kΩ pull-ups to Vcc

TXD *pin 14*

This is inverted RS232 data input at 5V CMOS logic level. It can be directly interfaced to data output of a UART in a microcontroller or to a TXD pin of an RS232 serial port via a MAX232 or equivalent RS232-CMOS level converter. TXD does not have an internal pull-up. If TDL2A is used in Receive only mode, TXD should be tied to Vcc.

NC *pin 13*

There is no pin in this position.

RXD *pin 12*

This is inverted RS232 data output at 5V CMOS logic level. It can be directly interfaced to data input of a UART in a microcontroller or to a RXD pin of an RS232 serial port via a MAX232 or equivalent RS232-CMOS level converter.

STATUS *pin 11*

This pin goes high when valid data is present in the receive buffer. It can be used to trigger an interrupt in the host to download received data packet instead of waiting for it. It can be also be used as a primitive CTS signal. It is inverted RS232 data output at 5V CMOS logic level. It can be directly interfaced to an input of a microcontroller as a Data Detect (DD) or to CTS, DSR, DCD pins of an RS232 serial port via a MAX232 or equivalent RS232-CMOS level converter. This is can only be used to prevent host from uploading any data before downloading already received data, because transmission is prioritised over reception and any data to be transmitted will erase received data which is in the common buffer.

Serial interface – modem operation

To connect to a true RS232 device, inverting RS232-CMOS level shifters must be used. Maxim MAX232 or equivalent are ideal, but simple NPN transistor switches with pull-ups often suffice. With typical microcontrollers and UARTs, direct connection is possible.

The Radio / data stream interface

A 32 byte software FIFO is implemented in both the transmit and receive sub-routine. At the transmitting end this is used to allow for the transmitter start up time (about 3mS), while on receiving end it buffers arriving packets to the constant output data rate. All timing and data formatting tasks are handled by the internal firmware. The user need not worry about keying the transmitter before sending data as the link is entirely transparent.

For transmission across the radio link data is formatted into packets, each comprising 3 bytes of data and a sync code. If less than 3 bytes are in the transmit end FIFO then a packet is still sent, but idle codes replaces the unused bytes. When the transmit end FIFO is completely emptied, then the transmitter is keyed off.

Operation: Radio interface.

Raw data is not fed to the radios. A coding operation in the transmit sub-routine, and decoding in the receiver, isolate the AC coupled, potentially noisy baseband radio environment from the datastream.

The radio link is fed a continuous tone by the modem. As in bi-phase codes, information is coded by varying the duration consecutive half-cycles of this tone. In our case half cycles of 62.5us and 31.25us are used. In idle (or 'preamble') state, a sequence of the longer cycles is sent (resembling an 8KHz tone).

A packet comprises the Synchronising (or address) part, followed by the Data part, made up of twelve Groups (of four half cycles duration). Each Group encodes 2 data bits, so one byte is encoded by 4 Groups.

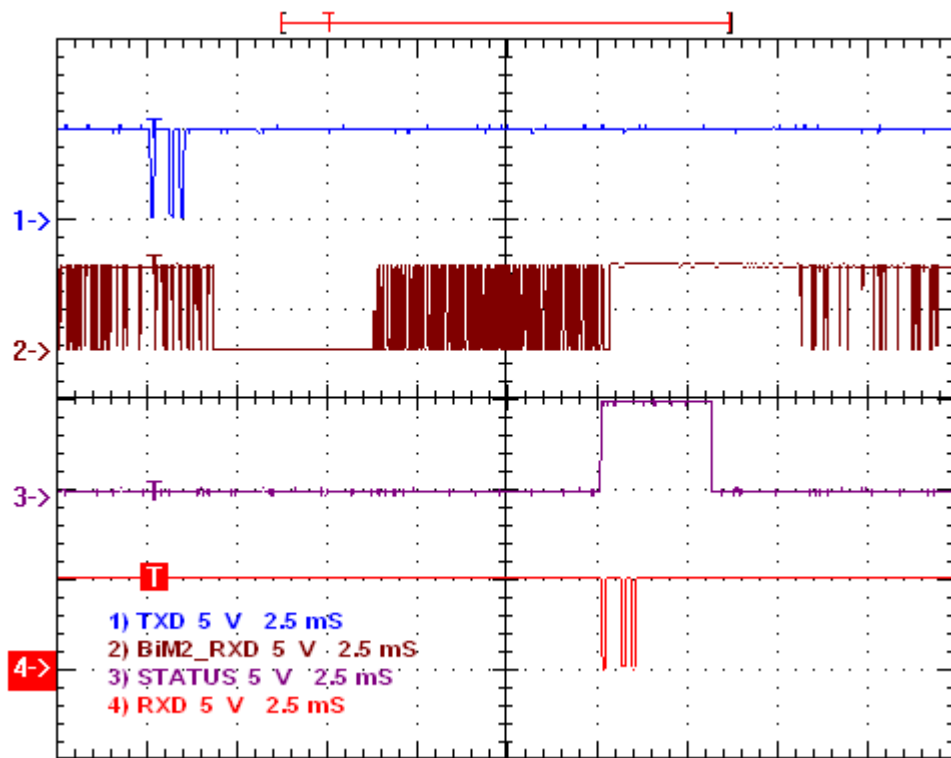


Figure 4: TDL2A transmitting and receiving

The oscilloscope screen capture shows a single byte being transmitted by TDL2A. A BiM2-433-64 transceiver is used to capture the transmitted data. The character appears on the serial data output (RXD) pin of the other TDL2A after about 12.5ms. Busy (STATUS) pin is momentarily set high to indicate the presence of a valid data in the receive buffer of the TDL2A.

It can be clearly seen that unlike raw radio modules, TDL2A does not output any noise when there is not any transmission. Data fed into the TXD input of a TDL2A appears at the RXD output of another TDL2A within radio range in the original form it was fed.

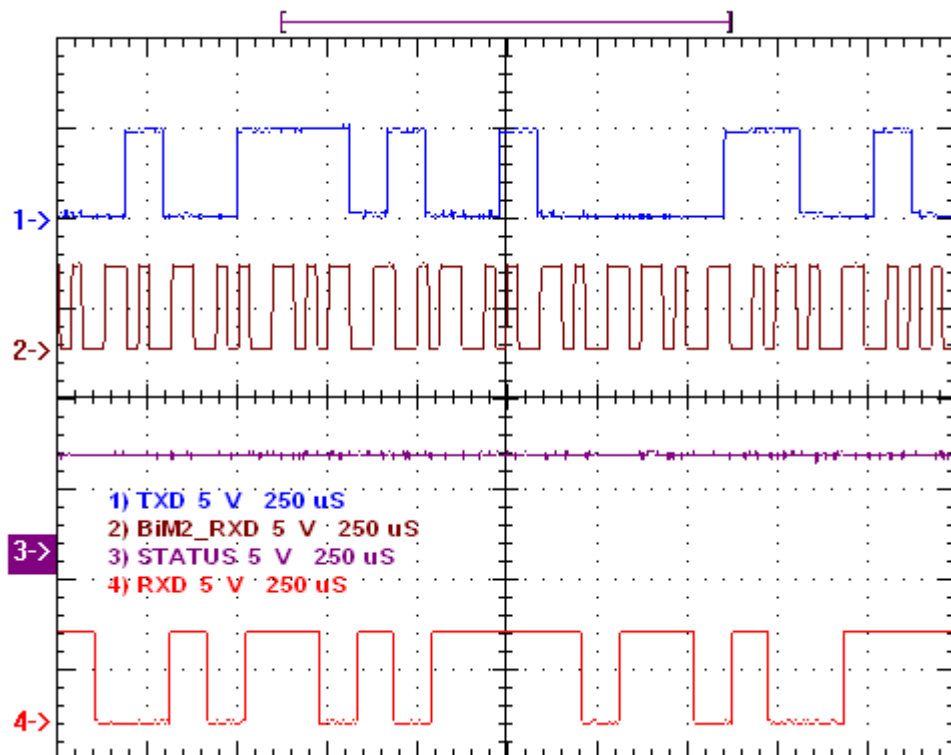


Figure 5: 16kbps Bi-phase encoded continuous data stream (expanded view)

Continuous serial data at 9600bps (above) is encoded as half-cycles of 8kHz (62.5µs long bit) and 16kHz (31.25µs short bit).

Programming the TDL2A

In order to use all the functions embedded in the TDL2A, the user must be aware of the setup/programming facility, which allow different addresses and frequency channels to be set up, and if necessary accesses diagnostic test modes.

The TDL2A is programmed through the same RS232 port that is used for sending/receiving data. An RS232 terminal emulator (such as Aterm or HyperTerminal) is an ideal tool.

To enter program mode, the **SETUP pin** must be **pulled low**. In this mode the radio link is disabled, but characters sent (at 9600 baud, as normal) to the unit are echoed back on the RXD pin.

The unit will only respond to certain command strings:

ADDR0 to ADDR7 <CR>: These commands set up one of 8 unique addresses.
CHAN0 to CHAN4 <CR>: These commands select one of 5 preset channels

A TDL2A will only communicate with a unit set to the same address and the same channel.

Address and channel numbers are stored in volatile memory. On power-up the TDL2A reverts to the default in EEPROM (as supplied this is always address 0 and Channel 0)

SETPROGRAM <CR>: Writes the current address and current channel into EEPROM as the new default.
A tilde character (~, ascii 126dec) sent by the unit indicates end of EEPROM write sequence

(these commands are normally only used for factory diagnostics)

NOTONE <CR>: Transmit unmodulated carrier
LFTONE <CR>: Transmit carrier modulated with 8KHz squarewave
HFTONE <CR>: Transmit carrier modulated with 16KHz squarewave
<CR>: Transmitter off

A Carriage Return '<CR>' (00Dhex) should be entered after each command sequence to execute it.

Releasing the SETUP pin to high state returns the TDL2A to normal operation.

Interfacing a microcontroller to TDL2A

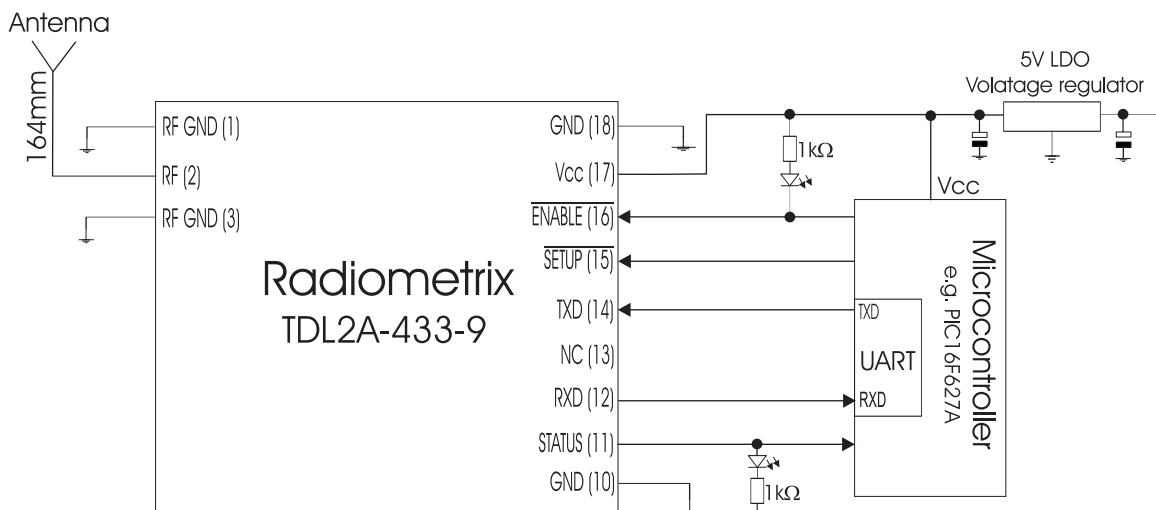


Figure 6: TDL2A interfaced directly to a microcontroller

TDL2A can be directly interfaced to any microcontrollers. If the microcontroller has a built-in UART, it can concentrate on its main task and leave the packet formatting, bit balancing and error checking of serial data to TDL2A.

Serial data should be in the following format:

1 start bit, 8 data bits, no parity, 1 or 2 stop bits
9600bps
0V=low, 5V=high

STATUS pin can be connected to one of the port pins which can generate an interrupt on low-to-high transition (e.g. RB0/INT pin in the PIC). This can be used to enter a receive sub-routine to download data received from remote TDL2A. Therefore, the host does not need to wait in a loop for a packet.

Range test and site survey can be carried out by connecting an LED on the STATUS pin. Every time, TDL2A is within range to receive valid data, the LED will flicker.

Interfacing RS232 port to TDL2A

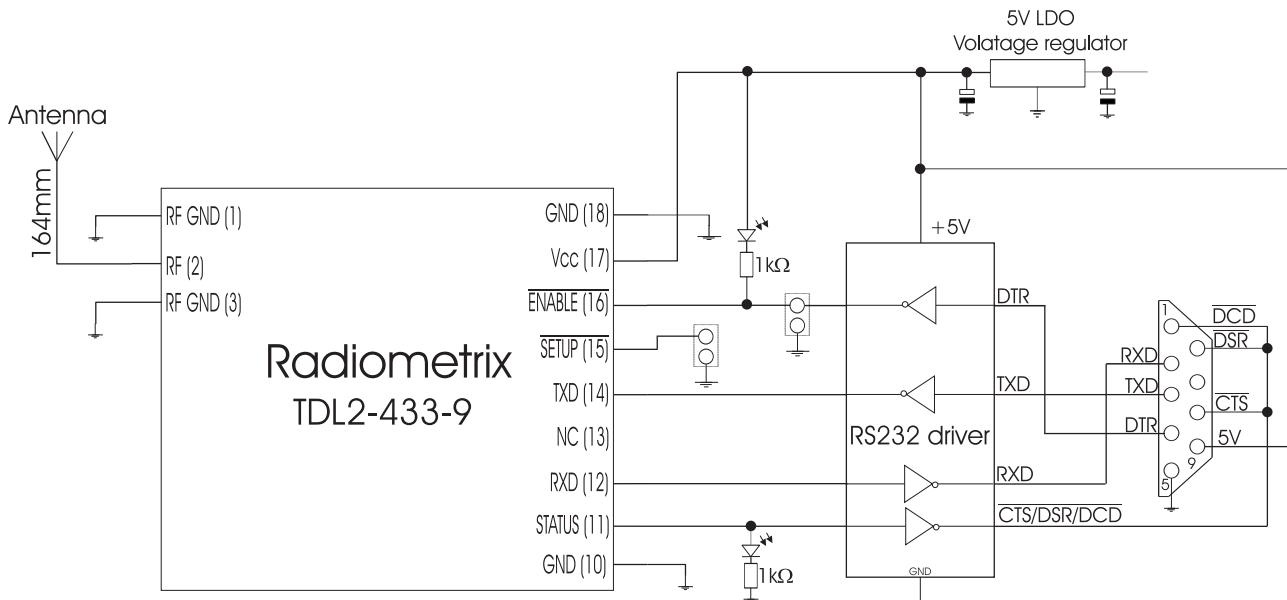


Figure 7: TDL2A interfaced to an RS232 port via an RS232 line driver/receiver

STATUS pin in this can be connected to CTS, DSR and DCD pin to simulate a flow control signal.

TDL2A is capable of continuously streaming data at 9600bps. Therefore, STATUS pin is not asserted to stop the Host from sending data as in normal RTS/CTS flow control method, but merely to warn the host that there is already data in the receive buffer which need to be downloaded before sending any more data.

Some DTE hosts assert DTR signal when they are active and this can be used via RS232 line receiver to enable TDL2A. Otherwise the ENABLE must be physically pulled-low to activate the TDL2A.

NOTE:

An interface board (with MAX232 type buffer, 9 way D connector, 5V voltage regulator and SMA RF connector) is available. This board is 61mm x 33mm in size.

Condensed specifications

Frequency	433.925MHz – CHAN0 (default channel)
	433.285MHz – CHAN1
	433.605MHz – CHAN2
	434.245MHz – CHAN3
	434.565MHz – CHAN4
<i>Frequency stability</i>	±10kHz
<i>Channel width</i>	320kHz
<i>Number of channels</i>	1 of 5, user programmed
Supply Voltage	5V
<i>Current</i>	28mA transmit
	22mA receive/idle
Operating temperature	-20 °C to +70 °C (Storage -30 °C to +70 °C)
Spurious radiations	Compliant with ETSI EN 300 220-3 and EN 301 489-3
Interfaces	
<i>User</i>	9pin 0.1" pitch molex
<i>RF</i>	3pin 0.1" pitch molex
Size	33 x 23 x 7mm
Transmitter	
Output power	10dBm (10mW) ±1dB
TX on switching time	<4ms
Modulation type	16kbps bi-phase FSK
FM peak deviation	+/-25KHz
Adjacent channel TX power	<-37dBm
TX spurious	<-45dBm
Receiver	
Sensitivity	-107dBm for 1% BER
image	-50dB
spurious / adjacent channel	-65dB
Blocking	-84dB nominal, 75dB worst case
LO re-radiation	<-60dBm
Interface	
Data rate	9600baud, Half duplex
Format	1 start, 8 data, 1 stop, no parity
Levels	5V CMOS (inverted RS232. Mark = 5V = idle)
Buffers	32 byte FIFO
Flow control	None ('RX busy' pin provided)
Addressing	1 of 8, user programmed
Data latency	14ms (first byte into TX, to first byte out of RX)

Antenna requirements

Three types of integral antenna are recommended and approved for use with the module:

- A) **Whip** This is a wire, rod ,PCB track or combination connected directly to RF pin of the module. Optimum total length is 16cm (1/4 wave @ 433MHz). Keep the open circuit (hot) end well away from metal components to prevent serious de-tuning. Whips are ground plane sensitive and will benefit from internal 1/4 wave earthed radial(s) if the product is small and plastic cased
- B) **Helical** Wire coil, connected directly to RF pin, open circuit at other end. This antenna is very efficient given it's small size (20mm x 4mm dia.). The helical is a high Q antenna, trim the wire length or expand the coil for optimum results. The helical de-tunes badly with proximity to other conductive objects.
- C) **Loop** A loop of PCB track tuned by a fixed or variable capacitor to ground at the 'hot' end and fed from RF pin at a point 20% from the ground end. Loops have high immunity to proximity de-tuning.

Features	A <i>whip</i>	B <i>helical</i>	C <i>loop</i>
Ultimate performance	***	**	*
Easy of design set-up	***	**	*
Size	*	***	**
Immunity proximity effects	*	**	***

The antenna choice and position directly controls the system range. Keep it clear of other metal in the system, particularly the 'hot' end. The best position by far, is sticking out the top of the product. This is often not desirable for practical/ergonomic reasons thus a compromise may need to be reached. If an internal antenna must be used, try to keep it away from other metal components, particularly large ones like transformers, batteries and PCB tracks/earth plane. The space around the antenna is as important as the antenna itself.

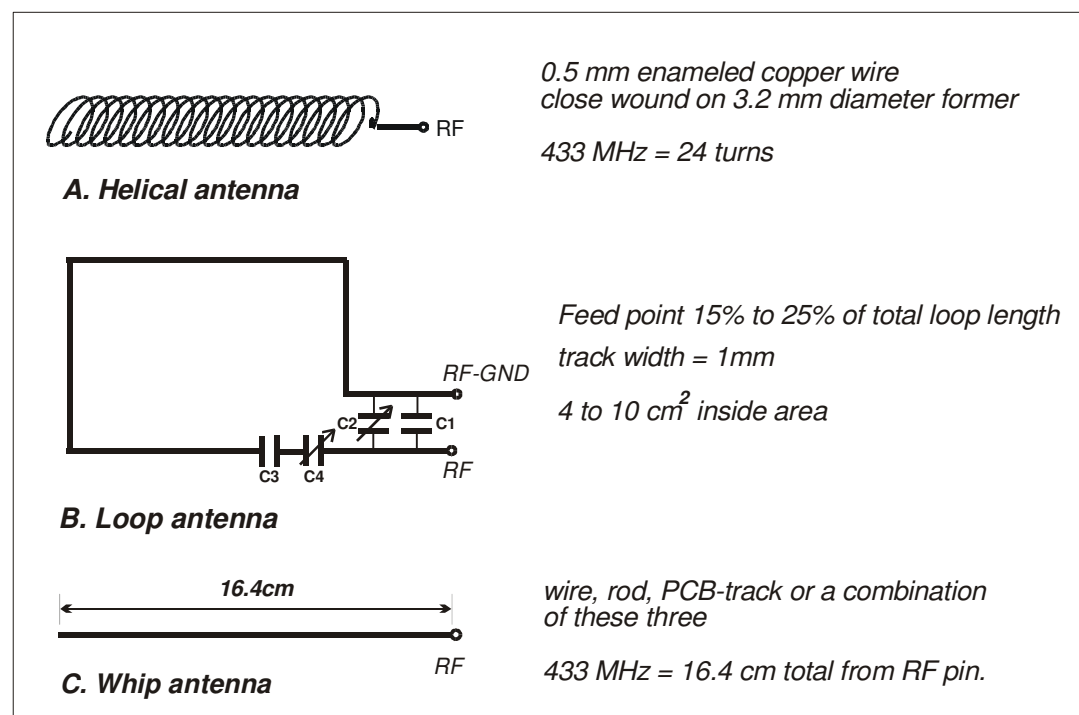


Figure 8: Antenna types

Ordering information

The TDL2A radio modem is manufactured in the following variants as standard:

Part Number	Description	Frequency band	Maximum baud rate
TDL2A-433-9	Half duplex modem	433.925 - 434.565 MHz	9.6kbps
TDL2T-433-9	Transmitter only	433.925 - 434.565 MHz	9.6kbps
TDL2R-433-9	Receiver only	433.925 - 434.565 MHz	9.6kbps
TDL2A-433-4	Half duplex modem	433.925 - 434.565 MHz	4.8kbps
TDL2T-433-4	Transmitter only	433.925 - 434.565 MHz	4.8kbps
TDL2R-433-4	Receiver only	433.925 - 434.565 MHz	4.8kbps

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The Intrastat commodity code for all our modules is: 8542 6000

R&TTE Directive

After 7 April 2001 the manufacturer can only place finished product on the market under the provisions of the R&TTE Directive. Equipment within the scope of the R&TTE Directive may demonstrate compliance to the essential requirements specified in Article 3 of the Directive, as appropriate to the particular equipment.

Further details are available on The Office of Communications (Ofcom) web site:

<http://www.ofcom.org.uk/>

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