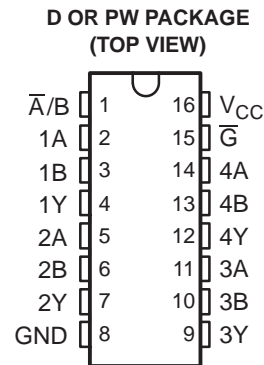


## QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

### FEATURES

- Qualified for Automotive Applications
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Operates From 2 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 5.4 ns at 3.3 V
- Typical  $V_{OLP}$  (Output Ground Bounce) < 0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot) > 2 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$



### DESCRIPTION/ORDERING INFORMATION

The SN74LVC157A quadruple 2-line to 1-line data selector/multiplexer is designed for 2.7-V to 3.6-V  $V_{CC}$  operation.

The device features a common strobe ( $\overline{G}$ ) input. When  $\overline{G}$  is high, all outputs are low. When  $\overline{G}$  is low, a 4-bit word is selected from one of two sources and is routed to the four outputs. The device provides true data.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

### ORDERING INFORMATION<sup>(1)</sup>

| $T_A$          | PACKAGE <sup>(2)</sup> |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------------------|---------------|-----------------------|------------------|
| -40°C to 125°C | SOIC – D               | Tape and reel | SN74LVC157AQDRQ1      | L157AQ1          |
|                | TSSOP – PW             | Tape and reel | SN74LVC157AQPWRQ1     | L157AQ1          |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

(2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

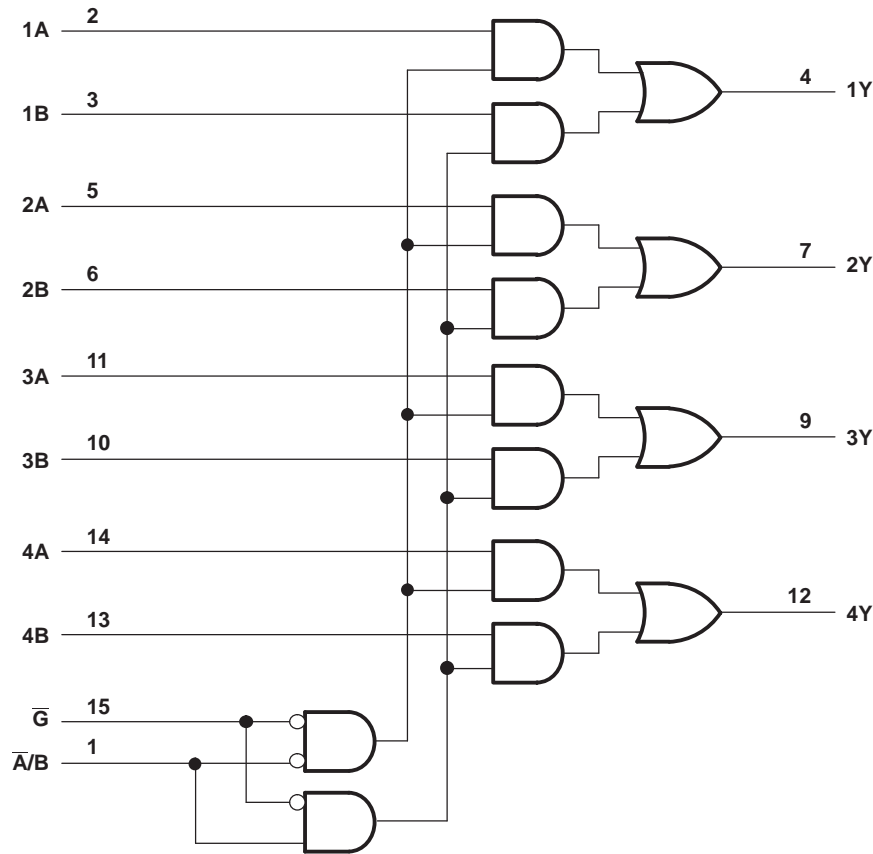
### FUNCTION TABLE

| INPUTS         |                  |   |   | OUTPUT<br>Y |
|----------------|------------------|---|---|-------------|
| $\overline{G}$ | $\overline{A/B}$ | A | B |             |
| H              | X                | X | X | L           |
| L              | L                | L | X | L           |
| L              | L                | H | X | H           |
| L              | H                | X | L | L           |
| L              | H                | X | H | H           |



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**LOGIC DIAGRAM (POSITIVE LOGIC)**



**Absolute Maximum Ratings<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

|                  |   | MIN                | MAX                   | UNIT     |
|------------------|---|--------------------|-----------------------|----------|
| V <sub>CC</sub>  | Supply voltage range                              | -0.5               | 6.5                   | V        |
| V <sub>I</sub>   | Input voltage range <sup>(2)</sup>                | -0.5               | 6.5                   | V        |
| V <sub>O</sub>   | Output voltage range <sup>(2)(3)</sup>            | -0.5               | V <sub>CC</sub> + 0.5 | V        |
| I <sub>IK</sub>  | Input clamp current                               | V <sub>I</sub> < 0 |                       | -50 mA   |
| I <sub>OK</sub>  | Output clamp current                              | V <sub>O</sub> < 0 |                       | -50 mA   |
| I <sub>O</sub>   | Continuous output current                         |                    |                       | ±50 mA   |
|                  | Continuous current through V <sub>CC</sub> or GND |                    |                       | ±100 mA  |
| θ <sub>JA</sub>  | Package thermal impedance <sup>(4)</sup>          | D package          |                       | 73 °C/W  |
|                  |   | PW package         |                       | 108 °C/W |
| T <sub>stg</sub> | Storage temperature range                         | -65                | 150                   | °C       |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V<sub>CC</sub> is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51.

**Recommended Operating Conditions<sup>(1)</sup>**

|                 |                                    |                                  | MIN | MAX             | UNIT |
|-----------------|------------------------------------|----------------------------------|-----|-----------------|------|
| V <sub>CC</sub> | Supply voltage                     | Operating                        | 2   | 3.6             | V    |
|                 |                                    | Data retention only              | 1.5 |                 |      |
| V <sub>IH</sub> | High-level input voltage           | V <sub>CC</sub> = 2.7 V to 3.6 V | 2   |                 | V    |
| V <sub>IL</sub> | Low-level input voltage            | V <sub>CC</sub> = 2.7 V to 3.6 V |     | 0.8             | V    |
| V <sub>I</sub>  | Input voltage                      |                                  | 0   | 5.5             | V    |
| V <sub>O</sub>  | Output voltage                     |                                  | 0   | V <sub>CC</sub> | V    |
| I <sub>OH</sub> | High-level output current          | V <sub>CC</sub> = 2.7 V          |     | -12             | mA   |
|                 |                                    | V <sub>CC</sub> = 3 V            |     | -24             |      |
| I <sub>OL</sub> | Low-level output current           | V <sub>CC</sub> = 2.7 V          |     | 12              | mA   |
|                 |                                    | V <sub>CC</sub> = 3 V            |     | 24              |      |
| Δt/Δv           | Input transition rise or fall rate |                                  |     | 10              | ns/V |
| T <sub>A</sub>  | Operating free-air temperature     |                                  | -40 | 125             | C    |

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**Electrical Characteristics**

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER        | TEST CONDITIONS |  | V <sub>CC</sub> | MIN                   | MAX | UNIT |
|------------------|-----------------|--|-----------------|-----------------------|-----|------|
| V <sub>OH</sub>  |                 | I <sub>OH</sub> = -100 μA  | 2.7 V to 3.6 V  | V <sub>CC</sub> - 0.2 |     | V    |
|                  |                 | I <sub>OH</sub> = -12 mA   | 2.7 V           | 2.2                   |     |      |
|                  |                 |  | 3 V             | 2.4                   |     |      |
|                  |                 |  | 3 V             | 2.2                   |     |      |
| V <sub>OL</sub>  |                 | I <sub>OL</sub> = 100 μA   | 2.7 V to 3.6 V  | 0.2                   |     | V    |
|                  |                 | I <sub>OL</sub> = 12 mA  | 2.7 V           | 0.4                   |     |      |
|                  |                 | I <sub>OL</sub> = 24 mA  | 3 V             | 0.55                  |     |      |
| I <sub>I</sub>   | All inputs      | V <sub>I</sub> = 5.5 V or GND  | 3.6 V           | ±5                    |     | μA   |
| I <sub>CC</sub>  |                 | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0                  | 3.6 V           | 10                    |     | μA   |
| ΔI <sub>CC</sub> |                 | One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND | 2.7 V to 3.6 V  | 500                   |     | μA   |

**Switching Characteristics**

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

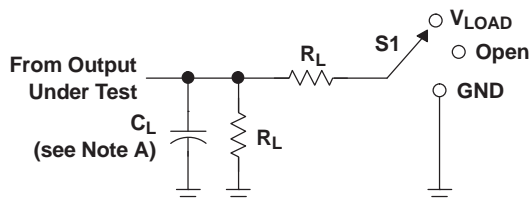
| PARAMETER       | FROM (INPUT)     | TO (OUTPUT) | V <sub>CC</sub> = 2.7 V |     | V <sub>CC</sub> = 3.3 V ± 0.3 V |     | UNIT |
|-----------------|------------------|-------------|-------------------------|-----|---------------------------------|-----|------|
|                 |                  |             | MIN                     | MAX | MIN                             | MAX |      |
| t <sub>pd</sub> | A or B           | Y           | 6.2                     | 0.8 | 5.4                             | ns  |      |
|                 | $\overline{A/B}$ |             | 8.2                     | 0.8 | 7                               |     |      |
|                 | $\overline{G}$   |             | 7.8                     | 0.8 | 6.5                             |     |      |

**Operating Characteristics**

T<sub>A</sub> = 25°C

| PARAMETER       | TEST CONDITIONS | V <sub>CC</sub> = 2.5 V | V <sub>CC</sub> = 3.3 V | UNIT |
|-----------------|-----------------|-------------------------|-------------------------|------|
|                 |                 | TYP                     | TYP                     |      |
| C <sub>pd</sub> | f = 10 MHz      | 15                      | 16                      | pF   |

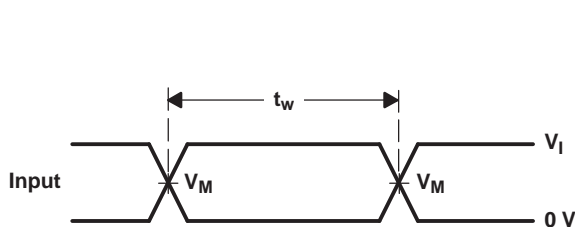
PARAMETER MEASUREMENT INFORMATION



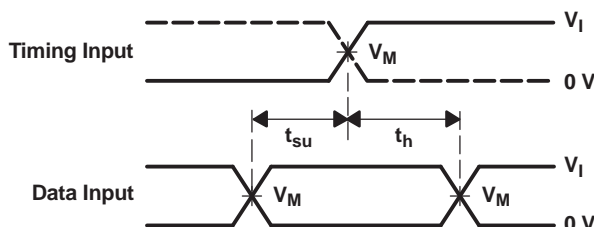
LOAD CIRCUIT

| TEST              | S1         |
|-------------------|------------|
| $t_{PLH}/t_{PHL}$ | Open       |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND        |

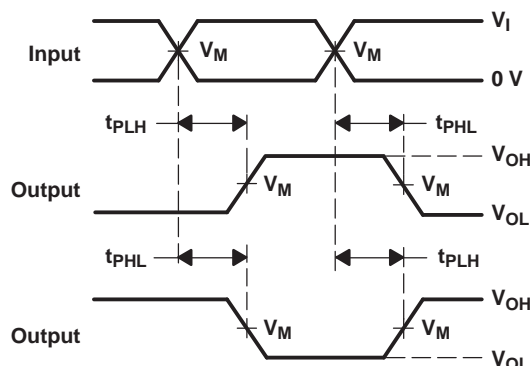
| $V_{CC}$                          | INPUTS |               | $V_M$ | $V_{LOAD}$ | $C_L$ | $R_L$        | $V_{\Delta}$ |
|-----------------------------------|--------|---------------|-------|------------|-------|--------------|--------------|
|                                   | $V_I$  | $t_r/t_f$     |       |            |       |              |              |
| 2.7 V                             | 2.7 V  | $\leq 2.5$ ns | 1.5 V | 6 V        | 50 pF | 500 $\Omega$ | 0.3 V        |
| $3.3 \text{ V} \pm 0.3 \text{ V}$ | 2.7 V  | $\leq 2.5$ ns | 1.5 V | 6 V        | 50 pF | 500 $\Omega$ | 0.3 V        |



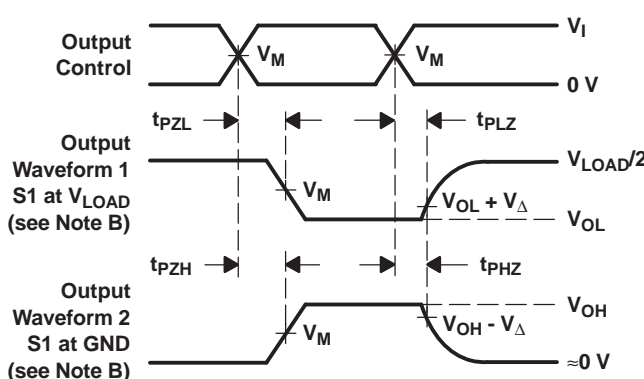
VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ .
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

| Orderable Device   | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|--------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| CLVC157AQPWRG4Q1   | ACTIVE        | TSSOP        | PW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | L157AQ1                 | <a href="#">Samples</a> |
| SN74LVC157AQDRG4Q1 | ACTIVE        | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | L157AQ1                 | <a href="#">Samples</a> |
| SN74LVC157AQDRQ1   | OBSOLETE      | SOIC         | D               | 16   |             | TBD                     | Call TI                 | Call TI              | -40 to 125   |                         |                         |
| SN74LVC157AQPWRQ1  | ACTIVE        | TSSOP        | PW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | L157AQ1                 | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN74LVC157A-Q1 :**

- Catalog: [SN74LVC157A](#)
- Enhanced Product: [SN74LVC157A-EP](#)
- Military: [SN54LVC157A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CLVC157AQPWRG4Q1  | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74LVC157AQPWRQ1 | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CLVC157AQPWRG4Q1  | TSSOP        | PW              | 16   | 2000 | 367.0       | 367.0      | 35.0        |
| SN74LVC157AQPWRQ1 | TSSOP        | PW              | 16   | 2000 | 367.0       | 367.0      | 35.0        |



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4211284-3/G 08/15

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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| Data Converters              | <a href="http://dataconverter.ti.com">dataconverter.ti.com</a>                       |
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|                               |  |
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